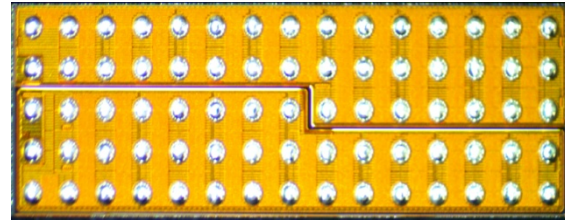


# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet

## Features:

- Greater than 97% System Efficiency at 22 A
  - 48 V<sub>IN</sub> to 12 V<sub>OUT</sub>, 300 kHz
  - Includes driver, inductor, and output filter
- High Frequency Operation
- High Density Footprint
- Low Inductance Package
- Pb-Free (RoHS Compliant), Halogen Free

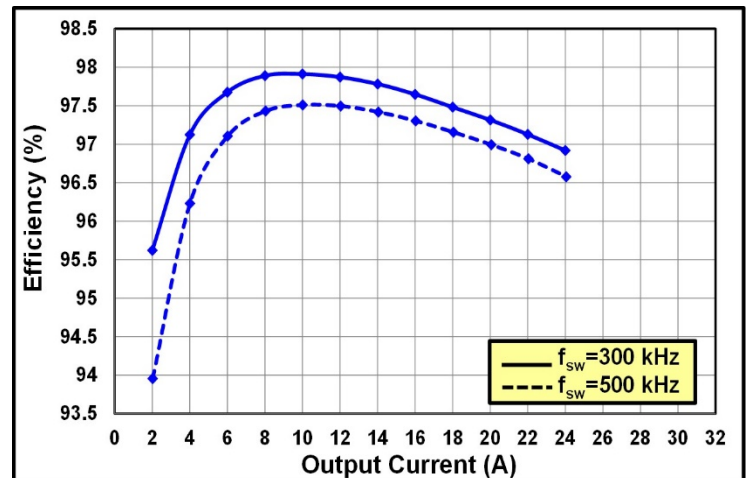


EPC2104 devices are supplied only in passivated die form with solder balls  
Die Size: 6.05 mm x 2.3 mm

## Applications:

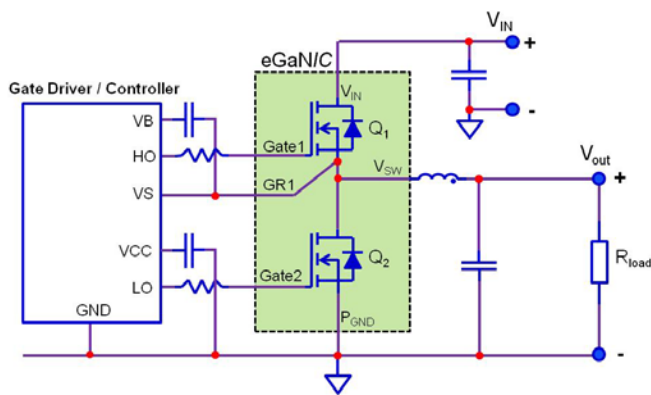
- High Frequency DC-DC Conversion
- Motor Drive

## Typical System Efficiency



V<sub>IN</sub> = 48 V, V<sub>OUT</sub> = 12 V

## Typical Circuit



## MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage (V <sub>SW</sub> to P <sub>GND</sub> , V <sub>IN</sub> to V <sub>SW</sub> )	100 V
Maximum Gate – Source Voltage Range (Gate 1 to V <sub>SW</sub> , Gate 2 to P <sub>GND</sub> )	-4 V < V <sub>GS</sub> < 6 V
Continuous Drain Current, 25 °C, R <sub>θJA</sub> = 21 °C/W	23 A
Maximum Pulsed Drain Current, 25 °C, T <sub>pulse</sub> = 300 μs	165 A
Optimum Temperature Range	-40 °C < T <sub>J</sub> < 150 °C

# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet



## STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Voltage ( $BV_{DSS}$ )	$V_{GS} = 0\text{ V}$ , $I_D = 400\ \mu\text{A}$	100 V
Maximum Drain – Source Leakage	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$	320 $\mu\text{A}$
Maximum $R_{DS(on)}$	$V_{GS} = 5\text{ V}$ , $I_D = 20\text{ A}$	6.3 m $\Omega$
Typical $R_{DS(on)}$	$V_{GS} = 5\text{ V}$ , $I_D = 20\text{ A}$	5 m $\Omega$
Gate – Source Threshold Voltage	$I_D = 5.5\text{ mA}$ , $V_{DS} = V_{GS}$	$0.8\text{ V} < V_{GS(TH)} < 2.5\text{ V}$
Gate – Source Maximum Positive Leakage	$V_{GS} = 5\text{ V}$	5 mA
Gate – Source Maximum Negative Leakage	$V_{GS} = -4\text{ V}$	-320 $\mu\text{A}$

$T_J = 25\text{ }^\circ\text{C}$  unless otherwise stated

## DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value		
		Q1 Control FET	Q2 Sync FET	Unit
$C_{ISS}$ (Input Capacitance)	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$	800		pF
$C_{OSS}$ (Output Capacitance)		450	600	
$C_{RSS}$ (Reverse Transfer Capacitance)		7		
$Q_G$ (Total Gate Charge)	$V_{DS} = 50\text{ V}$ , $I_D = 20\text{ A}$ , $V_{GS} = 5\text{ V}$	7		nC
$Q_{GS}$ (Gate to Source Charge)	$V_{DS} = 50\text{ V}$ , $I_D = 20\text{ A}$	2		
$Q_{GD}$ (Gate to Drain Charge)		1.2		
$Q_{G(TH)}$ (Gate Charge at Threshold)		1.4		
$Q_{OSS}$ (Output Charge)	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$	35	47	
$Q_{RR}$ (Source-Drain Recovery Charge)		0		

$T_J = 25\text{ }^\circ\text{C}$  unless otherwise stated

# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet



## THERMAL CHARACTERISTICS

		TYPICAL		
		Q1 Control FET	Q2 Sync FET	
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	0.4		°C/W
R <sub>θJB</sub>	Thermal Resistance, Junction to Board (Note 2)	1.8	1.9	°C/W
R <sub>θ12</sub>	Thermal Resistance, Cross-Coupling	1.3		°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (Note 1)	42		°C/W

Note 1: R<sub>θJA</sub> is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Note 2: ΔT is determined by the following matrix equation:

$$\begin{pmatrix} \Delta T_{Q1} \\ \Delta T_{Q2} \end{pmatrix} = \begin{bmatrix} 1.8 & 1.3 \\ 1.3 & 1.9 \end{bmatrix} \cdot \begin{pmatrix} P_{Q1} \\ P_{Q2} \end{pmatrix}$$

This matrix equation lets you calculate the temperature rise of each FET, given the power dissipated in each FET.

Thermal models for EPC devices available at <http://epc-co.com/epc/DesignSupport/DeviceModels.aspx>

# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet



Figure 1a: EPC2104-Q1 Typical Output Characteristics at 25°C

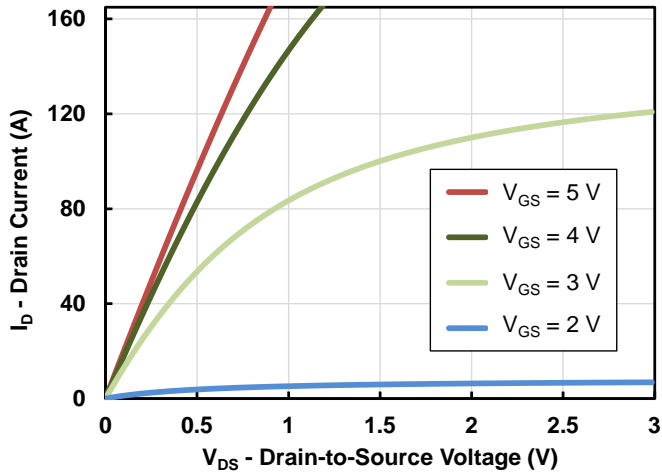


Figure 1b: EPC2104-Q2 Typical Output Characteristics at 25°C

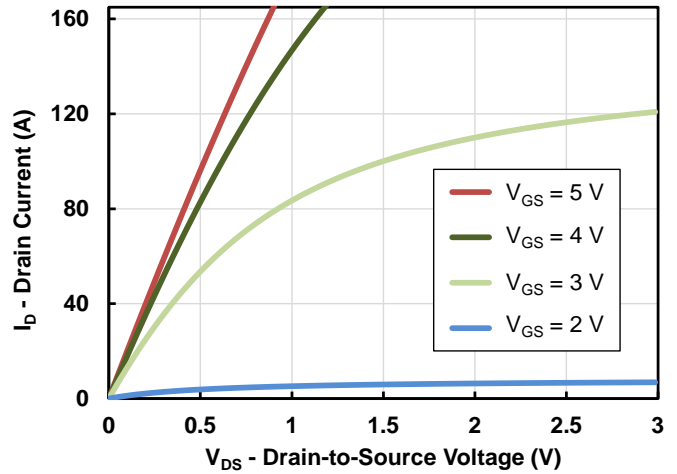


Figure 2a: EPC2104-Q1 Transfer Characteristics

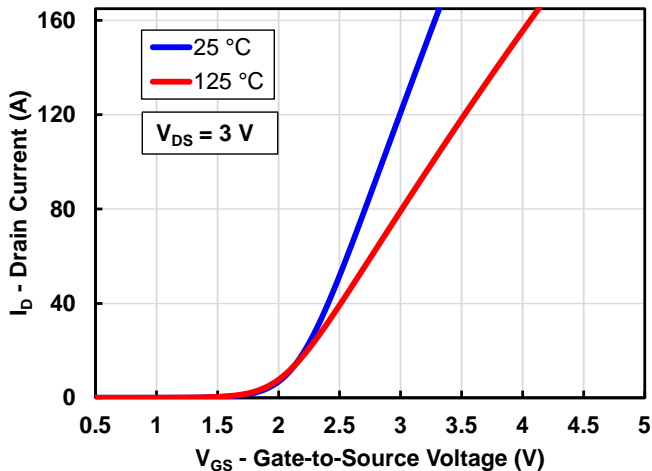


Figure 2b: EPC2104-Q2 Transfer Characteristic

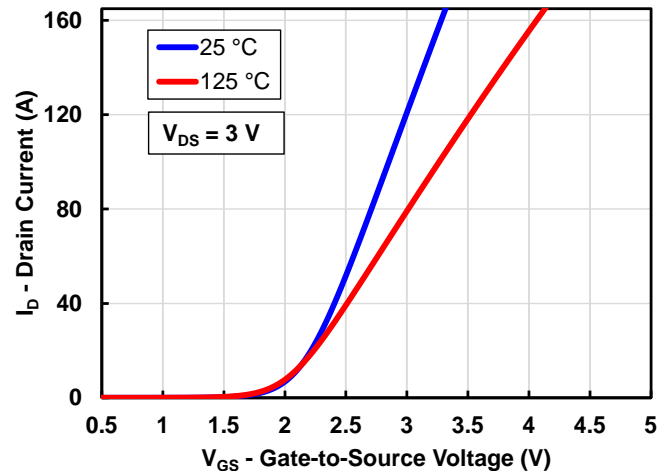


Figure 3a: EPC2104-Q1:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

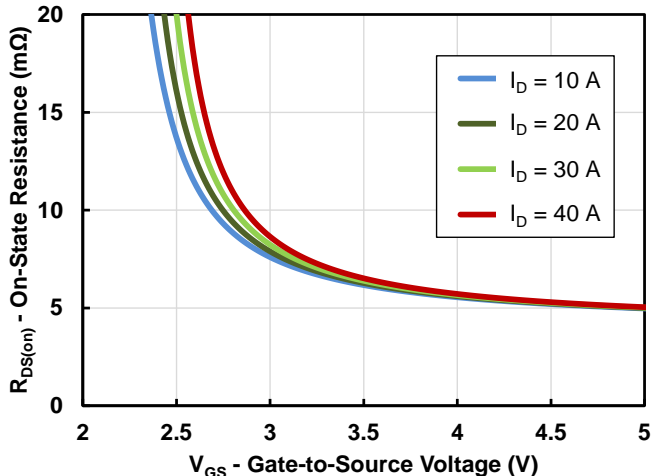
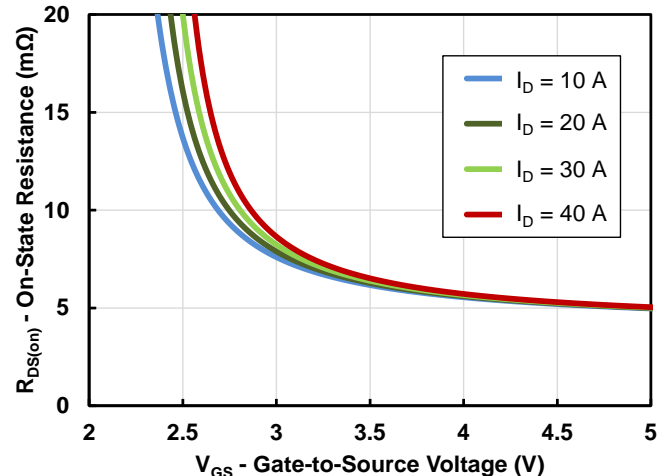


Figure 3b: EPC2104-Q2:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents



# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet



Figure 4a: EPC2104-Q1:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

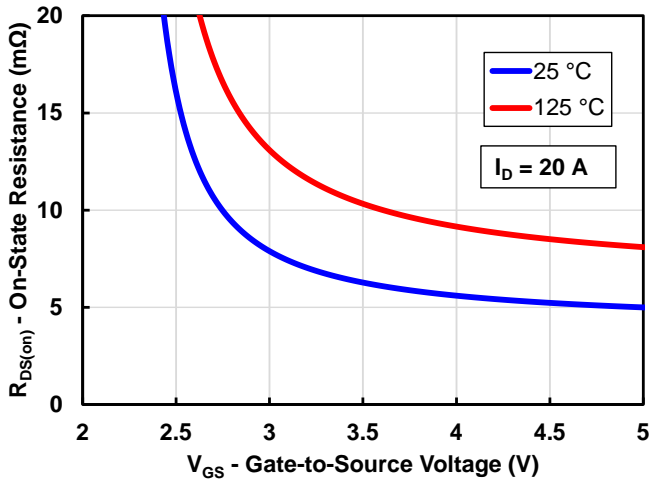


Figure 4b: EPC2104-Q2:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

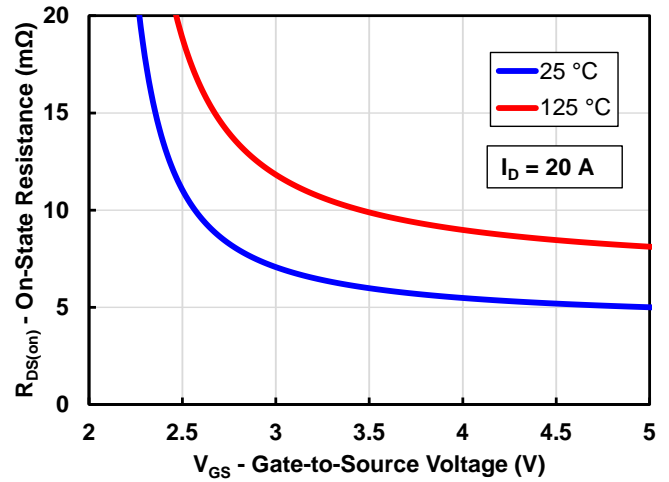


Figure 5a: EPC2104-Q1: Capacitance (Linear Scale)

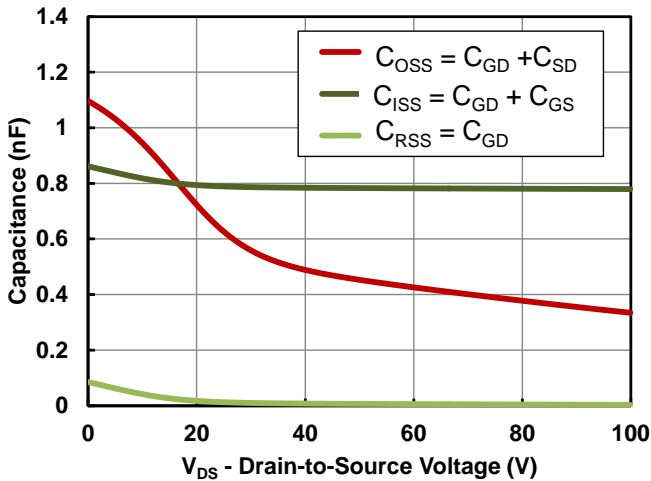


Figure 5b: EPC2104-Q2: Capacitance (Linear Scale)

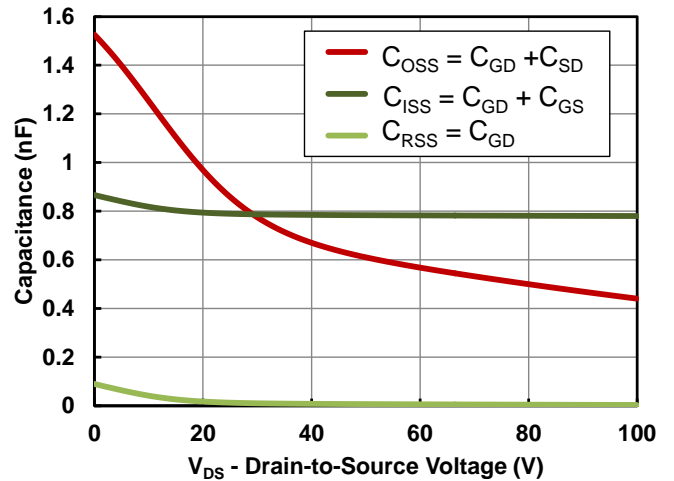


Figure 5c: EPC2104-Q1: Capacitance (Log Scale)

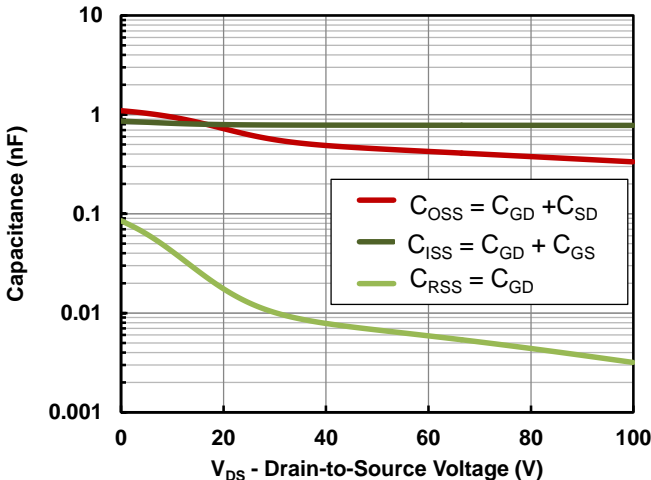
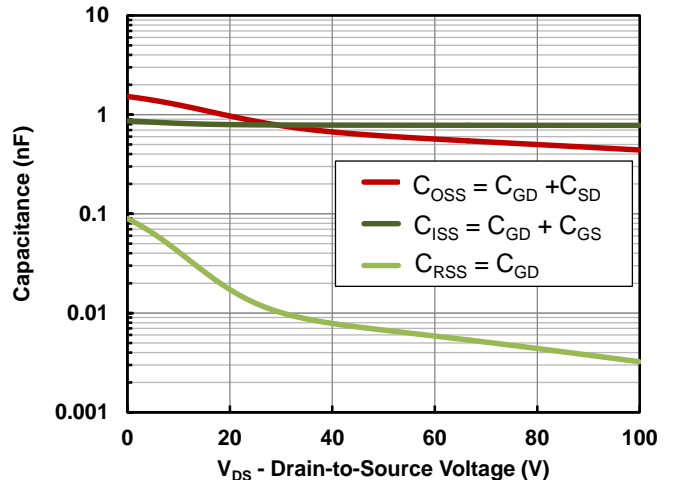


Figure 5d: EPC2104-Q2: Capacitance (Log Scale)



# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet



Figure 6a: EPC2104-Q1: Gate Charge

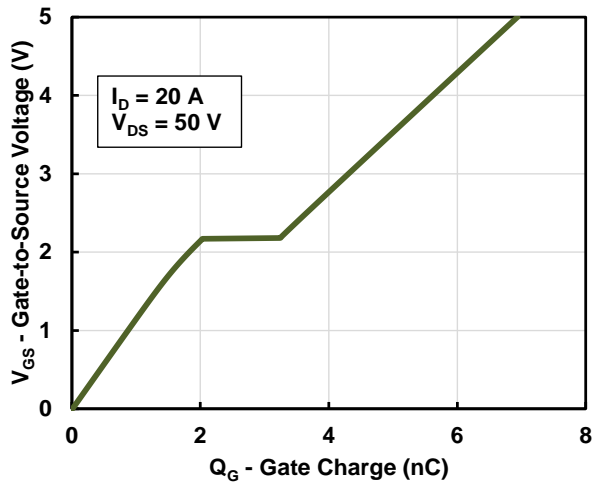


Figure 6b: EPC2104-Q2: Gate Charge

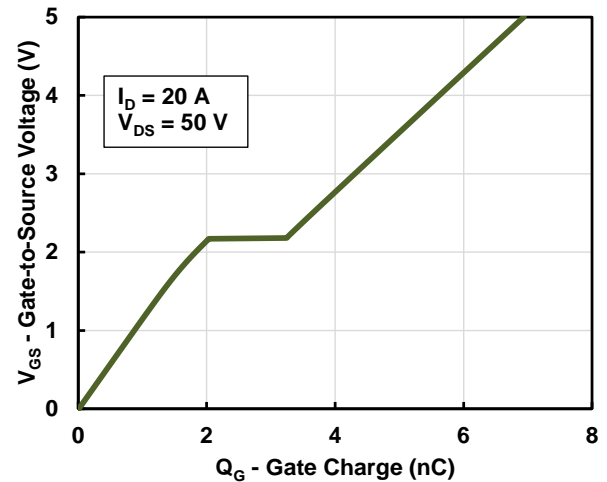


Figure 7a: EPC2104-Q1: Reverse Drain-Source Characteristics

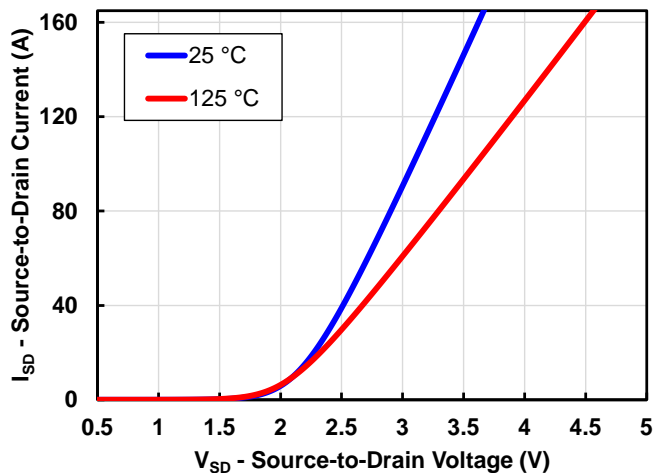


Figure 7b: EPC2104-Q2: Reverse Drain-Source Characteristics

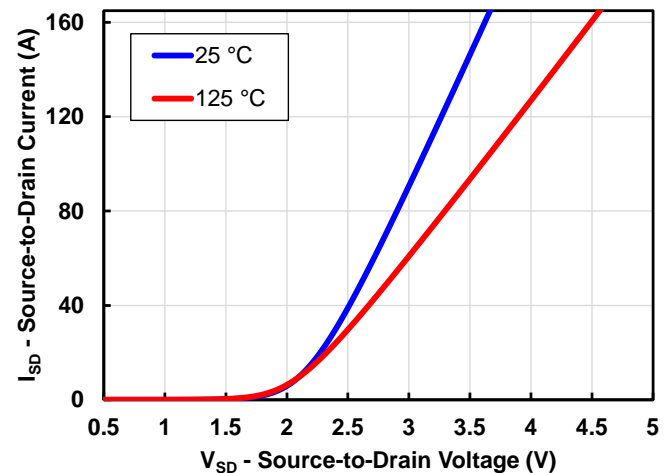


Figure 8a: EPC2104-Q1: Normalized On Resistance vs. Temperature

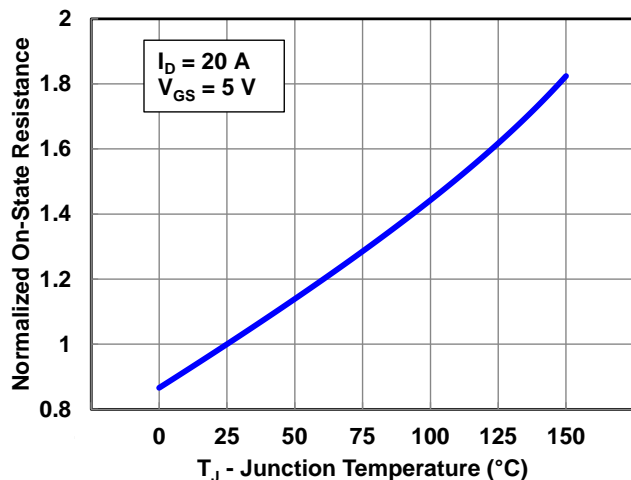
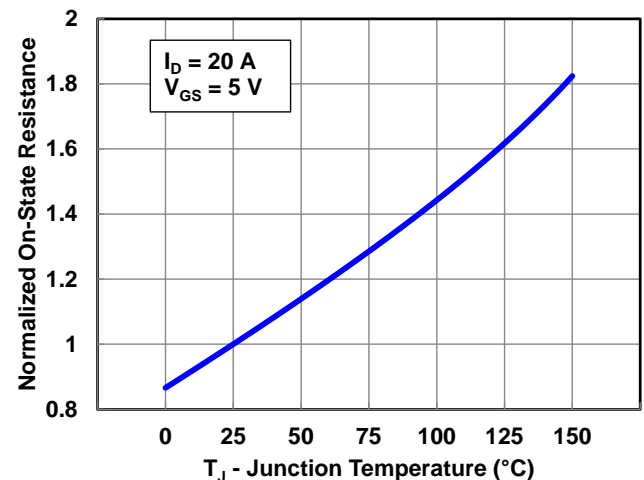


Figure 8b: EPC2104-Q2: Normalized On Resistance vs. Temperature



# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet



Figure 9a:  
EPC2104-Q1: Normalized Threshold Voltage vs. Temperature

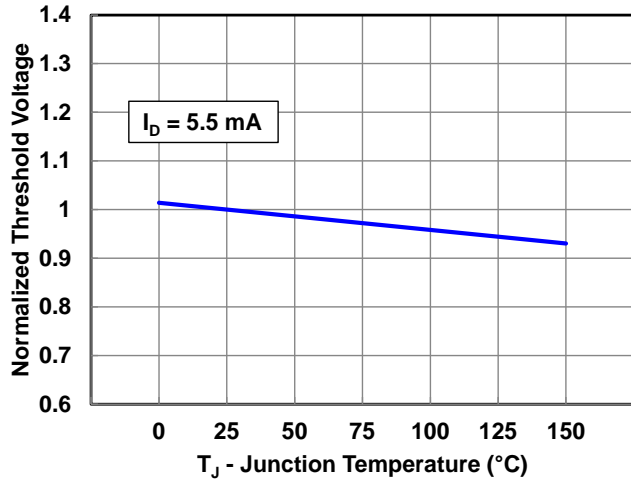
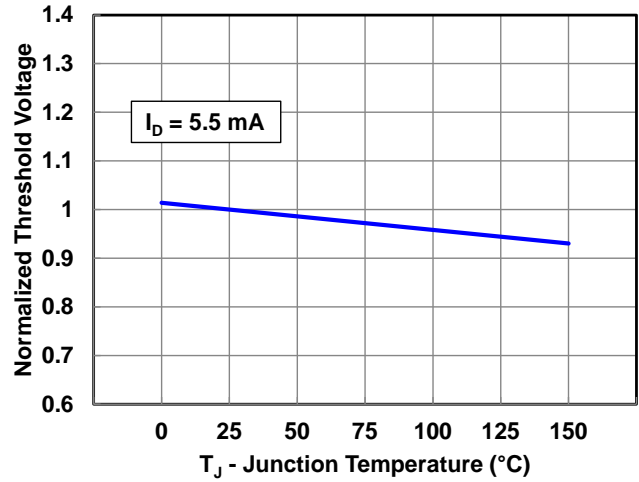


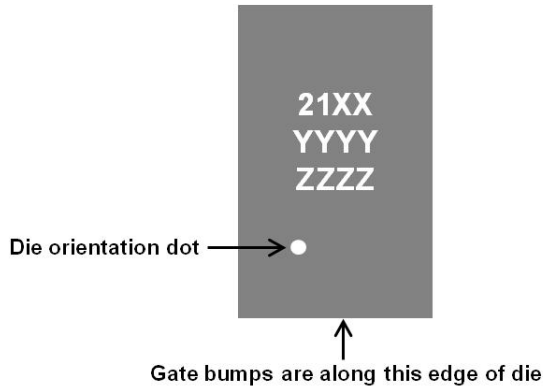
Figure 9b:  
EPC2104-Q2: Normalized Threshold Voltage vs. Temperature



# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet



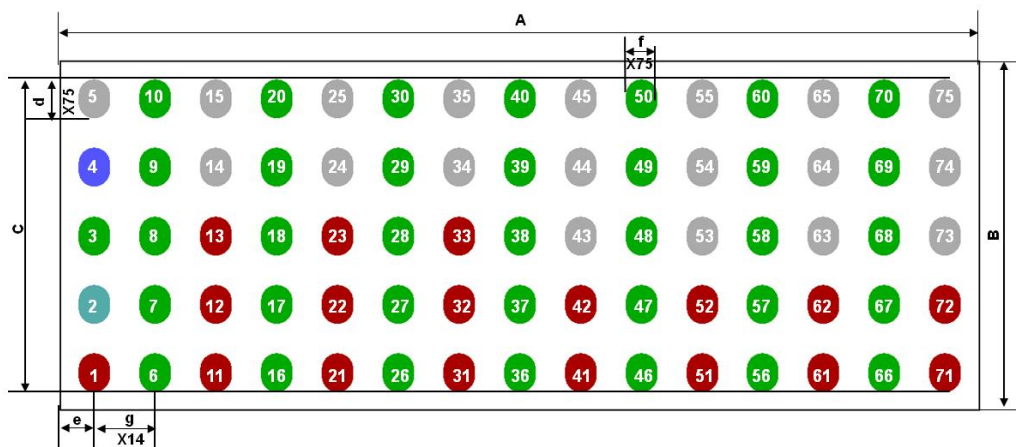
## DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2104ENGR	21XX	YYYY	ZZZZ

## DIE OUTLINE

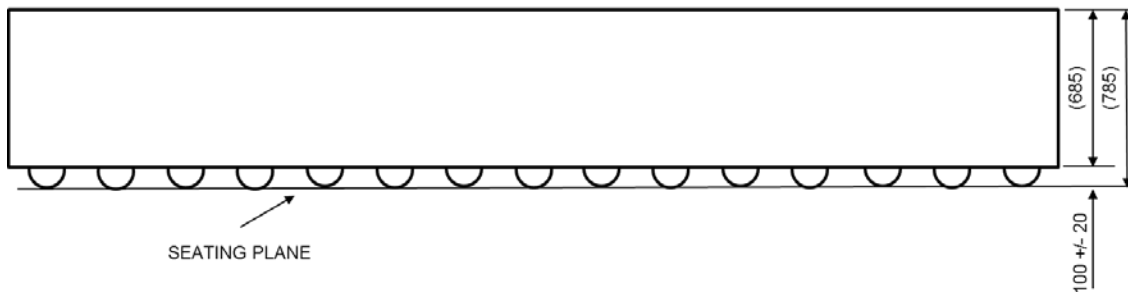
### Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	247	250	253
e	210	225	240
f	195	200	205
g	400	400	400

Pad 2 is Gate1 (high side); Pad 4 is Gate2 (low side); Pad 3 is HS Gate Return;  
 Pads 5, 14, 15, 24, 25, 34, 35, 43, 44, 45, 53, 54, 55, 63, 64, 65, 73, 74, 75 are Ground  
 Pads 1, 11, 12, 13, 21, 22, 23, 31, 32, 33, 41, 42, 51, 52, 61, 62, 71, 72 are  $V_{IN}$   
 Pads 3, 6, 7, 8, 9, 10, 16, 17, 18, 19, 20, 26, 27, 28, 29, 30, 36, 37, 38, 39, 40, 46, 47, 48, 49, 50, 56, 57, 58, 59, 60, 66, 67, 68, 69, 70 are switch node.

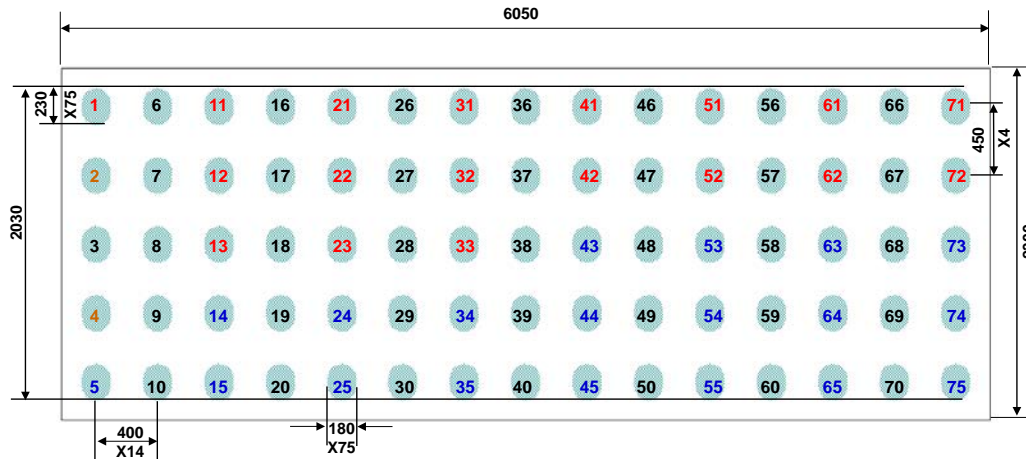
### Side View



# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet

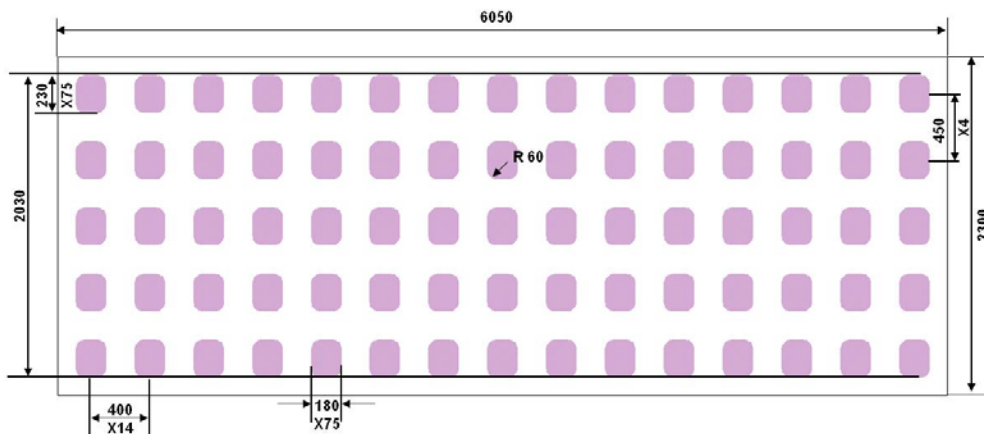


## RECOMMENDED LAND PATTERN (Units in $\mu\text{m}$ )



Pad 2 is Gate1 ( high side); Pad 4 is Gate2 ( low side); Pad 3 is HS Gate Return;  
 Pads 5, 14, 15, 24, 25, 34, 35, 43, 44, 45, 53, 54, 55, 63, 64, 65, 73, 74, 75 are Ground  
 Pads 1, 11, 12, 13, 21, 22, 23, 31, 32, 33, 41, 42, 51, 52, 61, 62, 71, 72 are VIN  
 Pads 3, 6, 7, 8, 9, 10, 16, 17, 18, 19, 20, 26, 27, 28, 29, 30, 36, 37, 38, 39, 40, 46, 47, 48, 49, 50, 56, 57, 58, 59, 60, 66, 67, 68, 69, 70 are switch node.

## RECOMMENDED STENCIL DESIGN (Units in $\mu\text{m}$ )



Recommended stencil should be 4mil (100 $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

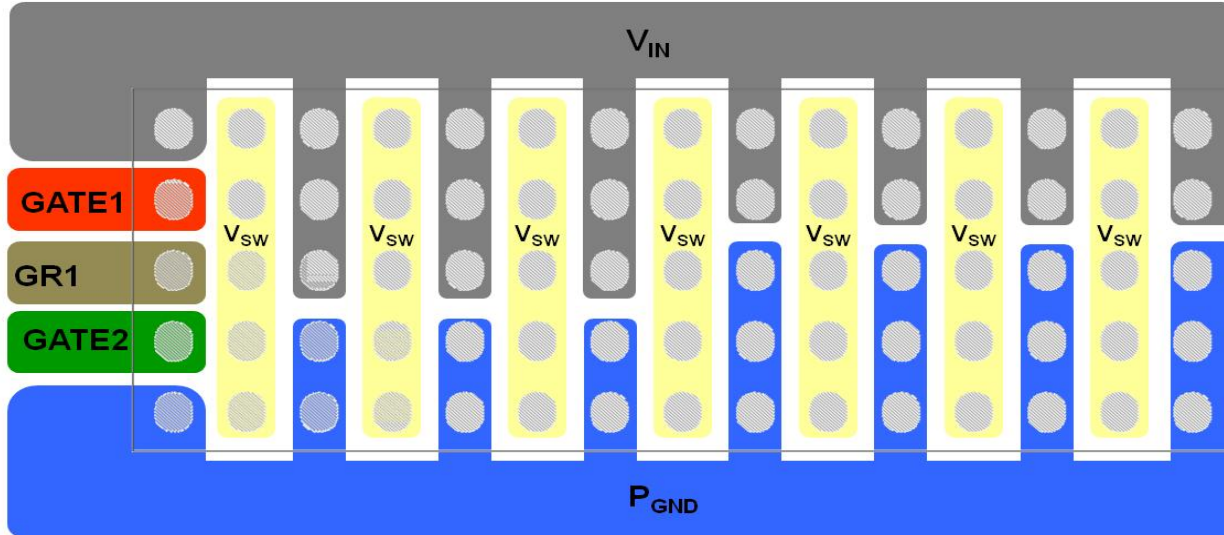
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

# EPC2104 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet

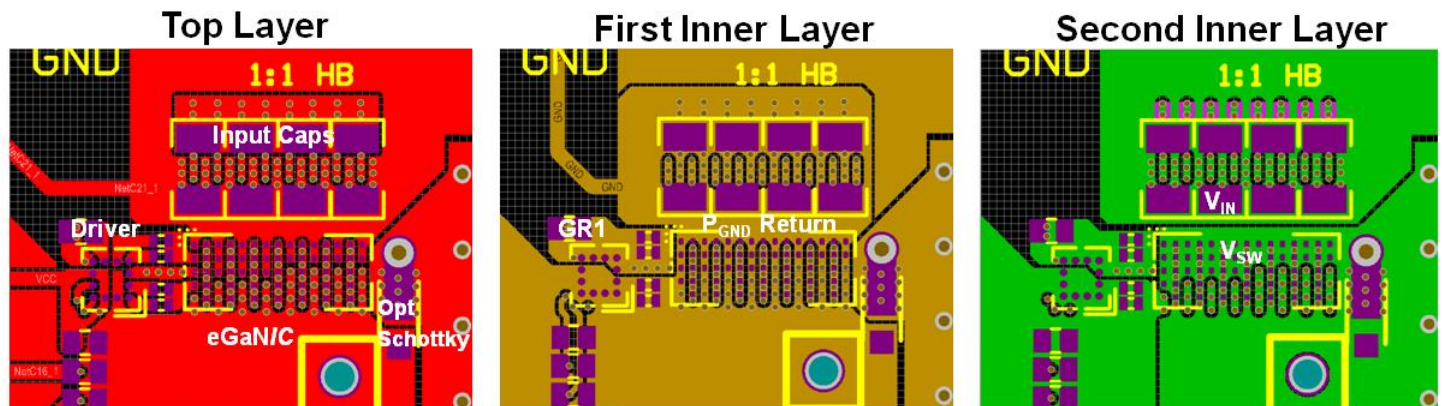


## RECOMMENDED PCB LAYOUT



Land pattern is solder mask defined

## PCB LAYOUT EXAMPLE



## Recommended PCB Layout

Gerber Files available at:

<http://epc-co.com/epc/documents/gerber-files/EPC9039%20Development%20Board%20Gerbers.zip>

Assembly Resources at: <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

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