Z86020

CARDBUS/PCI INTERFACE

FEATURES	BENEFITS
■ 256 Bytes of Internal 32-Bit Wide Configuration Memory.	Utilized for Card Initialization and Compatible with the PCMCIA CardBus Attribute Memory Specification.
■ 64 Internal PCI Compatible Configuration Registers.	Conforming to CardBus Standards
■ Six Programmable Memory or I/O Map Ranges.	PCI Configuration Software Compatible
■ Supports up to 64 Kbytes of FIFO Emulation Function.	Lower CPU Overhead when Interfacing with Real Time Peripherals
■ Supports Remote DMA Operation with Popular Ethernet Bus Master Devices.	Faster and more Efficient Operation, lower CPU Overhead.
■ On-Chip Local Peripheral Interface Bus (LPI) Arbitration is Supported.	Provide Hold/hold Acknowledge Protocol to Bus Master Devices.
■ This Device can Transfer Data to/from the CardBus 32-bit Interface to 8-, 16-, or 32-Bit Data Paths	Allow Easy Implementation of 8-Bit, 16-Bit or 32-Bit Peripheral Devices
■ One Programmable External ROM Base Address	Allow on Card BIOS PROM.
■ Internal Ethernet ID RAM is Loaded Remotely and Supports the Internal Ethernet ID Function.	Ethernet ID may be Modified Remotely, does not Require Additional Ethernet IO PROM.
■ External Bus Master Support can Provide Data from the Local Peripheral Device as DMA Device, Bus Mastering CPU Device	Permits Local CPU Bus Multi-Master Application.
■ ATA/IDE Drive Interface Compatible.	PCI/IDE, IDE/PCI Mapping.
■ +3V or +5V Operation.	Same IC may be used for Existing and Future Products.
■ 144-Pin Low Profile Package.	Smaller Foot Print.
■ 0.6 Micron Advance CMOS Process	Allowing a More Cost-Effective Solution.

GENERAL DESCRIPTION

The 86020 is a CardBus adapter integrated circuit that bridges existing bus interface logic chips to the CardBus architecture. CardBus, the newly adopted CardBus master interface is a subset of the electrical specification of the PCI (Personnel Computer Interconnect) standard. This CardBus device will support PCI Initiator or Target operation, 32-bit data path, 66 Mbytes per second transfer rates.

Two independent DMA channels have been included to perform DMA transfers to/from a local memory to a DMA requesting device. Local memory can be filled or emptied from the CardBus Host interface. The DMA operation can be controlled from the serial interface or the CardBus Host interface. The DMA channels source and destination addresses can be independently made to increment by byte, word, double word or stay in at one location.

DMA direction can be performed as defined below:

a) LPI to LPI device
b) LPI to CardBus device
c) CardBus to LPI device
d) CardBus to CardBus device.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

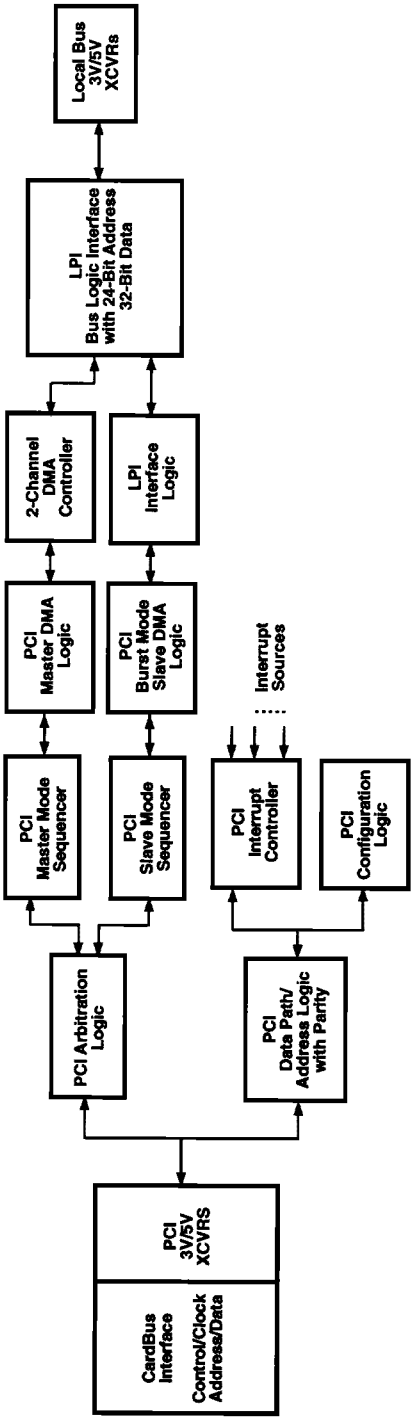

Figure 1. Z86020 Block Diagram

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GENERAL DESCRIPTION (Continued)

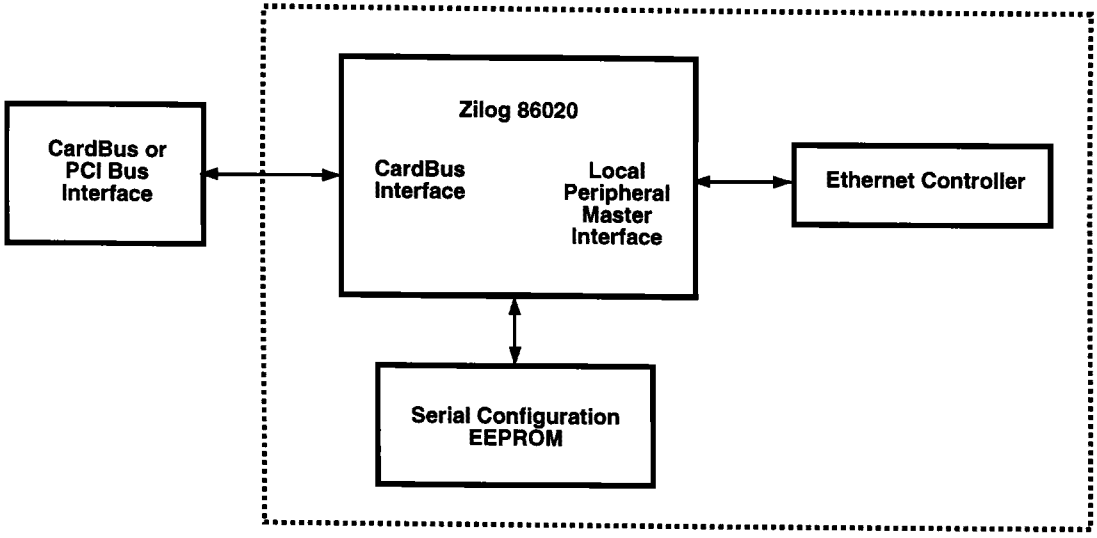

Figure 2. High-End Ethernet CardBus Card

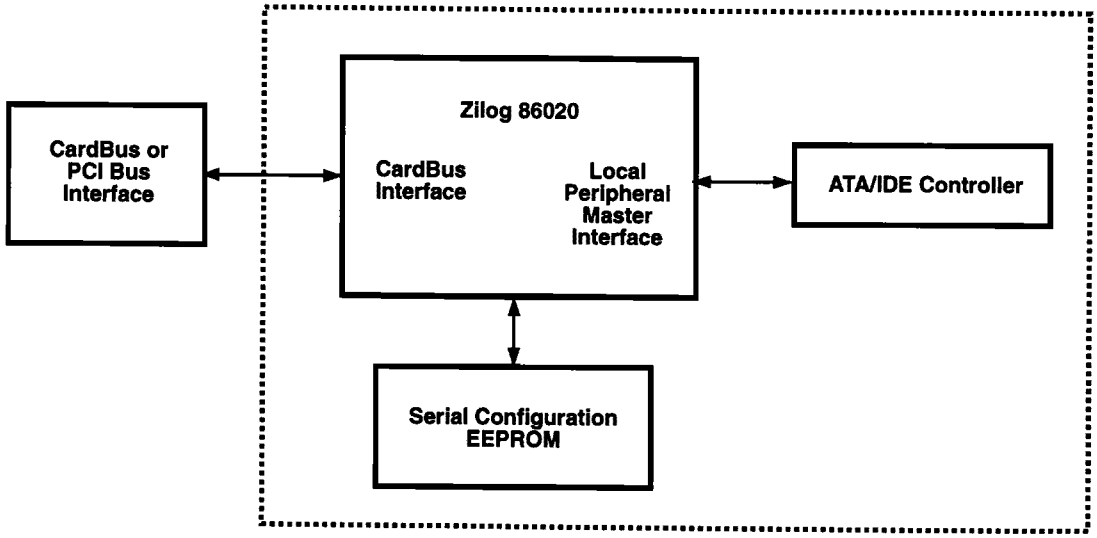

Figure 3. ATA/IDE CardBus Card

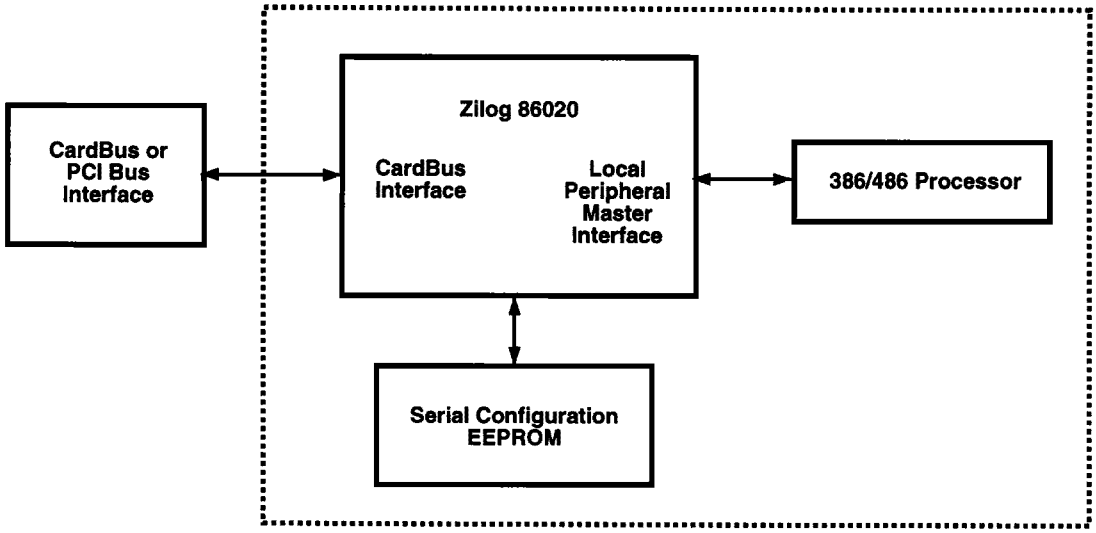

Figure 4. Local CPU CardBus Card

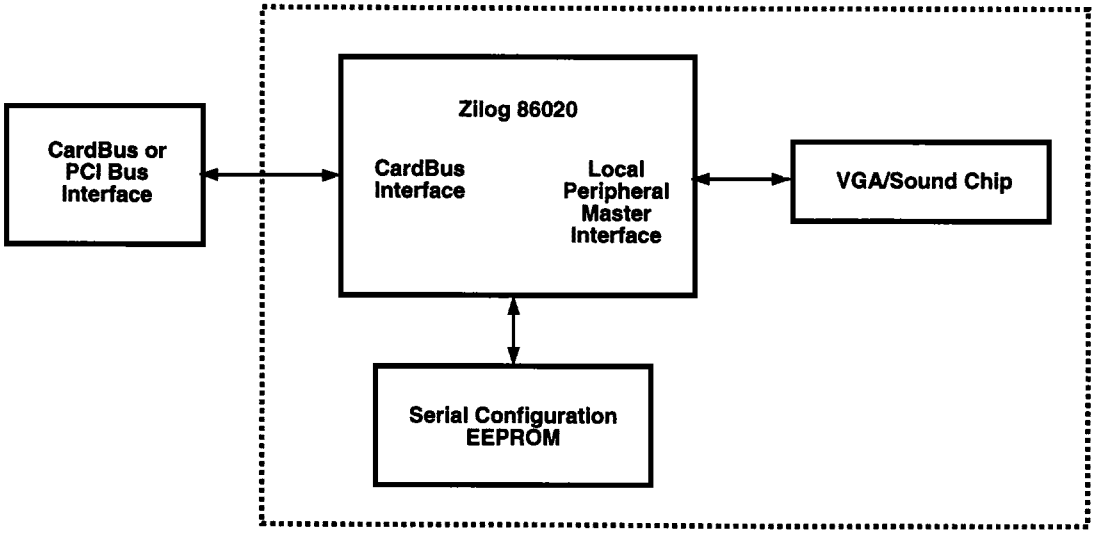

Figure 5. Multimedia CardBus Card

PIN DESCRIPTIONS

Table 1. Z86020 144-Pin Version

Item	Pin Name	Pin Function
1	'CAD0'	CardBus pin name: Address/data bus bit 11. Input/Output signal
2	'CAD1'	CardBus pin name: Address/data bus bit 1. Input/Output signal
3	'CAD2'	CardBus pin name: Address/data bus bit 2. Input/Output signal
4	'CAD3'	CardBus pin name: Address/data bus bit 3. Input/Output signal
5	'CAD4'	CardBus pin name: Address/data bus bit 4. Input/Output signal
6	'CAD5'	CardBus pin name: Address/data bus bit 5. Input/Output signal
7	'CAD6'	CardBus pin name: Address/data bus bit 6. Input/Output signal
8	'CAD7'	CardBus pin name: Address/data bus bit 7. Input/Output signal
9	'CAD8'	CardBus pin name: Address/data bus bit 8. Input/Output signal
10	'CAD9'	CardBus pin name: Address/data bus bit 9. Input/Output signal
11	'CAD10'	CardBus pin name: Address/data bus bit 10. Input/Output signal
12	'CAD11'	CardBus pin name: Address/data bus bit 11. Input/Output signal
13	'CAD12'	CardBus pin name: Address/data bus bit 12. Input/Output signal
14	'CAD13'	CardBus pin name: Address/data bus bit 13. Input/Output signal
15	'CAD14'	CardBus pin name: Address/data bus bit 14. Input/Output signal
16	'CAD15'	CardBus pin name: Address/data bus bit 15. Input/Output signal
17	'CAD16'	CardBus pin name: Address/data bus bit 16. Input/Output signal
18	'CAD17'	CardBus pin name: Address/data bus bit 17. Input/Output signal
19	'CAD18'	CardBus pin name: Address/data bus bit 18. Input/Output signal

Item	Pin Name	Pin Function
20	'CAD19'	CardBus pin name: Address/data bus bit 19. Input/Output signal
21	'CAD20'	CardBus pin name: Address/data bus bit 20. Input/Output signal
22	'CAD21'	CardBus pin name: Address/data bus bit 21. Input/Output signal
23	'CAD22'	CardBus pin name: Address/data bus bit 22. Input/Output signal
24	'CAD23'	CardBus pin name: Address/data bus bit 23. Input/Output signal
25	'CAD24'	CardBus pin name: Address/data bus bit 24. Input/Output signal
26	'CAD25'	CardBus pin name: Address/data bus bit 25. Input/Output signal
27	'CAD26'	CardBus pin name: Address/data bus bit 26. Input/Output signal
28	'CAD27'	CardBus pin name: Address/data bus bit 27. Input/Output signal
29	'CAD28'	CardBus pin name: Address/data bus bit 28. Input/Output signal
30	'CAD29'	CardBus pin name: Address/data bus bit 29. Input/Output signal
31	'CAD30'	CardBus pin name: Address/data bus bit 30. Input/Output signal
32	'CAD31'	CardBus pin name: Address/data bus bit 31. Input/Output signal
33	'CBE0*'	CardBus pin name: Command and byte enable bit 0
34	'CBE1*'	Command and byte enable bit 1.
35	'CBE2*'	Command and byte enable bit 2.
36	'CBE3*'	CardBus pin name: Command and Byte enable bit 3.
37	'CTRDY*'	Target Ready, Active low I/O pin.
38	'CIRDY*'	Initiator Ready, Active low I/O pin.
39	'CSERR*'	System Error.
40	'CBLOCK*'	CardBus lock, Active low I/O.
41	'CSTOP*'	CardBus Stop, Active low I/O.
42	'CDEVSEL*'	CardBus device select. Active Low I/O

PIN DESCRIPTIONS (Continued)

Item	Pin Name	Pin Function
43	'CREQ*'	CardBus pin name: CardBus request output. Used to request bus mastership.
44	'CVS2*'	CardBus, voltage sense input, bit 2
45	'CVS1*'	CardBus, voltage sense input, bit 1
46	'CAUDIO*'	CardBus, audio signal output.
47	'CSTSCHG*'	CardBus, status change output.
48	'CGNT*'	CardBus pin name: Card bus grant. Bus master output grant
49	'CRST*'	CardBus pin name: Card bus reset, active low input.
40	'CFRAME*'	CardBus pin name: CardBus frame signal. Input/output.
41	'CPERR*'	CardBus pin name: Parity Error. Input/output
42	'CIDSEL'	CardBus pin name: Identify Select bit. Input/Output signal.
43	'CINT*'	CardBus pin name: Interrupt output.
44	'CCLK'	CardBus pin name: CardBus clock, Input
45	'CPAR'	CardBus pin name: Even Parity bit
46	'LPI_HCS0'	Local Peripheral Interface, Chip select 0 output. This signal can be programmed low or high active
47	'LPI_HCS1A'	Local Peripheral Interface, Chip select 1A output. This signal can be programmed low or high active and also can be programmed to be active on LSB data transfers on a 32-bit wide peripheral bus.
48	'LPI_HCS1B'	Local Peripheral Interface, Chip select 1B output. This signal can be programmed low or high active and also can be programmed to be active on byte 1 data transfers on a 32-bit wide peripheral bus.
49	'LPI_HCS1C'	Local Peripheral Interface, Chip select 1A output. This signal can be programmed low or high active and also can be programmed to be active on byte 2 data transfers on a 32-bit wide peripheral bus.
50	'LPI_HCS1D'	Local Peripheral Interface, Chip select 1B output. This signal can be programmed low or high active and also can be programmed to be active on byte 3 data transfers on a 32-bit wide peripheral bus.

Item	Pin Name	Pin Function
51	'LPI_IREQ'	Local Peripheral Interface, interrupt request input.
52	'LPI_HIOR*'	Local Peripheral Interface, I/O read strobe, active low output.
53	'LPI_HIOW*'	Local Peripheral Interface, I/O write strobe, active low output.
54	'LPI_HRESET'	Local Peripheral Interface, Reset output.
55	'LPI_AD0/ LPI_DATA0'	Local Peripheral Interface, multiplexed address/databus I/O bit 0. Alternate pin definition: Local peripheral data bus bit 0.
56	'LPI_AD1/ LPI_DATA1'	Local Peripheral Interface, multiplexed address/databus I/O bit 1. Alternate pin definition: Local peripheral data bus bit 1.
57	'LPI_AD2/ LPI_DATA2'	Local Peripheral Interface, multiplexed address/data bus I/O bit 2. Alternate pin definition: Local peripheral data bus bit 2.
58	'LPI_AD3/ LPI_DATA3'	Local Peripheral Interface, multiplexed address/data bus I/O bit 3. Alternate pin definition: Local peripheral data bus bit 3.
59	'LPI_AD4/ LPI_DATA4'	Local Peripheral Interface, multiplexed address/data bus I/O bit 4. Alternate pin definition: Local peripheral data bus bit 4.
60	'LPI_AD5/ LPI_DATA5'	Local Peripheral Interface, multiplexed address/data bus I/O bit 5. Alternate pin definition: Local peripheral data bus bit 5.
61	'LPI_AD6/ LPI_DATA6'	Local Peripheral Interface, multiplexed address/data bus I/O bit 6. Alternate pin definition: Local peripheral data bus bit 6.
62	'LPI_AD7/ LPI_DATA7'	Local Peripheral Interface, multiplexed address/data bus I/O bit 7. Alternate pin definition: Local peripheral data bus bit 7.

PIN DESCRIPTIONS (Continued)

Item	Pin Name	Pin Function
63	'LPI_AD8/ LPI_DATA8'	Local Peripheral Interface, multiplexed address/data bus I/O bit 7. Alternate pin definition: Local peripheral data bus bit 8.
64	'LPI_AD9/ LPI_DATA9'	Local Peripheral Interface, multiplexed address/data bus I/O bit 9. Alternate pin definition: Local peripheral data bus bit 9.
65	'LPI_AD10/ LPI_DATA10'	Local Peripheral Interface, multiplexed address/data bus I/O bit 10. Alternate pin definition: Local peripheral data bus bit 10.
66	'LPI_AD11	Local Peripheral Interface, multiplexed address/data bus I/O bit 11. Alternate pin definition: Local peripheral data bus bit 11.
67	'LPI_AD12/ LPI_DATA12'	Local Peripheral Interface, multiplexed address/data bus I/O bit 12. Alternate pin definition: Local peripheral data bus bit 12.
68	'LPI_AD13/ LPI_DATA13'	Local Peripheral Interface, multiplexed address/data bus I/O bit 13. Alternate pin definition: Local peripheral data bus bit 13.
69	'LPI_AD14/ LPI_DATA14'	Local Peripheral Interface, multiplexed address/data bus I/O bit 14. Alternate pin definition: Local peripheral data bus bit 14.
70	'LPI_AD15/ LPI_DATA15'	Local Peripheral Interface, multiplexed address/data bus I/O bit 15. Alternate pin definition: Local peripheral data bus bit 15.
71	'LPI_DATA16'	Local Peripheral Interface, Local peripheral data bus bit 16.
72	'LPI_DATA17'	Local Peripheral Interface, Local peripheral data bus bit .
73	'LPI_DATA18'	Local Peripheral Interface, Local peripheral data bus bit.

Item	Pin Name	Pin Function
74	'LPI_DATA19'	Local Peripheral Interface, Local peripheral data bus bit .
75	'LPI_DATA20'	Local Peripheral Interface, Local peripheral data bus bit .
76	'LPI_DATA21'	Local Peripheral Interface, Local peripheral data bus bit .
77	'LPI_DATA22'	Local Peripheral Interface, Local peripheral data bus bit .
78	'LPI_DATA23'	Local Peripheral Interface, Local peripheral data bus bit .
79	'LPI_DATA24'	Local Peripheral Interface, Local peripheral data bus bit .
80	'LPI_DATA25'	Local Peripheral Interface, Local peripheral data bus bit .
81	'LPI_DATA26'	Local Peripheral Interface, Local peripheral data bus bit .
82	'LPI_DATA27'	Local Peripheral Interface, Local peripheral data bus bit .
83	'LPI_DATA28'	Local Peripheral Interface, Local peripheral data bus bit .
84	'LPI_DATA29'	Local Peripheral Interface, Local peripheral data bus bit .
85	'LPI_DATA30'	Local Peripheral Interface, Local peripheral data bus bit .
86	'LPI_DATA31'	Local Peripheral Interface, Local peripheral data bus bit .
87	'LPI_MRD*'	Local Peripheral Interface, memory read strobe, active low output.
88	'LPI_MWR*'	Local Peripheral Interface, memory write strobe, active low output.
89	'LPI_IOCHRDY'	Local Peripheral Interface, I/O channel ready input. Programmable active high or active low.
90	EE_CS	Serial interface chip select, active high. IN master mode, this is an output pin, in slave mode, this is an input pin.
91	'DRQ0'	DMA channel 0, data request 0. Active high input used to request a data transfer from the 86020's DMA controller.
92	'DACK0*'	DMA channel 0, data Acknowledge 0. Active low output used to acknowledge that a data transfer with the 86020's DMA controller and the peripheral device.
93	'DRQ1'	DMA channel 1, data request 1. Active high input used to request a data transfer from the 86020's DMA controller.
94	'DACK1*'	DMA channel 1, data Acknowledge 1. Active low output used to acknowledge that a data transfer with the 86020's DMA controller and the peripheral device.
95	'BSCK'	Master bus clock input.
96	'WACK*	Write acknowledge output. This signal is used to indicate that the CardBus host system has written data in the internal holding latches during remote DMA transfers.
97	'RACK*'	Read acknowledge output. This signal is used to indicate that the CARDBUS host system has read data from the internal holding latches during remote DMA transfers.

PIN DESCRIPTIONS (Continued)

Item	Pin Name	Pin Function
98	'PRD*'	Port read input. Used to enable data from the internal latch to the local bus during a memory write cycle to local memory and remote DMA operation.
99	'PWR*'	Port write input. Used to enable data from the internal latch to the local bus during a memory write cycle to local memory and remote DMA operation.
100	ADS	Address strobe, programmable active high or low output, or an input when the 015 is not mastering the local data bus. This signal is used to latch the address on the multiplexed address/data peripheral bus.
	AEN	Alternate pin definition: Address enable. Used to indicate when a DMA transfer is in progress. AEN is set high or low (Programmable)
101	'LPI_LADR23/ M_PINT'	Local peripheral interface, latched address output bit. Alternate pin definition: Local processor interrupt
102	'LPI_LADR22/ EE_SK'	Local peripheral interface, latched address output bit. Alternate pin definition: Serial clock output connect to Serial EEPROM clock input, or remote programming serial clock input.
103	'LPI_LADR21/ EE_DO'	Local peripheral interface, latched address output bit. Alternate pin definition: Serial data output connected to serial EEPROM data input or remote programming device input.
104	'LPI_LADR20/ EE_DI'	Local peripheral interface, latched address output bit. Alternate pin definition: Serial data input connected to EEPROM data output or remote programming device output
105	'LPI_LADR19/ EE_MASTER'	Local peripheral interface, latched address output bit. Alternate pin definition: After power on reset, the local peripheral address bus is not driven and this bit is sampled as: Pulled up: Serial bus is master. The 86020 will initiate all writing to a local serial EEPROM
106	'LPI_LADR18/ EXT_PROM*'	Local peripheral interface, latched address output bit. Alternate pin definition: On power on reset, this pin is sampled to determine the method of reading the configuration memory. If the line is tied low during power on, the 86020 will fetch all internal programming information from an external prom, and all configuration memory fetches will be done in the external parallel (8-bit) prom. The prom size can be up to 64 Kbytes deep

Item	Pin Name	Pin Function
107	'LPI_LADR17'	Local peripheral interface, latched address output bit.
108	'LPI_LADR16'	Local peripheral interface, latched address output bit.
109	'LPI_LADR15'	Local peripheral interface, latched address output bit.
110	'LPI_LADR14'	Local peripheral interface, latched address output bit.
111	'LPI_LADR13'	Local peripheral interface, latched address output bit
112	LPI_LADR12'	Local peripheral interface, latched address output bit
113	'LPI_LADR11'	Local peripheral interface, latched address output bit
114	'LPI_LADR10'	Local peripheral interface, latched address output bit
115	'LPI_LADR9'	Local peripheral interface, latched address output bit
116	'LPI_LADR8'	Local peripheral interface, latched address output bit
117	'LPI_LADR7'	Local peripheral interface, latched address output bit
118	'LPI_LADR6'	Local peripheral interface, latched address output bit
119	'LPI_LADR5'	Local peripheral interface, latched address output bit 5.
120	'LPI_LADR4'	Local peripheral interface, latched address output bit 4.
121	'LPI_LADR3'	Local peripheral interface, latched address output bit 3.
122	'LPI_LADR2'	Local peripheral interface, latched address output bit 2.
123	'LPI_LADR1'	Local peripheral interface, latched address output bit 1.
124	'LPI_LADR0'	Local peripheral interface, latched address output bit 0..
125	'BACK'	Bus Acknowledge. Output signal granting peripheral master device on the peripheral bus permission to acquire the bus
126	'BREQ'	Bus request. Input signal from the peripheral master device requesting the local peripheral bus
127	'SELECT'	When master has on the LPI interface has requested the bus and it is granted, the local peripheral can access the CardBus interface whenever the SELECT single is set.
128	'BUSWIDE0'	Input bus bit 0, indicates peripheral is: Buswide<1:0> 00 Byte wide, lsb 01 Word wide, 11 32 bits wide
129	'BUSWIDE1'	Input bus bit 0, indicates peripheral is: Buswide<1:0> 00 Byte wide, lsb 01 Word wide, 11 32 bits wide
130	'RING_IN'	Ring indicate input
131	'PACKET_IN'	Packet Indicate input.
132	'AUDIO_IN'	Audio Input Pin

PIN DESCRIPTIONS (Continued)

Item	Pin Name	Pin Function
133	V_{DD}	Power pin
134	V_{DD}	Power pin
135	V_{DD}	Power pin
136	VDD	Power pin
137	V_{SS}	Ground pin
138	V_{SS}	Ground pin
139	V_{SS}	Ground pin
140	V_{SS}	Ground pin
141	V_{SS}	Ground pin
142	V_{SS}	Ground pin
143	EXP_CS	Expansion ROM Chip select
144	Reserved	

**Note: actual pin out of this device is to be defined