mosaic

Mosaic Semiconductor Inc.

# PUMA 2U4002

## PUMA 2U4002-45/55/70/90

Issue 1.0 : February 1990

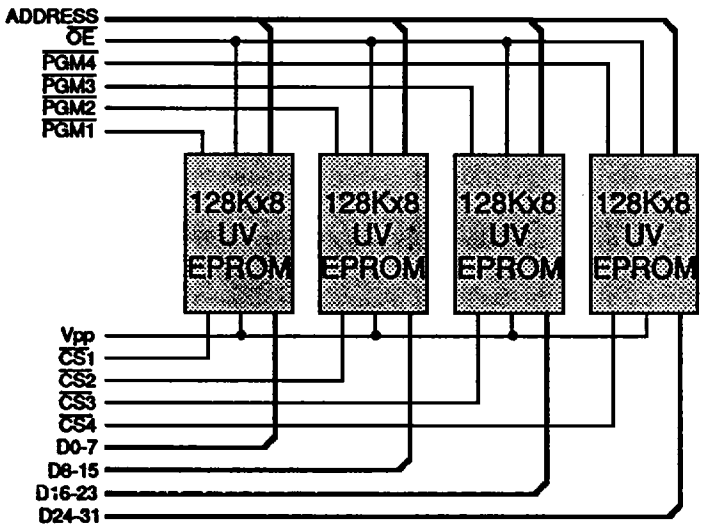
## ADVANCE PRODUCT INFORMATION

4,194,304 bit CMOS High Speed UVEPROM

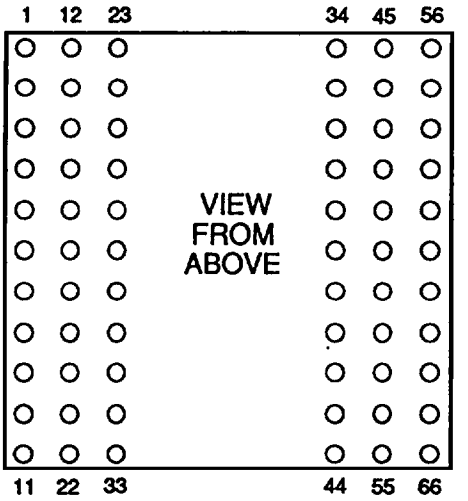
### Features

Very Fast Access times of 55/70/90 ns
(45 ns Under Development)
Pin grid array gives 2:1 improvement over DIL
Package Suitable for Thermal Ladder Applications
On board decoupling capacitors
Configurable as 8 / 16 / 32 bit wide
Operating Power 305 / 370 / 500 mW (typ)
Standby Power 200 mW (typ)
$V_{PP}$ Voltage of 12.5V
Complete Device Programming in 30 sec. (typ)
May be screened in accordance with MIL-STD-883C

### Block Diagram




### Pin Definition

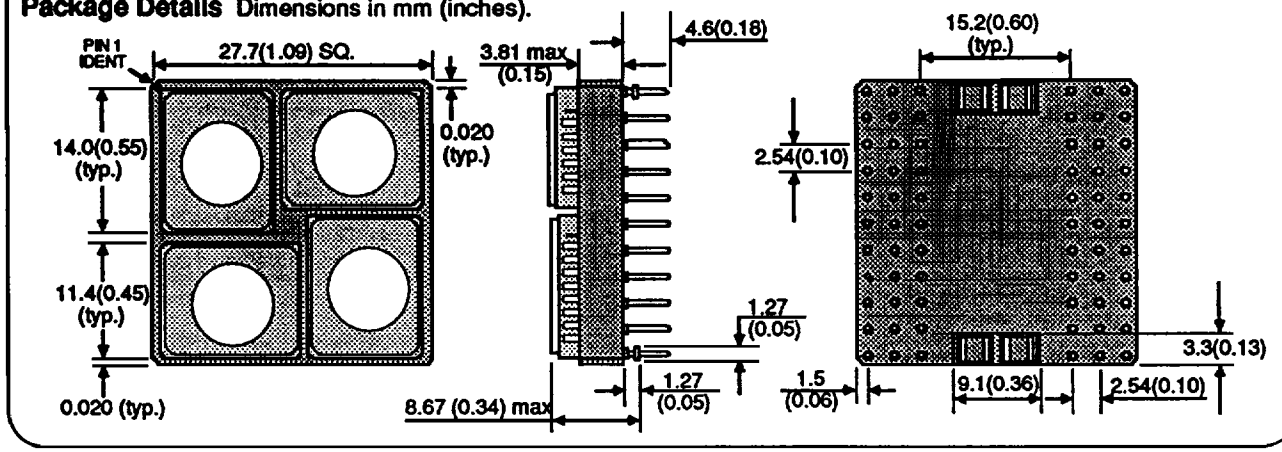



See page 5 for pinout

### Pin Functions

| | |
|---|---|
| A0 - A16 | Address Inputs |
| D0 - D31 | Data Inputs/Outputs |
| $\overline{CS1\text{-}4}$ | Chip Select |
| $\overline{OE}$ | Output Enable |
| $\overline{PGM1\text{-}4}$ | Program Enable |
| NC | No Connect |
| $V_{PP}$ | Programming Voltage |
| $V_{CC}$ | Power (+5V) |
| GND | Ground |

### Package Details Dimensions in mm (inches).




MOSCS107

## Absolute Maximum Ratings (1,2)

| | | | | |
|---|---|---|---|---|
| Voltage on pins $V_{PP}$ and $A_9$ (3) | $V_{TPP}$ | -0.6V to +13.5 | V | |
| Voltage on pin $V_{CC}$ (3) | $V_{TCC}$ | -0.6V to + 7.0 | V | |
| Voltage on any other pins (3) | $V_T$ | -0.6V to $+V_{CC}$+0.5 | V | |
| Power Dissipation | $P_T$ | 2 | W | |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C | |

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) With respect to GND.
(3) Pulse width:- 2.0V for less than 10ns.

## Recommended Operating Conditions

| | | *min* | *typ* | *max* | |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | - | $V_{CC}$+0.5 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | - | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | - | 70 | °C (2U4000) |
| | $T_{AI}$ | -40 | - | 85 | °C (2U4000I) |
| | $T_{AM}$ | -55 | - | 125 | °C (2U4000M, MB) |

## DC Electrical Characteristics ($V_{CC}$=5V±10%,$T_A$=-55°C to +125°C)

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ*(1) | *max* | *Unit* | *Notes* |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$=0V to $V_{CC}$ | -4 | - | 4 | µA | |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$=0V to $V_{CC}$ | -40 | - | 40 | µA | (2) |
| $V_{PP}$ Leakage Current | $I_{PP}$ | $\overline{CS}$=OE=$V_{IL}$, $V_{PP}$=$V_{CC}$ | - | - | 400 | µA | |
| Average Supply Current | | $\overline{CS}$=$V_{IL}$, $f$=10MHz, $I_{OUT}$=10mA | | | | | (2) |
| | $I_{CC32}$ | 32 BIT MODE | - | - | 240 | mA | |
| | $I_{CC16}$ | 16 BIT MODE | - | - | 190 | mA | |
| | $I_{CC8}$ | 8 BIT MODE | - | - | 165 | mA | |
| Standby Supply Current | $I_{SB}$ | CS=$V_{IH}$ | - | - | 140 | mA | (2) |
| Output Voltage Low | $V_{OL}$ | $I_{OL}$=8.0mA | - | - | 0.45 | V | |
| Output Voltage High | $V_{OH}$ | $I_{OH}$=-4.0mA | 2.4 | - | - | V | |

Notes: (1) Typical values are at $V_{CC}$=5.0V,$T_A$=25°C and specified loading.
(2) CS above is accessed through CS1-4 These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

## Capacitance ($V_{CC}$=5V±10%,$T_A$=25°C)

| *Parameter* | | *Symbol* | *Test Condition* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| Input Capacitance | Address, $\overline{OE}$ | $C_{IN1}$ | $V_{IN}$=0V | 28 | 36 | pF |
| | $\overline{PGM1-4}$, $\overline{CS1-4}$ | $C_{IN2}$ | $V_{IN}$=0V | 7 | 9 | pF |
| I/O Capacitance | 32 Bit Mode | $C_{IO}$ | $V_{IO}$=0V | 6 | 9 | pF |

Note: This parameter is calculated and not measured.

## AC Test Conditions

*Input pulse levels: 0.0V to 3.0V
*Input rise and fall times: 5 ns
*Input and Output timing reference levels: 1.5V
*Output load: 1 TTL gate + 100pF
*$V_{CC}$=5V±10%

## Operating Modes

The Table below shows the logic inputs required to control the operating modes of each of the UV EPROMs on the PUMA 2U4002.

| MODE | | $\overline{CS}$ | $\overline{OE}$ | $\overline{PGM}$ | $A_0$ | $A_9$ | $V_{PP}$ | OUTPUTS |
|---|---|---|---|---|---|---|---|---|
| Read | | $V_{IL}$ | $V_{IL}$ | X | X | X | $V_{IH}$ | $D_{OUT}$ |
| Output Disable | | $V_{IL}$ | $V_{IH}$ | X | X | X | $V_{IH}$ | High Z |
| Standby | | $V_{IH}$ | X | X | X | X | $V_{IH}$ | High Z |
| Program | | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | $V_{PP}$ | $D_{IN}$ |
| Program Verify | | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | $V_{PP}$ | $D_{OUT}$ |
| Program Inhibit | | $V_{IH}$ | X | X | X | X | $V_{PP}$ | High Z |
| Identifier (NOTE 1) | Manufacturer | $V_{IL}$ | $V_{IL}$ | X | $V_{IL}$ | $V_H$ | $V_{CC}$ | $01_H$ |
| | Device Code | $V_{IL}$ | $V_{IL}$ | X | $V_{IH}$ | $V_H$ | $V_{CC}$ | $0E_H$ |

$V_H$=12.0V±0.5V
X=$V_{IH}$ or $V_{IL}$
A1-A8=A10-A16=$V_{IL}$

Notes (1) A1 - A8 = A10 - A16 = $V_{IL}$
(2) $\overline{CS}$ is accessed through $\overline{CS1\text{-}4}$, and PGM is accessed through $\overline{PGM1\text{-}4}$. For correct operation, $\overline{CS1\text{-}4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{PGM1\text{-}4}$ must also be operated in the same manner.

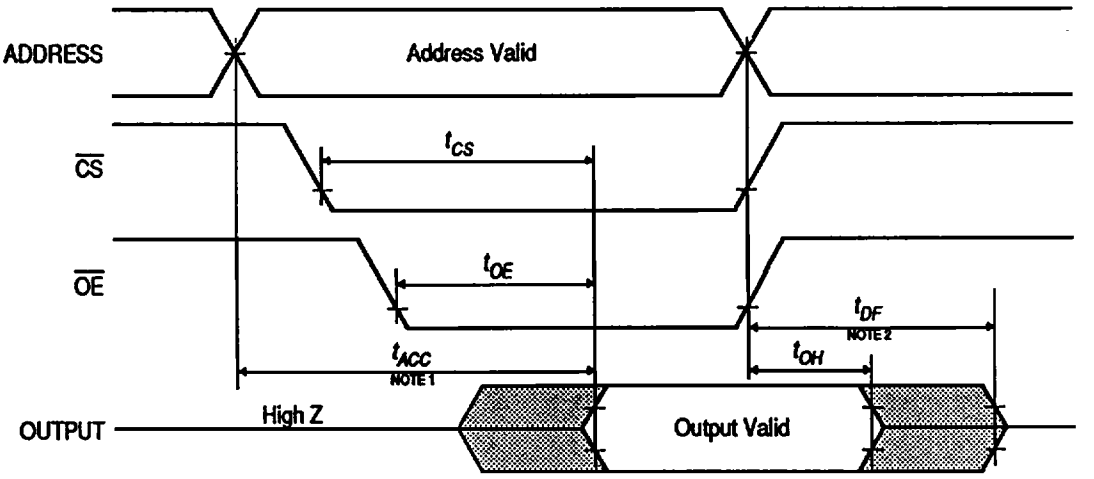
## Electrical Characteristics & Recommended AC Operating Conditions

### Read Cycle (1,3)

| Parameter | Symbol | -45 min | -45 max | -55 min | -55 max | -70 min | -70 max | -90 min | -90 max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Address to Output Delay | $t_{ACC}$ | | | - | 55 | - | 70 | - | 90 | ns |
| Chip Select Access Time | $t_{CE}$ | | TBA | - | 55 | - | 70 | - | 90 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | | - | 25 | - | 35 | - | 40 | ns |
| Chip Deselect to O/P high Z (2) | $t_{DF}$ | | | 0 | 25 | 0 | 35 | 0 | 40 | ns |
| Output Hold from Address Change | $t_{OH}$ | | | 0 | - | 0 | - | 0 | - | ns |

Notes (1) $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
(2) This parameter is sampled, not 100% tested.
(3) **CAUTION:**The PUMA 2U4002 must not be removed from (or inserted into) a socket when $V_{PP}$ or $V_{CC}$ is applied.

### Read Cycle Timing Waveform




Notes: (1) $\overline{OE}$ may be delayed up to $t_{ACC}$-$t_{OE}$ after the falling edge of $\overline{CS}$ without impact on $t_{ACC}$.
(2) $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first.

## PROGRAMMING OPERATION

### DC Electrical Characteristics ($V_{CC}$=6.25V±0.25V,$V_{PP}$=12.75V±0.25V,$T_A$=25°C±5°C)

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ*(1) | *max* | *Unit* | *Notes* |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$=0V to $V_{CC}$ | -40 | - | 40 | µA | |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$=0V to $V_{CC}$ | -40 | - | 40 | µA | (2) |
| Program Supply Current | $I_{CC32}$ | 32 BIT MODE | - | - | 200 | mA | |
| | $I_{CC16}$ | 16 BIT MODE | - | - | 170 | mA | |
| | $I_{CC8}$ | 8 BIT MODE | - | - | 155 | mA | |
| $V_{PP}$ Supply Current | $I_{PP1}$ | $\overline{CS}$=$V_{IL}$, OE=$V_{IH}$, 32 BIT MODE | - | - | 120 | mA | (1) |
| Identifier Select Voltage | $V_H$ | | 11.5 | - | 12.5 | V | |
| Programming Voltage | $V_{PP}$ | | 12.5 | - | 13.0 | V | |
| Supply Voltage | $V_{CC1}$ | | 6.0 | - | 6.5 | V | |
| Output Voltage Low | $V_{OL}$ | $I_{OL}$=8.0mA | - | - | 0.45 | V | |
| Output Voltage High | $V_{OH}$ | $I_{OH}$=-4.0mA | 2.4 | - | - | V | |

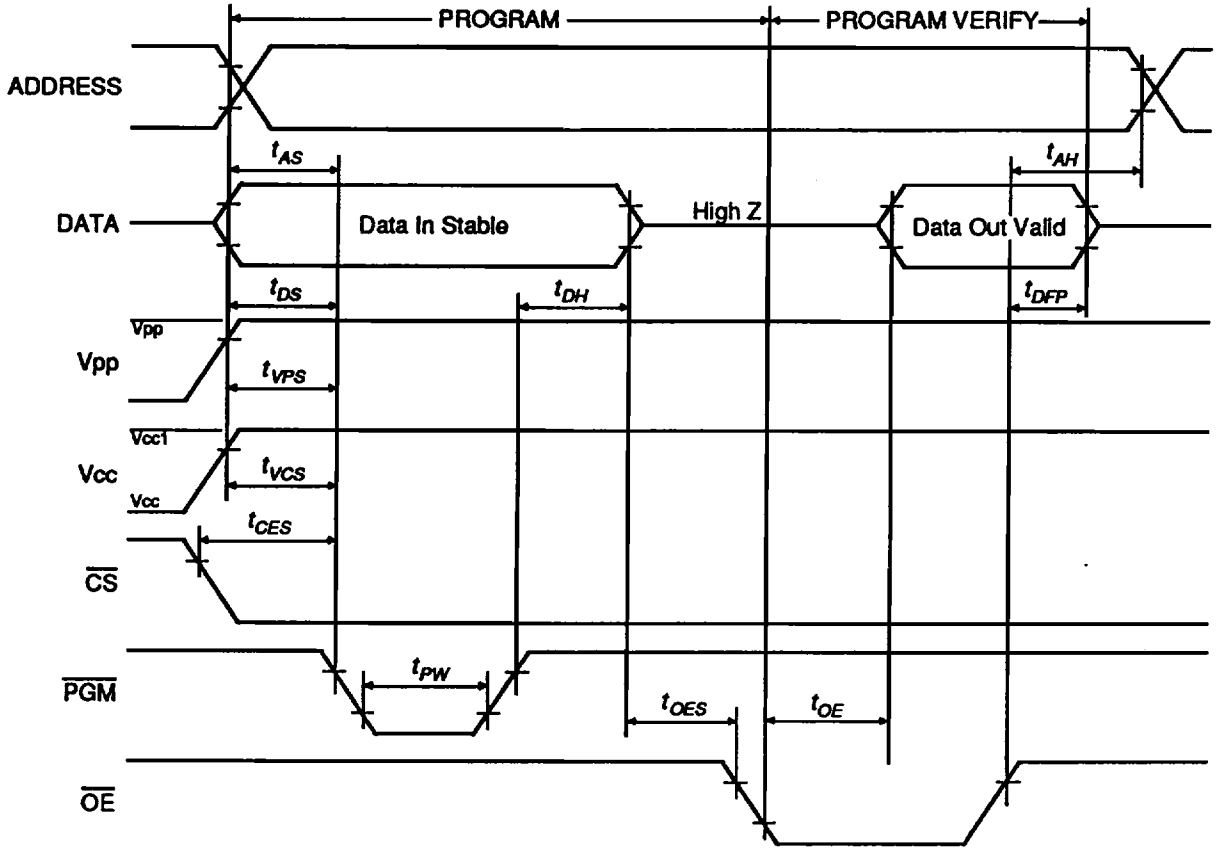
Notes: (1) $\overline{CS}$ above is accessed through $\overline{CS1-4}$ These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

### AC Characteristics (1,2,3)

| *Parameter* | *Symbol* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|
| Address Setup Time | $t_{AS}$ | 2 | - | - | µs |
| $\overline{OE}$ Setup Time | $t_{OES}$ | 2 | - | - | µs |
| Data Setup Time | $t_{DS}$ | 2 | - | - | µs |
| Address Hold Time | $t_{AH}$ | 0 | - | - | µs |
| Data Hold Time | $t_{DH}$ | 2 | - | - | µs |
| $\overline{OE}$ High to Output Float Delay | $t_{DFP}$ | 0 | - | 130 | ns |
| $V_{PP}$ Setup Time | $t_{VPS}$ | 2 | - | - | µs |
| $\overline{PGM}$ Pulse Width | $t_{PW}$ | 95 | - | 105 | µs |
| $V_{CC}$ Setup Time | $t_{VCS}$ | 2 | - | - | µs |
| $\overline{CS}$ Setup Time | $t_{CES}$ | 2 | - | - | µs |
| Data Valid from $\overline{OE}$ | $t_{OE}$ | - | - | 150 | ns |

Notes (1) $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
(2) When programming the PUMA 2U4002 a 0.1µF capacitor is required across $V_{PP}$ and GND to suppress noise transients which may damage the module.
(3) Programming characteristics are sampled but not 100% tested at worst case conditions.

## Programming Cycle Timing Waveform



## High Performance Programming Algorithm

The PUMA2U4002 can be programmed using the alogorithm shown here. This allow faster programming times without stressing the device or causing deterioration in Data Retention Time.

Although the flow chart specifically refers to a single EPROM, all four devices on the PUMA tile can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode. Obviously 32 bit mode is potentially the fastest programming time, but this makes greater demands on the $V_{PP}$ Supply Current as shown on the Programming Operation DC Characteristics on page 4.

## Programming

Upon delivery, or after each erasure, the PUMA 2U4002 has all 4,194,304 bits in the ONE or HIGH state. ZEROs are loaded into the devices through the procedure of programming.

This mode is entered when 12.75V±0.25V is applied to the $V_{PP}$ pin, CS and $\overline{PGM}$ are at $V_{IL}$ and $\overline{OE}$ is at $V_{IH}$, as shown on the Table on page 2. Data may be applied in 8, 16 or 32 bits in parallel depending on how $\overline{CS1-4}$ and $\overline{PGM1-4}$ are controlled.

The algorithm reduces programming time by using 100µs pulses followed by byte verification to determine if the byte has been successfully programmed. If the data does not verify, up to 25 such pulses can be applied, after which, if verification fails, programming stops. This proccess is repeated for each memory location within the PUMA 2U4002.

This algorithm programs at $V_{CC}$=6.25V and $V_{PP}$=12.75V. After programming is complete, all bytes are compared with the original data with $V_{CC}$=$V_{PP}$=5.25V.

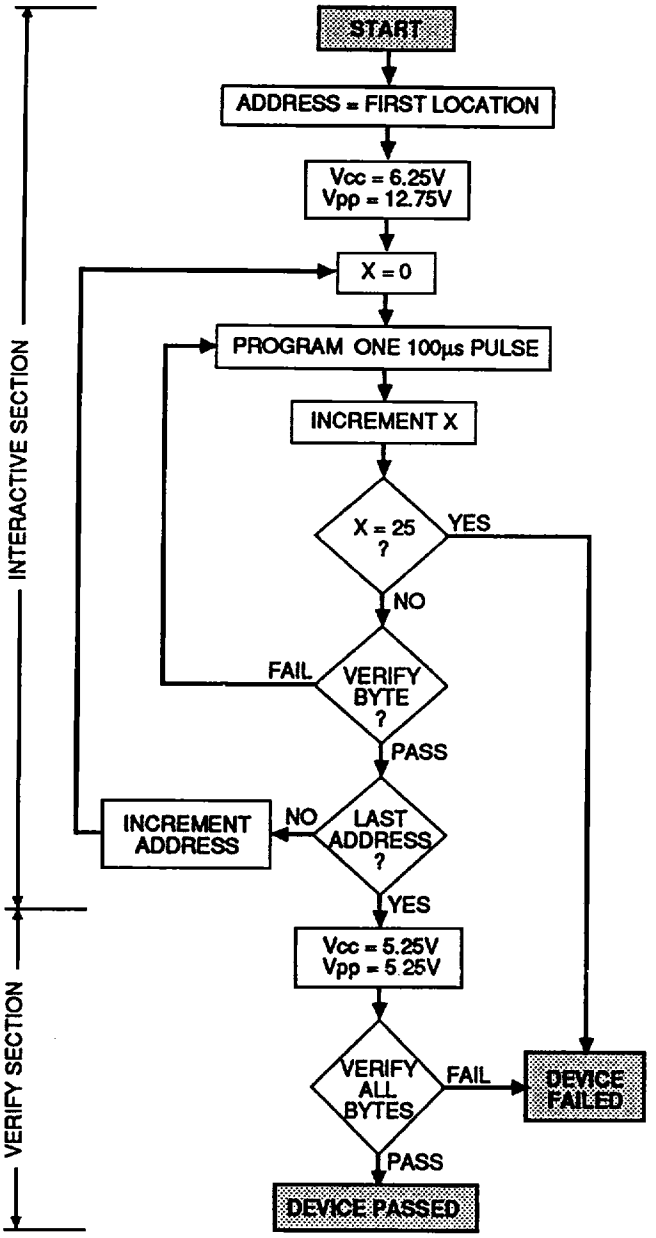
In order to overcome the voltage drop caused by the inductive effects of the printed circuit board on which the PUMA 2U4002 module is used, it is recommended that a 4.7µF electrolytic capacitor is used between $V_{CC}$ and GND for every two PUMA modules. This capacitor should be placed close to the point where the power supply is routed to the UV EPROM array.

## ERASE

Complete erasure of the devices used on the PUMA 2U4002 is performed by exposure to an ultraviolet light source giving a dosage of 15WS/cm². This dosage can be obtained by using an ultraviolet lamp with a wavelength of 2537 Å at a minimum intensity of 12,000µW/cm², for approximately 15 - 20 minutes. The PUMA 2U4002 should be directly under and about 1 inch from the light source.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. Although erasure times will be much longer at these levels, the transparent lids on this module should be covered with an opaque label to realise maximum system reliability.

## Programming Algorithm Flowchart




**NOTE: THE ALGORITHM SHOWN HERE MUST BE USED TO ENSURE CORRECT PROGRAMMING OF THE PUMA 2U4002; THIS MAXIMISES THE DATA RETENTION TIME OF THE UV EPROMS AND DOES NOT STRESS THE MEMORY CELL..**

**PUMA2U4002 BASED ON AMD AM27H010 DEVICE**

## Connection Table

| PGA Pin No. | Signal Name | PGA Pin No. | Signal Name | PGA Pin No. | Signal Name | PGA Pin No. | Signal Name | PGA Pin No. | Signal Name |
|---|---|---|---|---|---|---|---|---|---|
| 1 | D8 | 2 | D9 | 3 | D10 | 4 | A14 | 5 | A16 |
| 6 | A11 | 7 | A0 | 8 | NC | 9 | D0 | 10 | D1 |
| 11 | D2 | 12 | $\overline{PGM2}$ | 13 | $\overline{CS2}$ | 14 | GND | 15 | D11 |
| 16 | A10 | 17 | A9 | 18 | A15 | 19 | $V_{CC}$ | 20 | $\overline{CS1}$ |
| 21 | NC | 22 | D3 | 23 | D15 | 24 | D14 | 25 | D13 |
| 26 | D12 | 27 | $\overline{OE}$ | 28 | NC | 29 | $\overline{PGM1}$ | 30 | D7 |
| 31 | D6 | 32 | D5 | 33 | D4 | 34 | D24 | 35 | D25 |
| 36 | D26 | 37 | A7 | 38 | A12 | 39 | $V_{PP}$ | 40 | A13 |
| 41 | A8 | 42 | D16 | 43 | D17 | 44 | D18 | 45 | $V_{CC}$ |
| 46 | $\overline{CS4}$ | 47 | $\overline{PGM4}$ | 48 | D27 | 49 | A4 | 50 | A5 |
| 51 | A6 | 52 | $\overline{PGM3}$ | 53 | $\overline{CS3}$ | 54 | GND | 55 | D19 |
| 56 | D31 | 57 | D30 | 58 | D29 | 59 | D28 | 60 | A1 |
| 61 | A2 | 62 | A3 | 63 | D23 | 64 | D22 | 65 | D21 |
| 66 | D20 | | | | | | | | |

## Military Screening Procedure

**Module Screening Flow** for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

| MB MODULE SCREENING FLOW | | |
|---|---|---|
| *SCREEN* | *TEST METHOD* | *LEVEL* |
| **Visual and Mechanical** | | |
| External visual | 2017 Condition B (or manufacturers equivalent) | 100% |
| Temperature cycle | 1010 Condition C (10 Cycles,-65°C to +150°C) | 100% |
| **Burn-in** | | |
| Pre Burn-in Electrical | Per Applicable device Specifications at $T_A$ = +25°C (optional) | 100% |
| Burn-in | Method 1015, Condition D, $T_A$ = +125°C | 100% |
| **Final Electrical Tests** | Per applicable Device Specification | |
| Static (dc) | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Functional | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Switching (ac) | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| **Percent Defective Allowable (PDA)** | Calculated at Post Burn-in at $T_A$=+25°C | 10% |
| **Quality Conformance** | Per applicable Device Specification | Sample |
| **External Visual** | 2009 Per vendor or customer specification | |

## Ordering Information

**PUMA 2U4002MB-55**

| | | |
|---|---|---|
| Speed | 45 | = Under Development |
| | 55 | = 55 ns |
| | 70 | = 70 ns |
| | 85 | = 85 ns |
| Temp. range/screening | Blank | = Commercial Temp. |
| | I | = Industrial Temp. |
| | M | = Military Temp. |
| | MB | = Screened in accordance with MIL-STD 883C |
| Memory Type | U4002 | = 128K x 32 UV EPROM (user configurable as 256Kx16 or 512 Kx8) |

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