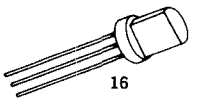
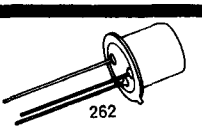
SILICON UNILATERAL AND BILATERAL SWITCHES
(SUS, SBS)


16


262

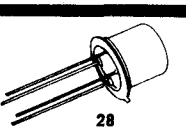
The General Electric SUS is a silicon, planar monolithic integrated circuit having thyristor electrical characteristics closely approximating those of an "ideal" four-layer diode. The device is designed to switch at 8 volts with a typical temperature coefficient of 0.02%/°C. A gate lead is provided to eliminate rate effect, obtain triggering at lower voltages, and to obtain transient-free waveforms.

The SBS is a bilateral version of the forward characteristics of the SUS. It provides excellently matched characteristics in both directions with the same low temperature coefficient.

	GE Type	V_{ACR} Reverse Voltage Max. (V)	I_F Continuous Forward Current Max. (mA)	I_F Peak Recurrent Forward Current @ 100°C, 10 μs, 1% duty cycle (A)	P_T Dissipation (mW)	T_C Temperature Coefficient of Switching Voltage (%/°C)	V_S Switching Voltage Min. (V)	V_S Switching Voltage Max. (V)	I_S Switching Current Max. (μA)	I_B Forward Blocking Current @ 5V (μA)	V_F Forward Voltage @ 200mA (V)	I_H Holding Current (mA)	V_O Peak Pulse Voltage Min. (V)	Package
Unilateral	2N4987	30	175	1.0	300	—	6	10	500	1.0	1.5	1.5	3.5	16
	2N4988	30	200	1.0	350	±.05	7.5	9	150	0.1	1.5	.5	3.5	
	2N4989	30	200	1.0	350	±.02	7.5	8.2	300	0.01	1.5	1.0	3.5	H
	2N4990	30	175	1.0	300	—	7	9	200	0.1	1.5	.75	3.5	
	2N4983	30	175	1.0	300	—	6	10	500	1.0	1.5	1.5	3.5	G
	2N4984	30	200	1.0	350	±.05	7.5	9	150	0.1	1.5	.5	3.5	
	2N4985	30	200	1.0	350	±.02	7.5	8.2	300	0.01	1.5	1.0	3.5	262
	2N4986	30	175	1.0	300	—	7	9	200	0.1	1.5	.75	3.5	
Bilateral	2N4991	—	175	1.0	300	—	6	10	500	1.0	1.7	1.5	3.5	16
	2N4992	—	200	1.0	350	±.05	7.5	9	120	0.1	1.7	.5	3.5	
	2N4993	—	175	1.0	300	—	6	10	500	1.0	1.7	1.5	3.5	262

SILICON CONTROL SWITCHES
(SCS)

High triggering sensitivity. 4 lead capability for multiple load or dv/dt suppression.


28

						Cutoff Characteristics	Conducting Characteristics	Max. Gate Ratings		Gate triggering Characteristics					
GE Type	V_{AK} Anode Voltage Blocking (V)	I_F Continuous DC Forward Current (mA)	Peak Recurrent Forward Current @ 100μsec (A)	Cathode Gate Peak Current (mA)	P_T (mW)	I_B @ V_{AK} R_{GK}= 10KΩ 150°C (μA)	I_H R_{GK}= 10KΩ (mA)	V_{GK} I_{GK}= 20μA (V)	V_{GA} I_{GA}= 1μA (V)	I_{GTK} @ V_{AK}=40V, R_L=800Ω, R_{GA}=∞ (μA)	V_{GTK} (V)	I_{GTA} @ V_{AK}=40V, R_L=800Ω, R_{GK}=10K (mA)	V_{GTA} (V)	Package
3N81	65	200	1.0	500	400	20	1.5	5	65	1.0	.4 to .65	1.5	—.4 to —.8	28
3N82	100	200	1.0	500	400	20	1.5	5	100	1.0	.4 to .65	1.5	—.4 to —.8	28
3N83	70	50	0.1	50	200	20 *	4.0 †	5	70	150 †	.4 to .80	—	—	28
3N84	40	175	0.5	100	320	20 *	2.0	5	40	10	.4 to .65	—	—	28
3N85	100	175	0.5	100	320	20 *	2.0	5	100	10	.4 to .65	—	—	28
3N86	65	200	1.0	500	400	20	0.2	5	65	1.0	.4 to .65	0.1	—.4 to —.8	28

* Measured @125°C. † Measured in special test circuit (See specification sheet).

ADDITIONAL REFERENCE PUBLICATIONS
ORDER BY PUBLICATION NUMBER

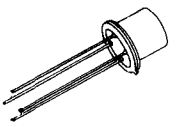
90.10 The Unijunction Transistor Characteristics and Applications
90.12 Unijunction Temperature Compensation
90.19 Unijunction Frequency Divider
90.70 The D13T—A Programmable Unijunction Transistor
90.72 Complementary Unijunction Transistors

Silicon Control Switch

PNPN 3N81,2

The General Electric Types 3N81 and 3N82 are PLANAR PNPN silicon controlled switches (SCS) offering outstanding circuit design flixibility by providing leads to all four semiconductor regions. Unique fabrication processes based on planar oxide passivation have resulted in high reliability and uniformity at low cost. The SCS is thoroughly characterized at temperature extremes to permit worst-case circuit design.

Types 3N81 and 3N82 can be considered an integrated PNP-NPN transistor pair in a positive feedback configuration. As such they offer fewer connections, fewer parts, lower cost and better characterization than are available from two separte transistors. Their characterization permits them to be used as an extremely sensitive SCR, as a complementary SCR, or as a "transistor" with "latching" capabilities.

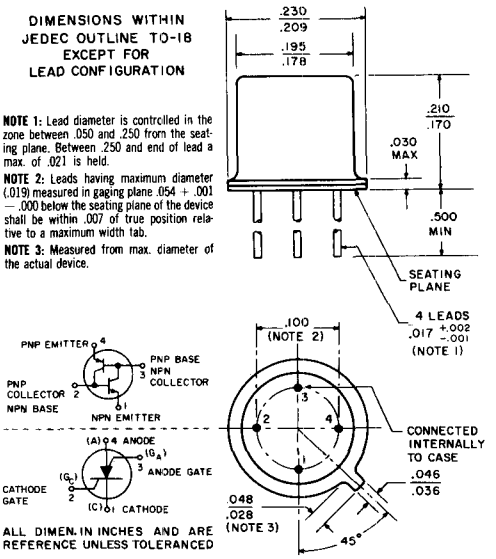


FEATURES:

- **Completely eliminates rate effect problems**
- **Dynamic and static breakover voltages are identical**
- **Extremely high triggering sensitivity**
- **Design parameters specified at worst-case temperatures**
- **Characterized for SCR and complementary SCR type applications**
- **Characterized as PNPN and also as transistor integrated pair**
- **All planar, completely oxide passivated**
- **Leads to all four semiconductor regions**

absolute maximum ratings:[1] (25°C) (unless otherwise specified)

	3N81	3N82	
Voltage			
Anode to cathode forward and reverse	65	100	volts
Anode gate to anode reverse	65	100	volts
Cathode gate to cathode reverse	5	5	volts
Total Current			
Continuous DC forward[2]	200	200	ma
Peak recurrent forward ($T_A = 100°C$, 100 μsec. pulse width, 1% duty cycle)	1.0	1.0	amps
Peak non-recurrent forward (10 μsec. pulse width)	5.0	5.0	amps
Gate Current (Forward Bias)			
Continuous DC anode gate	100[2]	100[2]	ma
Peak anode gate ($T_A = 100°C$, 100 μsec. pulse width, 1% duty cycle)	200	200	ma
Peak cathode gate ($T_A = 100°C$, 100 μsec. pulse width, 1% duty cycle)	500	500	ma
Continuous DC cathode gate	20	20	ma
Dissipation			
Total power[2]	400	400	mw
Cathode gate power[2]	100	100	mw
Temperature			
Operating junction	−65 to +150		°C
Storage	−65 to +200		°C

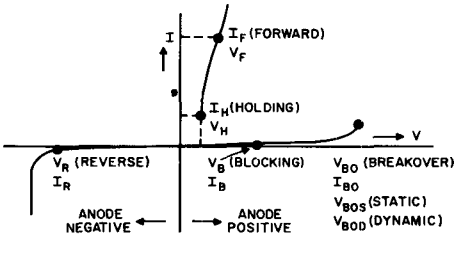


NOTE 1: Symbols and nomenclature are defined below.

NOTE 2: Derate currents and power linearly to 150°C, the maximum rated temperature. The absolute maximum rating at any given temperature shall be in terms of the more conservative of the two parameters, i.e. current or power.

definition of terms used in scs specifications

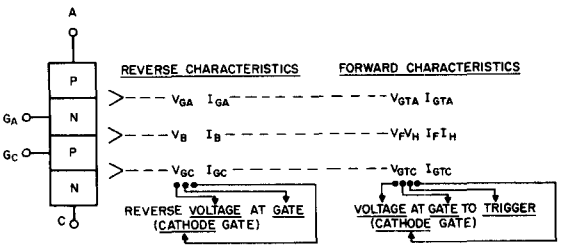
PNPN devices available at present do not have a common nomenclature. In part, this is due to their different construction and varied applications. SCS nomenclature permits the reverse characteristics of all three junctions to be specified. The anode forward characteristics and gate triggering characteristics can also be specified fully. The principles used in assigning symbols are illustrated below, and with outline drawing above.



ANODE TO CATHODE CHARACTERISTICS

NOTE — ABSENCE OF G INDENTIFIES ANODE TO CATHODE SYMBOLS. DOT IDENTIFIES OPERATING POINT. BRACKETS INDICATE MEANING OF SUBSCRIPT LETTER.

FIG. 1



NOTE: G IDENTIFIES GATE SYMBOLS. LAST LETTER (A OR C) MAY BE DROPPED IF NO AMBIGUITY RESULTS IN SPECIFIC CHARACTERIZATION. F MEANS "FORWARD" AND T MEANS "TRIGGER"

FIG. 2

SCS CHARACTERIZATION

electrical characteristics:[1]

	Symbol[1]	Temp.	3N81	3N82		Typical Curves Fig. #
CUTOFF CHARACTERISTICS						
Forward Blocking Current (R_{GC} = 10K, V_{AC} = Rated Voltage)	$I_{B\ max}$	@ 25°C	1.0		μa max	14
		@ 150°C	20		μa max	
Reverse Blocking Current (R_{GC} = 10K, V_{CA} = Rated Voltage)	$I_{R\ max}$	@ 25°C	1.0		μa max	20
		@ 150°C	20		μa max	
Cathode Gate Reverse Cutoff Current (at Rated Voltage)	I_{GC}	@ 25°C	20		μa max	
Anode Gate Reverse Cutoff Current (at Rated Voltage)	I_{GA}	@ 25°C	1.0		μa max	
CONDUCTING CHARACTERISTICS						
Forward Voltage (at 200 ma Anode current R_{GC} = 10K)	$V_{F\ max}$	@ 25°C	2.0	2.0	V max	15, 16
		@ −65°C	2.5	2.5	V max	
Holding Current (R_{GC} = 10K)	$I_{H\ max}$	@ 25°C	1.5	1.5	ma max	11, 12, 13
		@ −65°C	6.0	6.0	ma max	
Saturation Voltage (G_A to C) (I_{GC} = 5ma, I_{GA} = 50ma, I_A = 0)	$V_{CEsat\ NPN}$	@ 25°C	2.0	2.0	V max	22, 23, 25
TRIGGERING CHARACTERISTICS						
Cathode Gate Current to Trigger (I_{GTC} from current source, V_{AC} = 40V, R_A = 800Ω)	$I_{GTC\ max}$	@ 25°C	1.0	1.0	μa max	4
		@ −65°C	50	50	μa max	
Cathode Gate Voltage to Trigger (V_{AC} = 40V, R_A = 800Ω, R_{GC} = 10K, R_{GA} = ∞, I_{GTC} from current source)	$V_{GTC\ max}$	@ 25°C	.65	.65	V max	5
		@ −65°C	1.0	1.0	V max	
	$V_{GTC\ min}$	@ 25°C	0.4	0.4	V min	
		@ 150°C	0.15	0.15	V min	
Anode Gate Current to Trigger (I_{GTA} from current source, V_{AC} = 40V, R_C = 800Ω, R_{GC} = 10K)	$I_{GTA\ max}$	@ 25°C	1.0	1.0	ma max	3
		@ −65°C	3.0	3.0	ma max	
Anode Gate Voltage to Trigger (I_{GTA} from current source, V_{AC} = 40V, R_C = 800Ω, R_{GC} = 10K, R_{GA} = 1K)	$V_{GTA\ max}$	@ 25°C	0.8	0.8	V max	6
		@ −65°C	1.0	1.0	V max	
	$V_{GTA\ min}$	@ 25°C	0.4	0.4	V min	
		@ 150°C	0.2	0.2	V min	
TRANSIENT CHARACTERISTICS						
Turn-On Time (V_{AC} = 20V, I_A = 100 ma, I_{GC} = 100 μa) (See circuits Fig. 9 and 10)	$t_{on\ max}$	@ 25°C	1.5	1.5	μs max	7, 8
		@ −65°C	2.0	2.0	μs max	
Recovery Time (V_{AC} = 20V, I_A = 100ma, R_{GC} = 10K) (See circuit Fig. 17)	$t_{rec\ max}$	@ 25°C	15	15	μs max	18, 19
		@ 150°C	25	25	μs max	
Collector Capacitance Voltage Gate to Gate = 20V	$C_{ob\ max}$	@ 25°C	15	15	pf	26
Rate of Rise of Forward Blocking Voltage	dv/dt max	@ 25°C	See Note 5		V/μs max	

NOTE 3: The transistor characterization is essentially a restatement of the SCS characterization and is meant to facilitate using the SCS as a complementary PNP-NPN integrated transistor pair.

NOTE 4: The [±] sign indicates that the PNP and NPN transistors require opposite polarites as identified by the test conditions.

NOTE 5: The dv/dt rating is unlimited when the anode gate lead is returned to the anode voltage through a current limiting resistor. An example of this technique is shown in Figure 33

TRANSISTOR CHARACTERIZATION[3]

electrical characteristics: (25°C) (unless otherwise specified)

		3N81				3N82					Typical Curves
		PNP[1]		NPN[1]		PNP[1]		NPN[1]			
DC CHARACTERISTICS		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Fig. #
Collector to Base Breakdown Voltage (I_C = [±][4] 1.0μa, I_E = 0)	BV_{CBO}	−65		65		−100		100		volts	
Emitter to Base Breakdown Voltage (I_C = 0, I_E [NPN] = 20μa, I_E [PNP] = −1μa)	BV_{EBO}	−65		5		−100		5		volts	
Collector Saturation Voltage (I_C = 50ma, I_B = 5ma)	$V_{CE(SAT)}$				2				2	volts	22, 23, 25
Base Saturation Voltage (I_B = 1ma, I_C = 5ma)	$V_{BE(SAT)}$				0.9				0.9	volts	
Forward Current Transfer Ratio (V_{CE} = 0.5V, I_C = 3ma)	h_{FE}			15				15			21
Forward Current Transfer Ratio (V_{CE} = −2.0V, I_C = −1ma)	h_{FE}	0.1				0.1					24
CUTOFF CHARACTERISTICS (3N81 at 65 volts; 3N82 at 100 volts)											
Collector to Emitter Leakage Current (T_A = 150°C)	I_{CEO}		−20				−20			μa	
(R_B = 10K Ω T_A = 150°C)	I_{CER}				20				20	μa	
Collector to Base Leakage Current (I_E = 0, T_A = 150°C)	I_{CBO}		−20		20		−20		20	μa	
Emitter to Base Leakage Current (I_C = 0, T_A = 150°C)	I_{EBO}		−20				−20			μa	
(V_{EB} = 5Vdc, I_C = 0)	I_{EBO}				20				20	μa	
TRANSIENT CHARACTERISTICS											
Collector Capacitance (I_E = 0, V_{CB} = [±][4] 20V)	C_{ob}		15		15		15		15	pf	26
Gain Bandwidth Product	f_T			75				75		mc	

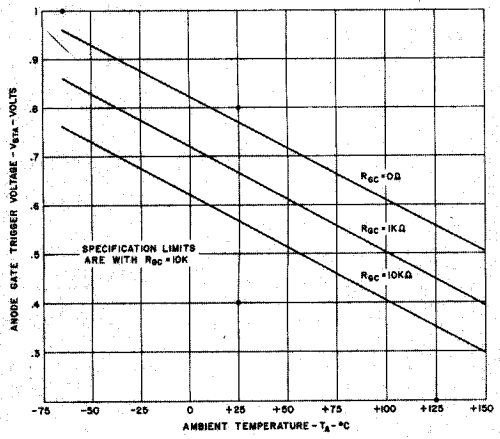


FIG. 6

turn-on time

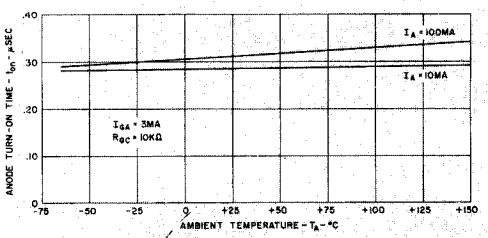


FIG. 7

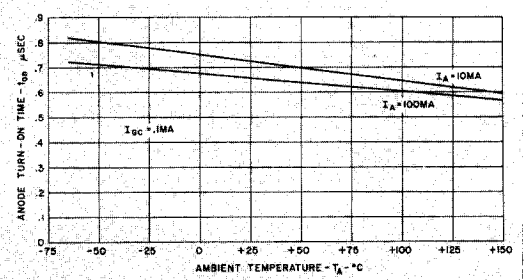
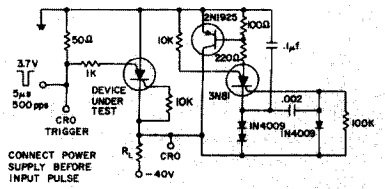
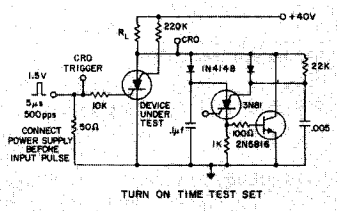


FIG. 8



TURN ON TIME TEST SET
TURN ON BY ANODE GATE

FIG. 9



TURN ON TIME TEST SET

FIG. 10

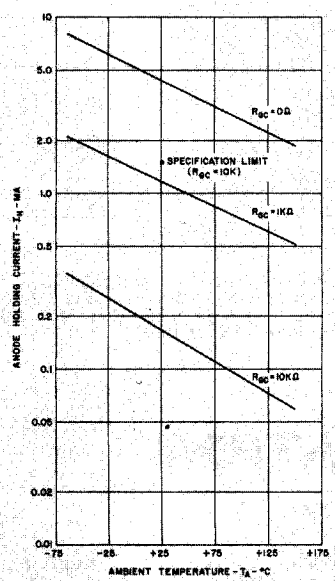


FIG. 11

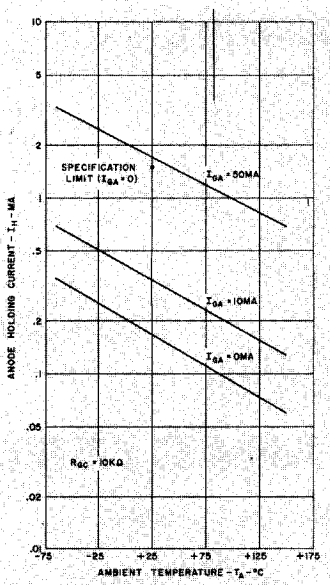


FIG. 12

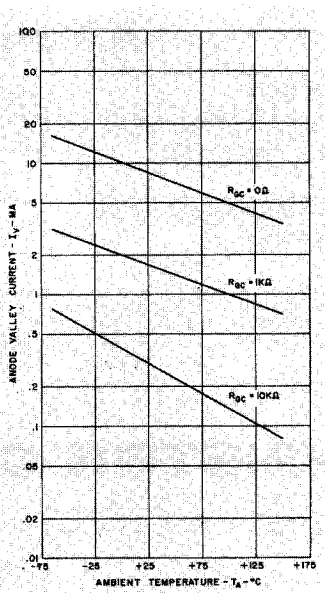


FIG. 13

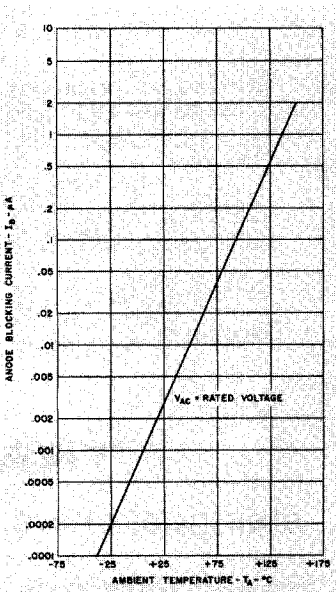


FIG. 14

forward characteristics

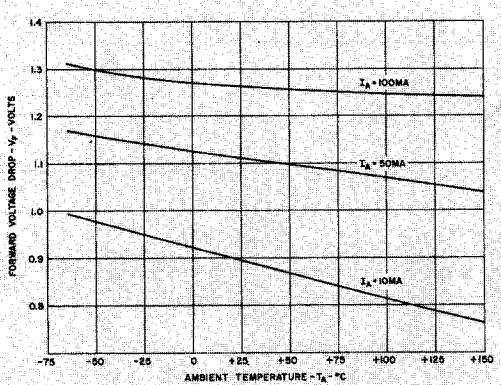


FIG. 15

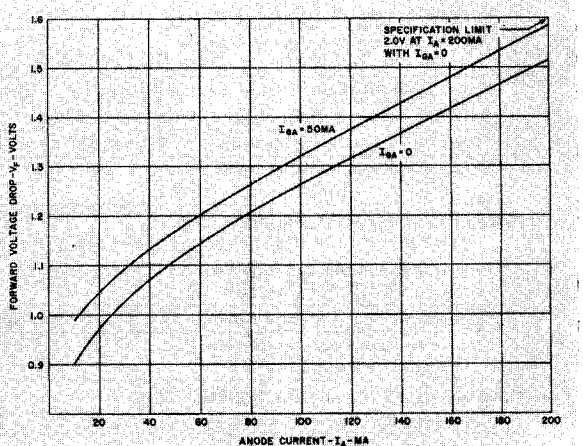
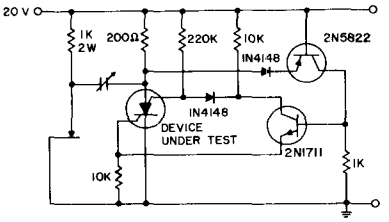


FIG. 16

reverse characteristics



RECOVERY TEST SET

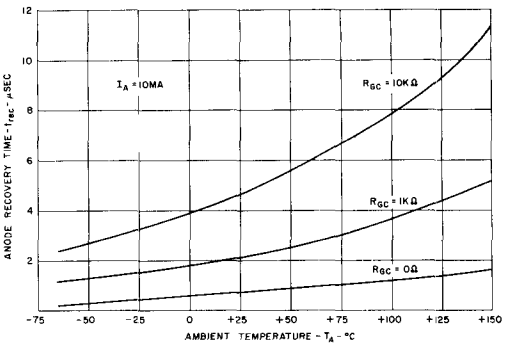


FIG. 18

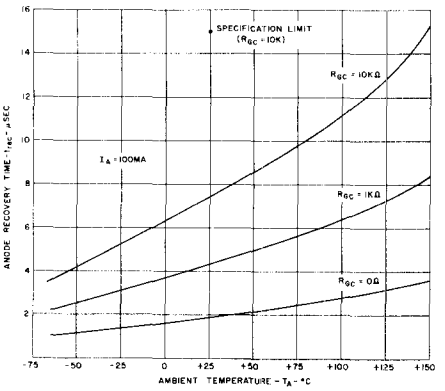


FIG. 19

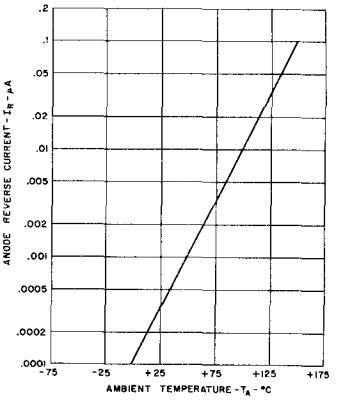


FIG. 20

triggering characteristics

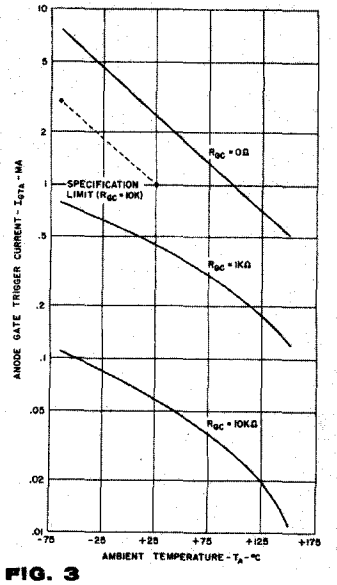


FIG. 3

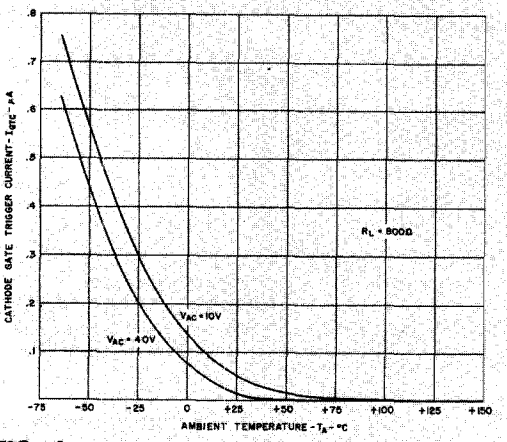


FIG. 4

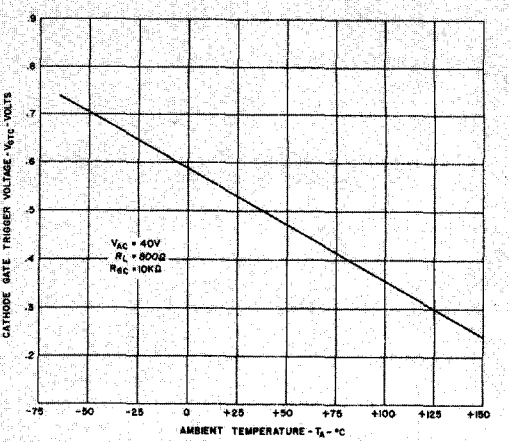


FIG. 5

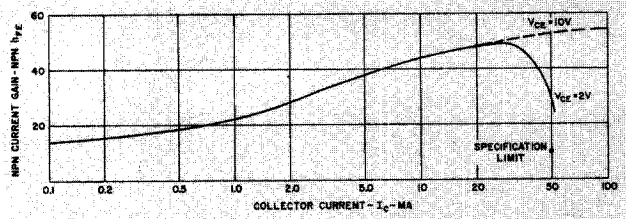


FIG. 21

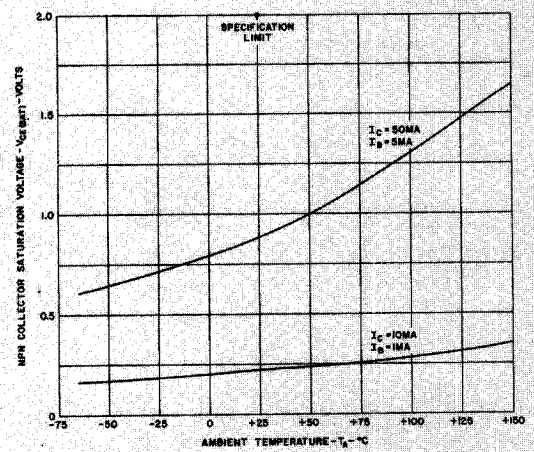


FIG. 22

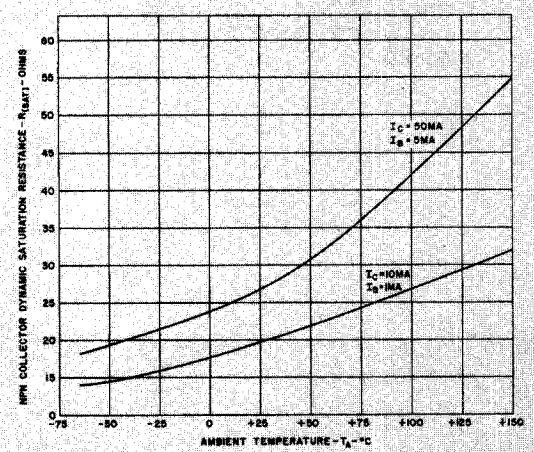


FIG. 23

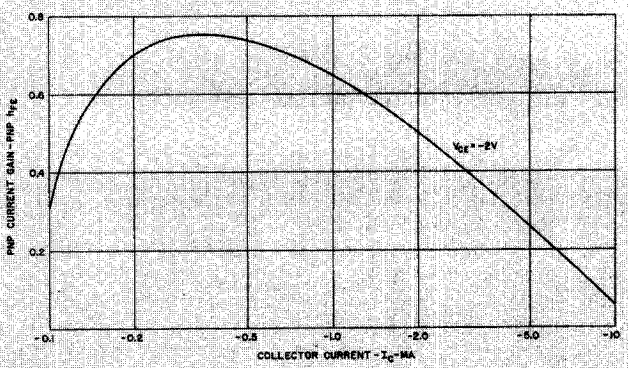


FIG. 24

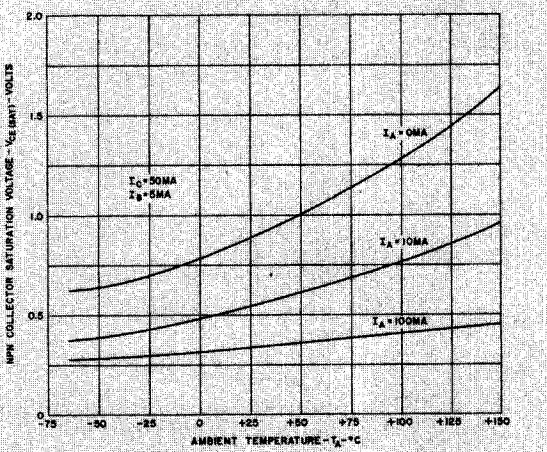


FIG. 25

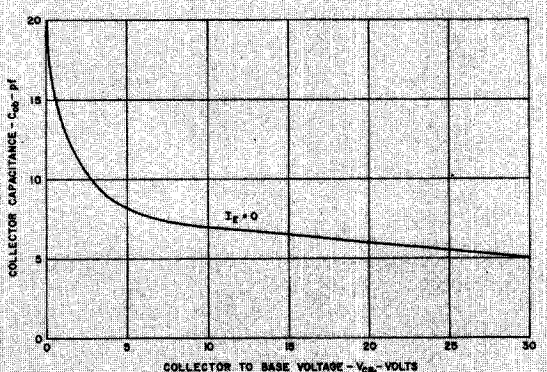
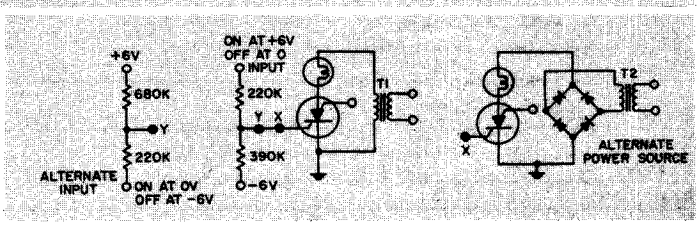


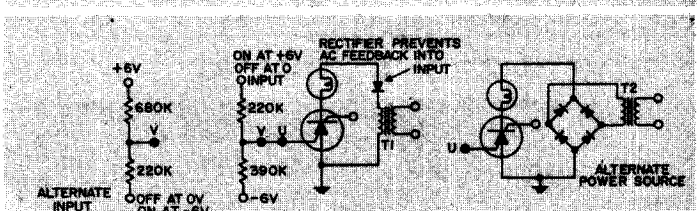
FIG. 26

APPLICATIONS

LAMP	RATING VOLTS	RATING AMPS	SCS	SEC. VOLTS RMS T1*	SEC. VOLTS RMS T2
24	24	.035	3N81	34	24
327	28	.04	3N81	40	28
330	14	.08	3N81	20	14
344	10	.015	3N81	14	10
1829	28	.07	3N81	40	28

*INCREASED VOLTAGE GIVES NORMAL BRIGHTNESS IN HALF WAVE CIRCUIT.





INCANDESCENT LAMP DRIVERS

FIG. 27