D2875, APRIL 1985

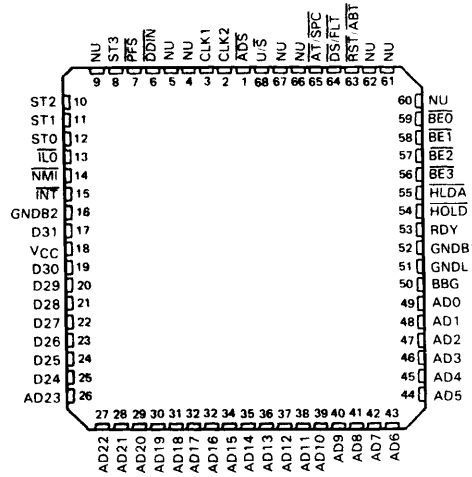
- High-Speed NMOS Technology
- 32-Bit Architecture and Implementation with 24-Bit Address
- 16-Megabyte Uniform Addressing Space
- Powerful Instruction Set with:
  - General 2-Address Capability
  - Very High Degree of Symmetry
  - Addressing Modes Optimized for High-Level Language References
- TI32000 Coprocessor Support
- Single 5-V Operation
- Direct Replacement for National Semiconductor NS32032-10

description

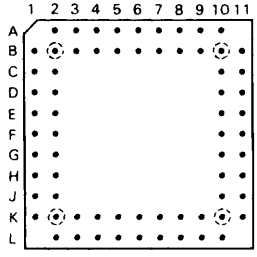
The TI32032T-2 is a monolithic high-performance high-speed NMOS microprocessor designed to function as a central processing unit (CPU) in the TI32000 microprocessor family. The device has been designed primarily to support microprocessor users who require the ability to use a large addressing space for large programs and/or large data structures. Because large programs must realistically be generated and maintained in high-level languages, the TI32000 family architecture provides for very efficient compilation while remaining easy to program at the assembler level. The TI32000 family architecture in conjunction with the TI32082 Memory Management Unit (MMU) provides full support for demand-paged virtual memory management. High-performance floating-point instructions are provided by the TI32081 Floating Point Unit (FPU).

The TI32032T is characterized for operation from 0°C to 70°C.

FK OR FN . . . CHIP-CARRIER PACKAGE
(TOP VIEW)



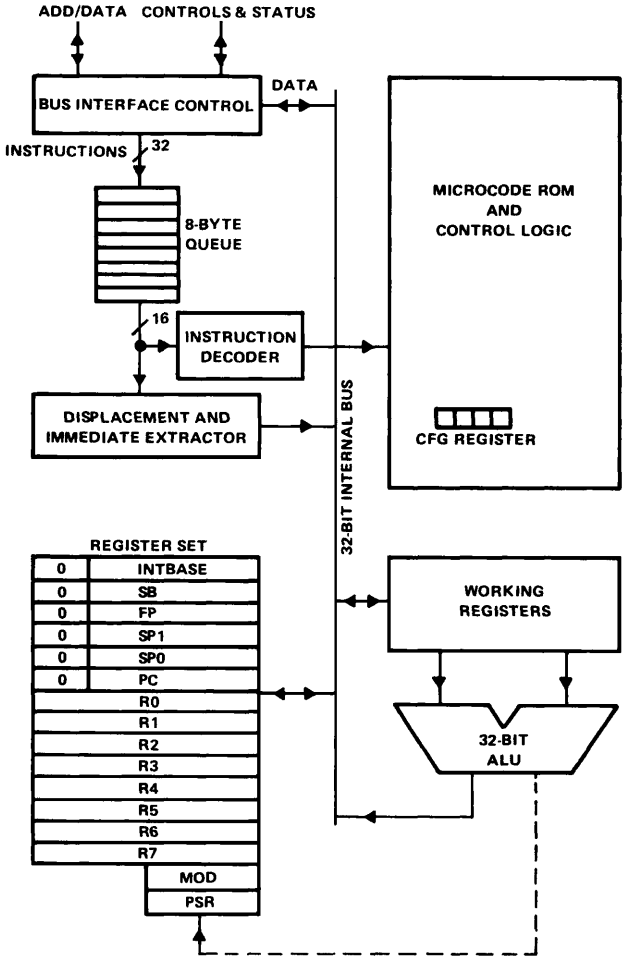
PIN GRID ARRAY PACKAGE
(TOP VIEW)



PIN	NAME	PIN	NAME
A2	NU	F10	RDY
A3	$\overline{PFS}$	F11	GNDB1
A4	NU	G1	D29
A5	CLK1	G2	D28
A6	$\overline{ADS}$	G10	GNDL
A7	NU	G11	BBG
A8	$\overline{AT}$ $\overline{SPC}$	H1	D27
A9	$\overline{RST}$ $\overline{ABT}$	H2	D26
A10	NU	H10	AD0
B1	ST2	H11	AD1
B2	ST1	J1	D25
B3	ST3	J2	D24
B4	$\overline{DDIN}$	J10	AD2
B5	NU	J11	AD3
B6	CLK2	K1	AD23
B7	U $\overline{S}$	K2	AD21
B8	NU	K3	AD19
B9	$\overline{DS}$ $\overline{FLT}$	K4	AD17
B10	NU	K5	AD15
B11	NU	K6	AD13
C1	ST0	K7	AD11
C2	$\overline{ILO}$	K8	AD9
C10	$\overline{BE0}$	K9	AD7
C11	$\overline{BE1}$	K10	AD4
D1	$\overline{NMI}$	K11	AD5
D2	$\overline{INT}$	L2	AD22
D10	$\overline{BE2}$	L3	AD20
D11	$\overline{BE3}$	L4	AD18
E1	GNDB2	L5	AD16
E2	D31	L6	AD14
E10	$\overline{HLDA}$	L7	AD12
E11	$\overline{HOLD}$	L8	AD10
F1	V_{CC}	L9	AD8
F2	D30	L10	AD6

NU—Reserved for future use. Make no external connection.

functional block diagram



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PIN FUNCTIONAL DESCRIPTION

PIN NO.		NAME	I/O	DESCRIPTION
PIN GRID ARRAY	CHIP CARRIER			
A6	1	$\overline{ADS}$	O	Address strobe output. Available to the system for address latch control. Indicates start of a bus cycle by going low
B6	2	CLK2	I	Clock 2 input. One phase of a two-phase clock input
A5	3	CLK1	I	Clock 1 input. One phase of a two-phase clock input
B5	4	NU		Reserved for future use. Make no external connection.
A4	5	NU		Reserved for future use. Make no external connection.
B4	6	$\overline{DDIN}$	O	Data Direction In output. Status signal that indicates the direction of data transfer during a bus cycle, low for read, high for write
A3	7	$\overline{PFS}$	O	Program Flow Status output. Low-going pulse indicates beginning of an instruction execution.
B3	8	ST3	O	Status bit 3 output. Bus cycle status code
A2	9	NU		Reserved for future use. Make no external connection.
B1	10	ST2	O	Status bit 2 output. Bus cycle status code
B2	11	ST1	O	Status bit 1 output. Bus cycle status code
C1	12	ST0	O	Status bit 0 (least significant bit) output. Bus cycle status code
C2	13	$\overline{ILO}$	O	Interlocked Operation Output. When low, indicates that an interlocked instruction is being executed
D1	14	$\overline{NMI}$	I	Nonmaskable Interrupt input. Nonmaskable interrupt request
D2	15	$\overline{INT}$	I	Interrupt input. Maskable interrupt request
E1	16	GNDB2		Buffer Ground 2. Ground reference for half of the on-chip drivers connected to output pins
E2	17	D31	I/O	Data bit 31 of the data bus
F1	18	V_{CC}		+5 V supply voltage
F2	19	D30	I/O	Data bit 30 of the data bus
G1	20	D29	I/O	Data bit 29 of the data bus
G2	21	D28	I/O	Data bit 28 of the data bus
H1	22	D27	I/O	Data bit 27 of the data bus
H2	23	D26	I/O	Data bit 26 of the data bus
J1	24	D25	I/O	Data bit 25 of the data bus
J2	25	D24	I/O	Data bit 24 of the data bus
K1	26	AD23	I/O	Address bit 23. Multiplexed address/data information
L2	27	AD22	I/O	Address bit 22. Multiplexed address/data information
K2	28	AD21	I/O	Address bit 21. Multiplexed address/data information
L3	29	AD20	I/O	Address bit 20. Multiplexed address/data information
K3	30	AD19	I/O	Address bit 19. Multiplexed address/data information
L4	31	AD18	I/O	Address bit 18. Multiplexed address/data information
K4	32	AD17	I/O	Address bit 17. Multiplexed address/data information
L5	33	AD16	I/O	Address bit 16. Multiplexed address/data information
K5	34	AD15	I/O	Address bit 15. Multiplexed address/data information
L6	35	AD14	I/O	Address bit 14. Multiplexed address/data information
K6	36	AD13	I/O	Address bit 13. Multiplexed address/data information
L7	37	AD12	I/O	Address bit 12. Multiplexed address/data information
K7	38	AD11	I/O	Address bit 11. Multiplexed address/data information
L8	39	AD10	I/O	Address bit 10. Multiplexed address/data information
K8	40	AD9	I/O	Address bit 9. Multiplexed address/data information
L9	41	AD8	I/O	Address bit 8. Multiplexed address/data information
K9	42	AD7	I/O	Address bit 7. Multiplexed address/data information
L10	43	AD6	I/O	Address bit 6. Multiplexed address/data information
K11	44	AD5	I/O	Address bit 5. Multiplexed address/data information

PIN FUNCTIONAL DESCRIPTION

PIN NO. PIN GRID ARRAY	PIN NO. CHIP CARRIER	NAME	T/O	DESCRIPTION
K10	45	AD4	I/O	Address bit 4. Multiplexed address/data information
J11	46	AD3	I/O	Address bit 3. Multiplexed address/data information
J10	47	AD2	I/O	Address bit 2. Multiplexed address/data information
H11	48	AD1	I/O	Address bit 1. Multiplexed address/data information
H10	49	AD0	I/O	Address bit 0 (least significant bit). Multiplexed address/data information
G12	50	BBG	O	Back-Bias Generator supply. Output of on-chip substrate voltage generator
G10	51	GNDL		Logic ground. Ground reference for on-chip logic.
F11	52	GNDB1		Buffer Ground 1. Ground reference for half of the on-chip drivers connectd to output pins.
F10	53	RDY	I	READY input. When high, causes the CPU to terminate the bus cycle. when low. causes the CPU to extend the current bus cycle to provide for a slower memory or peripheral reference.
E11	54	$\overline{\text{HOLD}}$	I	Hold request input. When low, causes the CPU to release the bus for DMA or multiprocessing purposes.
E10	55	$\overline{\text{HLDA}}$	O	Hold acknowledge output. Applied by the CPU in response to a $\overline{\text{HOLD}}$ input. Low level indicates that the bus has been released for DMA or multiprocessing purposes.
D11	56	$\overline{\text{BE3}}$	O	Byte Enable 3 output. When low, (with $\overline{\text{BE0}}$ through $\overline{\text{BE2}}$) enables data transfers on individual bus bytes.
D10	57	$\overline{\text{BE2}}$	O	Byte Enable 2 output. When low, (when $\overline{\text{BE0}}$, $\overline{\text{BE1}}$ and $\overline{\text{BE3}}$) enables data transfers on individual bus bytes.
C11	58	$\overline{\text{BE1}}$	O	Byte Enable 1 output. When low, (with $\overline{\text{BE0}}$, $\overline{\text{BE2}}$ and $\overline{\text{BE3}}$) enables data transfers on individual bus bytes.
C10	59	$\overline{\text{BE0}}$	O	Byte Enable 0 output. When low, (with $\overline{\text{BE1}}$ through $\overline{\text{BE3}}$) enables data transfers on individual bus bytes.
B11	60	NU	I	Reserved for future use. Make no external connection.
A10	61	NU		Reserved for future use. Make no external connection.
B10	62	NU		Reserved for future use. Make no external connection.
A9	63	$\overline{\text{RST}}$/$\overline{\text{ABT}}$	I	Reset/Abort input. If held low for one clock cycle and released, causes an abort command. If held low for longer than one clock cycle, initiates a reset.
B9	64	$\overline{\text{DS}}$/$\overline{\text{FLT}}$	I/O	Data Strobe/Float. Data strobe output or float command input. Function is selected by $\overline{\text{AT}}$/$\overline{\text{SPC}}$ input.
A8	65	$\overline{\text{AT}}$/$\overline{\text{SPC}}$	I/O	Address Translation/Coprocessor Control. Used by the CPU as the data strobe output for coprocessor transfers. Used by coprocessors to acknowledge completion of an instruction. Sampled on the trailing edge of reset pulse as address translation strap.
B8	66	NU		Reserved for future use. Make no external connection.
A7	67	NU		Reserved for future use. Make no external connection.
B7	68	U/$\overline{\text{S}}$	O	User/Supervisor status output. When high, indicates user mode. When low, indicates supervisor mode.

absolute maximum ratings over recommended operating conditions (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −5 V to 7 V
Output voltage range . . . . . −5 V to 7 V
Continuous total dissipation at (or below) 70°C free-air temperature . . . . . 1.5 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C

NOTE 1: All voltage values are with respect to the common ground.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	CLK1, CLK2	$V_{CC}-0.5$		$V_{CC}+0.5$	V
	All other inputs	2		$V_{CC}+0.5$	
Low-level input voltage, V_{IL}	CLK1, CLK2	−0.5		0.3	V
	All other inputs	−0.5		0.8	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITION	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.45	V
I_I	Input current	$\overline{AT}/\overline{SPC}$	V_I = 0.4 V	50		1000	μA
		All other inputs except CLK1, CLK2, and $\overline{AT}/\overline{SPC}$	V_I = 0 to V_{CC}			±20	
$I_{O(off)}$	Off-state output current		V_O = 0.4 V to V_{CC}			±20	μA
I_{CC}	Supply current		I_O = 0, T_A = 25°C		180	300	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, the pin names have been further abbreviated as follows:

AD	A	$\overline{FCLK}$	F
CLK1	C or C1	$\overline{HLDA}$	HA
$\overline{CLK2}$	C2	$\overline{HOLD}$	HD
$\overline{DDIN}$	DD	U/$\overline{S}$	US

Lowercase subscripts and their meaning are:

c	cycle time (period)
dis	disable time (H or L to Z)
en	enable time (Z to H or L)
f	fall time
p	propagation delay time
pwr	supply voltage stable
r	rise time
su	setup time
w	pulse duration

Parentheses have been omitted except when required for separation of a final subscript representing special conditions. The columns titled NSC SYMBOL show the symbols used by National Semiconductor for the parameters shown in the timing requirements and switching characteristics tables.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		FIGURE	NSC SYMBOL	MIN	MAX	UNIT
$t_{suD(RD)}$	Setup time, read data before CLK2↓	2,11	t_{DIs}	10		ns
$t_{hD(RD)}$	Hold time, read data after CLK1↑	2,11	t_{DIh}	10		ns
t_{suHDL}	Setup time, $\overline{HOLD}$ Low before CLK2↓ (see Note 3)	3, 4	t_{HLDa}	25		ns
t_{hHD}	Hold time, $\overline{HOLD}$ low or high after CLK1↑	3,4,5	t_{HLDh}	0		ns
t_{suHDH}	Setup time, $\overline{HOLD}$ high before CLK2↓	5	t_{HLDia}	25		ns
t_{suFLTL}	Setup time, $\overline{FLT}$ low before CLK2↓	6	t_{FLTa}	25		ns
t_{suFLTH}	Setup time, $\overline{FLT}$ high before CLK2↓	7	t_{FLTia}	25		ns
t_{suRDY}	Setup time, RDY low or high before CLK2↓	8, 9	t_{RDYs}	15		ns
t_{hRDY}	Hold time, RDY low or high after CLK1↓	8, 9	t_{RDYh}	0		ns
t_{wSPC}	Pulse duration, $\overline{SPC}$ low at 0.8 V (both edges)	10	t_{SPCw}	20		ns
t_{suAT}	Setup time, $\overline{AT}/\overline{SPC}$ low before CLK1↑	13	t_{ATs}	$1t_{cC}$		
t_{hAT}	Hold time, $\overline{AT}/\overline{SPC}$ low after CLK1↓	13	t_{ATh}	$2t_{cC}$		
t_{rC}	Rise time, CLK1 or CLK2	14	t_{CLr}		7	ns
t_{fC}	Fall time, CLK1 or CLK2	14	t_{CLf}		7	ns
t_{cC}	Clock period	14	t_{Cp}	100	5000	ns
t_{wC1H}	Pulse duration, CLK1 high	14	t_{CLh}	$0.5t_{cC}-10$		ns
t_{wC2H}	Pulse duration, CLK2 high	14	t_{CLl}	$0.5t_{cC}-10$		ns
	Clock pulse asymmetry, t_{wC1H}-t_{wC2H}		t_{CLwas}		±5	ns
t_{C1LC2H}	Nonoverlap time at 10% of CLK1↓ and CLK2↑	14	$t_{nOVL(1)}$	0	7	ns
t_{C1LC2L}	Nonoverlap time at 10% of CLK2↓ and CLK1↑	14	$t_{nOVL(2)}$	0	7	ns
	Nonoverlap asymmetry, $t_{C1LC2H}-t_{C12LC1H}$		t_{nOVLas}		±4	ns
t_{suABT}	Setup time, $\overline{ABT}$ low before CLK2↓	22,23	t_{ABTs}	20		ns
t_{hABT}	Hold time, $\overline{ABT}$ Low after CLK1↑	22,23	t_{ABTh}	0		ns
t_{pwr}	Supply voltage stable (above 4.5 V) to $\overline{RST}$ high	24	t_{PWR}	50		μs
t_{suRST}	Setup time, $\overline{RST}$ high before CLK1↓	24, 25	t_{RSTs}	20		ns
t_{wRST}	Puls duration, $\overline{RST}$ low at 0.8 V (both edges)	25	t_{RSTw}	$64t_{cC}$		
t_{suINT}	Setup time, $\overline{INT}$ low before CLK1↓	26	t_{INTs}	20		ns
t_{wNMI}	Pulse duration, $\overline{NMI}$ low at 0.8 V (both edges)	27	t_{NMIw}	70		ns
t_{LX-PFS}	Last operand transfer of an instruction to next $\overline{PFS}$ clock cycle	28	t_{LXPF}	$0t_{cC}$		

NOTE 3: This setup time is necessary to ensure prompt acknowledgement via $\overline{HLDA}$ and the ensuing floating of the CPU off the buses. The time from the receipt of the $\overline{HOLD}$ signal until the CPU floats is a function of the time $\overline{HOLD}$ signal goes low, the state of the RDY input (in MMU systems), and the length of the current MMU cycle.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 100 pF (unless otherwise noted)

PARAMETER		FIGURE	NSC SYMBOL	MIN	MAX	UNIT
t_{aA}	Access time, AD0 through AD23 after CLK1↑	1	t_{ALv}		50	ns
t_{vA}	Valid time, AD0 through AD23 after CLK1↑	1	t_{ALh}	10		ns
t_{aD}	Access time, AD0 through AD23 and D24 through D31 after CLK1↑	1	t_{Dv}		50	ns
t_{vD}	Valid time, AD0 through AD23 and D24 through D31 after CLK1↑	1	t_{Dh}	0		ns
t_{aBE}	Access time, $\overline{BE0}$ through $\overline{BE3}$ after CLK2↑	1	t_{BEv}		45	ns
t_{vBE}	Valid time, $\overline{BE0}$ through $\overline{BE3}$ after CLK2↑	1	t_{BEh}	0		ns
t_{aST}	Access time, ST0 through ST3 after CLK1↑	1	t_{STv}		45	ns
t_{vST}	Valid time, ST0 through ST3 after CLK1↑	1	t_{STh}	0		ns
t_{pADSL}	Propagation delay time, CLK1↑ to $\overline{ADS}$ low	1	t_{ADSa}		35	ns
t_{pADSH}	Propagation delay time, CLK2↑ to $\overline{ADS}$ high	1	t_{ADSia}	15	45	ns
t_{wADS}	Pulse duration, $\overline{ADS}$ low at 0.8 V (both edges)	1	t_{ADSw}	35		ns
t_{pDSL}	Propagation delay time, CLK1↑ to $\overline{DS}$ low	1	t_{DSa}		45	ns
t_{pDSH}	Propagation delay time, CLK1↑ to $\overline{DS}$ high	1	t_{DSia}	†	40	ns
$t_{AV-ADSH}$	Time interval, AD0 through AD23 valid to $\overline{ADS}$ high	2	t_{ALADSs}	25		ns
t_{disA}	Disable time, AD0 through AD23 after CLK1↑ (without MMU)	2	t_{ALf}		25	ns
t_{disD}	Disable time, D24 through D31 after CLK1↑ (without MMU)	2	t_{ADf}		25	ns
t_{aDD}	Access time, $\overline{DDIN}$ after CLK1↑	2	t_{DDINv}		65	ns
t_{vDD}	Valid time, $\overline{DDIN}$ after CLK1↑	2	t_{DDINh}	0		ns
t_{disA}	Disable time, AD0 through AD23 after CLK1↑ ($\overline{HOLD}$ low)	3	t_{ALf}		25	ns
t_{disD}	Disable time, D24 through D31 after CLK1↑ ($\overline{HOLD}$ low)	3	t_{ADf}		25	ns
t_{disADS}	Disable time, ADS after CLK1↑ ($\overline{HOLD}$ low)	3,4	t_{ADSf}		55	ns
t_{disBE}	Disable time, $\overline{BE0}$ through $\overline{BE3}$ after CLK1↑ ($\overline{HOLD}$ low)	3,4	t_{BEf}		55	ns
t_{disDD}	Disable time, $\overline{DDIN}$ after CLK1↑ ($\overline{HOLD}$ low)	3,4	t_{DDINf}		55	ns
t_{pHAL}	Propagation delay time, CLK1↑ to $\overline{HLDA}$ low	3,4	t_{HLDAa}		75	ns
t_{pHAH}	Propagation delay time, CLK1↑ to $\overline{HLDA}$ high	5	t_{HLDAia}		75	ns
t_{enADS}	Enable time, $\overline{ADS}$ after CLK1↑ ($\overline{HOLD}$ high)	5	t_{ADSr}		55	ns
t_{enBE}	Enable time, $\overline{BE0}$ through $\overline{BE3}$ after CLK1↑($\overline{HOLD}$ high)	5	t_{BEr}		55	ns
t_{enDD}	Enable time, $\overline{DDIN}$ after CLK1↑ ($\overline{HOLD}$ high)	5	t_{DDINr}		55	ns
$t_{vADSH-A}$	Valid time, AD0 through AD23 after $\overline{ADS}$↑	6	t_{ALADSh}	10		ns
$t_{disA(1)}$	Disable time, AD0 through AD23 after CLK1↑ (with MMU)	6	t_{ALMf}		25	ns
t_{disD}	Disable time, D24 through D31 after CLK1↑ (with MMU)	6	t_{ADMf}		25	ns
$t_{disA(2)}$	Disable time, AD0 through AD23 after CLK1↑ ($\overline{FLT}$ Low)	6	t_{ALf}		30	ns
t_{disDD}	Disable time, $\overline{DDIN}$ after $\overline{FLT}$↑	6	t_{DDINf}		55	ns
t_{enDD}	Enable time, $\overline{DDIN}$ after $\overline{FLT}$↑	7	t_{DDINr}		50	ns
t_{pSPCL}	Propagation delay time, CLK1↑ to $\overline{SPC}$ low	10	t_{SPCa}		35	ns
t_{pSPCH}	Propagation delay time, CLK1↑ to $\overline{SPC}$ high	10	t_{SPCia}		35	ns
t_{aD}	Access time, write data (bits AD0 through AD15) after CLK1↑	10	t_{Dv}		50	ns
t_{vD}	Valid time, write data (bits AD0 through AD15) after CLK1↑	10	t_{Dh}	0		ns

switching characteristics (continued)

PARAMETER		FIGURE	NSC SYMBOL	MIN	MAX	UNIT
t_{disSPC}	Disable time, $\overline{SPC}$ output nonforcing after CLK2↑	12	t_{SPCnf}		10	ns
t_{wPFS}	Pulse duration, $\overline{PFS}$ low at 0.8 V (both edges)	15	t_{PFSw}	70		ns
t_{pPFSL}	Propagation delay time, CLK2↑ to $\overline{PFS}$ low	15	t_{PFSa}		50	ns
t_{pPFSH}	Propagation delay time, CLK2↑ to $\overline{PFS}$ high	15	t_{PFSia}		50	ns
t_{PFS-NS}	Time interval, $\overline{PFS}$ clock cycle to next nonsequential fetch	16	t_{PFNS}	$4t_{cC}$		
t_{NS-PFS}	Time interval, nonsequential fetch to next $\overline{PFS}$ clock cycle	17	t_{NSPF}	$4t_{cC}$		
$t_{ILOL-C1}$	Time interval, $\overline{ILO}$ low to CLK1↑	18	t_{ILOs}	30		ns
t_{vILO}	Valid time, $\overline{ILO}$ low after CLK1↑	19	t_{ILOh}	10		ns
t_{pILOL}	Propagation delay time, CLK1↑ to $\overline{ILO}$ low	20	t_{ILOa}		70	ns
t_{pILOH}	Propagation delay time, CLK1↑ to $\overline{ILO}$ high	20	t_{ILOia}		70	ns
t_{aUS}	Access time, U/$\overline{S}$ after CLK1↑	21	t_{USv}		70	ns
t_{vUS}	Valid time, U/$\overline{S}$ after CLK1↑	21	t_{USh}	10		ns

PARAMETER MEASUREMENT INFORMATION†

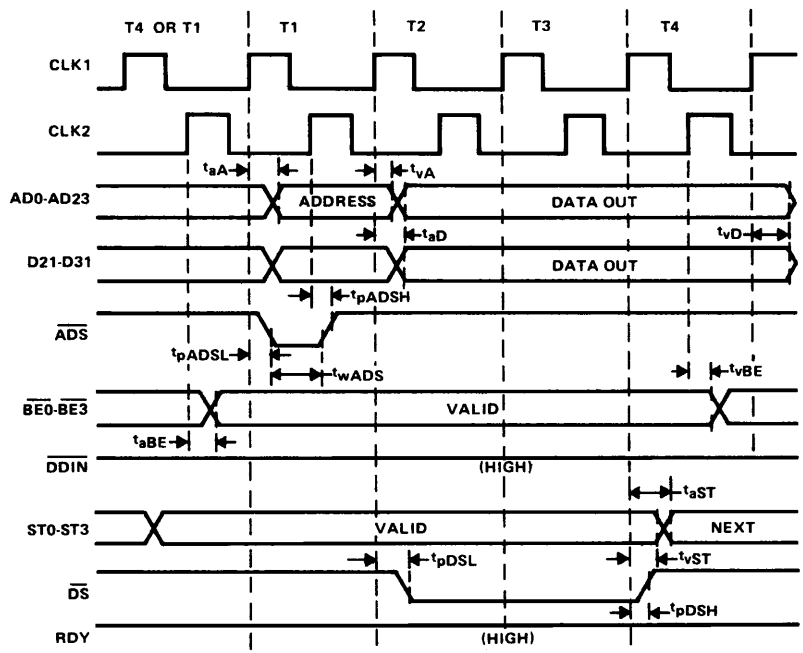

FIGURE 1. WRITE CYCLE

†In Figures 1 through 28, time intervals are defined with respect to the following reference points:
For clock signals, the 50% points.
For all other signals, 2 V if the high level is indicated and 0.8 V if the low level is indicated.

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PARAMETER MEASUREMENT INFORMATION

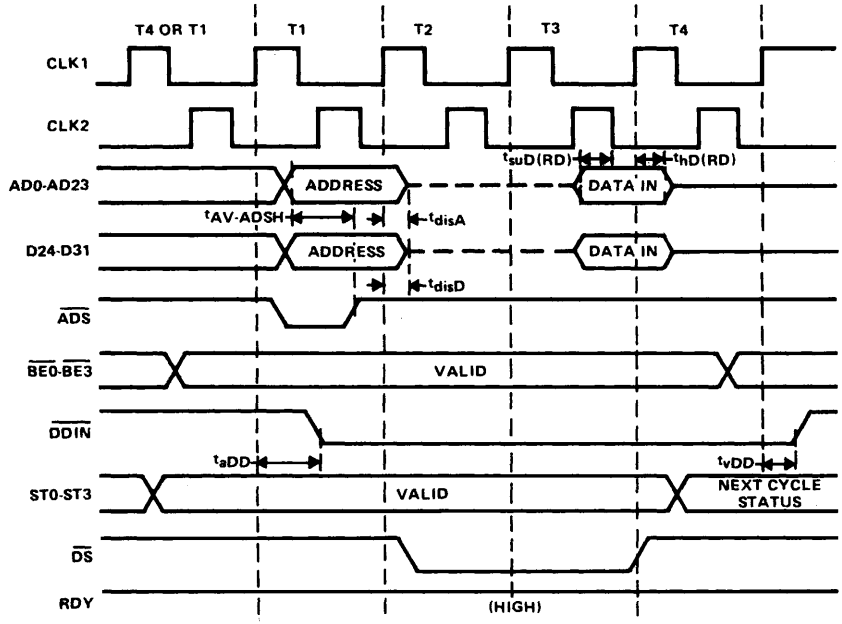
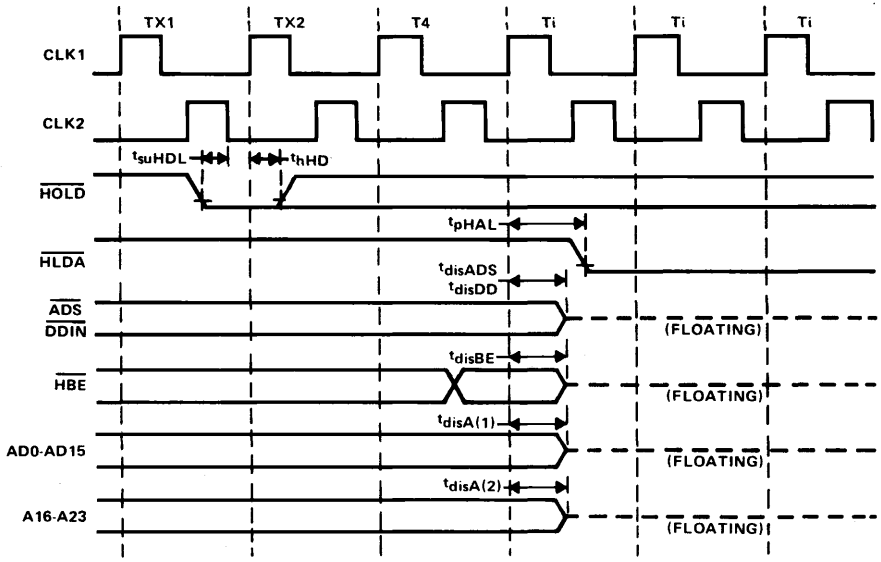


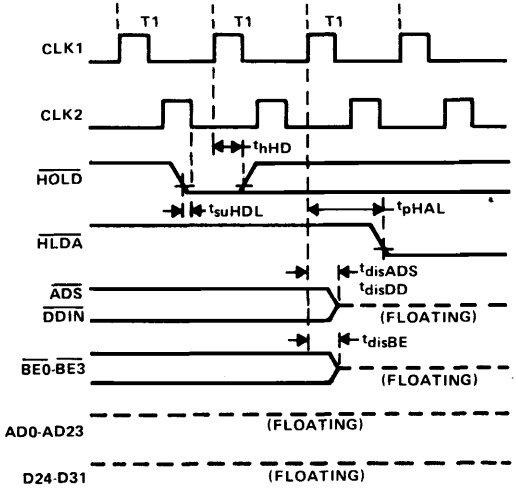
FIGURE 2. READ CYCLE

PARAMETER MEASUREMENT INFORMATION



NOTE: When the CPU is not idling (not in Ti), the $\overline{HOLD}$ request ($\overline{HOLD}$ low) must be active before the trailing edge of CLK2 that appears two clock cycles before T4 (TX1) and stay low until t_{hHDL} after the leading edge of CLK1 that precedes T4 (TX2) for the request to acknowledge.

FIGURE 3. FLOATING BY $\overline{HOLD}$ TIMING (CPU NOT IDLE INITIALLY)



NOTE: During T1 the CPU is already idling.

FIGURE 4. FLOATING BY $\overline{HOLD}$ TIMING (CPU INITIALLY IDLE)

PARAMETER MEASUREMENT INFORMATION

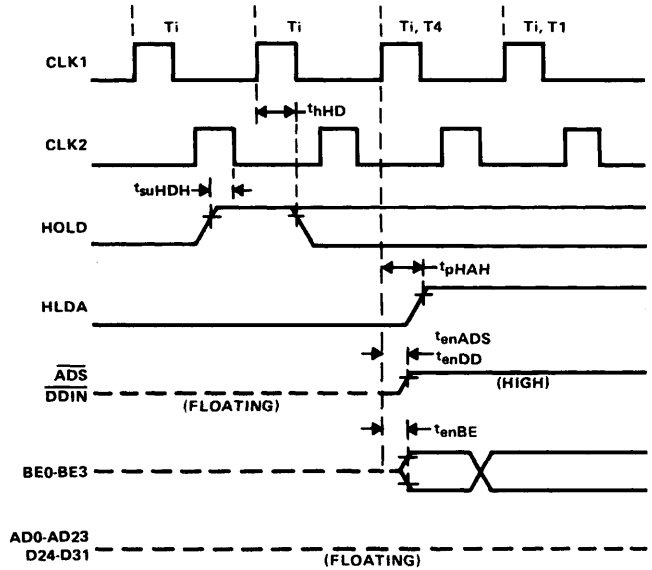


FIGURE 5. RELEASE FROM $\overline{\text{HOLD}}$

PARAMETER MEASUREMENT INFORMATION

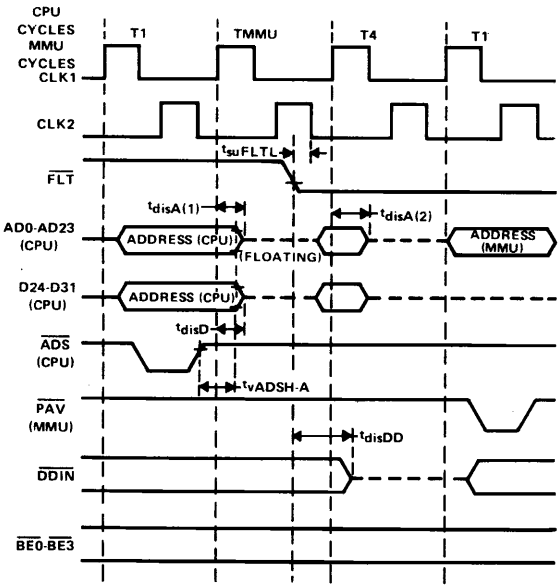


FIGURE 6. $\overline{FLT}$ INITIATED FLOAT CYCLE TIMING

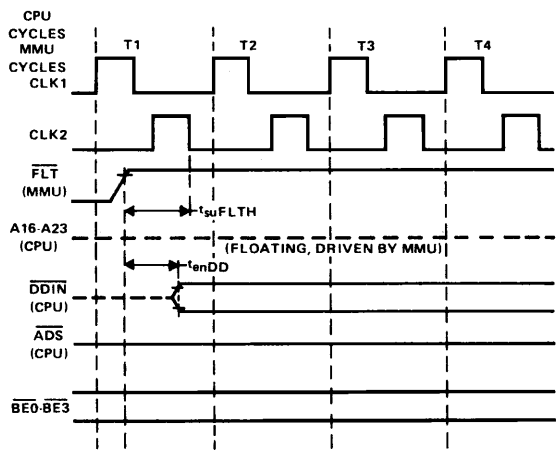


FIGURE 7. RELEASE FROM $\overline{FLT}$ TIMING

NOTE: When $\overline{FLT}$ goes high, the CPU restarts driving $\overline{DDIN}$ before the MMU releases it. This does not cause any conflict since both CPU and MMU force $\overline{DDIN}$ to the same logic level.

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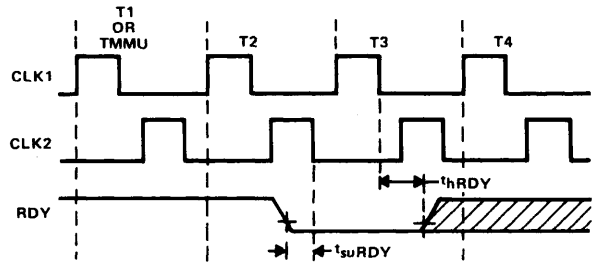

FIGURE 8. READY SAMPLING (CPU INITIALLY READY)

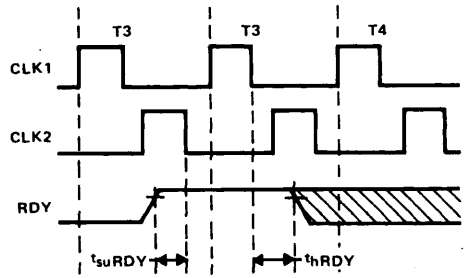

FIGURE 9. READY SAMPLING (CPU INITIALLY NOT READY)

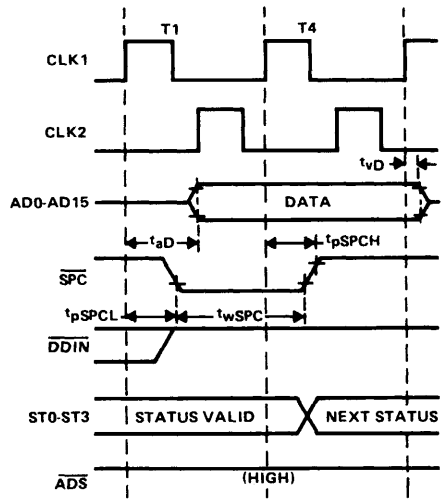

FIGURE 10. COPROCESSOR WRITE TIMING

PARAMETER MEASUREMENT INFORMATION

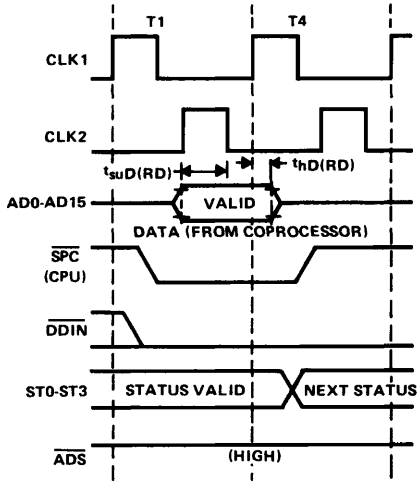

FIGURE 11. COPROCESSOR READ TIMING

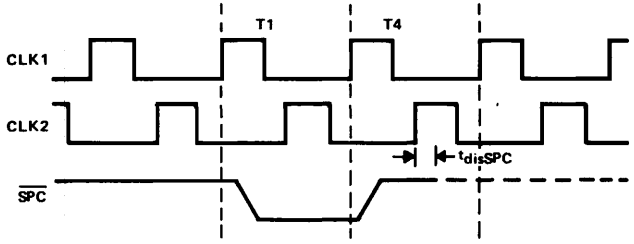

FIGURE 12. SPC NONFORCING DELAY

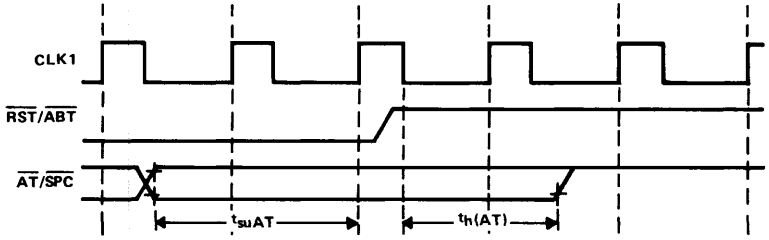

FIGURE 13. RESET CONFIGURATION TIMING

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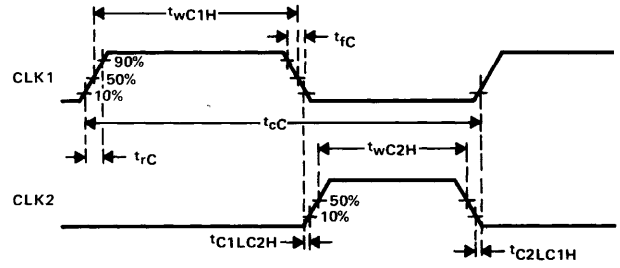

FIGURE 14. CLOCK WAVEFORMS

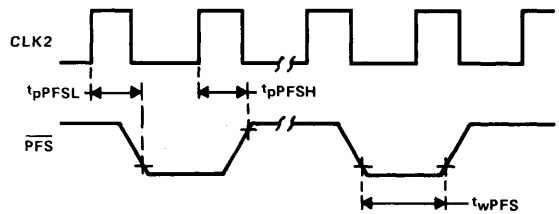

FIGURE 15. RELATIONSHIP OF $\overline{PFS}$ TO CLOCK CYCLES

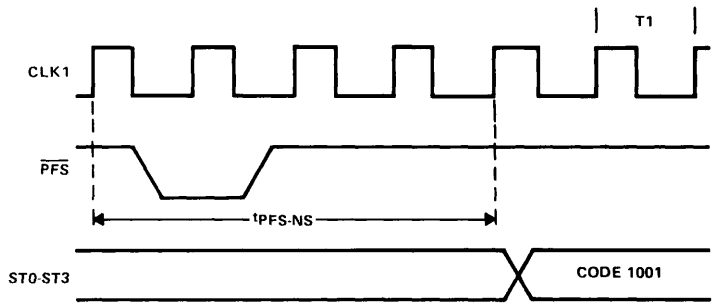

FIGURE 16. GUARANTEED DELAY, $\overline{PFS}$ TO NONSEQUENTIAL FETCH

PARAMETER MEASUREMENT INFORMATION

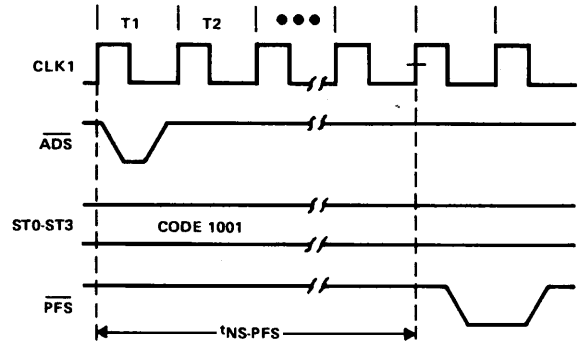

FIGURE 17. GUARANTEED DELAY, NONSEQUENTIAL FETCH TO $\overline{PFS}$

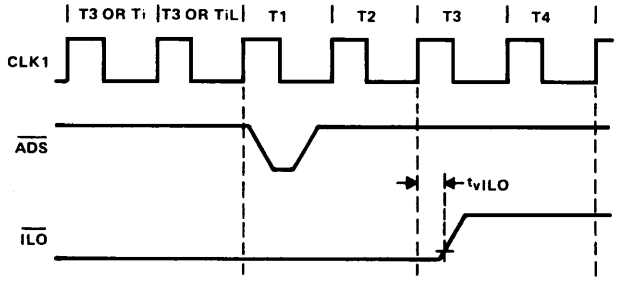

FIGURE 18. RELATIONSHIP OF ILO TO FIRST OPERAND CYCLE OF AN INTERLOCKED INSTRUCTION

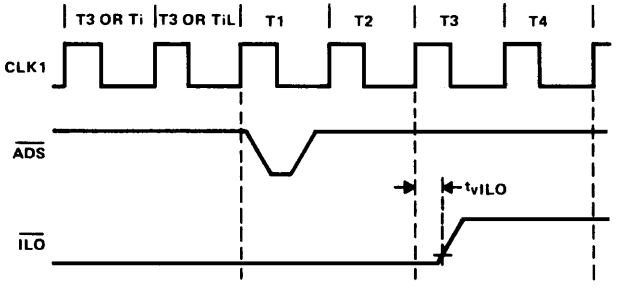

FIGURE 19. RELATIONSHIP OF $\overline{ILO}$ TO LST OPERAND CYCLE OF AN INTERLOCKED INSTRUCTION

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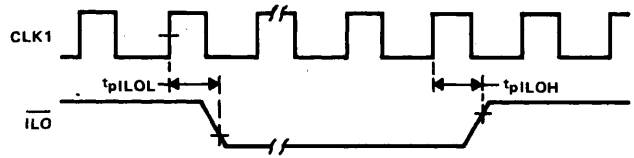

FIGURE 20. RELATIONSHIP OF $\overline{ILO}$ TO ANY CLOCK CYCLE

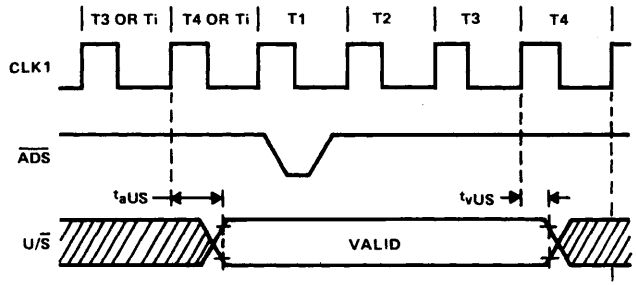

FIGURE 21. RELATIONSHIP TO ANY BUS CYCLE, GUARANTEED VALID INTERVAL

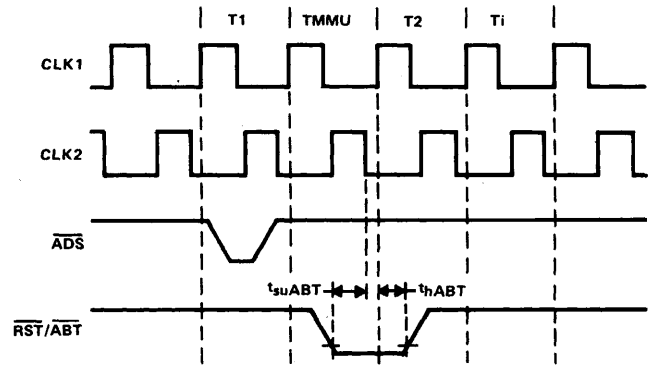

FIGURE 22. ABORT TIMING, $\overline{FLT}$ NOT APPLIED

4

Data Sheets

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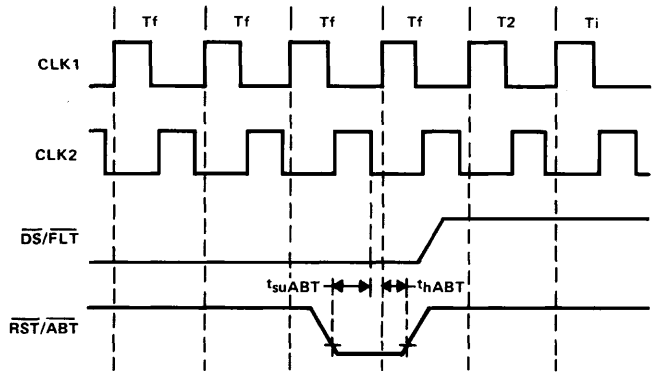

FIGURE 23. ABORT TIMING, $\overline{FLT}$ APLIED

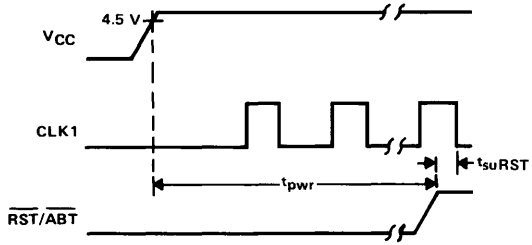

FIGURE 24. POWER-ON RESET

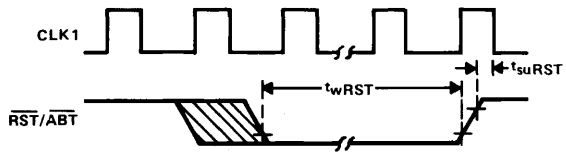

FIGURE 25. NONPOWER-ON RESET

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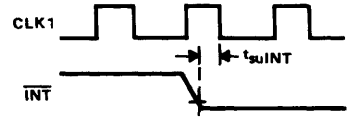

FIGURE 26. $\overline{INT}$ INTERRUPT SIGNAL DETECTION

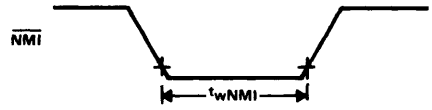

FIGURE 27. $\overline{NMI}$ INTERRUPT SIGNAL TIMING

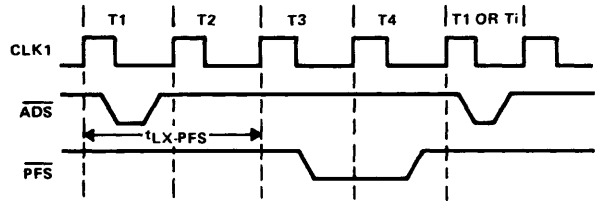

FIGURE 28. RELATIONSHIP BETWEEN LAST DATA TRANSFER OF AN INSTRUCTION AND $\overline{PFS}$ ON NEXT INSTRUCTION