Bt8071A

32-Channel HDLC Controller

Distinguishing Features

- Simplifies ISDN/DMI Implementation.
- Provides up to 32 Full-Duplex Channels With HDLC/SDLC Protocol Formatting.
- Provides Fully Programmable Hyperchannel Configuration.
- Supports All Four DMI B-Channel Data Options:
  - –Mode 0 (Clear Channel 64 kbps Synchronous).
  - –Mode 1 (56 kbps Synchronous Data With or Without HDLC Protocol).
  - –Mode 2 (up to 19.2 kbps Synchronous or Asynchronous)
  - –Mode 3 (64 kbps Virtual Circuit Service).
- Supports Both DMI D-Channel Signaling Options:
  - –Bit-Oriented Signaling (BOS)
  - –Message-Oriented Signaling (MOS).
- Programmable Three-State Output on T1/E1 Serial Interface.
  - –Allows Subchannel Access to T1/E1 Data.
  - –Eight Devices Can Attach to Common TDM Bus.
- Compatible With 1.544 Mbps T1 SF and ESF, as well as 2.048 Mbps CEPT PCM-30 Carrier Format.
- Supports Both Flag Stuffing (I.462, DMI mode 2) and RA2 Intermediate Rate Adaption (I.460, X.30, V.110, or ECMA-102).
- Compatible With HDLC, SNA SDLC, X.25, X.75, LAPB, and LAPD Protocols.
- Provides On-Board Buffer Memory Management Function.
- Provides On-Board CRC-16 Generation and Checking, Automatic Flag Detection and Transmission, and Zero-bit Insertion and Deletion.
- Interfaces to Brooktree Bt8070 T1/CEPT PCM Transceiver or BtT/P9170 Intelligent T1/E1 Controllers.
- Backward Compatible With The Bt8071.
- Available in 64-pin Quad In-Line Package (QUIP), 68-pin Leaded Chip Carrier (PLCC), or 68-pin Pin Grid Array (PGA).
- Operates From a Single +5 Vdc Supply.
- Low Power CMOS Technology.

Applications

- Primary Rate Interfaces
- Basic-Rate D-Channel Controller
- Multi-Channel HDLC Interfaces

Product Description

The Brooktree Bt8071A HDLC Controller multiplexes/demultiplexes up to 32 high-speed data channels to support HDLC and ISDN implementations (see Figure 2). The Bt8071A operates at layer 2 (data link protocol level) of the Open Systems Interconnection (OSI) reference model recommended by the International Organization for Standardization (ISO) and resides between the T1/E1 serial bus and a buffer memory shared with one or more host processors.

The Bt8071A processes transmit and receive data on a T1 communications link compatible with ANSI T1.403-1989 for 1.544 Mbps systems, or an E1 link at 2.048 Mbps in the CEPT PCM-30 carrier format. The device provides HDLC formatting functions for synchronous data and manages buffer memory for each of the active data channels, including the common signaling channel, with simple linked-list structures.

The Bt8071A is compatible with the ISDN (Integrated Services Digital Network) specified by the International Telegraph and Telephone Consultative Committee (CCITT) and supports connections to the ISDN at the primary rate. It also supports clear channel transmission of data at 64 kbps, 56 kbps synchronous, and supports 64 kbps virtual circuit protocol with LAPD, respectively.

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Product Description *(continued)*

The Bt8071A provides additional functions that support X.30 and X.31 rate adaption, as well as ISDN and fully flexible hyperchannels. The device is also compatible with HDLC, SNA SDLC, X.25, X.75, LAPB, and LAPD protocols. These features allow the use of the Bt8071A in applications that go beyond the host-end computer-PBX interface.

The Bt8071A complements the Brooktree Bt8070 T1/CEPT PCM Transceiver and the BtT/P9170 Intelligent T1/E1 Controllers. Those devices operate at layer 1 (physical interface level) of the OSI reference model, and provide basic T1/E1 framing and maintenance functions of the T1/E1 link.

The Bt8071A finds applications in diverse areas of telecommunications (including TDM machines, central-office switches, and PBX) as well as the basic host computer-PBX links. In ISDN switching applications, the Bt8071A can function as a multiplexed controller for as many as 32 ISDN basic access D-channels and can substantially off-load LAPD processing from the switch central control.

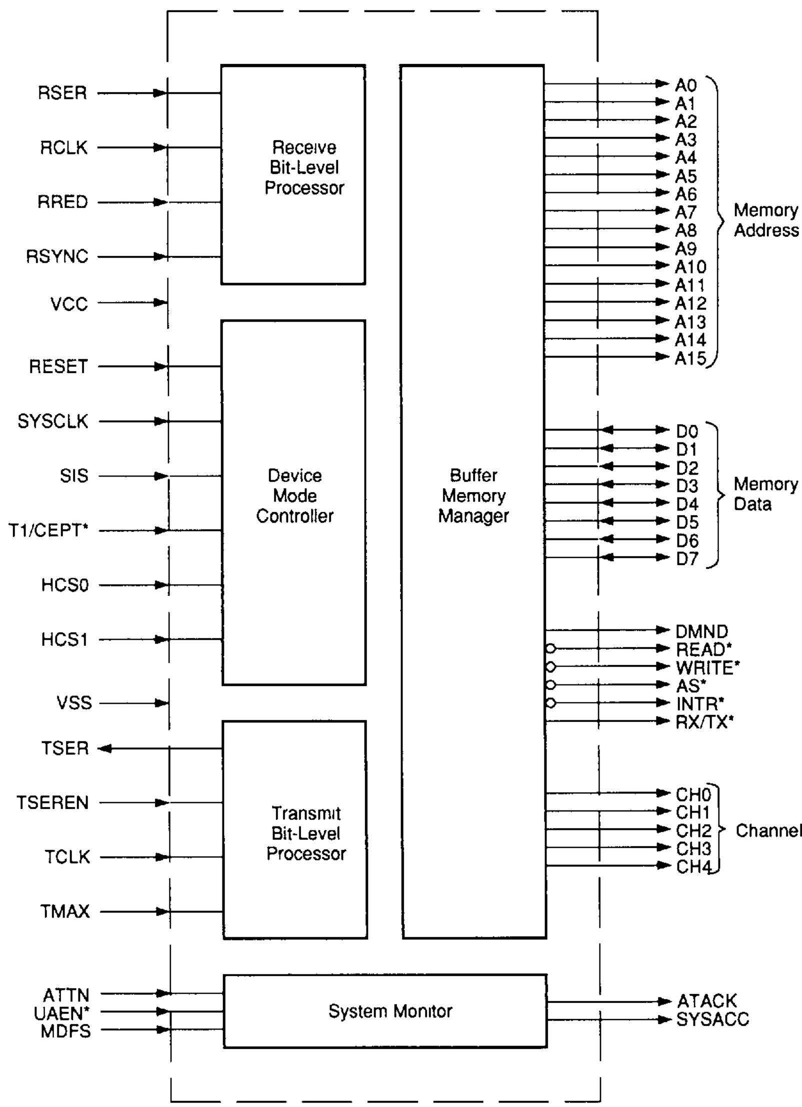


Figure 1. Bt8071A Functional Block Diagram.

Product Description *(continued)*

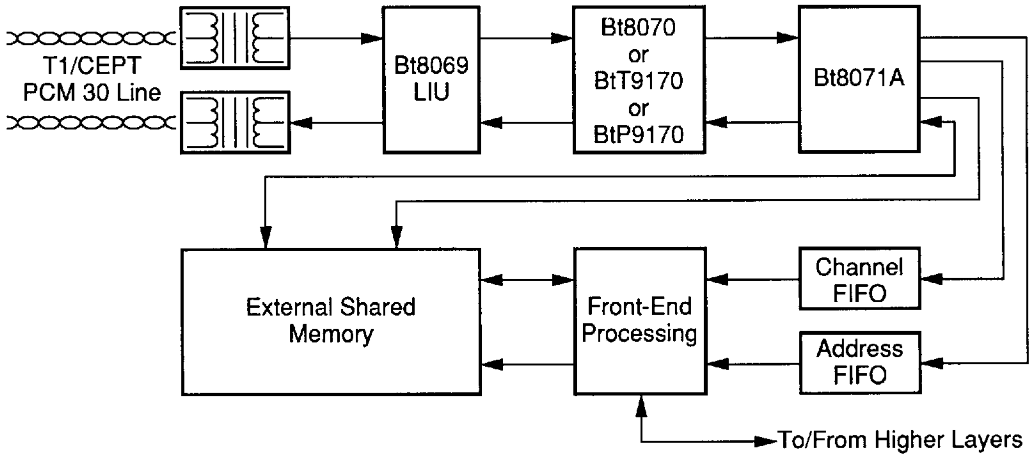


Figure 2. Functional Architecture for Host ISDN Primary Rate Access and PBX ISDN Trunkside Adapter.

Interface

The Bt8071A ISDN Link Layer Controller transmits data to, and receives data from, a Bt8070 T1/CEPT PCM Transceiver or the BtT/P9170 Intelligent T1/E1 Controllers as illustrated in Figure 2. The Bt8071A transfers the data in 8-bit parallel form to and from an external buffer memory shared by a host computer system. (The external buffer memory is referred to as "shared memory," and the host computer system is referred to as the "host.") The Bt8071A interface signals are functionally grouped in Figure 3. The Bt8071A pin assignments are shown in Figure 4, and the Bt8071A interface signals are defined in Table 1.

Bt8071A Enhancements

The Bt8071A adds two major enhancements to the Bt8071: partial command buffers and software-programmable flexible hyperchannel. The Bt8071A is hardware and software compatible with the Bt8071.

Partial Command Buffers

This new command is incorporated to significantly lower the overhead needed to initiate the transmission of a new chain of data buffer after the transmitter of a chain has entered the idle flag (HDLC mode) or all-ones (non-HDLC mode) transmission state.

The COMPLETE/PARTIAL bit of the STATUS byte of the command buffers is not accessed on the Bt8071; it is a "don't-care" bit. The Bt8071A uses this bit in conjunction with the COMMAND/DATA bit to determine if the partial command buffer is to be used. If this bit was always set to one in a Bt8071 system, then the Bt8071A can directly replace the Bt8071.

A detailed description is under "Transmit Data/Command Buffer Organization" in the External Shared Memory Organization and Definition section.

Flexible Hyperchannel

Flexible hyperchannel allows software to dynamically group multiple individual 64 kbps channels into hyperchannels, thus allowing users to allocate bandwidth according to channel requirements. The flexible hyperchannel supports grouping of any number of contiguous and noncontiguous individual channels for both the T1 and the PCM-30 environments. This enhancement also supports independent transmit and receive hyperchannel assignments.

DATA LENGTH in the command buffers is used by the Bt8071A to determine whether flexible hyperchannels are to be activated. If DATA LENGTH = 002, then no flexible hyperchannel is used for this channel, and the Bt8071A functions the same as the Bt8071. If DATA LENGTH > 002, then the Bt8071A will enter the flexible hyperchannel mode for this

Product Description *(continued)*

channel. The Bt8071 does not access DATA LENGTH in the command buffers. If DATA LENGTH in the command buffers always equals two in a Bt8071 system, then the Bt8071A can directly replace the Bt8071.

A detailed description is under "Flexible Hyperchannels" in the External Shared Memory Organization and Definition section.

The CH0–CH4 pins of the Bt8071 and Bt8071A indicate which channel is being processed at any given time. On the Bt8071 the channel numbers are always sequential for both the receiver and transmitter; the channel number increments by one until it wraps around to zero, then counts by one again. If the Bt8071A is not running flexible hyperchannels, then the channel numbers operate the same as the Bt8071. If flexible hyperchannels are used, then the channel numbers may not be sequential, but instead, display the channels as they are arranged in the flexible hyperchannel scheme. The channel numbers still reflect the actual channel being processed and may be used as part of the dual-port memory addressing circuit, but the Bt8071A system design may not depend on sequential channel numbers.

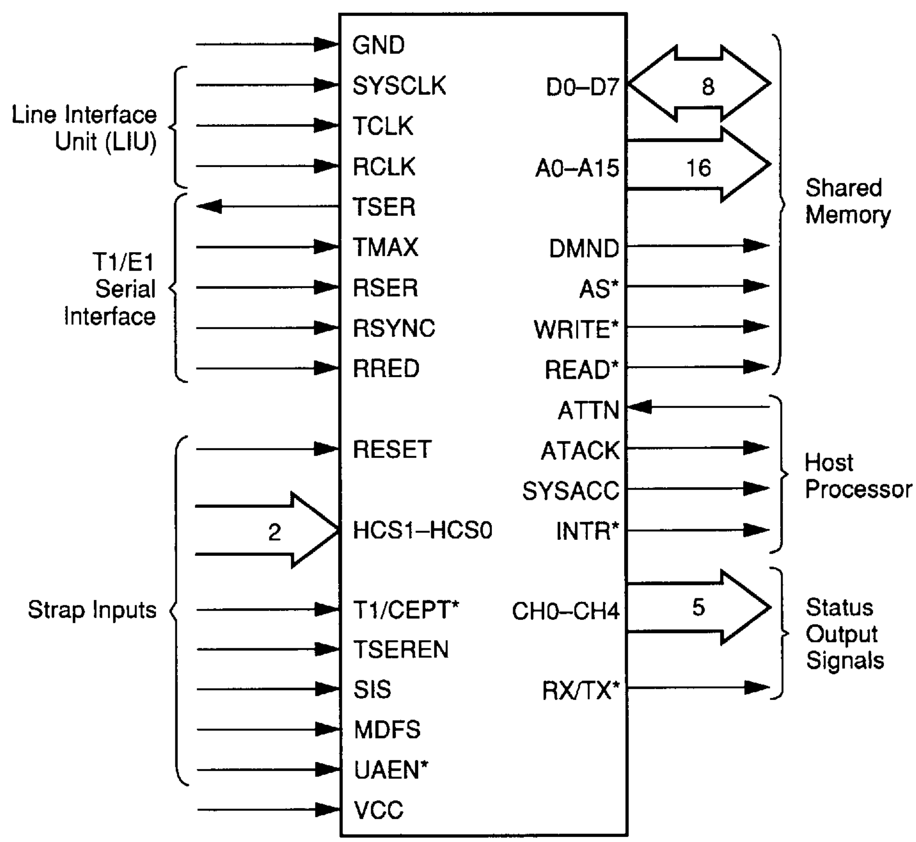


Figure 3. Bt8071A Interface Signals.

Pin Descriptions

Symbol	I/O	Signal Name/Description
Memory Interface		
D0–D7	I/O	**Memory Data Lines.** Bidirectional 8-bit memory data bus between the Bt8071A and the shared memory. D0 is the LSB, and D7 is the MSB.
A0–A15	O	**Memory Address Lines.** Output lines to the shared memory. A0 is the LSB, and A15 is the MSB.
DMND	O	**Memory Demand.** Active high output to the shared memory. The Bt8071A accesses shared memory within one TCLK period after assertion (rising edge) of DMND. DMND is negated at completion of the memory access cycle.
AS*	O	**Memory Address Strobe**. A valid memory address is present on the memory address lines at the falling edge of the active low AS*.
WRITE*	O	**Memory Write.** Active low output to the shared memory to perform a write cycle.
READ*	O	**Memory Read.** Active low output to the shared memory to perform a read cycle. Data from memory is latched in the Bt8071A on the rising edge of SYSCLK prior to the negation of READ*.
ATTN	I	**Attention.** Active, high input that commands Bt8071A to read and process the CAB (Channel Activation Byte) at system memory location 0000h. A sequence of memory accesses is performed soon after ATTN is asserted. ATTN must be negated in response to ATACK.
ATACK	O	**Attention Acknowledge.** Active high output asserted when the sequence of memory accesses (in response to ATTN) is complete. ATACK is negated in response to negation of ATTN.
SYSACC	O	**System Access.** Active high output asserted to indicate the Bt8071A is accessing 1 of the 128 system memory locations (channel activation byte or channel buffer pointers).
INTR*	O	**Interrupt.** Active low output pulse of one SYSCLK period to the host system to indicate that the buffer status is being updated.
LIU Interface		
SYSCLK	I	**System Clock.** Square-wave input from the LIU. Nominally, 3.088 MHz for T1 and 4.096 MHz for CEPT PCM-30. Bt8071A uses SYSCLK to generate all of the shared memory interface timing.
TCLK	I	**Transmit Clock.** Square-wave input from the LIU clock generator, providing the timing source for the Transmit T1/E1 Serial Interface. The frequency is one half that of the SYSCLK and must remain phase aligned with SYSCLK.
RCLK	I	**Received Clock.** Input from the external LIU/clock recovery for the Bt8071A to sample RSER, the received serial data. Nominally, 1.544 MHz for T1 and 2.048 MHz for CEPT PCM-30 (E1).
Serial Interface		
TSER	O	**Transmitter Serial Data.** Three-state output from the Bt8071A to the T1/E1 Serial Interface, representing the transmit serial data bit stream.
TMAX	I	**Transmit Multiframe Sync.** Active high input pulse from the T1/E1 Serial Interface, indicating the beginning of a multiframe.
RSER	I	**Received Serial Data.** Input from the T1/E1 Serial Interface, representing the received serial data bit stream.
RSYNC	I	**Receive Synchronization**. Active high input level or pulse for receive frame synchronization reference.
RRED	I	**Receive Red Alarm.** Active, high input indicating T1/E1 receive data is invalid due to a loss of frame alignment or similar alarm condition. Bt8071A aborts all receive channel processing while RRED is active. Receive channel processing is enabled when RRED is inactive.

Table 1. Bt8071A Interface Signal Definitions.

Pin Descriptions *(continued)*

Symbol	I/O	Signal Name/Description
Strap Option Inputs		
T1/CEPT*	I	**T1 or CEPT Framing Select.** "High" selects the T1 framing mode. "Low" selects the CEPT PCM-30 framing mode.
HCS1,HCS0	I	**Hyperchannel Select.** Encoded inputs select the T1/CEPT PCM–30 hyperchannels (See Figure 4).

T1/CEPT* (Note 1)	HCS1	HCS0	Channel Selection
X	Low	Low	All channels are 64 Kbps.
High	High	Low	Four channels of 384 Kbps (H0) (Note 2).
High	Low	High	Single channel of 1.536 Mbps (H11) (Note 2).
Low	High	Low	Single channel of 1.92 Mbps (H12) (Note 3), time slots 0 and 16 are 64 Kbps.
X	High	High	Reserved.
Low	Low	High	Reserved.

Note 1: "X" denotes don't care.
Note 2: Valid for T1 only.
Note 3: Valid for CEPT only.

Symbol	I/O	Signal Name/Description
TSEREN	I	**TSER Enable.** Active high input that works in conjunction with the FILL/MASK bit as follows:

TSEREN	FILL/MASK Bit	
	0 (Note 1)	1
High	Send a 1 on TSER	Send data on TSER
Low	High-impedance output on TSER	Send data on TSER

Note 1: Or any F bit, or any bit during RESET, Bt8071A initialization, until a channel is activated.

Symbol	I/O	Signal Name/Description
SIS	I	**Serial Interface Select.** "High" identifies a Bt8070 or BtT/P9170 compatible serial interface. "Low" identifies AT&T compatible interface.
MDFS	I	**Memory Data Format Select.** "High" indicates that the most and least significant bytes of next buffer start address, buffer size, and data length in shared memory reside at even and odd addresses, respectively (68,000 MPU word addressing compatible). "Low" indicates that the least and most significant bytes of next buffer start address, buffer size, and data length reside at even and odd addresses, respectively (8,086 MPU word addressing compatible).
UAEN*	I	**Upper Address Enable.** High-level input causes the upper address bus lines (A8–A15) to be in the high-impedance state during system shared memory access when SYSACC is asserted. Low input causes the upper address outputs to be forced low by the Bt8071A when SYSACC is asserted.

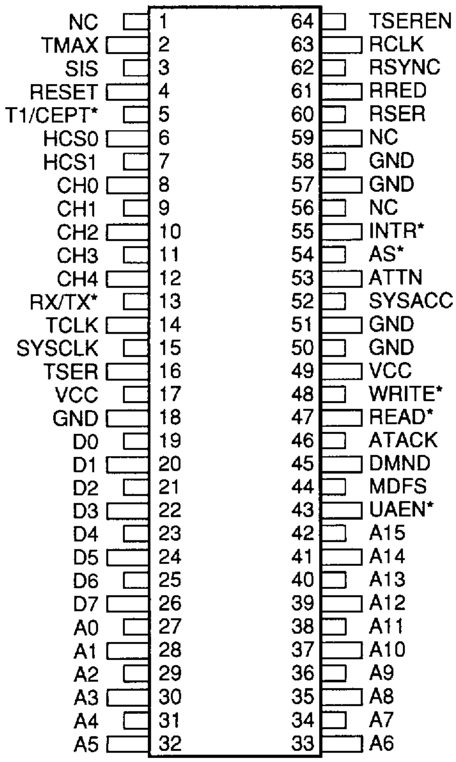
Table 1**(continued). **Bt8071A Interface Signal Definitions.

Pin Descriptions *(continued)*

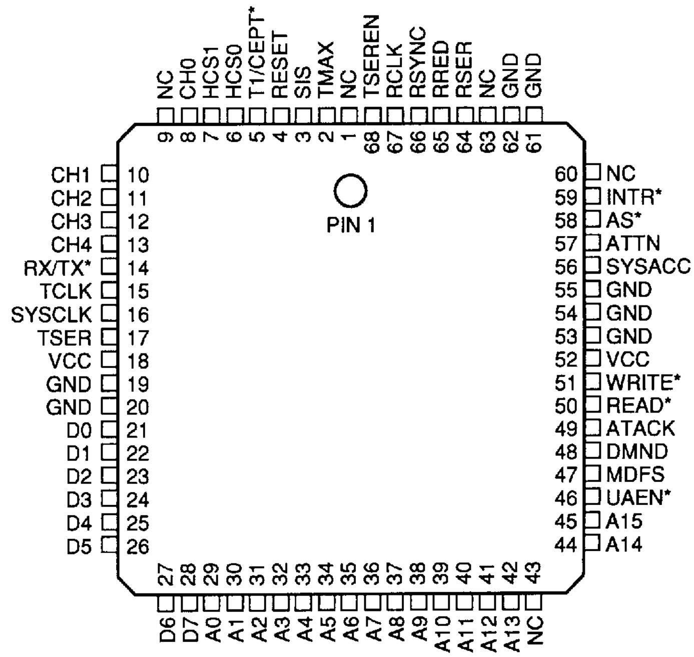
Symbol	I/O	Signal Name/Description
Status Outputs		
CH0–CH4	O	**Channel Number (0–4).** Encoded output indicating the channel number being served. CH0 is the LSB, and CH4 is the MSB.
RX/TX*	O	**Receive/Transmit Channel.** Output used in conjunction with the channel number (CH0–CH4). "High" indicates a receive channel, and "low" indicates a transmit channel.
Reset and Power		
RESET	I	**Reset.** Active high input that initializes all Bt8071A functions. RESET causes the Bt8071A to default to HDLC mode, causes all zeros in the FILL/MASK, and deactivates all channels. Inactive transmit channels output all ones. Bt8071A initialization is complete within 90 SYSCLK periods after RESET returns low.
VCC		**Power Supply Voltage.** +5 Vdc with respect to VSS.
VSS		**Ground.** Ground reference voltage.

Table 1** (continued). **Bt8071A Interface Signal Definitions.

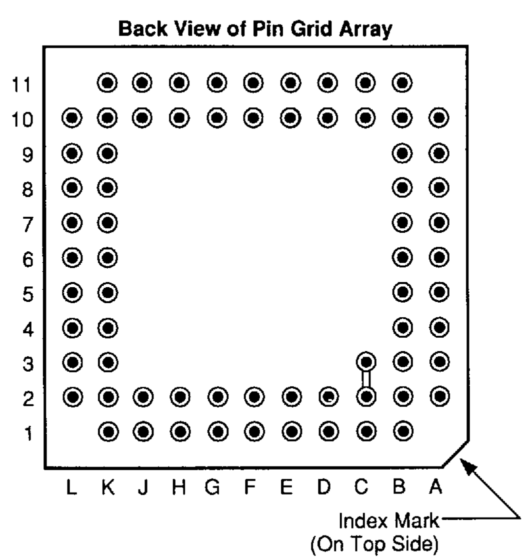
Pin Descriptions *(continued)*



64-Pin QUIP



68-Pin PLCC



PIN	Signal	PIN	Signal	PIN	Signal	PIN	Signal
A2	NC	B9	MDFS	F10	A6	K4	TCLK
A3	INTR*	B10	A15	F11	A7	K5	TSER
A4	ATTN	B11	A14	G1	RESET	K6	Vcc
A5	GND	C1	RSER	G2	SIS	K7	GND
A6	GND	C2	NC	G10	A4	K8	D1
A7	VCC	C10	A12	G11	A5	K9	D3
A8	READ*	C11	A13	H1	HCSO	K10	D6
A9	DMND	D1	RSYNC	H2	T1/CEPT*	K11	D7
A10	UAEN*	D2	RRED	H10	A2	L2	CH3
B1	GND	D10	A10	H11	A3	L3	RX/TX*
B2	GND	D11	A11	J1	CH0	L4	SYSCLK
B3	AS*	E1	TSEREN	J2	HCS1	L5	VCC
B4	SYSACC	E2	RCLK	J10	A0	L6	GND
B5	GND	E10	A8	J11	A1	L7	D0
B6	VCC	E11	A9	K1	CH1	L8	D2
B7	WRITE*A	F1	TMAX	K2	CH2	L9	D4
B8	TACK	F2	NC	K3	CH4	L10	D5

NC = No connection to be made with this pin

68-Pin PGA

Figure 4. Bt8071A Pin Assignments.

Functional Description

The Bt8071A fetches the data to be transmitted from the shared memory. It then processes the data for up to 32 channels, channel-by-channel, by performing protocol formatting and rate adaption. Finally, it transmits the data to the T1/E1 Transceiver in serial form. Similarly, the Bt8071A processes, on a channel-by-channel basis, the received serial data on up to 32 channels by performing protocol deformatting and rate adaption, and stores the data into the shared memory.

Each channel is processed depending on the operational mode specified by the host as set up in the shared memory. For any channel, the transmitter and the receiver operating modes may be specified independently of each other.

The internal functions of the Bt8071A are partitioned logically into five major blocks (See Figure 1 in the Product Description section):

1. Transmit Bit-Level Processor
2. Receive Bit-Level Processor
3. Buffer Memory Manager
4. Device Mode Controller
5. System Monitor

Transmit Bit-Level Processor

HDLC and Non-HDLC Modes

The transmit bit-level processor performs basic HDLC (Note 1) protocol formatting (DMI data modes 2 and 3, ISDN LAPD, and IBM SNA) or other nonprotocol transmit functions (DMI data modes 0 and 1, and bit-oriented signaling mode) for each channel independently of any other channel.

In the HDLC mode, this processor generates flags, and abort and idle codes; inserts zeros for bit transparency; computes the HDLC frame check sequence (FCS); and composes HDLC frames from the data provided in the shared memory.

In the non-HDLC data mode, the data from the shared memory is not framed.

In either mode, the Bt8071A performs rate adaption of sub-64 kbps data rates of the form,

n x 8 kbps (n = 1 through 8)

Note 1. The Bt8071A does not distinguish between the High Level Data Link Control (HDLC) and the Synchronous Data Link Control (SDLC) protocols but implements the common link-layer functions for both. Reference to HDLC in this document also implies SDLC unless otherwise stated.

to the standard 64 kbps bearer rate (I.460, second stage RA2). An 8-bit FILL/MASK sequence (specified in shared memory) is applied to the HDLC-formatted or non-HDLC data on a bit-by-bit basis (see FILL/MASK description in the External Shared Memory Organization and Definition section. The resulting 8-bit sequence, consisting of the actual data bits and any time-fill bits (always a one) based on the FILL/MASK sequence, is then transmitted over the channel. Figure 5 illustrates this process.

In the HDLC mode, the Bt8071A adapts the standard sub-64 kbps data rates (CCITT X.1 or DMI mode 2, but not necessarily n x 8 kbps) directly to the 64 kbps bearer rate (I.462 and DMI).

A number (specified in the shared memory) of HDLC flags are appended to the end of an HDLC frame as time-fill sequences.

The Bt8071A monitors the number of intentionally inserted zeros (which may be viewed as nondata intraframe time-fill bits). The programmed number of flags are adjusted based on the number of zeros inserted. Reset activates the HDLC mode for all channels.

Logical Inversion

This logical inversion of data, as well as of abort, flag, and FCS bits, before transmission is programmable. RESET activates inversion for all channels.

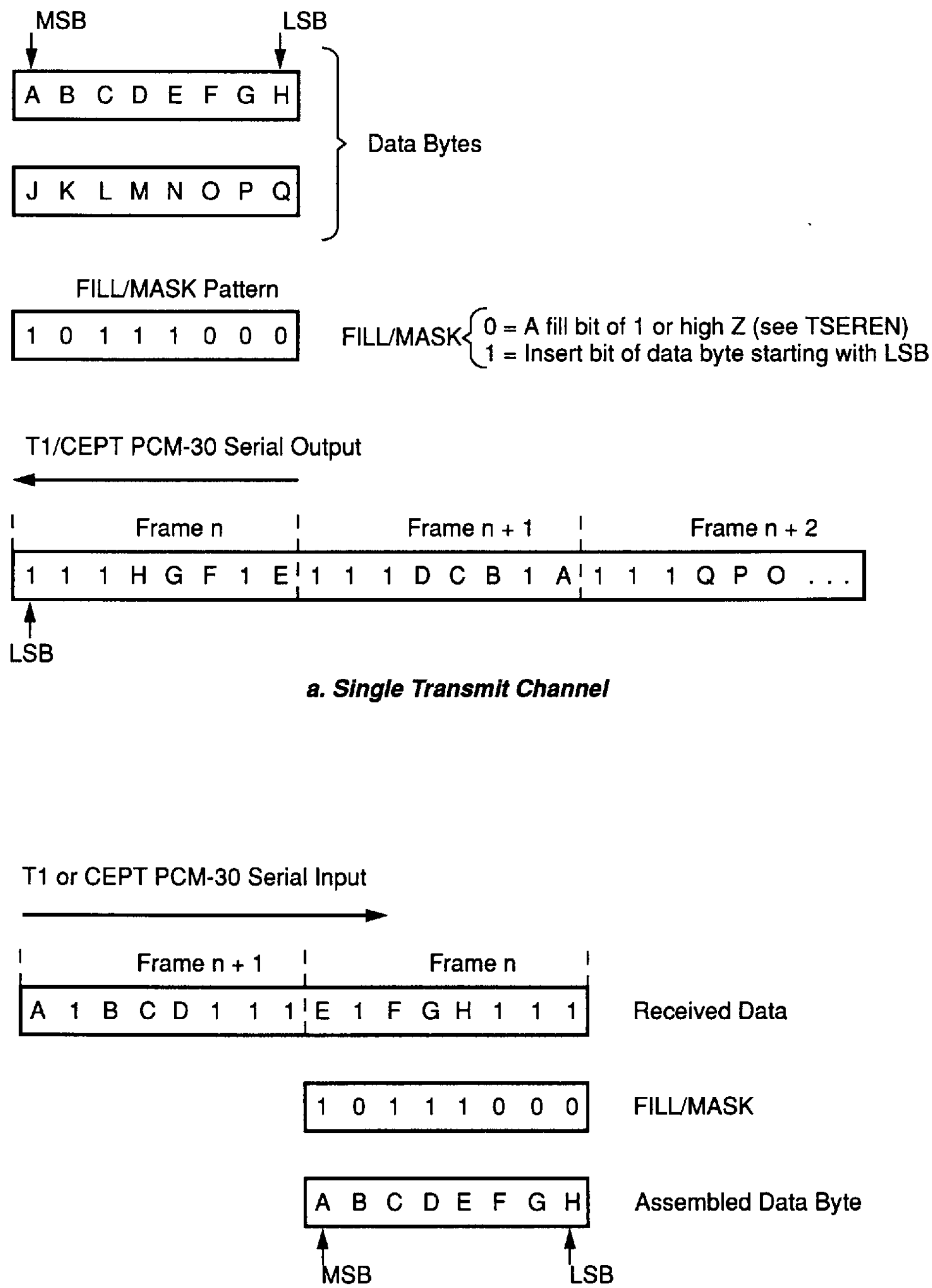
Loop Mode

Loop mode for both the transmit and receive channels is also programmable in shared memory. For a channel in the near-end loop mode, the Bt8071A stores the data transmitted during the channel period in an intermediate buffer. Such data is to be taken by the receive data channel programmed in the loop mode and eventually sent back to the shared memory. Only a single transmit channel and a single receive channel may be placed in the loop mode at one time for proper operation. Loop mode does not support H0 hyperchannel operation. RESET deactivates the loop mode for all channels.

Signaling

Bit-oriented signaling and LAPD-based message-oriented signaling channels are directed to the non-HDLC processing elements with no special consideration.

Functional Description *(continued)*

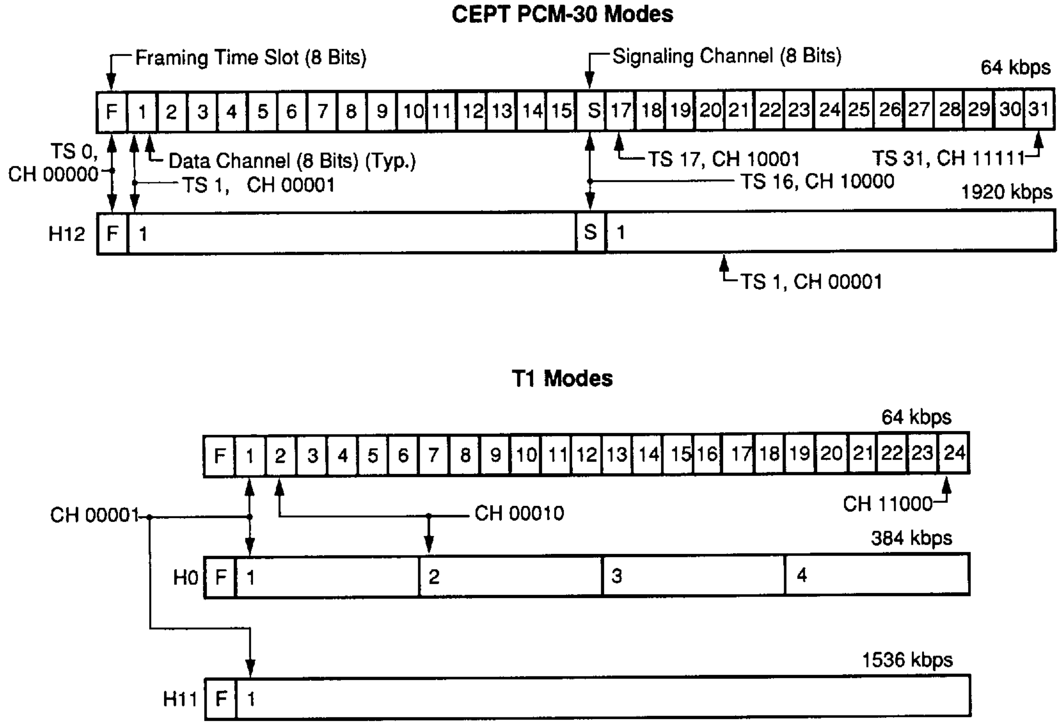


a. Single Transmit Channel

b. Single Receive Channel

Figure 5. 32 kbps Subrate Operation.

Functional Description *(continued)*



Note: Grouping of 64 kbps channels into standard hyperchannels is fixed as shown. Timeslot assignments can be changed (when HCS1–0 = 00) to create flexible hyperchannels by programming command buffers.

Figure 6. Bt8071A Standard Hyperchannel Provisory.

ISDN Hyperchannels

The 64 kbps channels (or time slots) are grouped into the ISDN standard hyperchannels (see Figure 6). One hyperchannel grouping is specified by the HCS1 and HCS0 inputs (see Table 1, "Strap Input Options"). RESET deactivates signaling mode for all channels.

Alternatively, the 64 kbps timeslots may be grouped randomly to form nonstandard, fully flexible hyperchannels. Each hyperchannel contains any number of 64 kbps timeslots, which allows customizing the data channel bandwidth.

Transmit Interface

The transmit bit-level processor interfaces directly to a Bt8070 T1/CEPT PCM Transceiver or BtT/P9170 T1/E1 Controllers with no external circuitry. All the channel counter functions are built in. The TSER (Transmit Serial Data) output is driven with the transmit serial data bit stream acquired from the shared memory. The TCLK (Transmit Clock) input is the timing reference for TSER. The TMAX (Transmit Multiframe Sync) input is the starting reference for the TDM frame.

TSER is placed in the high-impedance (three-state) mode whenever the TSEREN input is low and the FILL/MASK bit is 0 (see Table 1, "Strap Input Options"). This enables the TSER outputs of up to eight Bt8071As to be connected together and allows them to be programmed with mutually exclusive FILL/MASK sequences in order to accomplish subrate time-division multiplexing over a 64 kbps channel.

In summary, each channel may be programmed by the host system independent of any other channel by specifying HDLC-mode, FILL/MASK, data-inversion, and loop-mode options. Both the rate adaption recommendation, namely HDLC flag insertion and the second-stage intermediate rate adaption, are implemented. In addition, various other HDLC-formatted rates of the form n x 8 kbps (n = 1 – 8) are also adapted to the 64 kbps bearer rate.

Functional Description *(continued)*

Receive Bit-Level Processor

HDLC and Non-HDLC Modes

The receive bit-level processor performs basic HDLC/SDLC protocol deformatting (DMI data modes 2 and 3, ISDN LAPD, and IBM SNA) or other non-protocol receive functions (DMI data modes 0 and 1, and bit-oriented signaling channels) for each channel independent of any other channel.

In the HDLC mode, the Bt8071A detects flags, aborts, inserts zeros, and checks the FCS (Frame Check Sequence). It also filters out any time-fill patterns received by applying the 8-bit FILL/MASK sequence specified in the shared memory. The resulting serial data, including the HDLC header (i.e., address and control fields), is then assembled into bytes for storage in the shared memory (Figure 4b). The validity of every HDLC frame is checked and reported to the shared memory appropriately. RESET activates HDLC mode for all channels.

In the non-HDLC data mode, any time-fill patterns received are also filtered out based on the 8-bit FILL/MASK sequence. The resulting serial data is grouped into bytes for transfer to the shared memory.

Logical Inversion

Logical inversion of all the received serial data is programmable in the external shared memory. RESET activates inversion for all channels.

Loop Mode

Loop mode for receive channels is also programmable in shared memory. For a channel in the near-end loop mode, the input data is taken from an internal buffer rather than from the external data. The internal buffer presumably has been filled with data from a transmit channel in the loop mode. Thereafter, the looped data is processed according to the specified mode of operation. RESET deactivates loop mode for all channels.

Non-HDLC Signaling Mode

In the non-HDLC signaling channel mode, the Bt8071A detects the multiframe (or extended superframe) alignment sequence for DMI bit-oriented signaling (G.732 and DMI). If a valid multiframe alignment is found, the received data is transferred to shared memory. If the multiframe alignment sequence is found to be in error, transfer of signaling data to the shared memory is suspended until a valid multiframe is detected (G.732 and DMI). Loss of multiframe is reported to the shared memory. Any channel(s) can be specified to receive bit-oriented signaling. This feature is very useful in central-office switching applications. RESET deactivates signaling for all channels.

ISDN Hyperchannels

The 64 kbps channels are grouped into the ISDN standard hyperchannels (see Figure 6) based on the input strap pins HCS0 and HCS1 (see Table 1, "Strap Input Options" in the Pin Description section).

Alternatively, the 64 kbps timeslots may be grouped randomly to form nonstandard, fully flexible hyperchannels. Each hyperchannel is made up of any number of timeslots, which allows customizing the bandwidth of data channels.

Elastic Buffer

The received serial data from a T1/CEPT PCM-30 mutiframe, in general, has no relationship to the transmit data multiframe in terms of frame beginning. Both the receive bit-level processor and the transmit bit-level processor exchange data with the shared memory over a single data bus. In order to handle contention for the data bus, an elastic buffer is used in the receive bit-level processor.

The elastic buffer input is clocked by the RCLK (Receive Data Clock), and the output is re-timed with the TCLK (Transmit Data Clock). Thus the TCLK is used as a reference for both the transmit and the re-timed receive data. As a result, the shared memory access is simple and predictable. The looped data bypasses the elastic buffer. Also, any overflow or underflow of the elastic buffer is reported to the shared memory for all the channels. The elastic buffer also protects the shared memory against underflow or overflow in the remote loopback (i.e., echo) mode.

Receive Interface

The receive bit-level processor interfaces directly to the Bt8070 or BtT/P9170 with no need for additional logic. All the needed channel counters are supplied internally. Received serial data is extracted from the RSER (Received Serial Data) input bit stream on the falling edge of the RCLK (Receive Clock) input. (Bt8070/BtT/P9170 mode, see SIS input).

The RSYNC (Receive Synchronization) input provides a frame synchronization reference. The RRED input is monitored for loss of T1/CEPT PCM-30 frame synchronization and reported to the shared memory.

Functional Description (continued)

Buffer Memory Manager

The buffer memory manager controls the flow of data between the transmit bit-level processor/receive bit-level processor and the data buffers in external shared memory. Shared memory is allocated for each transmit or receive channel as a linked list of buffers that are set up by the host. The shared memory is managed with minimal intervention from the host. The host allocates enough memory in the buffers for the real-time operation of transmission and reception to take place with no data underrun or overrun, respectively.

The buffers contain such information as operational modes, buffer or HDLC frame completion status, size of the buffer, number of transmit or receive data bytes, link to the next buffer, and the transmit or receive data bytes.

The Bt8071A updates the status of each channel buffer as each buffer or HDLC frame is completed and simultaneously asserts the interrupt indication (INTR*) output to the host.

During transmission, the MPTY (Empty), CMND (Command), and CF/P* (Complete Frame/Partial Data Buffer) bits are monitored in the transmit status byte (see the External Shared Memory Organization and Definition section). The MPTY, IVBA (Invalid Buffer Address), and UNDR (Underrun) bits in the transmit status byte in shared memory are updated.

During reception, the MPTY, CMND, and CF/P* bits are monitored in the receive status byte. The MPTY, IVBA (Invalid Buffer Address), and CF/P* bits in the receive status byte in shared memory are updated. Three encoded error reporting bits in the receive status byte, ABRT (Abort), FCER (Frame Check Error) and SHER (Short HDLC Frame Error), are also updated to report such conditions as invalid HDLC frame, frame check error, abort code received, loss of T1/CEPT PCM 30 frame synchronization, loss of T1/CEPT PCM 30 signaling channel multiframe alignment, and elastic buffer underrun or overrun.

Operational modes, loop, invert commands, and the FILL/MASK patterns are extracted from the transmit and receive command buffers and passed to the transmit bit-level processor and the receive bit-level processor, respectively. The modes are decoded from the HDLC (HDLC Mode Select) and SIG (Signaling Mode Select) bits. Loop and invert commands are pulled from the LOOP and INV bits, respectively.

The buffer memory manager responds to host processor-initiated changes in the operational modes of a channel or relocation of the allocated buffers without affecting the operation of the other channels.

The channel number (CH0–CH4) and RX/TX* (Receive/Transmit Channel) outputs are updated to reflect to the channel being served.

The buffer memory manager also causes mode changes in the transmit bit-level processor and the receive bit-level processor in response to the host processor-initiated mode changes.

Device Mode Controller

The device mode controller provides the central device timing and control for the other device functions. General and memory interface internal timing is derived from the SYSCLK (System Clock) input. Device reset to the other functions is distributed based on the RESET (Reset) input.

The selected carrier and framing format based on the T1/CEPT* (T1/CEPT PCM-30 Carrier Select) input and the encoded hyperchannel select inputs (HCS0 and HCS1) is passed to the transmit bit-level processor and the receive bit-level processor. The transceiver interface specified by the SIS (Serial Interface Select) input is also routed to those functions (see Table 1, "Strap Input Options" in the Pin Description section).

System Monitor

The system monitor informs the buffer memory manager of a host-initiated ATTN (Attention) command. Prior to asserting ATTN, the host will have set up, in shared memory, the actual channel number that needs the Bt8071A's attention, its mode of operation, and the start address of the linked list of buffers.

Whenever the Bt8071A accesses the channel activation byte or channel buffer pointers in shared memory, the SYSACC (System Access) output is asserted, indicating that system memory is being accessed. At that time, the upper order address lines (A8–A15) are placed in the high-impedance state or driven low, depending on whether the UAEN (Upper Address Enable) input is high or low, respectively. In the high-impedance state, the host can drive the A8–A15 lines to any logic level. When the Bt8071A completes the ATTN command processing, the ATACK (Attention Acknowledgment) output is asserted. The falling edge of ATTN causes ATACK to return low.

In addition, the relative locations of the upper (most significant) and the lower (least significant) bytes of certain 16-bit words (i.e., next buffer address, buffer size, and data length) in the shared memory are determined based on the MDFS (Memory Data Format Select) input (see Table 1, "Strap Input Options" in the Pin Description section).

Serial Interface to Bt8070/BtT/P9170 (SIS = HIGH)

Transmit

T1 Mode (T1/CEPT* Input High)

The TSER (Serial Data Output) from the Bt8071A changes in response to the falling edge of the TCLK as shown in Figure 7. Setup and hold time periods for TSER are such that TSER can be sampled reliably at the next rising edge of the TCLK inside the Bt8070/BtT/P9170. TSER is a three-state output. Its actual logic level and impedance level over any bit period are determined by the combination of the corresponding FILL/MASK bit and the TSEREN input.

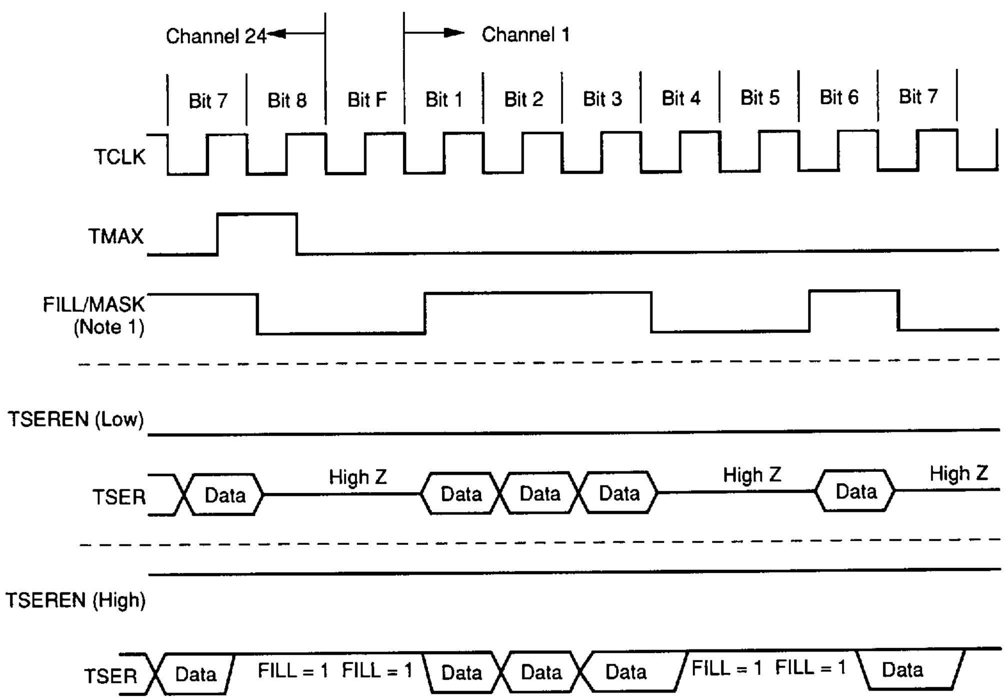
Transmit synchronous operation between the Bt8070/BtT/P9170 and the Bt8071A is attained by TMAX application.

When TMAX is synchronously asserted, the Bt8071A will be transmitting the last bit of a frame. TMAX may be applied synchronously as frequently as a frame rate or as seldom as when a system needs to re-initiate synchronism.

When TMAX is applied to initiate synchronism, the transmitter completes the processing of the current channel, fills the interim time with ones or goes high impedance (see TSEREN), and begins transmitting the first bit of time slot one, which will occur nine or ten (CEPT/T1) bit times after TMAX.

CEPT PCM-30 Mode (T1/CEPT* Input Low)

TSER from the Bt8071A changes in response to the falling edge of the TCLK as shown in Figure 8. Setup and hold time periods for TSER are such that TSER can be sampled reliably at the next rising edge of the TCLK by the Bt8070/BtT/P9170. TSER is a three-state output. Its actual logic level and impedance level over any bit period are determined by the combination of the corresponding FILL/MASK bit and the TSEREN input.



Note 1: The F-Bit time is processed as if the FILL/MASK = 0. However, this actual FILL/MASK does not apply to the F-Bit.

Figure 7. Transmit Frame Synchronization Timing–T1 Mode (Bt8070/BtT/P9170 Interface).

Serial Interface to Bt8070/BtT/P9170 (SIS = HIGH) *(continued)*

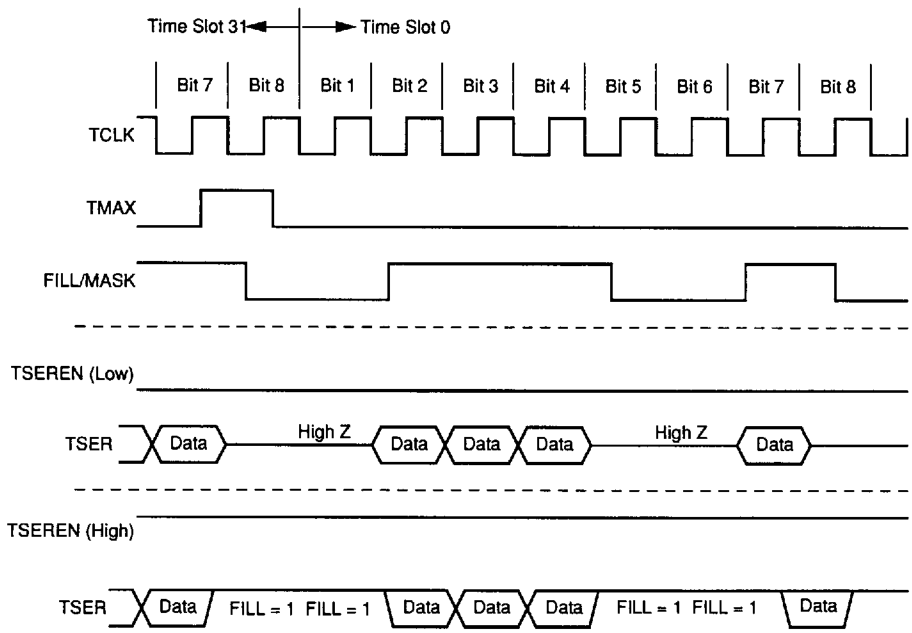


Figure 8. Transmit Frame Synchronization Timing–CEPT PCM 30 Mode (Bt8070 Interface).

Receive

T1 Mode (T1/CEPT* Input High)

The RSER (Receive Data) is processed serially and sampled at the negative edge of RCLK at a rate of 1.544 MHz. The Bt8070/BtT/P9170 multiframe synchronizes at the third assertion of RSYNC after RRED (internally delayed) goes low. RSYNC is synchronous with the rising edge of RCLK and the first F-bit of a multiframe. Figure 9 illustrates the timing.

CEPT PCM-30 Mode (T1/CEPT* Input Low)

RSER is processed serially and sampled by the negative edge of RCLK at a rate of 2.048 MHz. RSYNC is synchronous with the rising edge of RCLK and bit 1 in time slot zero of the first frame of a multiframe. Figure 10 illustrates the timing.

Serial Interface to Bt8070/BtT/P9170 (SIS = HIGH) *(continued)*

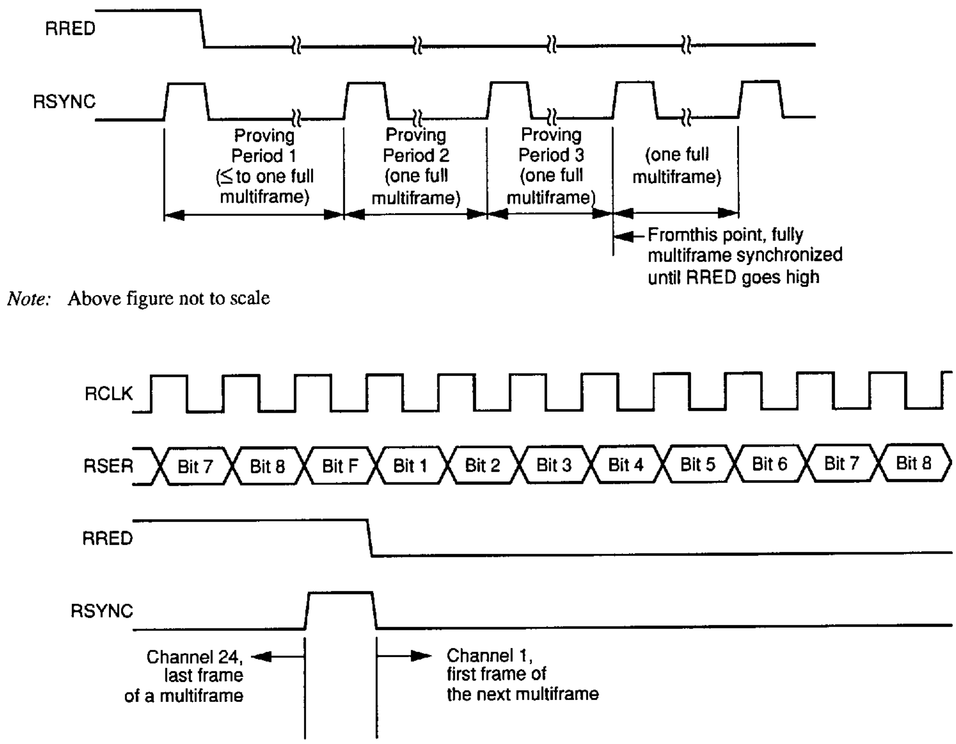


Figure 9. Receive Frame Synchronization Timing–T1 Mode (Bt8070/BtT/P9170 Interface).

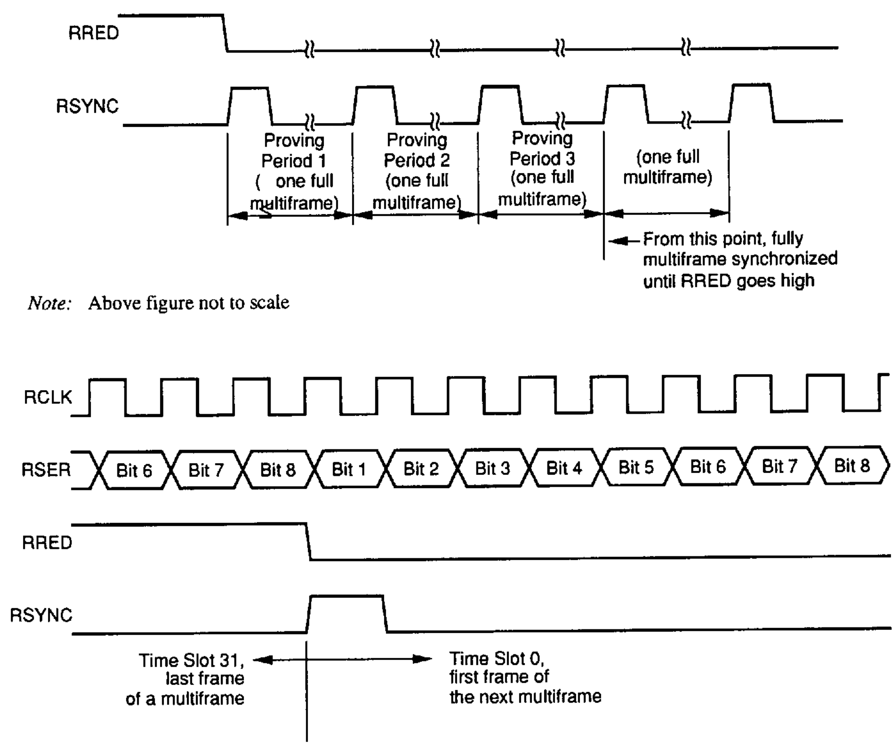


Figure 10. Receive Frame Synchronization Timing–CEPT PCM 30 Mode (Bt8070 Interface).

External Shared Memory Organization and Definition

General Structure

Transmit data, received data, channel commands, and channel pointers are organized in the external memory shared by the host and Bt8071A.

For each transmit and receive channel, the host must allocate shared memory for a channel activation byte, channel buffer pointers, and a set of channel data buffers. Figure 11 illustrates an arrangement of shared buffer memory within the host computer main memory.

The channel-activation byte and the channel buffer pointers are located in a 256-byte address space referred to as "system memory" (see Figure 12). The channel-activation byte is located at address j followed by 127 unassigned bytes. The channel buffer pointers are located at addresses j + 128 through j + 255. The channel data buffers are located at starting addresses specified by the channel pointers. The length of the data buffers is specified in data descriptors included within the data buffer.

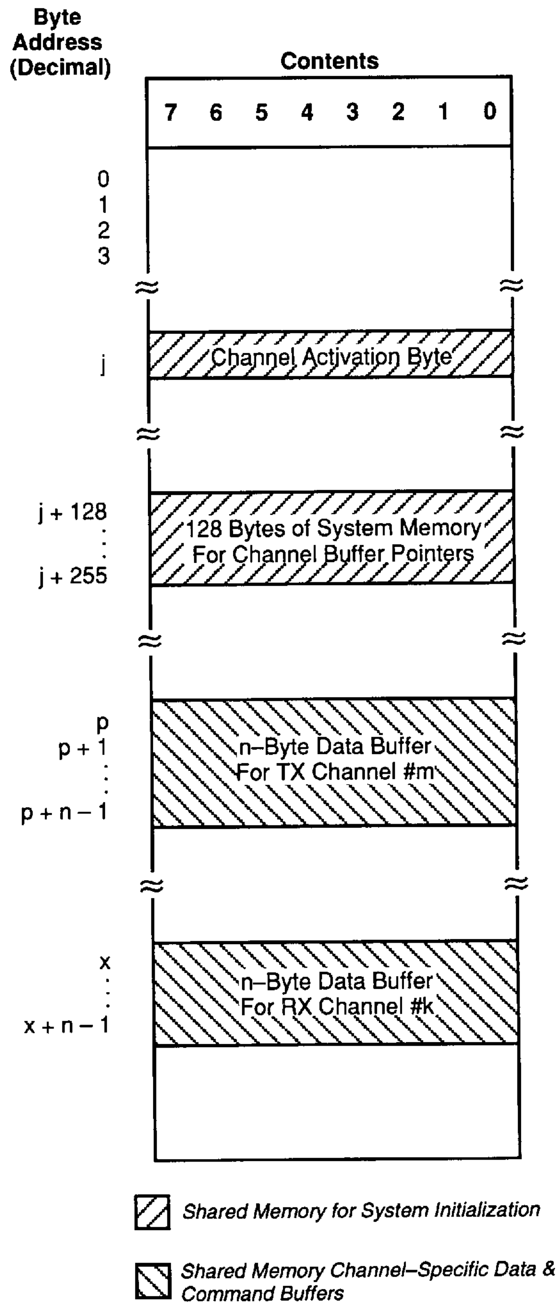


Figure 11. External Shared Memory Map — Top Level.

Channel-Activation Byte

The channel-activation byte (see Figure 11) contains a command to activate or deactivate the channel number identified within the byte. The direction of data travel is also specified. The individual bits are defined as follows:

Activate Channel (ACTIVE)

When set by the host, the indicated channel (CHANNEL number) is activated. When reset by the host, the channel is deactivated.

Receive/Transmit (RX/TX*)

When set by the host, the indicated channel is a receive channel. When reset by the host, the channel is a transmit channel.

Channel Number (CHANNEL)

Set by the host to select the number of the channel:

Bit					
4	3	2	1	0	Channel Number
0	0	0	0	0	0
		.			
		.			
1	1	1	1	1	31

External Shared Memory Organization and Definition *(continued)*

Word Address (HEX)	Byte Address (HEX)	Contents	Remarks
		7 6 5 4 3 2 1 0	
XXX00	XXX00	Active | X | RX/TX* | Channel Number	Channel Activation Byte
	XXX01 : : XXX7F	Byte Addresses XX01 Through XX7F Are Not Used by Bt8071A	
XXX40	XXX80	Transmitter Channel 0 Start Address (High-Order Byte)	Channel Buffer Pointers
	XXX81	Transmitter Channel 0 Start Address (Low-Order Byte)	
XXX41	XXX82	Transmitter Channel 1 Start Address (High-Order Byte)	
	XXX83	Transmitter Channel 1 Start Address (Low-Order Byte)	
. . .	. . .	Transmitter Channels 2 to 30 Start Addresses	
XXX5F	XXXBE	Transmitter Channel 31 Start Address (High-Order Byte)	
	XXXBF	Transmitter Channel 31 Start Address (Low-Order Byte)	
XXX60	XXXC0	Receiver Channel 0 Start Address (High-Order Byte)	
	XXXC1	Receiver Channel 0 Start Address (Low-Order Byte)	
. . .	. . .	Receiver Channels 1 to 30 Start Addresses	
XXX7F	XXXFE	Receiver Channel 31 Start Address (High-Order Byte)	
	XXXFF	Receiver Channel 31 Start Address (Low-Order Byte)	

a. MDFS = High (68000-Based)

Word Address (HEX)	Byte Address (HEX)	Contents	Remarks
		7 6 5 4 3 2 1 0	
XXX00	XXX00	Active | X | RX/TX* | Channel Number	Channel Activation Byte
	XXX01 : : XXX7F	Byte Addresses XX01 Through XX7F Are Not Used by Bt8071A	
XXX40	XXX80	Transmitter Channel 0 Start Address (Low-Order Byte)	Channel Buffer Pointers
	XXX81	Transmitter Channel 0 Start Address (High-Order Byte)	
XXX41	XXX82	Transmitter Channel 1 Start Address (Low-Order Byte)	
	XXX83	Transmitter Channel 1 Start Address (High-Order Byte)	
. . .	. . .	Transmitter Channels 2 to 30 Start Addresses	
XXX5F	XXXBE	Transmitter Channel 31 Start Address (Low-Order Byte)	
	XXXBF	Transmitter Channel 31 Start Address (High-Order Byte)	
XXX60	XXXC0	Receiver Channel 0 Start Address (Low-Order Byte)	
	XXXC1	Receiver Channel 0 Start Address (High-Order Byte)	
. . .	. . .	Receiver Channels 1 to 30 Start Addresses	
XXX7F	XXXFE	Receiver Channel 31 Start Address (Low-Order Byte)	
	XXXFF	Receiver Channel 31 Start Address (High-Order Byte)	

b. MDFS = Low (iAPX 86-Based)

Figure 12. System Memory Map Locations.

External Shared Memory Organization and Definition *(continued)*

Channel Buffer Pointers

The channel buffer pointers specify the start addresses for the channel data buffers. The pointers must be stored by the host in 128 contiguous bytes beginning at j + 128. For each channel, the buffer start address is to be specified as a 16-bit (2-byte) word. The relative location of the upper and lower bytes of the 16-bit word is determined by the MDFS input (see Figure 12). Pointers for up to 32 transmit and 32 receive channels can be specified. The upper address lines (A8–A15) are placed in the high-impedance state by the Bt8071A during the system memory accesses (i.e., while the channel activation byte or channel buffer pointers are being accessed) when the UAEN input is high.

Channel Data Buffers

A buffer is a group of contiguous memory locations for each meaningful group of ordered data. The number of memory locations in a buffer depends on memory availability and user data frame size, if any. For example, a group of contiguous memory locations may be assigned to the data that must be framed according to HDLC protocol. The data must be grouped into an 8-bit entity, also referred to as "octet" or "byte." If necessary, one octet is read from or written to the data buffer by the Bt8071A during a single memory access.

The channel data buffers (also referred to as the "data buffers") may reside anywhere in the memory within the addressing range of the channel buffer pointers. Any number of data buffers may be assigned for any channel, and their starting addresses may be changed at any time. A set of data buffers is usually assigned to each active channel for storing the data to be transmitted. Another set of data buffers is usually assigned for the received data.

Transmit Data/Command Buffer Organization

A general organization of data within a buffer and the linking of buffers are illustrated in Figure 13. The detail contents of a transmit data buffer are shown in Figure 14. The contents of a transmit command buffer are shown in Figure 15. Information within the buffer is organized into two groups: descriptors and data.

The first group of 7 bytes contains the buffer descriptors, e.g., the link (pointer) to the next transmit data buffer, buffer size, the number of data bytes in the buffer, or buffer status. This group of information is mandatory for each buffer.

The second group contains k-bytes of information, k being a variable number. This group contains user data (including any header) that must be framed according to HDLC, data to be transmitted unframed, or channel mode and fill/mask information.

Transmit Channel Descriptors

The breakdown and the ordering of the 7 bytes of descriptors appears in Figure 14. The first 6 bytes contain the next buffer address, the buffer size, and the data length, each consisting of 2 bytes. The relative locations of the upper and the lower bytes are interchangeable by the use of the input strap pin MDFS. The seventh byte contains the status of the current transmit buffer as well as the status of the transmit channel. A byte not used by the Bt8071A and free to be used by the host will precede or follow the status byte as determined by MDFS (see Figure 14).

Next Buffer Start Address

Bytes 0 and 1 contain the 16-bit start address of the next buffer. The next buffer start address can be the same as that of the current buffer. Such a buffer is referred to as a "recirculating buffer."

Buffer Size

Bytes 2 and 3 contain the 12-bit BUFFER SIZE, k. The BUFFER SIZE specifies the total number of memory bytes allocated by the host processor for storing the data to be transmitted. The 4 most significant bits are not used by the Bt8071A.

The Bt8071A reads the buffer size only if the status indicates that the data buffer contains partial data. The Bt9071A then interprets the buffer size to be the actual number of data bytes in this buffer. The Bt8071A does not read this word when the data buffer is a command buffer.

Data Length

Bytes 4 and 5 contain the 12-bit DATA LENGTH field and a 2-bit field containing host processor options for rate adaptation and timer functions. The remaining 2-bit field is not used by the Bt8071A.

Data Length—DATA LENGTH j, specifies the actual number of data bytes in a data buffer to be trans-

External Shared Memory Organization and Definition *(continued)*

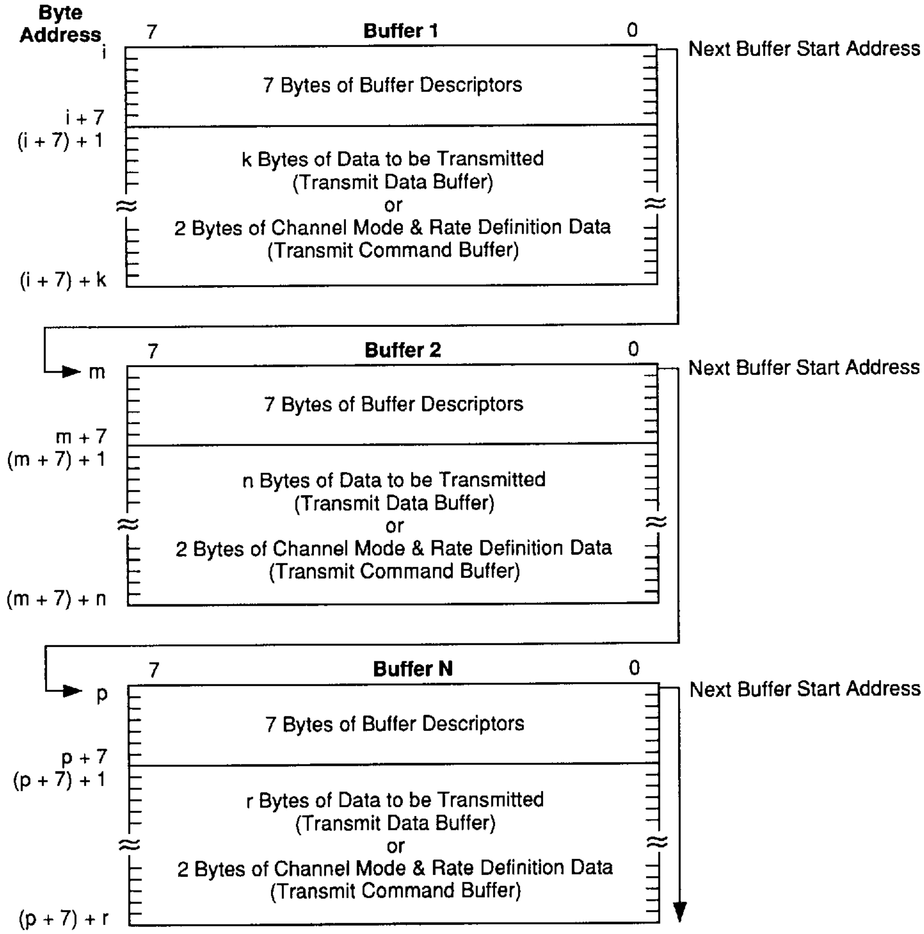


Figure 13. Organization and Linking of Transmit Buffers.

mitted. The Bt8071A reads DATA LENGTH only if the status indicates that the buffer contains the last byte of an HDLC frame or non-HDLC data (CF/P* = 1).

In a command buffer, data length is used to define the hyperchannel configurations.

Flag Offset Control (FO). This bit is meaningful only when FC is set. When FO is set by the host, the transmitter of the specific channel counts the total number of HDLC zeros intentionally inserted over the data and the CRC fields for the entire duration of transmission. At the end of each HDLC frame, the transmitter divides the accumulated number by eight and retains the remainder. The quotient is known as the "flag count offset." The quotient represents the number of bytes of nondata entities transmitted and can be viewed as the HDLC intraframe fill. The Bt8071A subtracts the flag count offset from the FLAG COUNT, which was specified without the knowledge of the inserted zeros. The resultant count equals the actual number of additional flags that are transmitted by the Bt8071A. This is useful in synchronous data rate-adaption applications.

The flag count offset can be any number from 0–3, implying that HDLC frames long enough to cause up to 24 zero insertions can be monitored by the transmitter without overflow of the internal 2-bit flag count offset. If the resultant flag count after subtracting the offset is zero or negative, no additional flags are transmitted.

When FC is a zero, the FLAG COUNT is not adjusted. For applications such as LAPD, which require an opening flag and a separate closing flag, FC should be set, FO reset, and FLAG COUNT set to one.

In a non-HDLC mode, the flag-count offset will always be zero. The state of FO does not matter.

Flag Control (FC). When set by the host, this bit specifies that the corresponding HDLC channel transmitter contains a certain number of HDLC flags after

External Shared Memory Organization and Definition *(continued)*

the CRC. A minimum of one FLAG plays the dual role of the closing FLAG of the current frame and the opening FLAG of the next frame. This flag is sent regardless of FC. When FC is a one, the actual number of additional flags to be transmitted depends on the optional FLAG COUNT byte shown in Figure 14.

This flag control feature is useful in rate adaption of sub-64 kbps data rates to the 64 kbps bearer channel rate. It is also useful as a timer. The Bt8071A automatically goes to the next buffer after it sends the specified number of flags.

In the non-HDLC data mode, the Bt8071A sends the specified number of all-ones octets after the last data byte.

For the non-HDLC signaling channel, buffers must be specified to be partial data buffers for meaningful operation. In such a case, FC will not be read.

When FC is reset, no additional flags are transmitted. The Bt8071A does not process the FC bit in a command buffer.

Transmit Buffer Status

The transmit buffer STATUS byte contains the status of the current transmit buffer as well as the status of the transmit channel (see Figure 14). The individual bits are defined as follows.

Empty (MPTY). This bit is set by the host to inform the Bt8071A that the data buffer is empty, i.e., data is not ready for transmission. The host resets this bit when the buffer contains valid data ready for transmission. When the buffer is empty, the Bt8071A continues polling this bit until it is non-empty.

This bit is set by the Bt8071A to inform the host that the Bt8071A has completed transmission of all the data in this buffer or completed processing a command buffer.

Command (CMND). This bit is set by the host to inform the Bt8071A that this buffer is a command buffer. A command buffer contains channel-specific mode definition and FILL/MASK information. This bit is reset by the host to indicate that the buffer is a data buffer that contains transmit data. Upon writing status, the Bt8071A will update the CMND bit according to the buffer type just processed.

Complete Frame/Partial Data Buffer (CF/P*). This bit is set by the host to indicate that a data buffer contains the last byte of a sequence of bytes to be formatted according to HDLC. The Bt8071A automatically appends CRC and FLAG to the data before looking for more data in the next buffer. The actual number of data bytes is specified by the 12-bit DATA LENGTH words.

In non-HDLC applications, this bit must be reset to indicate continuous data transmission; otherwise the all ones octet pattern will be transmitted after the last byte of data in a buffer.

This bit is reset by the host to indicate that this buffer contains only a part of the data to be transmitted; the rest may be in one or more succeeding buffers. Such a buffer is referred to as a "partial data buffer." In this case, the Bt8071A transmits all the data in this buffer and then automatically transmits any data in the next buffer. The actual number of data bytes is specified by the 12-bit BUFFER SIZE word.

This bit is also used in a command buffer to indicate partial or complete command buffer.

Invalid Buffer Address (IVBA). This bit is set by the Bt8071A if it encounters an invalid next buffer address, i.e., a next buffer address with a starting address of 16 zeros or hexadecimal FFFX (X = don't care). In this case, the specific transmit channel of the Bt8071A enters the inactive state and continuously transmits octets of all ones until a channel is reactivated by the host.

Underrun (UNDR). This bit is set by the Bt8071A when its transmit channel runs out of data. Such is the case when the Bt8071A encounters either an invalid buffer address, an empty data buffer, or a command buffer following a partial data buffer. In HDLC mode, the transmitter of the specific channel automatically transmits an ABORT code followed by FLAGs until the condition is cleared. In all cases of underrun, the non-HDLC transmit channel sends the all-ones octet pattern repeatedly until a valid nonempty data buffer is set up by the host. The remaining bits in the status byte will not be read by the Bt8071A; however, they will be reset upon a status update.

Transmit Data Buffer

A transmit data buffer contains actual data to be transmitted and optional FLAG COUNT byte for rate adaption (see Figure 14).

Transmit Command Buffer

A transmit command buffer contains modes, fill/mask, and optional hyperchannel configuration data following the 7 bytes of descriptors (see Figure 15).

External Shared Memory Organization and Definition *(continued)*

Byte Address	7	6	5	4	3	2	1	0
i	msb Next Buffer Address							
i + 1								lsb
i + 2	X	X	X	X	msb Buffer Size (k)			
i + 3								lsb
i + 4	FC	FO	X	X	msb Data Length (j)			
i + 5								lsb
i + 6	Not Used by Bt8071A							
i + 7	Status: UNDR	IVBA	X	X	X	CF/P*	CMND (0)	MPTY
(i + 7) + 1	First Data Byte							
(i + 7) + 2	Second Data Byte							
:	:							
(i + 7) + j	Last Data Byte							
(i + 7) + j + 1	Flag Count (Optional)							
:	:							
(i + 7) + k	Last Location in Buffer							

a. MDFS = High

Byte Address	7	6	5	4	3	2	1	0
i	Next Buffer Address							lsb
i + 1	msb							
i + 2	Buffer Size (k)							lsb
i + 3	X	X	X	X	msb			
i + 4	Data Length (j)							lsb
i + 5	FC	FO	X	X	msb			
i + 6	Status: UNDR	IVBA	X	X	X	CF/P*	CMND (0)	MPTY
i + 7	Not Used by Bt8071A							
(i + 7) + 1	First Data Byte							
(i + 7) + 2	Second Data Byte							
:	:							
(i + 7) + j	Last Data Byte							
(i + 7) + j + 1	Flag Count (Optional)							
:	:							
(i + 7) + k	Last Location in Buffer							

b. MDFS = Low

Figure 14. Transmit Data Buffer Contents.

Byte Address	7	6	5	4	3	2	1	0
i	msb Next Buffer Address (i)							
i + 1								lsb
i + 2	Not Used by Bt8071A							
i + 3								
i + 4	Not Used by Bt8071A							msb
i + 5	Data Length (j)							lsb
i + 6	Not Used by Bt8071A							
i + 7	Status: UNDR	IVBA	X	X	X	CF/P*	CMND (1)	MPTY
(i + 7) + 1	Modes: 0	0	0	0	INV	LOOP	SIG	HDLC
(i + 7) + 2	FILL/MASK							
(i + 7) + 3	E	A	X	Channel Number				
:	:							
(1 + 7) + j	E	A	X	Channel Number				

a. MDFS = High

Byte Address	7	6	5	4	3	2	1	0
i	Next Buffer Address (i)							lsb
i + 1	msb							
i + 2	Not Used by Bt8071A							
i + 3								
i + 4	Data Length (j)							lsb
i + 5	Not Used by Bt8071A							msb
i + 6	Status: UNDR	IVBA	X	X	X	CF/P*	CMND (1)	MPTY
i + 7	Not Used by Bt8071A							
(i + 7) + 1	Modes: 0	0	0	0	INV	LOOP	SIG	HDLC
(i + 7) + 2	FILL/MASK							
(i + 7) + 3	E	A	X	Channel Number				
:	:							
(1 + 7) + j	E	A	X	Channel Number				

b. MDFS = Low

Figure 15. Transmit Command Buffer Contents.

External Shared Memory Organization and Definition *(continued)*

The first byte (MODE) defines the channel modes of operation—specifically, HDLC, signaling, data inversion, and loop back. The second byte (FILL/MASK) defines the data rate. The breakdown and the ordering of bytes within the command buffer are illustrated in Figure 15.

For a command buffer, the Bt8071A will not process the bytes at address i+2 or i+3 but will read the data length. The Bt8071A will read the next buffer address at locations i and i+1 as part of processing the command buffer. The relative locations of the upper and the lower bytes (of the next buffer address and data length) are interchangeable by means of MDFS. The mode and FILL/MASK bytes locations are not interchangeable by MDFS.

Modes

The MODES byte specifies the operational modes of the given channel—specifically, HDLC or non-HDLC, signaling channel or nonsignalling channel, data to be inverted bit by bit prior to transmission or not to be inverted, and channel transmit data to be looped back through the receiver to the host shared memory or not to be looped back (see Figure 14).

SIG and HDLC—Mode Select

These two bits select the Bt8071A framing mode.

SIG	HDLC	Mode
1	0	Non-HDLC Signaling Channel Mode
0	0	Non-HDLC Data Channel Mode
0	1	HDLC Data Channel Mode
1	1	Reserved

Non-HDLC Signaling Channel Mode

The channel carries bit-oriented signaling data without an HDLC format. The Bt8071A treats this channel without special consideration to signaling. However, the Bt8071A assumes that no more than two linked data buffers are assigned to the signaling channel by the host. Additionally, the last data buffer (even if it is the only buffer) is assumed to be a recirculating buffer.

Non-HDLC Data Channel Mode

The channel is a non-HDLC data channel. In DMI applications, data modes 0 and 1 may be specified by this combination. The CF/P* bit of the status byte of the allocated data buffers must be reset for uninterrupted data transmission, otherwise the Bt8071A will transmit the all-ones octet pattern repeatedly after the last byte as many times as is dictated by FC, FLAG COUNT, and the availability of the data in the next buffer. The channel time fill and the idle codes are the same.

HDLC Data Channel Mode

The channel is an HDLC data channel or an LAPD message-oriented HDLC signaling channel. No distinction is made between an HDLC data channel and an LAPD channel. No special handling is done on the header, i.e., address and control fields of the HDLC frame. The information field is assumed to be an integer number of octets or bytes. The 16-bit CRC-CCITT generator polynomial, $X^{16} + X^{12} + X^5 + 1$, is used to calculate the FCS. The transmitted ABORT sequence has 14 consecutive ones to satisfy SDLC and HDLC requirements.

Invert Data (INV)

When set by the host, the Bt8071A inverts the data prior to transmission whenever the channel is active. When reset by the host, the Bt8071A sends the data noninverted, i.e., as it is read from the transmit buffer. With INV bit set by the host (when the channel is idle), an octet of eight zeros is sent for HDLC or non-HDLC channels. However, when INV is not set, an octet of eight ones is sent for idle code. All other data including HDLC flag and ABORT is conditioned by the INV bit.

Note that the combination of the HDLC procedure and data inversion guarantee that there will not be more than five consecutive zero bits in any primary rate channel during data transmission or seven consecutive zero bits during ABORT transmission.

Loop Mode (LOOP)

When set by the host, the associated transmit channel data is stored internally in the Bt8071A and is also transmitted. If the LOOP bit for the corresponding receive channel is also set, the previously stored transmit channel data can be looped back to the shared memory through the receive channel.

Only one channel can be placed in LOOP mode at any time for reliable loop operation. But the loop channel number, the FILL/MASK and its mode can be specified independently for any transmit-and-receive channel and need not be identical. Such a provision makes possible powerful software-based diagnostic

External Shared Memory Organization and Definition *(continued)*

routines. Hyperchannel LOOP mode is not supported by the Bt8071A.

Note that the loop-mode operation will fail without informing the host if the host programs only a transmit channel in the loop mode without programming a receive channel. However, the host shared memory will still be filled with the external serial data of the channel, if the channel is active.

FILL/MASK

The second byte of a command buffer contains the FILL/MASK pattern. It is used as a masking pattern on the HDLC-formatted (including FLAG, header, data, CRC, and ABORT code) or non-HDLC data to adapt subrates that are multiples of 8 kbps to the 64 kbps rate.

Zero-Byte Buffers

Zero-byte buffers allow the Bt8071A to fill the gap between transmit data buffers with either flags (HDLC) or ones (non-HDLC). For example, a channel is expected to empty its transmit data buffer before the host controller can get the next buffer ready. So, the data buffer's NEXT BUFFER ADDRESS points to a zero-byte buffer, which automatically sends flags or ones until it is told to continue data transmission. Two types of command buffers are provided in the Bt8071A for this purpose: the COMPLETE COMMAND and the PARTIAL COMMAND.

Complete Command Buffer

The buffer is coded with both the CMND bit and CF/P* bit of the status byte in the command buffer set. This is processed by the Bt8071A as a COMPLETE COMMAND, in which case the MODES, FILL/MASK, and optional flexible hyperchannel information will be read and processed. When this type of buffer is being processed, the Bt8071A will transmit and HDLC ABORT if it is in the HDLC mode. This is the only method implemented in the Bt8071.

Partial Commands

This buffer is coded with the CMND bit set and CF/P* bit reset. This is processed as a PARTIAL COMMAND, in which case the Bt8071A reads the NEXT BUFFER ADDRESS, sends one HDLC flag or one non-HDLC all-ones octet, and proceeds to the new buffer chain. Neither MODE nor FILL/MASK changes. This process is as if a normal buffer completion has taken place by setting the MPTY and CF/P* bits of the status register. If the NEXT BUFFER ADDRESS is null, the channel will be deactivated with the status update indicating the appropriate error condition. Each PARTIAL COMMAND sends one HDLC flag or one non-HDLC all-ones octet. Chaining PARTIAL COMMAND buffers sends multiple flags or ones. If a PARTIAL COMMAND buffer is processed after an incomplete data frame, then HDLC ABORT or non-HDLC all-ones will be sent, since the initial buffer chain was not properly terminated.

Flexible Hyperchannels

Flexible hyperchannels are created by grouping any number of channels into a hyperchannel. These channels may be noncontiguous. Any number of hyperchannels may operate with any number of channels. A channel may be assigned to only one hyperchannel. Any transmit channel may be grouped into a particular hyperchannel by configuring the hyperchannel's transmit command buffer (see Figure 15). DATA LENGTH in the command buffer determines flexible hyperchannel or normal channel assignment as follows:

Command Buffer DATA LENGTH
= 0, 1, 2: normal channel process

Command Buffer DATA LENGTH
> 2: hyperchannel process

In Flexible-Hyperchannel mode, the least significant byte of DATA LENGTH is read to determine the number of additional channels to be assigned to the hyperchannel. The data bytes containing the additional channel numbers are read from the command buffer in sequence and passed to the transmitter. Previously active channels may be appropriated into a flexible hyperchannel. When they are appropriated, buffer activity on the original channel ceases; when they are released from the hyperchannel, the original channel will return to the state from which its activity was suspended.

The channel map may be updated within the time of a single pass through the channel counter. The number of the channel that activates the flexible hyperchannel becomes the number of the hyperchannel. Each data byte in the command buffer is structured as shown in Figure 15.

External Shared Memory Organization and Definition *(continued)*

Current Buffer Status as Set Up by Host			Next Buffer Status as Set Up by Host			Min. No. of Data Bytes in Next Buffer	Remarks
CMND	MPTY	CF/P*	CMND	MPTY	CF/P*		
1	0	X	0	0	1	2	Complete frame buffer following a command buffer
1	0	X	0	0	0	5	Partial data buffer following a command buffer
X	X	X	1	0	X	2	Command buffer following any buffer
0	0	1	0	0	0	5	Partial data buffer following a complete frame buffer
0	0	1	0	0	1	2	Complete frame buffer following a complete frame buffer
0	0	0	0	0	1	3	Complete frame buffer following a partial data buffer
0	0	0	0	0	0	6	Partial data buffer following a partial data buffer

Note 1: "Data byte" refers only to the actual header data or information, or mode; not to the buffer descriptors or the optional flag count.

Table 2. Minimum Number of Data Bytes.

E	A	
0	X	Hyperchannel assignment remains unchanged.
1	0	Delete channel number in bits 0–4 from hyperchannel.
1	1	Add channel number in bits 0–4 to hyperchannel.

Whenever a hyperchannel is deactivated, it is automatically cleared to the default channel value. This takes one frame time. The Bt8071A supports independent transmit and receive hyperchannel assignments. When flexible hyperchannel is used, the HCS0 and HCS1 bits should both be reset to zero. Otherwise, the standard hyperchannel defined by these two pins supersedes flexible hyperchannel.

Transmit Considerations

Minimum Number of Data Bytes in a Buffer

There is a minimum number of data bytes required in each buffer in order for the Bt8071A to maintain the buffer and still effect a smooth transition to the next buffer. The minimum number of bytes depends on the buffer type and that of the following buffer. Table 2 gives a summary.

Maximum Number of Data Bytes in a Buffer

The number of data bytes in a complete frame buffer, as specified by the DATA LENGTH word, should not exceed 4,095 (2^{12}–1). This does not include the optional 1-byte FLAG COUNT. The number of data bytes in a partial data buffer, as specified by the BUFFER SIZE word, should not exceed 4,095 (2^{12}–1).

External Shared Memory Organization and Definition *(continued)*

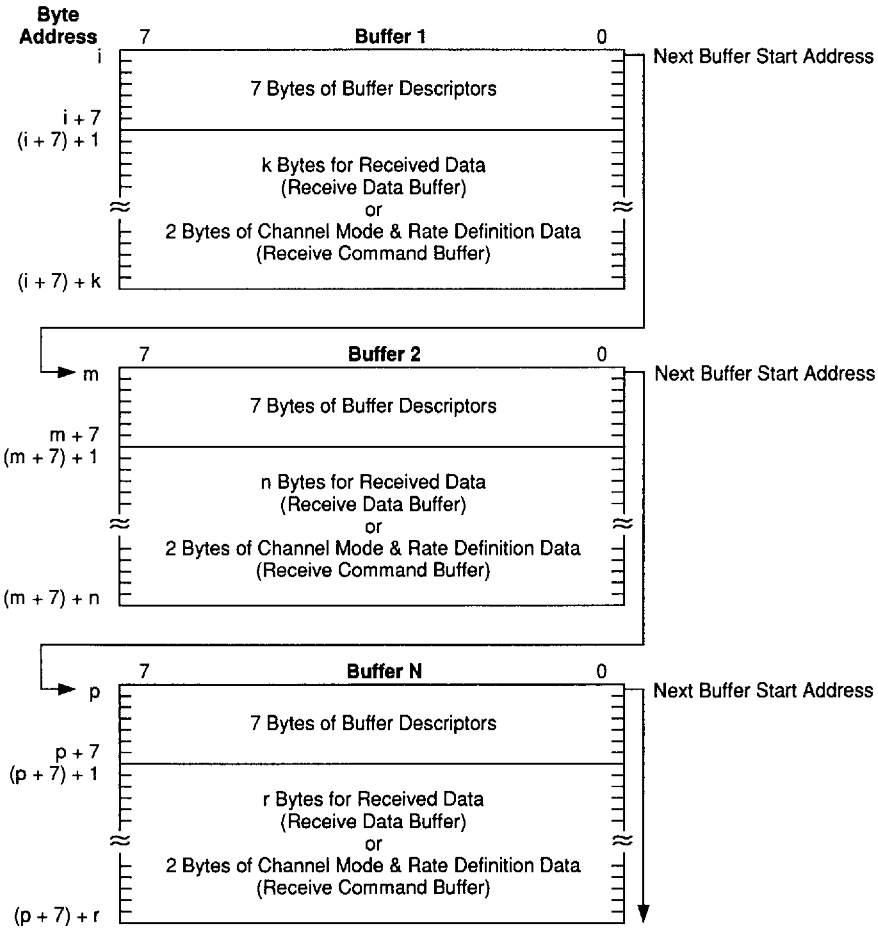


Figure 16. Organization and Linking of Receive Data Buffers.

Receive Data Buffer/ Command Organization

A general organization of data within a buffer and the linking of receive buffers is illustrated in Figure 16. The detail content of a receive data buffer is shown in Figure 17. The content of a receive command buffer is shown in Figure 18. Information within the buffer is organized into two groups: descriptors and data.

The first group of bytes contains the buffer descriptor, e.g., information such as the link to the next buffer, buffer size, the number of data bytes in the buffer, and buffer status. This group of information is mandatory for each buffer.

The second group contains k-bytes of information, k being a variable number. They may be the received data (including any header) after processing by the Bt8071A (if necessary), or channel-mode and data-rate definition information as specified by the host processor.

Receive Channel Descriptors

The breakdown and the ordering of the seven bytes of descriptors is shown in Figure 17. The first six bytes contain the next buffer address, the buffer size, and the data length, each consisting of two bytes. The relative locations of the upper and the lower bytes are interchangeable by the use of the input strap pin MDFS. The seventh byte contains the status of the current receive buffer as well as the status of the receive transmit channel. A byte not used by the Bt8071A and free to be used by the host will precede or follow the status byte as determined by MDFS (see Figure 14).

External Shared Memory Organization and Definition *(continued)*

a. MDFS = High

Byte Address	7	6	5	4	3	2	1	0
i	msb Next Buffer Address							
i + 1	Next Buffer Address							lsb
i + 2					msb Buffer Size (k)			
i + 3	Buffer Size (k)							lsb
i + 4	X	X	X	X	msb Data Length (j)			
i + 5	Data Length (j)							lsb
i + 6	Not Used by Bt8071A							
i + 7	Status: OVER	IVBA	ABRT	FCER	SHER	CF/P*	CMND (0)	MPTY
(i + 7) + 1	First Data Byte							
(i + 7) + 2	Second Data Byte							
:	:							
(i + 7) + j	Last Data Byte							
:	:							
(i + 7) + k	Last Location in Buffer							

b. MDFS = Low

Byte Address	7	6	5	4	3	2	1	0
i	Next Buffer Address							lsb
i + 1	msb Next Buffer Address							
i + 2	Buffer Size (k)							lsb
i + 3					msb Buffer Size (k)			
i + 4	Data Length (j)							lsb
i + 5	X	X	X	X	msb Data Length (j)			
i + 6	Status: OVER	IVBA	ABRT	FCER	SHER	CF/P*	CMND (0)	MPTY
i + 7	Not Used by Bt8071A							
(i + 7) + 1	First Data Byte							
(i + 7) + 2	Second Data Byte							
:	:							
(i + 7) + j	Last Data Byte							
:	:							
(i + 7) + k	Last Location in Buffer							

Figure 17. Receive Data Buffer Contents.

a. MDFS = High

Byte Address	7	6	5	4	3	2	1	0
i	msb Next Buffer Address (i)							
i + 1	Next Buffer Address (i)							lsb
i + 2	Not Used by Bt8071A							
i + 3	Not Used by Bt8071A							
i + 4	Not Used by Bt8071A							msb
i + 5	Data Length (j)							lsb
i + 6	Not Used by Bt8071A							
i + 7	Status: OVER	IVBA	X	X	X	CF/P*	CMND (1)	MPTY
(i + 7) + 1	Modes: X	X	X	X	INV	LOOP	SIG	HDLC
(i + 7) + 2	FILL/MASK							
(i + 7) + 3	E	A	X	Channel Number				
:	:							
(1 + 7) + j	E	A	X	Channel Number				

b. MDFS = Low

Byte Address	7	6	5	4	3	2	1	0
i	Next Buffer Address (i)							lsb
i + 1	msb Next Buffer Address (i)							
i + 2	Not Used by Bt8071A							
i + 3	Not Used by Bt8071A							
i + 4	Data Length (j)							lsb
i + 5	Not Used by Bt8071A							msb
i + 6	Status: UNDR	IVBA	X	X	X	CF/P*	CMND (1)	MPTY
i + 7	Not Used by Bt8071A							
(i + 7) + 1	Modes: 0	0	0	0	INV	LOOP	SIG	HDLC
(i + 7) + 2	FILL/MASK							
(i + 7) + 3	E	A	X	Channel Number				
:	:							
(1 + 7) + j	E	A	X	Channel Number				

Figure 18. Receive Command Buffer Contents.

External Shared Memory Organization and Definition *(continued)*

Next Buffer Start Address

Bytes 0 and 1 contain the 16-bit NEXT BUFFER ADDRESS written by the host. The meanings of "invalid buffer" and "recirculating buffer" are the same as those for the transmit buffer.

Buffer Size

Bytes 2 and 3 contain the 12-bit BUFFER SIZE, k, written by the host. The BUFFER SIZE specifies the total number of memory bytes allocated by the host for storing the data to be received. The 4 most significant bits are not used by the Bt8071A.

The Bt8071A reads BUFFER SIZE and stores it for all buffers, except command buffers. If the last byte of a receive HDLC frame is not received before the buffer is completely filled, the Bt8071A automatically searches for the availability of the next buffer specified.

Data Length

Bytes 4 and 5 contain the 12-bit DATA LENGTH field, j, written by the Bt8071A. DATA LENGTH specifies the actual number of received data bytes transferred to the receive data buffer by the Bt8071A. The 4 most significant bits are not used. The Bt8071A clears these bits to zeros.

DATA LENGTH is written by the Bt8071A after it receives the last byte of an HDLC frame or the HDLC ABORT code, or upon the loss of multiframe alignment error from a non-HDLC signaling channel. DATA LENGTH is not written if the end of the allocated buffer is reached before the last byte is received (i.e., if data frame length is greater than buffer size). In such a case, the data length is equal to the given buffer size. Also, data length may not be written if the ATTN input is asserted, resulting in the deactivation or reactivation of an active channel. DATA LENGTH will not exceed the programmed buffer size. DATA LENGTH > 2 in a command buffer is used to define hyperchannel configurations.

Receive Buffer Status

The receive buffer STATUS byte specifies the status of the current receive buffer as well as the status of the receive channel. The individual bits are defined as follows.

Empty (MPTY). This bit is set by the host to inform the Bt8071A that the buffer is empty, i.e., it is available for storing the received data. When the bit is reset, the buffer is not empty, i.e., it is not available to store the received data. The Bt8071A polls this bit until it is empty before it writes the received data.

This bit is reset by the Bt8071A whenever it updates the buffer status. This is the case even if the Bt8071A writes only a single byte and then is forced to update the buffer status because of abnormal conditions.

Command (CMND). This bit is set by the host to inform the Bt8071A that this buffer is a command buffer. The command buffer contains channel-specific mode definition and FILL/MASK information at the next two bytes following the STATUS byte. This bit is reset by the host to indicate that this buffer is a data buffer meant to store received data.

Complete Frame/Partial Data Buffer (CF/P*). This bit may be reset by the host at buffer initialization. This bit is set by the Bt8071A to indicate that this buffer contains the last byte of an HDLC frame. The Bt8071A automatically verifies the CRC and then starts the next HDLC frame before writing the data of the next HDLC frame in the next available buffer. In HDLC and non-HDLC modes, if the reception of data is truncated by a resync condition asserted by an ABORT, RSYNC, TMAX, or RRED, the Bt8071A sets the CF/P* bit and writes the DATA LENGTH of the truncated buffer. In signaling channel mode, when two consecutive signaling synchronization errors are encountered, the Bt8071A will also set the CF/P* bit.

This bit is reset by the Bt8071A to indicate that this buffer contains only a part of the received data and that more data is expected to be placed in one or more succeeding buffers. In HDLC mode, CF/P* implies that the last byte of the HDLC frame is not in this buffer. For non-HDLC data and signaling channels, this bit will be invariably reset after the buffer is filled. The Bt8071A does not read the CF/P* bit in a command buffer. The host can detect whether a received HDLC frame size exceeded the maximum anticipated buffer size by checking whether CF/P* is set in the starting buffer of the HDLC frame.

Abort (ABRT). This bit is written by the Bt8071A and, in conjunction with the FCER and SHER bits, reports abnormal conditions detected by the Bt8071A (see Table 3).

External Shared Memory Organization and Definition *(continued)*

ABRT	FCER	SHER	Description
0	0	0	No errors detected
0	0	1	Short or non-integer HDLC frame error
0	1	0	CRC error
0	1	1	CRC error & non-integer error
1	0	0	HDLC ABORT code received
1	0	1	Non-HDLC multiframe alignment lost
1	1	0	Elastic buffer error & RSYNC error
1	1	1	RRED Alarm

Table 3. Receive Buffer Status–Error Table.

Frame Check Error (FCER). This bit is written by the Bt8071A and, in conjunction with the ABRT and SHER bits, reports abnormal conditions detected by the Bt8071A (See Table 3).

Short HDLC Frame Error (SHER). This bit is written by the Bt8071A and, in conjunction with the ABRT and FCER bits, reports abnormal conditions detected by the Bt8071A (see Table 3).

Invalid Buffer Address (IVBA). This bit is set by the Bt8071A if it encounters an invalid next buffer address. In this case, the specific receive channel enters the idle state and will not receive more data until re-activated by the host.

Overrun (OVER). This bit is set by the Bt8071A after its receive channel has no next data buffer available for received data. A command buffer is not available for data. The OVER bit is written as part of the status of the just completed buffer. Also, no overrun will be reported for non-HDLC signaling channel data buffers. New data will be written in place of earlier received signaling data.

Receive Command Buffer

A receive command buffer is identical to the transmit command buffer in that both contain modes, fill/mask, and optional hyperchannel configuration data following the STATUS byte for defining the channel modes, data rate, and hyperchannel configuration.

The first byte (MODE) defines the channel modes of operation, specifically, HDLC, signaling, data inversion, and loop back. The second byte (FILL/MASK) defines the data rate. A data buffer contains the actual data received after it is processed by the Bt8071A.

The breakdown and the ordering of bytes within the command buffer are illustrated in Figure 18.

For a command buffer, the Bt8071A does not process the bytes at addresses i + 2 and i + 3 but will read the data length. The Bt8071A reads the next buffer address at locations i and i + 1 as part of processing the command buffer. The relative locations of the upper and the lower bytes of the next buffer address and data length are interchangeable by means of the MDFS input. The mode and FILL/MASK bytes locations are not interchangeable by MDFS.

Modes

The MODES byte is the first byte following the status byte, and specifies the operational modes of the given channel, specifically, HDLC or non-HDLC, signaling channel or not, data to be inverted bit by bit prior to receiver processing or not, and channel receive data source to be the loop register or not.

SIG	HDLC	Mode
1	0	Non-HDLC Signaling Channel Mode
0	0	Non-HDLC Data Channel Mode
0	1	HDLC Data Channel Mode
1	1	Reserved

Non-HDLC Signaling Channel Mode. The Bt8071A processes the received bit-oriented signaling data without the HDLC format (G.732 or DMI). The Bt8071A arranges the received signaling data as in Figure 19 for easy association of the channel number and its signaling bits. In addition, errors in multiframe alignment sequence will be detected, and any resulting loss of multiframe alignment will be reported in the STATUS byte.

External Shared Memory Organization and Definition *(continued)*

Non-HDLC Data Channel Mode. The channel is a non-HDLC data channel that can support DMI data modes 0 or 1.

When a channel receiver is activated with mode, the Bt8071A checks the availability of the allocated buffer and starts placing the received data in the buffer. After filling a buffer, the Bt8071A updates the status of the just-completed buffer, simultaneously asserting INTR*. It then moves to the next allocated buffer. Since non-HDLC data has no frame boundary, this process will continue until the host interrupts by an ATTN or the system runs out of allocated buffers.

HDLC Data Channel Mode. The channel is to receive HDLC-formatted data. It can imply an HDLC-formatted data channel, such as those in DMI mode 2 or 3 or X.25 LAPB, or a message-oriented signaling chan-

Byte Address	Contents							
	7	6	5	4	3	2	1	0
i i+1	Next Buffer Address = i or j							
i+2 i+7	Rest of the Descriptors							
(i+7)+1	X	1	X	X	X	B1	A1	A13
(i+7)+2	X	1	X	X	X	B2	A2	A14
(i+7)+3	X	1	X	X	X	B3	A3	A15
⋮	⋮							
(i+7)+11	X	1	X	X	X	B11	A11	A23
(i+7)+12	X	1	X	X	X	B12	A12	A1
(i+7)+13	X	1	X	X	X	B13	A13	A1
(i+7)+14	X	1	X	X	X	B14	A14	A2
(i+7)+15	X	1	X	X	X	B15	A15	A3
(i+7)+16	X	1	X	X	X	B16	A16	A4
(i+7)+17	X	1	X	X	X	B17	A17	A5
⋮	⋮							
(i+7)+23	X	1	X	X	X	B23	A23	A11
(i+7)+24	1	0	Ys	0	1	1	1	A12

a. T1 Mode

Figure 19. Receive Buffer Data Arrangement for Non-HDLC Bit-Oriented Signaling Channel.

External Shared Memory Organization and Definition *(continued)*

Byte Address	Contents							
	7	6	5	4	3	2	1	0
i i+1	Next Buffer Address = i or j							
i+2 i+7	Rest of the Descriptors							
(i+7)+1	D17	C17	B17	A17	D1	C1	B1	A1
(i+7)+2	D18	C18	B18	A18	D2	C2	B2	A2
(i+7)+3	D19	C19	B19	A19	D3	C3	B3	A3
. . .	. . .							
(i+7)+11	D27	C27	B27	A27	D11	C11	B11	A11
(i+7)+12	D28	C28	B28	A28	D12	C12	B12	A12
(i+7)+13	D29	C29	B29	A29	D13	C13	B13	A13
(i+7)+14	C30	C30	B30	A30	D14	C14	B14	A14
(i+7)+15	D31	C31	B31	A31	D15	C15	B15	A15
(i+7)+16	1	1	Ys	1	0	0	0	0

b. CEPT PCM 30 Mode

Figure 19** (continued)**. Receive Buffer Data Arrangement for Non-HDLC Bit-Oriented Signaling Channel.

nel as in LAPB. The Bt8071A treats each the same and de-formats the data. No special handling is performed on the header, (i.e., the address and control fields of the HDLC frame). The information field is assumed to be an integer number of octets or bytes. The 16 bit CRC-CCITT generator polynomial, $X^{16} + X^{12} + X^{5} + 1$, is used to recompute the FCS. Abort and flag characters are recognized, as are intentionally inserted zeros.

Invert Data (INV). When set by the host, the Bt8071A inverts the received data prior to processing. When INV is reset by the host, the Bt8071A does not invert the received data. The INV bit is applied to every received bit.

Loop Mode (LOOP). When set by the host, the Bt8071A selects as its input the serial output data from the internal loop data buffer, as opposed to the externally supplied serial data. If an identically numbered transmit channel was also programmed to be in the loop mode earlier, data from that channel is looped back to the shared memory through the receive channel. The loop channel number, FILL/MASK, and its mode can be specified independently for any transmit-and-receive channel and need not be identical. If no transmit channel has loop activated, the Bt8071A processes the channel as if a receiver RRED condition were active for that channel duration. Hyperchannel loop mode is not supported by the Bt8071A.

External Shared Memory Organization and Definition *(continued)*

Option Number	Data Rate	Bit								Remarks
		7 (MSB)	6	5	4	3	2	1	0 (LSB)	
0 (Note 1)	0 Kbps	0	0	0	0	0	0	0	0	No data will be sent. A time FILL of eight 1s will be sent provided TSEREN=1
1	8 Kbps	0	0	0	0	0	0	0	1	
		0	0	1	0	0	0	0	0	Arbitrary-user defined; a 1 in any one bit position, but only one 1.
2	16 Kbps	0	0	0	0	0	0	1	1	
		0	0	0	0	1	1	0	0	User defined patterns; a 1 in any two bit positions, but only two 1s.
		0	0	1	1	0	0	0	0	
		1	1	0	0	0	0	0	0	
3	24 Kbps	0	0	0	0	0	1	1	1	A total of three 1s anywhere as defined by user.
		0	1	0	1	0	1	0	0	
4	32 Kbps	0	0	0	0	1	1	1	1	A total of four 1s anywhere as defined by user.
		1	1	1	1	0	0	0	0	
		1	0	1	0	1	0	1	0	
5	40 Kbps	0	0	0	1	1	1	1	1	A total of five 1s anywhere as defined by user.
6	48 Kbps	0	0	1	1	1	1	1	1	A total of six 1s anywhere as defined by user.
7	56 Kbps	0	1	1	1	1	1	1	1	Standard rate in digital data service, restricted version of 64 Kbps
		1	1	1	1	1	1	1	0	A total of seven 1s anywhere as defined by user.
8	64 Kbps	1	1	1	1	1	1	1	1	

Note 1: A special purpose mode in which the transmitter operates as if it is at 64 Kbps including when it is fetching data from shared memory, even though no data is transmitted.

Table 4. Examples of FILL/MASK Options.

FILL/MASK

The second byte of a command buffer contains the FILL/MASK pattern. It is used as a masking pattern on the HDLC-formatted (including flag, header, data, CRC, and ABORT code) or non-HDLC data to adapt subrates that are multiples of 8 kbps to the 64 kbps rate.

Table 4 shows the data rates of the form n x 8 kbps (n = 1, 2,... 8) and several examples of codes for the FILL/MASK to adapt the subrates to the 64 kbps rate. The actual data bit is transmitted on TSER output while the FILL/MASK is a 1 at the corresponding bit position. If the FILL/MASK = 0, a FILL bit of 1 is transmitted in place of the data bit on TSER while TSEREN = 1. The data bit that is held in favor of the FILL bit is buffered internally until all the FILL bits have been transmitted corresponding to the FILL\MASK bits equaling zero.

External Shared Memory Organization and Definition *(continued)*

When the FILL/MASK bit becomes a 1 again, the buffered data bit is transmitted on a first-in-first-out basis [see Figure 7 in the Serial Interface to Bt8070/BtT/P9170 (SIS=HIGH) section].

Thus, there is a one-to-one correspondence between the FILL/MASK bit and the T1/CEPT PCM-30 channel serial data associated with the FILL/MASK bit position.

When the FILL/MASK bit is 0, TSEREN determines what is to be transmitted on TSER as follows:

Data Bit	FILL/MASK Bit	TSEREN	TSER (Output)
1	1	X	1
0	1	X	0
X	0	1	1
X	0	0	High Z

The data bit may be the same as or logical complement (inverted version) of the actual data.

A bit-oriented 64 kbps signaling channel should be programmed with 1111 1111 as the FILL/MASK. The Bt8071A will not override any other user-supplied FILL/MASK pattern even if it is erroneous, i.e., not equal to 1111 1111. An IDLE bit-oriented signaling channel will carry 1111 1111 while the channel is IDLE. Any remote receiver will not be able to achieve signaling channel multiframe alignment if 1111 1111 is received continuously.

Flexible Hyperchannels

Flexible hyperchannels are created by grouping any number of channels into a hyperchannel. These channels may be noncontiguous. Any number of hyperchannels may operate with any number of channels. A channel may be assigned to only one hyperchannel. Any receive channel may be grouped into a particular hyperchannel by configuring the hyperchannel's receive command buffer. (see Figure 18) DATA LENGTH in the command buffer determines flexible hyperchannel or normal channel assignment, i.e.

Command Buffer DATA LENGTH
= 0, 1, 2:normal channel process

Command Buffer DATA LENGTH
> 2:hyperchannel process

In flexible hyperchannel mode, the least significant byte of DATA LENGTH is read to determine the number of additional channels to be assigned to the hyperchannel. The data bytes containing the additional channel numbers are read from the command buffer in sequence and passed to the appropriate receiver. Previously active channels may be appropriated into a flexible hyperchannel. When they are appropriated, buffer activity on the original channel ceases; when released from the hyperchannel, the original channel will return to the state from which its activity was suspended. The channel map may be updated within the time of a single pass through the channel counter. The number of the channel that activates the flexible hyperchannel becomes the number of the hyperchannel. Each data byte in the command buffer is structured as shown in Figure 18.

E	A	
0	X	Hyperchannel assignment remains unchanged.
1	0	Delete channel number in bits 0–4 from hyperchannel.
1	1	Add channel number in bits 0–4 to hyperchannel.

Whenever a hyperchannel is deactivated, it is automatically cleared to the default channel value. This takes one frame time minimum. The Bt8071A supports independent transmit and receive hyperchannel assignments. When flexible hyperchannel is used, the HCS0 and HCS1 bits should both be reset to zero. Otherwise, the standard hyperchannel defined by these two pins supersedes flexible hyperchannel.

Receive Considerations

Minimum Buffer Size.

A minimum number of memory locations must be allocated in each buffer for the Bt8071A to perform the buffer maintenance and still effect a smooth transition to the next buffer without losing data. The minimum buffer allocations for data must allow six data bytes in addition to the seven bytes of descriptors. Command buffers have exactly two bytes and are processed without regard for the BUFFER SIZE word.

Note: The minimum HDLC frame received can have as few as two bytes of data, and the Bt8071A will still function properly; however, it is essential that a buffer size of six is allocated as a minimum since the received frame size is not known apriori.

Shared Memory Access

Shared Memory Access

The Bt8071A accesses shared memory for buffer maintenance, command data, information, and channel activation. It manages the buffer memory for up to 64 channels (32 transmit and 32 receive).

The T1/CEPT PCM-30 data throughput requires that one octet of data be supplied to the transmitter and one octet of data be taken from the receiver in a single channel period (eight TCLK periods). The host and the Bt8071A must work cooperatively to meet the data-throughput requirements. The Bt8071A uses a memory access scheme to simplify the system design for achieving the required data throughput.

The Bt8071A processes the memory requirements of up to 32 channels in the same order in which they are multiplexed in a T1/CEPT PCM-30 carrier system. Typically, during TX channel m, for example, the Bt8071A fetches a single data byte from memory for the transmitter so that it can transmit the data byte over channel m at the next appropriate T1/CEPT PCM-30 frame. Similarly, the last data byte received by channel j is written to the memory by the Bt8071A during the next appropriate receive channel j. Then the Bt8071A services TX channel (m+1) and RX channel (j+1), and so on.

The Bt8071A divides a channel period into two halves, each for a duration of four TCLK periods. During the first half-channel period, the Bt8071A accesses the shared memory for channel command information, buffer descriptors, and/or transmit-buffer data (including mode definition data) for a transmit channel. During the second half-channel period, the Bt8071A accesses the shared memory for channel command information, buffer descriptors (including mode definition data), and/or received data for a receive channel. Since the transmit and the receive channel boundaries are generally unrelated, an elastic buffer is used to synchronize the receive channel boundary to that of the transmit channel. Hence, no contention exists between a transmit channel and receive channel for the shared memory.

In each half-channel period, normally, the Bt8071A accesses shared memory once for data. If descriptor information is also to be updated, it accesses shared memory a second time. If system memory access is also required (as determined by assertion of the ATTN input), the Bt8071A accesses shared memory a third time. In summary, different states of buffer processing will cause from zero to three accesses to shared memory for an active channel during a half-channel period.

At the start of every half-channel period, the Bt8071A outputs the binary code for the 5-bit channel number (CH0–CH4) being served. It also specifies whether it is the receive or transmit channel via the RX/TX* output. About one-half TCLK period later, the Bt8071A asserts the memory Demand (DMND) output. DMND rising edge informs any external shared memory arbitration logic that the Bt8071A needs unconditional access to the shared memory within one TCLK period from DMND rising edge. Note that the Bt8071A will not wait for a memory acknowledge to start memory access. Thus, there is an implied memory acknowledge after one TCLK. (See Figure 20 for timing.) Prior to asserting READ* or WRITE* strobes, the Bt8071A asserts Memory Address Strobe (AS*).

At AS* falling edge, the memory address on the A0–A15 lines is valid. Simultaneously, when the memory address changes, the output SYSACC is asserted if the system memory is being addressed. Moreover, the Bt8071A will selectively tri-state the high-order memory address lines (A8–A15) during the system memory accesses when specified by UAEN.

Following AS*, the Bt8071A asserts the READ* or WRITE* output strobe for read or write operation, respectively. The data on the data bus (D0–D7) is latched by the Bt8071A prior to the rising edge of READ* during a read operation. Data placed on the data bus is written to the memory during the period that WRITE* is low.

Address setup time, address hold time, data setup time, and data hold time are specified such that a wide variety of off-the-shelf RAM devices may be used. The READ* output from the Bt8071A may be used as an Output Enable (OE*) input to the RAM devices. Since the Bt8071A uses its SYSCLK input to generate the various strobes for memory access, the access time requirements are automatically scaled depending on the T1/CEPT PCM-30 application.

Once the Bt8071A makes the first memory access, it assumes that continued access to the memory is guaranteed while DMND is active. It no longer waits for one TCLK period before the memory access. At the most, there may be up to two more memory accesses. Such a case is illustrated in Figure 20. After completing the needed memory accesses, the Bt8071A negates the DMND output, indicating that it no longer needs access to memory. It also negates the SYSACC output while it does not access system memory locations.

Shared Memory Access *(continued)*

The minimum one TCLK latency (two TCLK periods with ATTN inactivity) between DMND and the actual memory access is considered to be sufficient for an external arbitration logic to release the memory bus to the Bt8071A. Failure to do so may cause loss of data and unpredictable operation. The time between DMND going low and the start of the first memory access by the Bt8071A is considered to be sufficiently long for either a single complete memory bus cycle by the host or the completion of a pending host memory bus cycle. Since the Bt8071A does not wait for a memory acknowledgment, DMA-like operation within a single external shared address and a data bus cannot be guaranteed.

Examples of the Bt8071A to shared memory interface waveforms are shown in Figure 20.

Memory Address Extension

The 16-bit memory address output by the Bt8071A may be extended to more than 16 bits by the use of the channel number (CH0–CH4) and RX/TX* bits. These six bits may be used directly as higher order address bits for a 22-bit address, or they can be mapped by an external lookup table to another set of n bits (where n is specified by the host). Since the channel number and RX/TX* are output by the Bt8071A well in advance of the 16-bit address, address translation time is not a concern.

Address selection for the system locations can be achieved by the host by using the SYSACC output and the UAEN input. External hardware can jam any address on the upper 8 bits of the Bt8071A memory address, i.e., A8–A15, since the Bt8071A three-states them (if UAEN is active during SYSACC).

Memory Address Restrictions

System Memory Address

The Bt8071A checks the start address of the first buffer of any channel for an invalid address. It does this check immediately after it reads the 2-byte start address from the system memory, as part of servicing the ATTN interrupt from the host. If an invalid start address is detected for any channel, that channel is forced inactive automatically.

Data Buffer Memory Address

The Bt8071A checks the next buffer address for an invalid address for all the channels. If it is an invalid address, it forces the corresponding channel to an inactive state and sets the IVBA status bit. Recovery from an idle state to an active state is possible only if the host system asserts the ATTN input to the Bt8071A. In host systems that use more than 16 bits for shared memory address, an invalid address, as interpreted by the Bt8071A, refers to all addresses divisible exactly by 65,536 or an address of the form:

$$n \times 2^{16} \times (1111\ 1111\ 1111\ XXXX)$$

where n is a power of 2. Within each 64 kbyte address block, only addresses 0001–FFEF (hex) are valid.

The Bt8071A BMM internal adder calculates the absolute memory address from the given buffer start address and any offset needed to locate either the bookkeeping information or the data byte. The maximum address within a buffer for a given channel is the address of the last byte of the buffer. Since the address is always represented by the 16-bit binary number, it is restricted to 65,535 (decimal). In other words, it is reduced to modulo 65,536. Hence, the following bound, 16-bit address of the last byte: = 16-bit buffer start address; + 610 (for bookkeeping); − 12-bit data length or buffer size; ≤ 65,535 (decimal) or FFFF (hexadecimal), should be strictly adhered to when programming the buffer start address and the data length/buffer size; otherwise, the Bt8071A will access memory locations not intended for that channel.

It is to be emphasized that the Bt8071A *does check* for buffer start addresses in the range FFF0 through FFFF and declares them to be invalid addresses. For systems that use more than 65,535 byte addresses, all shared memory addresses must be within one 64 kbyte page or bank.

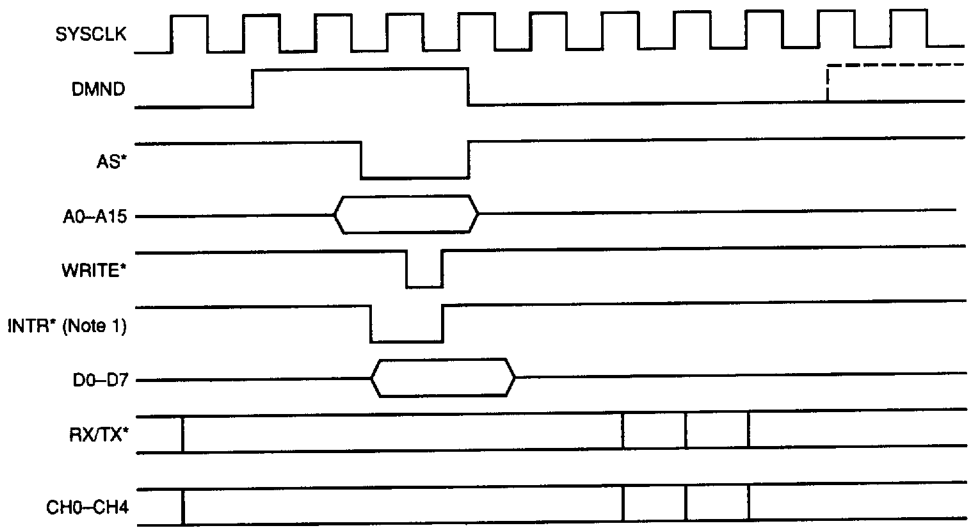
Interrupt Indication

The Bt8071A asserts the INTR* (Interrupt Indication) output anytime the status of any buffer is updated (written) by the Bt8071A. (See Figure 20 for timing illustration.) The active period of INTR* is one-half TCLK period. At the rising edge of INTR*, the channel number (including RX/TX*) and its current buffer status placed on the data bus are guaranteed to be valid so that they can be captured in an external FIFO queue. The Bt8071A does not queue the interrupts and their causes internally, nor does it wait for an interrupt acknowledge from the host before removing the interruption channel number and its buffer status. The Bt8071A processes a

Shared Memory Access *(continued)*

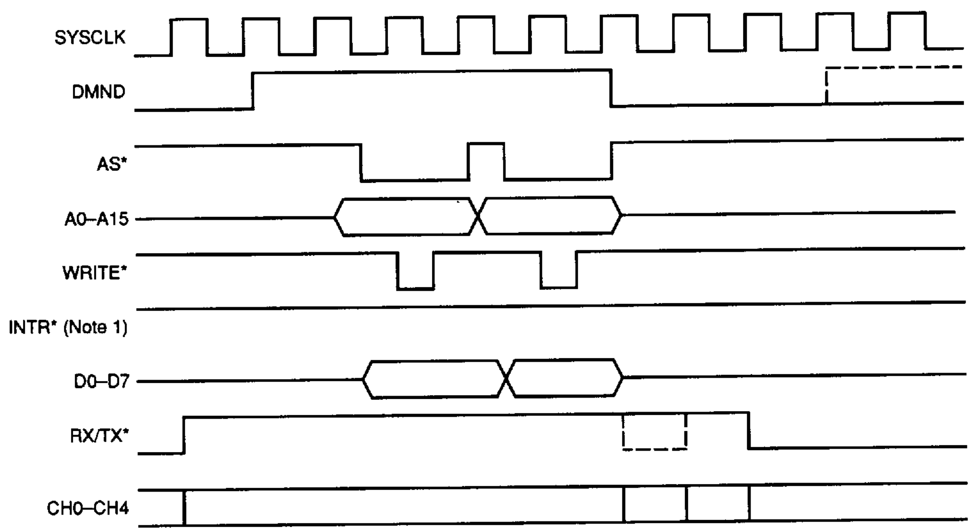
channel only for a half-channel period and then moves to the next channel.

In addition to capturing the channel number and buffer status, external hardware can also capture the actual memory address of the status byte in another FIFO queue. By reading such a queue, the host system can reallocate the completed buffers in any way it sees fit, and also cross-check against its own list of linked buffer addresses. If all the buffer start addresses are divisible exactly by eight, they can be derived from the STATUS byte addresses in the FIFO queue by setting the three LSB addresses to zero.



Note 1: Activated by status write only

a. Single Write Memory Access

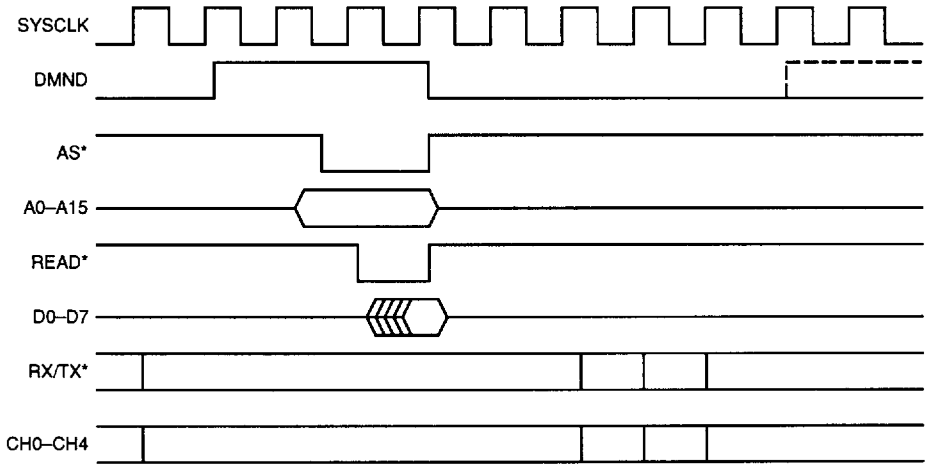


Note 1: Activated by status write only

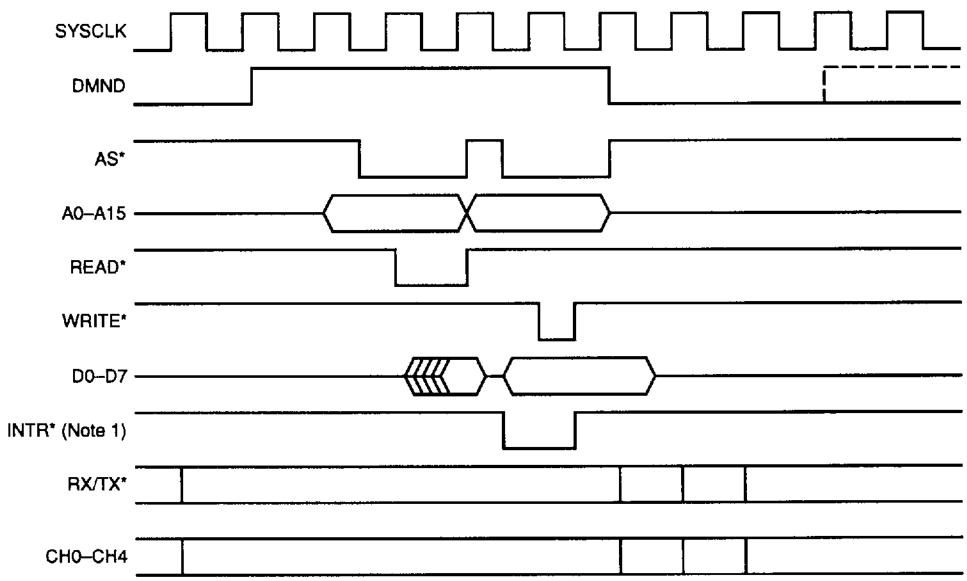
b. Double Write Memory Access

Figure 20 a & b. Bt8071A Shared Memory Example Interface Waveforms.

Shared Memory Access *(continued)*



c. Single Read Memory Access

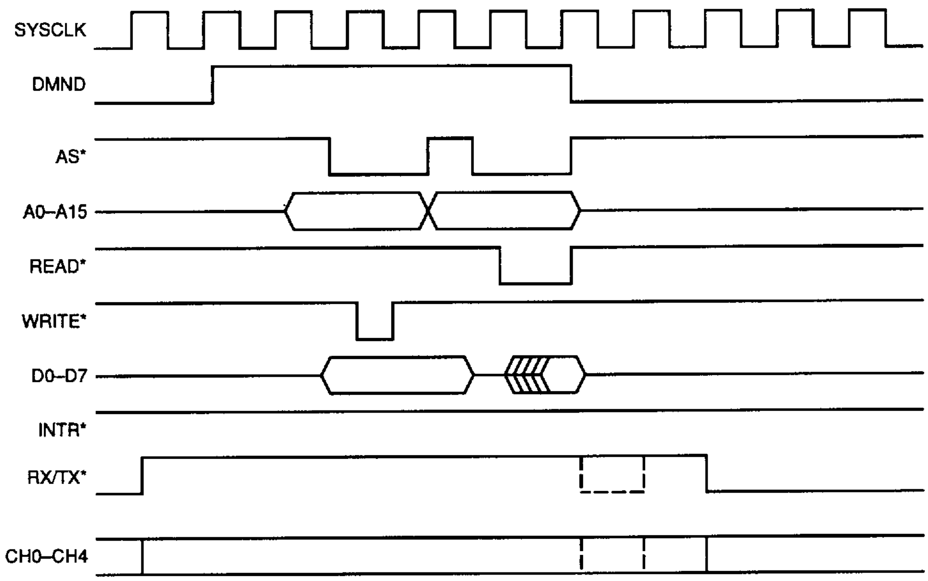


Note 1: Activated by status write only

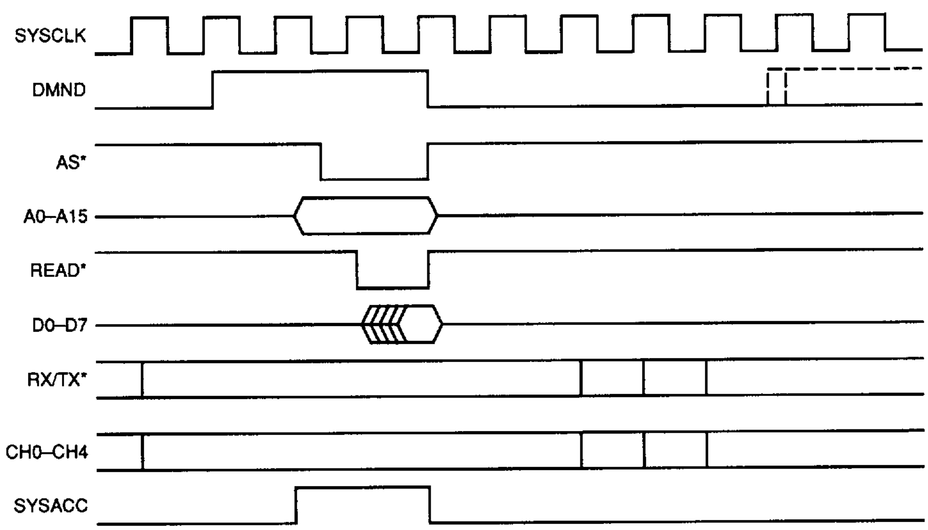
d. Read Write Double Memory Access

Figure 20** (continued) **c & d. Bt8071A Shared Memory Example Interface Waveforms.

Shared Memory Access *(continued)*



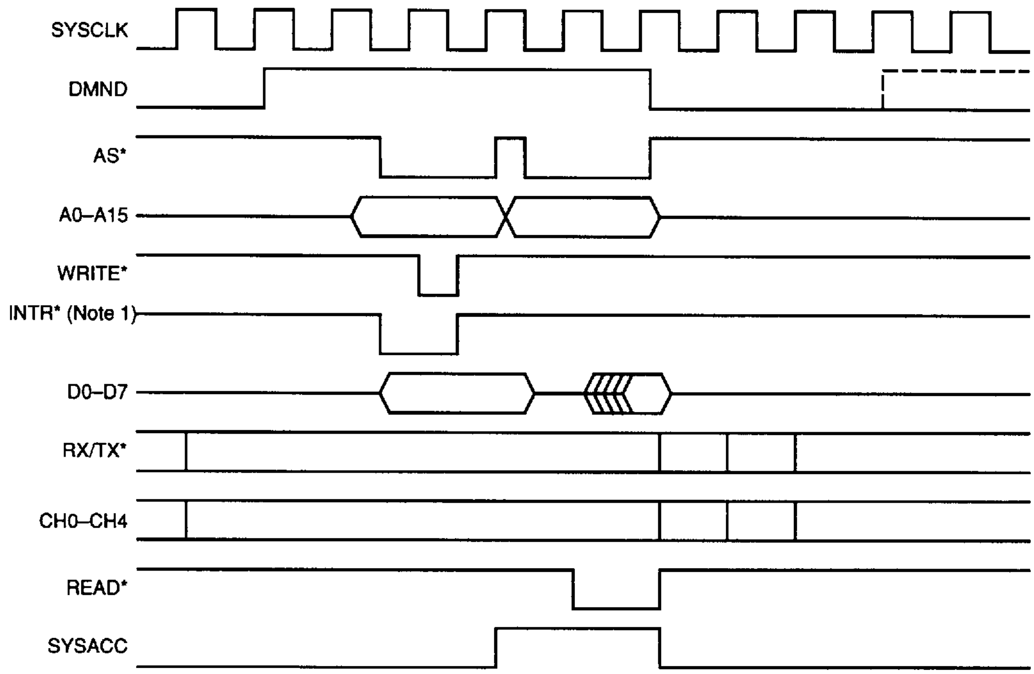
e. Write Read Double Memory Access



f. Single System Read Memory Access

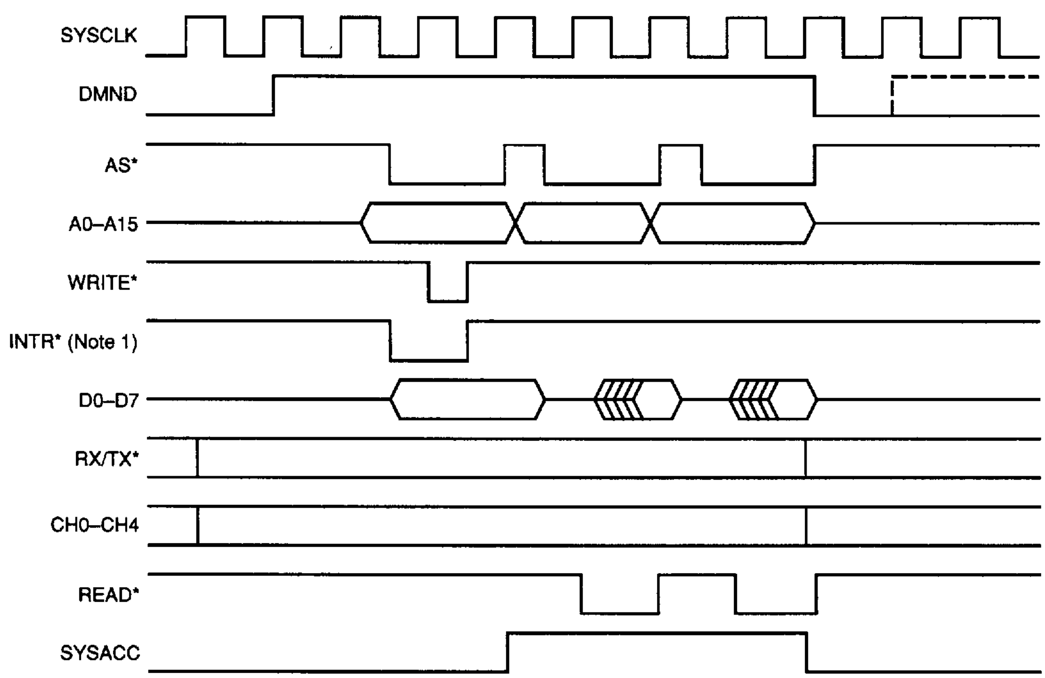
Figure 20** (continued) **e & f. Bt8071A Shared Memory Example Interface Waveforms.

Shared Memory Access *(continued)*



Note 1: Activated by status write only

g. Single Write Memory Access Plus a Single System Read Access

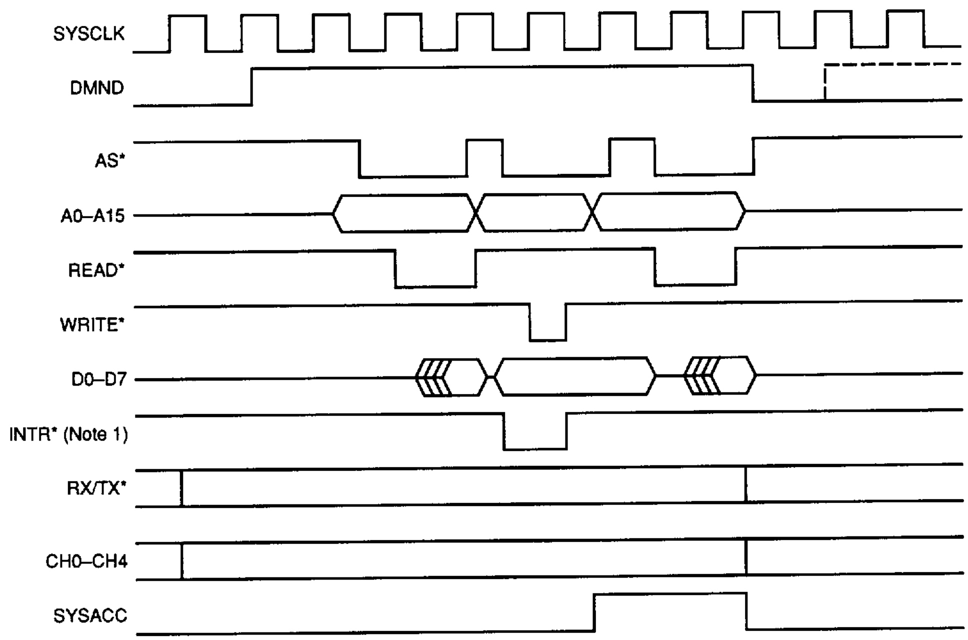


Note 1: Activated by status write only

h. Single Write Memory Access Plus a Double System Read Access

Figure 20** (continued) **g & h. Bt8071A Shared Memory Example Interface Waveforms.

Shared Memory Access *(continued)*



Note 1: Activated by status write only

i. Write /Read Double Memory Access Plus a Single System Read Access

Figure 20** (continued) **i. Bt8071A Shared Memory Example Interface Waveforms.

Device Initialization

Upon reset, all the transmit channels are forced to the inactive state. All the transmit channels are initialized to the HDLC INV, NON-SIG data mode with a FILL/MASK byte of eight zeros. No data is transferred from memory. All the receive channels are forced to the idle state. They are initialized to the HDLC data mode with a FILL/MASK byte of eight zeros. No data is written to the shared memory. The input strap pins define the TDM format, i.e., T1/CEPT PCM-30, and the hyperchannel grouping. The modes bits are assumed to be (INV = 1, LOOP = 0, SIG = 0) in addition to HDLC = 1 for each channel. Flexible hyperchannels are disabled.

The TMAX (Transmit Multiframe Sync) pulse is assumed to be valid to generate an internal channel number. The RSYNC (Receive Multiframe Sync) pulse and the RRED input are monitored by the Bt8071A to ascertain the receiver framing synchronization.

Shared Memory Access *(continued)*

Channel Initialization

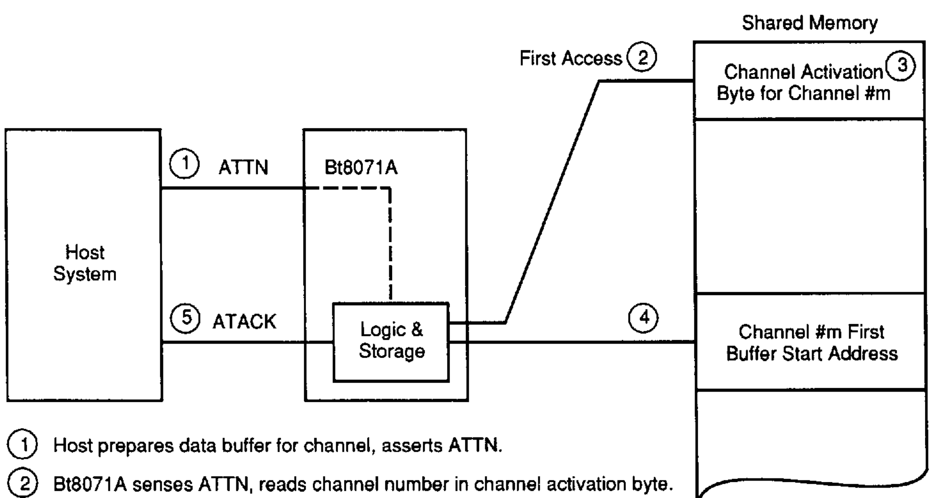
The host may activate any transmit or receive channel to any mode by pointing the channel to a command buffer. It does so in a simple and systematic manner as illustrated in Figure 21.

It chooses a starting address for a command buffer and writes the 2-byte starting address as the data at the system memory location dedicated to the channel to be initialized. It then prepares a command buffer at the above starting address by specifying the descriptor information and the mode of operation. A linked list of data buffers is set up by the host following the command buffer. If flexible hyperchannels are to be used, then the primary channel buffers will require additional memory to be allocated because of the high data rate. This completes the preparation for activating a channel.

As the last step, the host writes to the channel activation byte containing the channel number, the channel direction, and the activation command. The host then asserts the ATTN input to the Bt8071A.

When ATTN is asserted, the Bt8071A reads the channel activation byte. Based on the channel number, the Bt8071A then reads the starting address of the first buffer from the channel buffers pointers, one byte at a time. The Bt8071A stores the starting buffer address internally and acknowledges the task completion by asserting ATACK. The host system must respond to ATACK by negating ATTN.

The negation of ATTN causes ATACK output to be negated. Thus, the channel initialization process is complete. This process can be repeated for each channel that must be initialized. During each system memory access the Bt8071A asserts the SYSACC output. The Bt8071A must make three system memory accesses to complete the channel ATTN processing. The worst case time delay from ATTN assertion to ATACK assertion is three T1/CEPT PCM-30 channel periods. The earliest is 1.5 channel periods. Since this is guaranteed, the host need not poll the ATACK output blindly nor service the ATACK as an interrupt. Sample channel initialization sequences are shown in Figure 22 and Figure 23.



① Host prepares data buffer for channel, asserts ATTN.
② Bt8071A senses ATTN, reads channel number in channel activation byte.
③ Bt8071A addresses the memory location dedicated for the specific channel.
④ Bt8071A reads and stores the start address of the first buffer allocated for the channel.
⑤ Bt8071A acknowledges task completion by asserting ATACK.

Figure 21. Channel Initialization.

Shared Memory Access *(continued)*

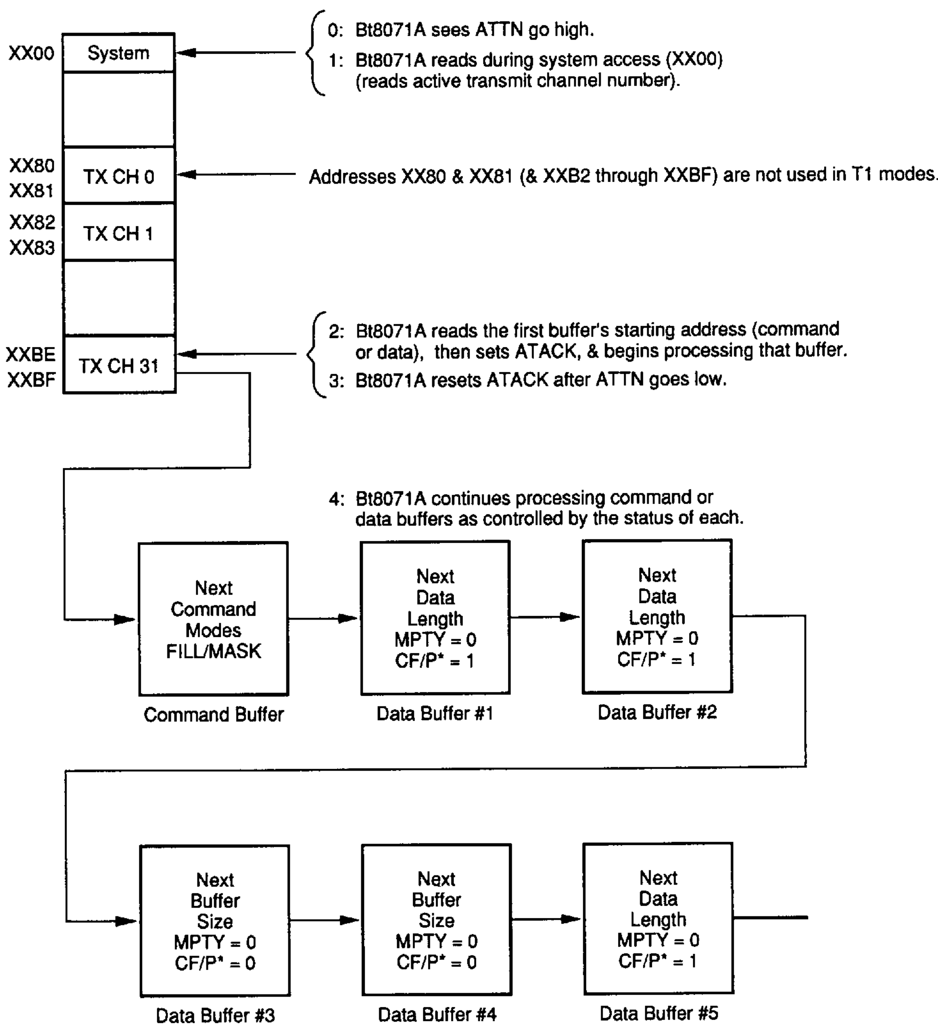


Figure 22. A Typical Linked Buffer Transmit Sequence.

Shared Memory Access *(continued)*

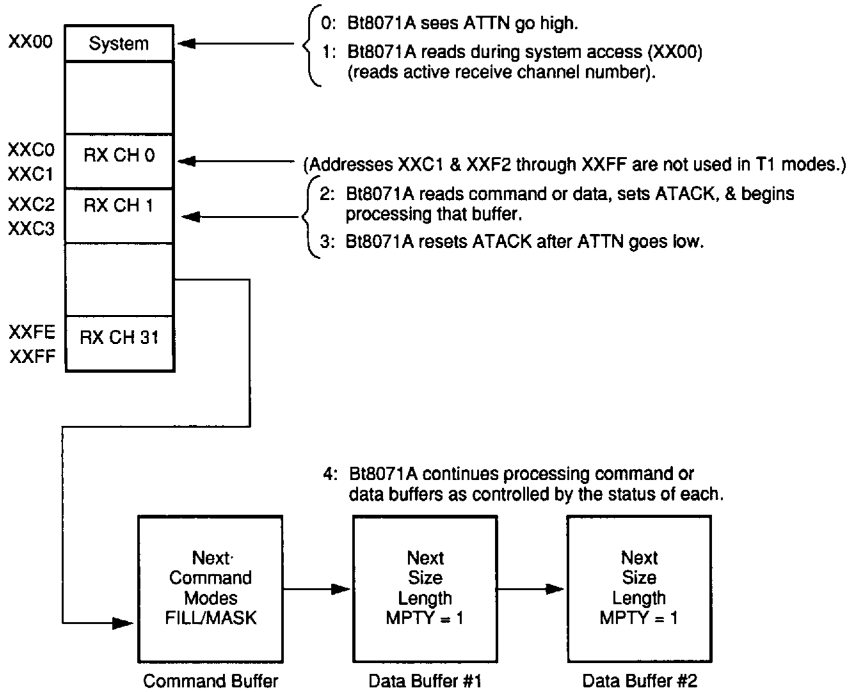


Figure 23. A Typical Linked Buffer Receiver Activity.

Order of Data

Transmission

The Bt8071A transmits data bytes in the same time sequence as they are arranged in ascending addresses in the external buffers. The data at byte address m is transmitted first, the data at address m+1 is transmitted next, and so on while the data bytes are in the same buffer. After the data in a single buffer is exhausted, the Bt8071A starts to transmit the next byte from the next buffer whose address is specified in the current buffer. The transition to the next buffer is transparent to the host while the flow of actual data is maintained.

This natural sequence of data flow is maintained for flexible hyperchannels, as well. It is not possible to transmit hyperchannel data in any sequence other than first in, first out.

The Bt8071A transmits the LSB (D0) of a data byte first; it transmits the next LSB second; and it transmits the MSB (D7) last. The only exception is that the MSB of the HDLC FCS (CRC-CCITT) is transmitted first; the LSB is transmitted last.

Reception

The Bt8071A writes received data bytes in the external shared memory in the same order in which they are received in time. The first received byte is written at byte m, the second received at byte address m+1, and so on as long as the buffer is not completely filled or an end-of-frame is not reached. After the end of the frame or the end of the buffer (whichever occurs first) is detected, the Bt8071A writes the next received data byte at the first allocated address of the next available buffer. The transition to the next buffer is transparent to the host and maintains the flow of the actual data.

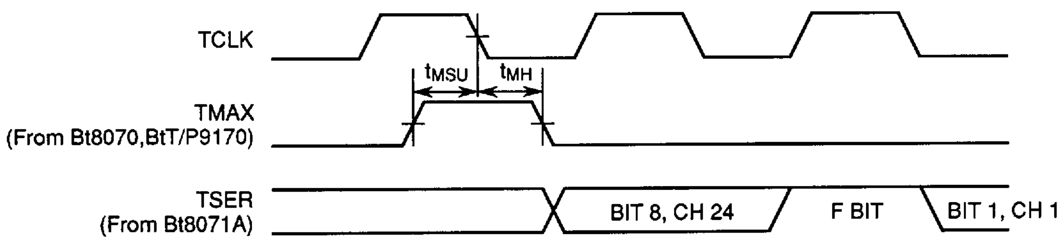
The Bt8071A writes the first received data bit of an octet at the LSB (D0) position of the external buffer byte, the second received data bit at the next to LSB position, and so on. The last (eighth) received data bit of an octet is written at the MSB (D7) position of the data byte.

Switching Characteristics

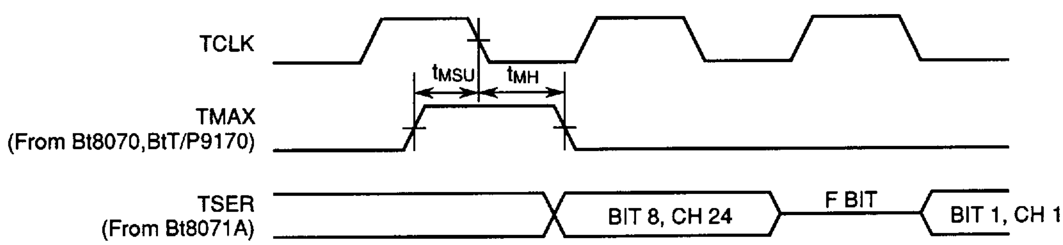
Bt8070/BtT/P9170 Interface —Bt8071A Transmit Frame Synchronization Timing

Symbol	Parameter	Min.	Max	Units
t_{MSU}	TMAX Setup time	60	—	ns
t_{MH}	TMAX Hold time	60	—	ns

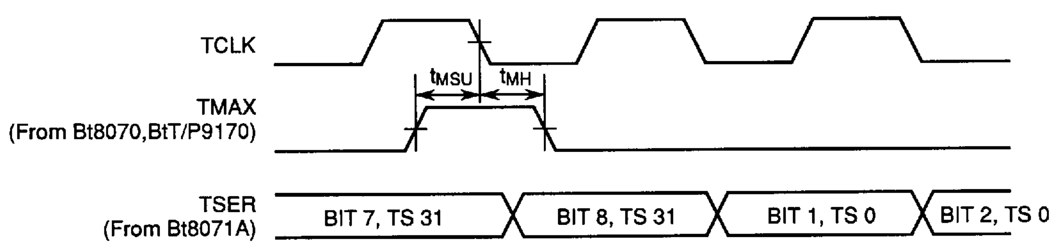
Bt8071A Transmit Frame Synchronization Timing.



a. Transmit Serial Output–T1 Mode, TSEREN = 1



b. Transmit Serial Output–T1 Mode, TSEREN = 0



c. Transmit Serial Output–CEPT PCM 30 Mode, TSEREN = 1 or 0

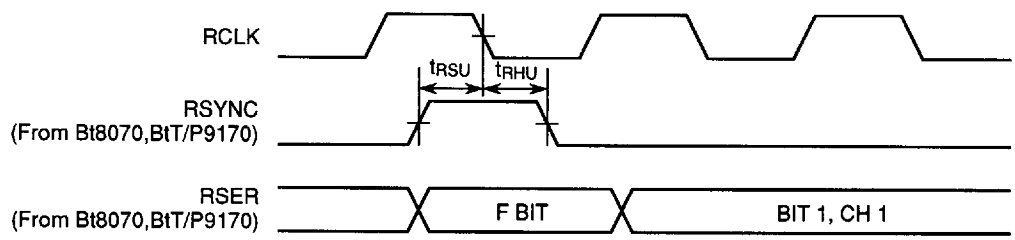
Bt8071A Transmit Frame Synchronization Waveforms.

Switching Characteristics *(continued)*

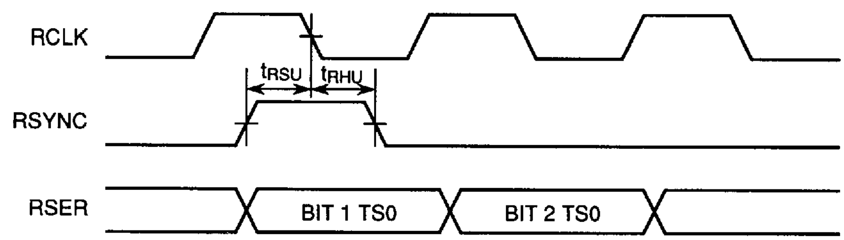
Bt8070/BtT/P9170 Interface —(continued)

Symbol	Parameter	Min.	Max.	Units
t_{RSU}	RSYNC Setup time	50	—	ns
t_{RHU}	RSYNC Hold time	50	—	ns

Bt8071A Receive Frame Synchronization Timing.



a. Receiver Serial Input–T1 Mode



b. Receiver Serial Input–CEPT PCM 30 Mode

Bt8071A Receive Frame Synchronization Waveforms.

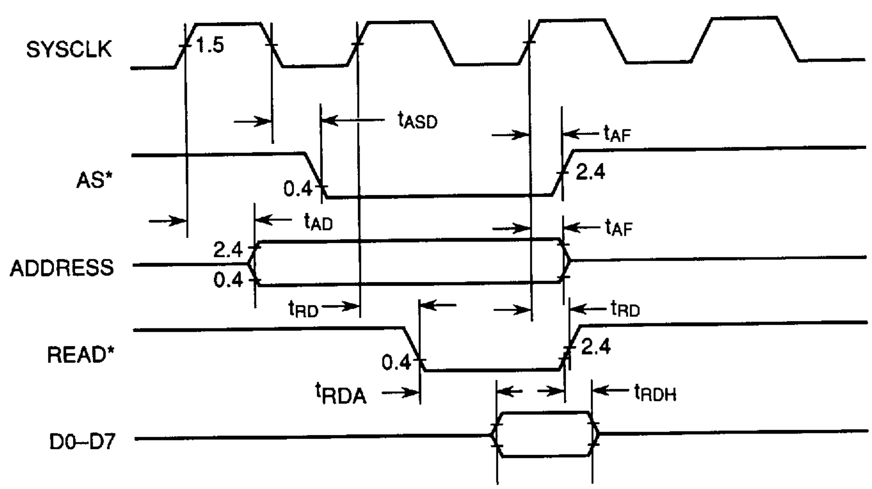
Switching Characteristics *(continued)*

Shared Memory Interface

Parameter	Symbol	Min.	Max	Units
Address Strobe Delay	t_{ASD}	10	75	ns
Address Delay	t_{AD}	10	90	ns
Address Float Delay	t_{AF}	10	90	ns
Read Enable Delay	t_{RD}	10	75	ns
Read Data Access Time	t_{RDA}	—	Note 1	ns
Read Data Hold Time	t_{RDH}	0	Note 2	ns

Note 1: Read data access time for shared memory = t_{SCP} – 125 ns.
Note 2: Data drive to data bus float = t_{SCPW} – 65 ns

Read Cycle Timing.



Read Cycle Waveforms.

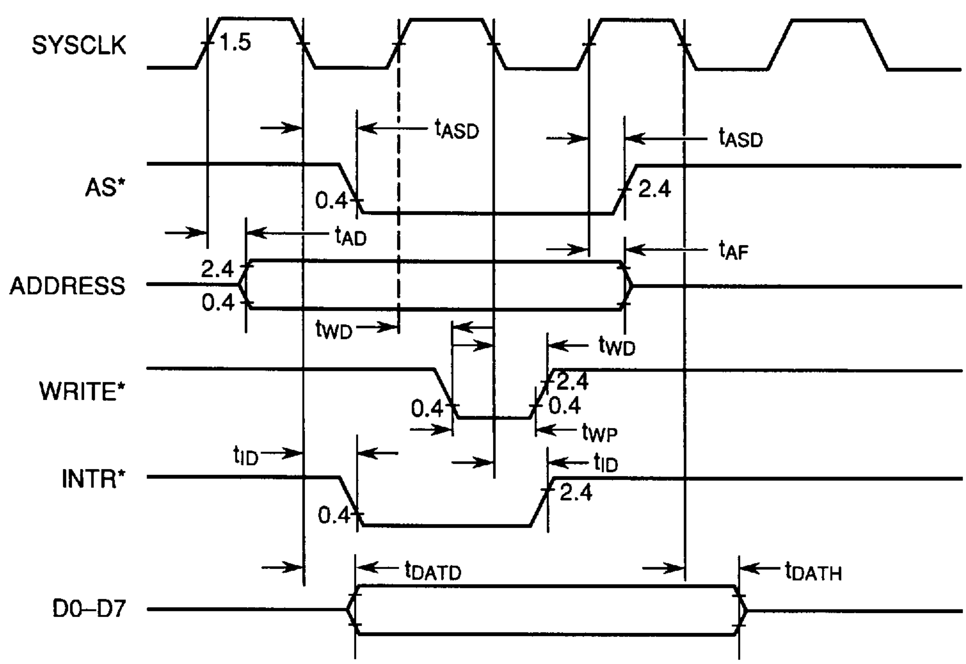
Switching Characteristics *(continued)*

Shared Memory Interface (continued)

Parameter	Symbol	Min.	Max.	Units
Address Strobe Delay	t_{ASD}	10	75	ns
Address Delay	t_{AD}	10	90	ns
Address Float Delay	t_{AF}	10	90	ns
Write Delay	t_{WD}	10	75	ns
Write Pulse Width	t_{WP}	80	—	ns
Interrupt Delay	t_{ID}	10	75	ns
Write Data Delay	t_{DATD}	10	90	ns
Write Data Hold Time (Note)	t_{DATH}	10	90	ns

Note: Data drive to data bus float time

Write Cycle Timing.



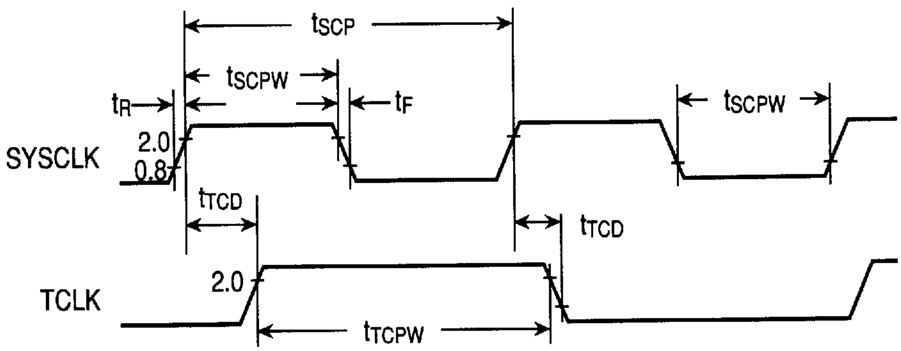
Write Cycle Waveforms.

Switching Characteristics *(continued)*

LIU Interface

Parameter	Symbol	Min.	Max.	Units
TCLK Delay	t_{TCD}	0	50	ns
SYSCLK Pulse Width	t_{SCPW}	110	—	ns
TCLK Pulse Width	t_{TCPW}	200	—	ns
SYSCLK Period	t_{SCP}	240	10,000	ns
Rise, Fall Time	t_r, t_f	—	5	ns

Bt8071A Clock Timing.



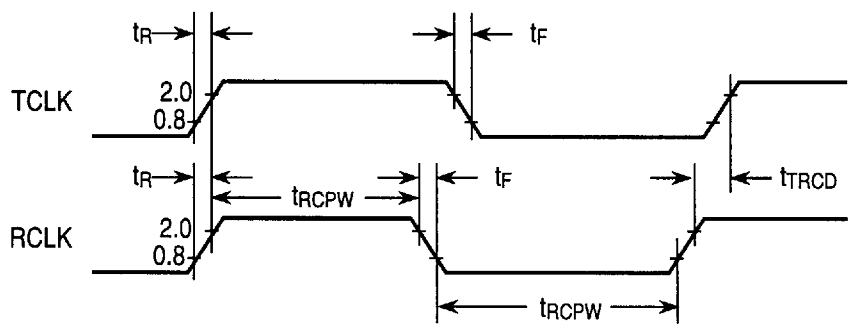
Bt8071A Clock Waveforms.

Switching Characteristics *(continued)*

LIU Interface (continued)

Parameter	Symbol	Min.	Max.	Units
Rise, Fall Time	t_r, t_f	—	10	ns
RCLK Pulse Width	t_{RCPW}	190	—	ns
TCLK, RCLK Difference	t_{TRCD}	—	Note 1	ns
Note: RCLK is to be centered around TCLK. The summation of RCLK and TCLK periodic differences over any duration of time must never exceed 14 TCLK periods.				

Bt8071A TCLK-RCLK Timing.



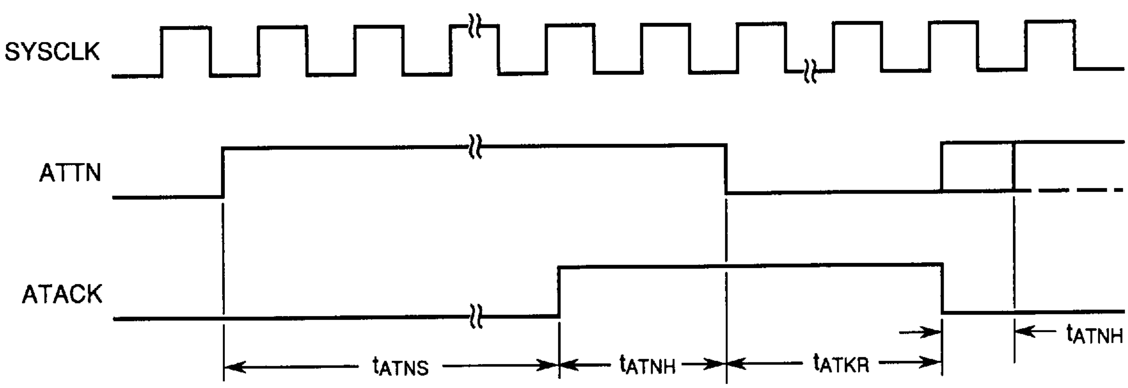
Bt8071A TCLK-RCLK Waveforms.

Switching Characteristics *(continued)*

Channel Activation/Deactivation

Parameter	Symbol	Min.	Max.	Units
ATTN to ATACK Response Time	t_{ATNS}	20	48	SYSCLKS
ATTN Hold time	t_{ATNH}	0	—	ns
ATACK Reset Delay	t_{ATKR}	2	4	SYSCLKS

Channel Activation/Deactivation Timing.



Channel Activation/Deactivation Waveforms.

Electrical Characteristics

Signal Name	Reference Signal	Edge (Note 1)	Setup (Min.)	Hold (Min.)	Units
ATTN	SYSCLK	PE	50	50	ns
RESET	TCLK	NE	60	60	ns
D0-D7	SYSCLK	PE	50	0	ns
TMAX (SIS = I)	TCLK	NE	60	60	ns
TMAX (SIS = O)	TCLK	PE	60	60	ns
RSER (SIS = I)	RCLK	NE	50	50	ns
RSER (SIS = O)	RCLK	PE	50	50	ns
RRED (SIS = I)	RCLK	NE	50	50	ns
RRED (SIS = O)	RCLK	PE	50	50	ns
RSYNC (SIS = I)	RCLK	NE	50	50	ns
RSYNC (SIS = O)	RCLK	PE	50	50	ns

Note 1: PE = positive edge; NE = negative edge.
All input AC timing measurements are referenced to the 0.8 and 2.0 Vdc logic levels.

Bt8071A Input AC Electrical Characteristics.

Signal Name	Reference Signal	Edge (Note 1)	Max. DELAY	Min. HOLD	Units
DMND	SYSCLK	PE	75	10	ns
AS*	SYSCLK	PE/NE	75	10	ns
A0–A15	SYSCLK	PE	90	10	ns
SYSACC	SYSCLK	PE	75	10	ns
READ*	SYSCLK	PE	75	10	ns
WRITE*	SYSCLK	PE/NE	75	10	ns
D0–D7	SYSCLK	NE	90	10	ns
INTR*	SYSCLK	NE	75	10	ns
CH0–CH4	SYSCLK	PE	140	10	ns
RX/TX*	SYSCLK	PE	140	10	ns
ATACK	SYSCLK	PE	75	10	ns
TSER	TCLK	NE	75	10	ns

Note 1: PE = positive edge; NE = negative edge.
All output AC timing measurements are referenced to the 0.4 and 2.4 Vdc logic levels

Bt8071A Output AC Electrical Characteristics.

Electrical Characteristics *(continued)*

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to 7.0	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +150	°C

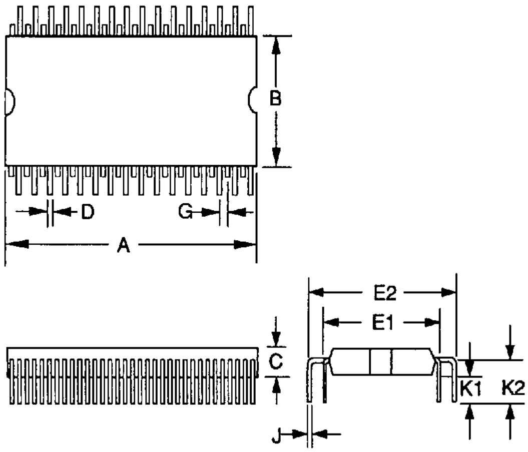
Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Low Voltage	V_{IL}	–0.3	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}	–	0.4	V	I_{LOAD} = + 1.6 mA
Output High Voltage CMOS	V_{OH}	3.5	–	V	I_{LOAD} = + 100 µA
Output Low Current	I_{OL}			mA	V_{OL} = 0.4 V
CH0–CH4, RX/TX*, TSER		+3.2	–		
Others		+1.6	–		
Output High Current	I_{OH}			µA	V_{OH} = 3.5 V
CH0–CH4, RX/TX*, TSER		–200	–		
Others		–100	–		
Input Capacitance	C_{IN}	–	5	pF	
Output Capacitance (load)	C_{OUT}	–			
TSER		–	100	pF	
Others		–	50	pF	
Power Dissipation	P_{WD}	–	250	mW	

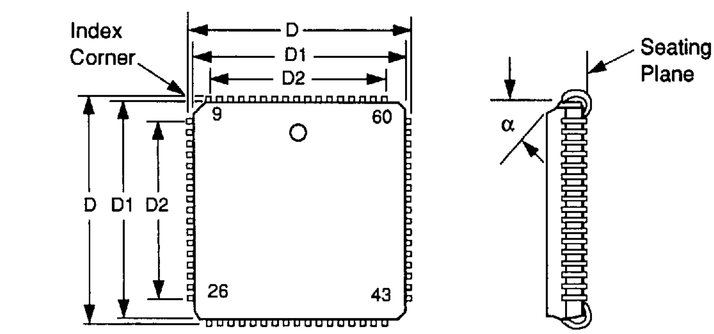
V_{CC} = 5 Vdc ± 5%, V_{SS} = 0 Vdc, and T_A = 0 to + 70°C, unless otherwise noted.

Package Drawings



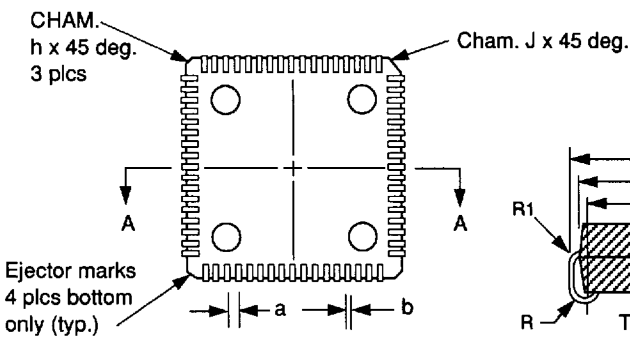
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	40.77	41.28	1.605	1.625
B	16.76	17.27	0.660	0.680
C	3.56	4.58	0.140	0.180
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.008	0.012
K1	2.92	3.18	0.115	0.125
K2	4.83	5.34	0.190	0.210

64-Pin Plastic Quad In-Line Package (QUIP)

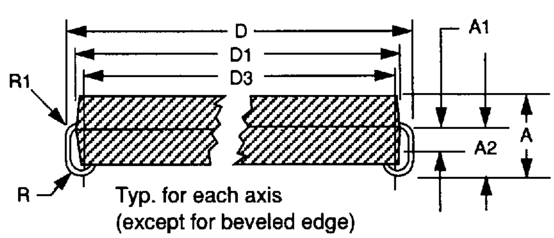


Top View **Side View**

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23.50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	



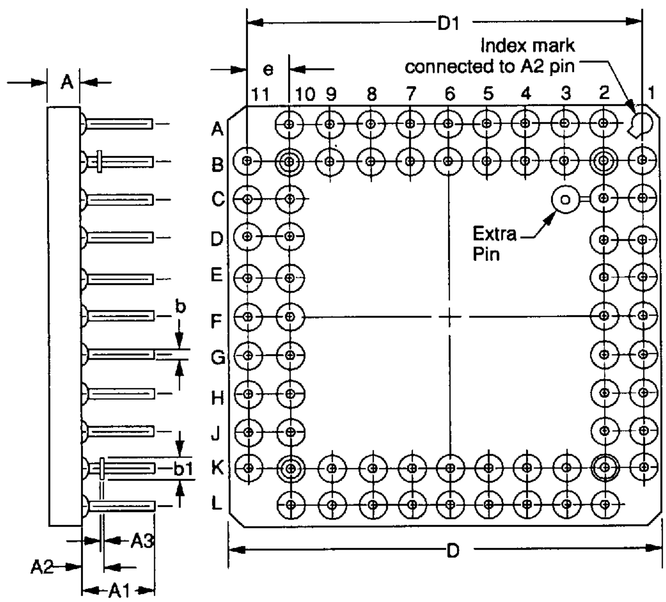
Bottom View



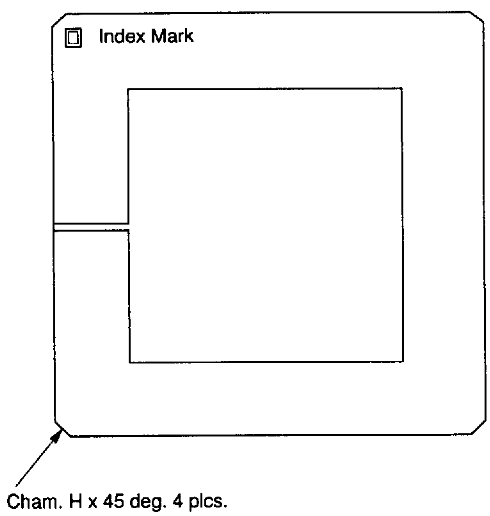
Section A-A

68-Pin Plastic LCC (PLCC)

Package Drawings



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	1.70	2.11	0.067	0.083
A1	4.45	4.70	0.175	0.185
A2	1.19	1.35	0.047	0.053
A3	0.20 REF		0.008 REF	
b	0.41	0.51	0.016	0.020
b1	1.19	1.35	0.047	0.053
D	27.58	28.19	1.086	1.110
D1	25.15	25.65	0.990	1.010
e	2.41	2.67	0.095	0.105
h	0.51 REF		0.020 REF	



68-Pin Grid Array (PGA)

Ordering Information

Part Number	Package	Temperature Range
Bt8071AKPQ	64-pin Plastic QUIP	0° to 70°C
Bt8071AKPJ	68-pin PLCC	0° to 70°C
Bt8071AEPJ	68-pin PLCC	–40° to 85°C
Bt8071AKG	68-pin PGA	0° to 70°C

Revision History

Revision	Description
B	On page 55 in the "Package" column of the Ordering Information table, 68-pin Plastic QUIP was changed to 64-pin Plastic QUIP.