High Power, Class B Output Stage

GS551 DATA SHEET

FEATURES

- **adjustable gain to 48 dB**
- **capable of driving low impedance receiver**
- **low component count, 3 small capacitors and 1 resistor**
- **gain trim can be used as vol. control for reduced noise**
- **minimal start-up transient**
- **no gain expansion**

STANDARD PACKAGING

- 10 pin MICROpac
- 10 pin PLID®
- 10 pin SLT
- Chip (68 x 60 mils)

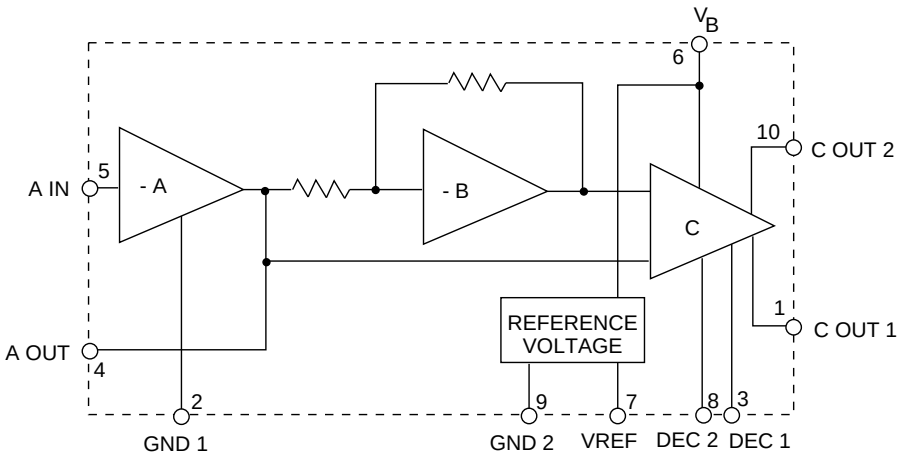
  Au Bump

CIRCUIT DESCRIPTION

The GS551 is a 10 pin, low voltage, class B amplifier which operates over a battery range of 1.1 VDC to 3 VDC.

The GS551 consists of three gain blocks. The first block is an inverting amplifier with the gain set by two external resistors. The gain trim feature can be used as a volume control in hearing aid applications. The second block is an inverting unity gain amplifier which serves as a phase splitter. The outputs from the first and second blocks drive the differential input of the third block. The third block has a fixed AC gain of 28 dB when driving a receiver.

The amplifier has internal compensation eliminating the need for a capacitor across the receiver. Two ground pins are available for "Star" grounding to reduce any second order harmonic distortion introduced by ground line resistance.



U.S. Patent No. 4,719,430
Other Patents Pending

BLOCK DIAGRAM

Revision Date: November 1993.

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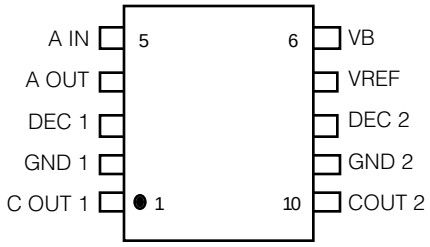
ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage	5 VDC
Operating Temperature	-10 to +40 °C
Storage Temperature	-20 to +70 °C

CAUTION
CLASS 1 ESD SENSITIVITY

PIN CONNECTION



ELECTRICAL CHARACTERISTICS

Conditions: Frequency = 1 kHz, Temperature = 25°C, Supply Voltage V_B = 1.3 VDC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain	A_V	V_O=0.707 VRMS	46	48	50	dB
Amplifier Current	I_{AMP}		120	220	335	µA
Transducer Current	I_{TRANS}		120	250	390	µA
Input Referred Noise	IRN	NFB 0.2 to 10 kHz at 12 dB/Oct	-	1.3	2.5	µV
Total Harmonic Distortion	THD	V_O=0.707 VRMS	-	0.25	1.3	%
		V_O=1.3 VRMS	-	0.3	1.5	%
Stable with R_B to	R_{STAB}	R_B=22Ω	-	-	22	Ω
Maximum Output Current	I_{OUT}	V_{P8}=0	-	>35	-	mA

All parameters remain as shown in Test Circuit unless otherwise stated in "Conditions" column

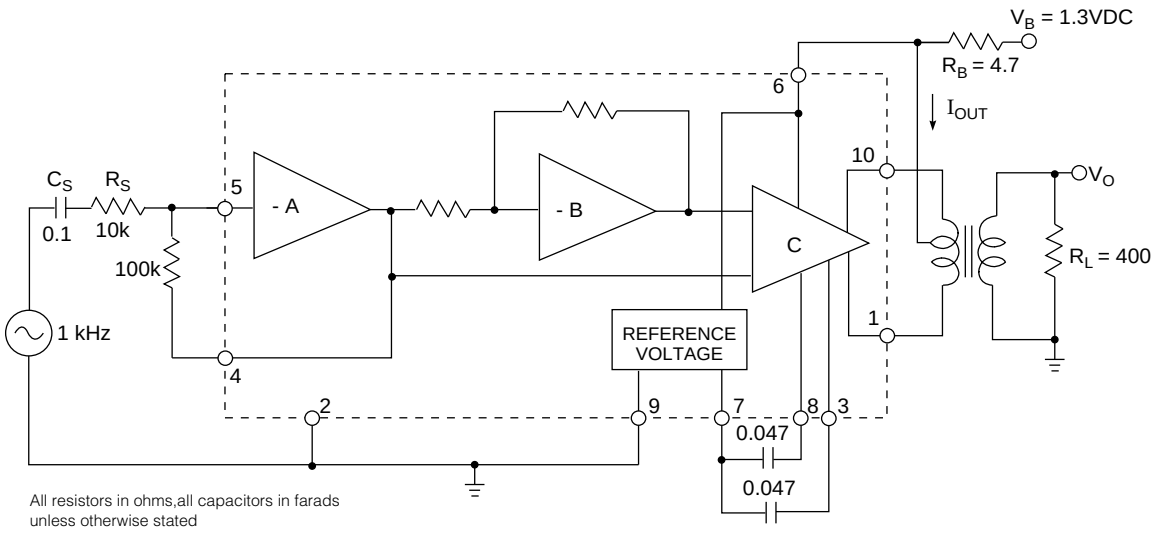


Fig. 1 Test Circuit

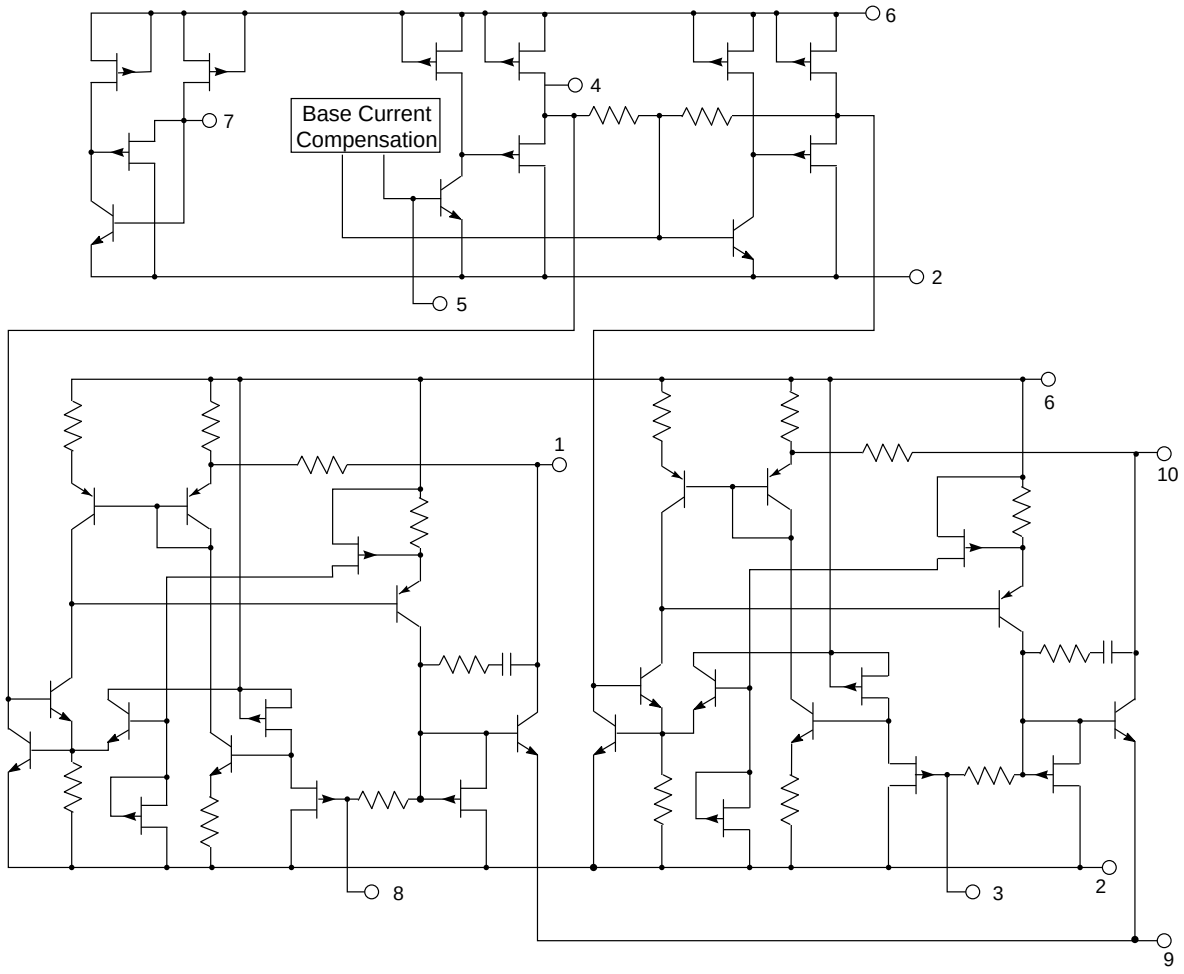


Fig. 2 GS551 Functional Schematic

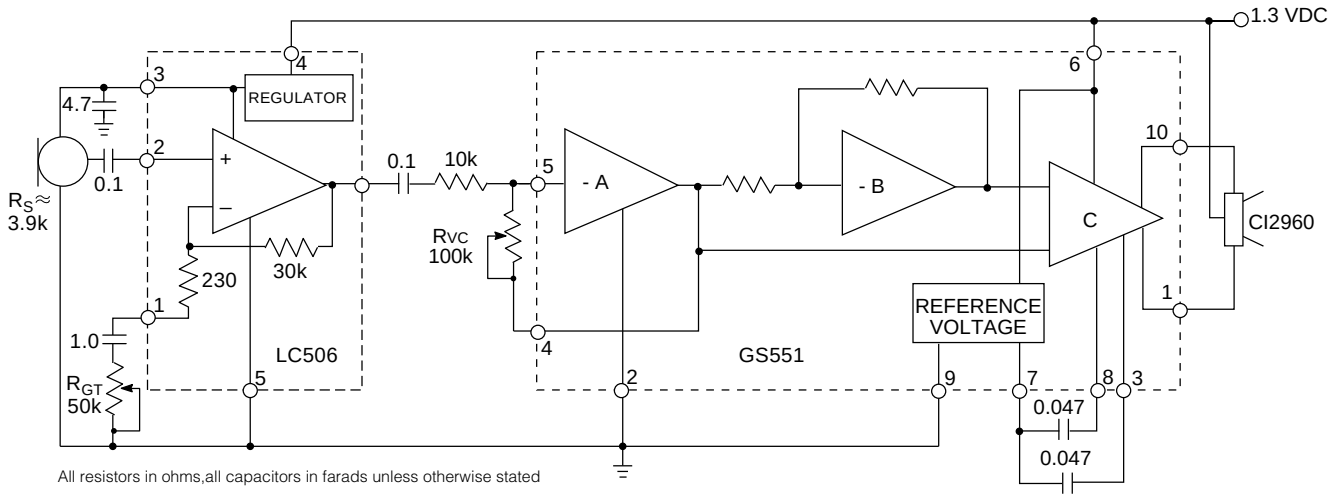


Fig. 3 Application Circuit

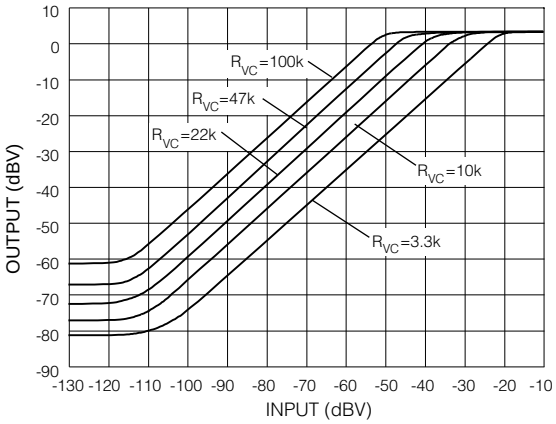


Fig. 4 I/O Characteristics at Various Gain Settings (R_S=3.92k)

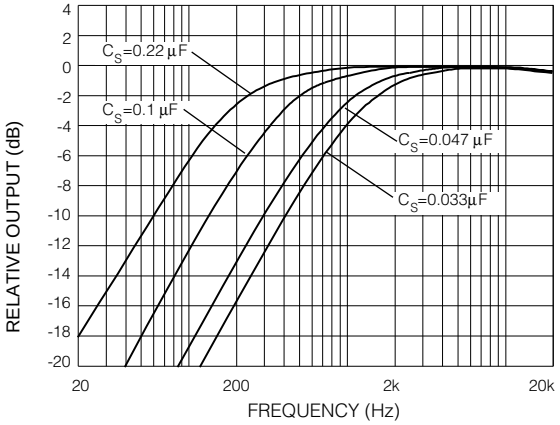


Fig. 5 Closed Loop Frequency Response at Various C_S Values (R_S=3.92k)

Fig. 6 Power Outout vs Load Resistance at 7% Distortion, R_B=0Ω, V_B=1.35V

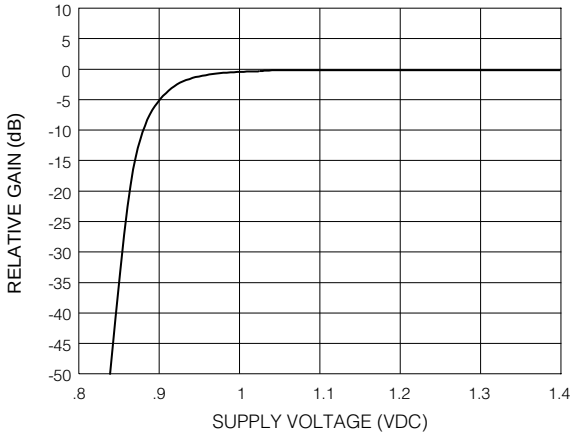


Fig. 7 Gain vs Supply Voltage

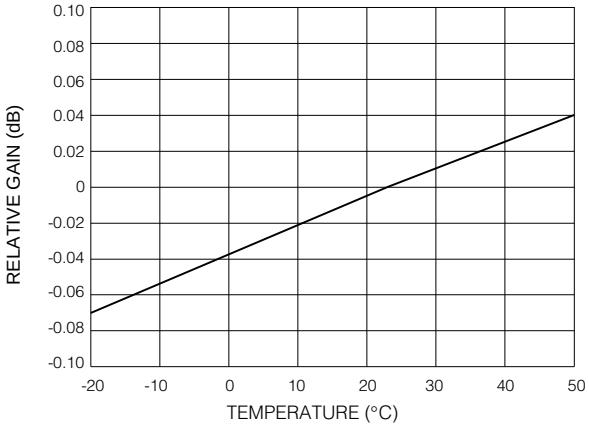


Fig. 8 Gain vs Temperature

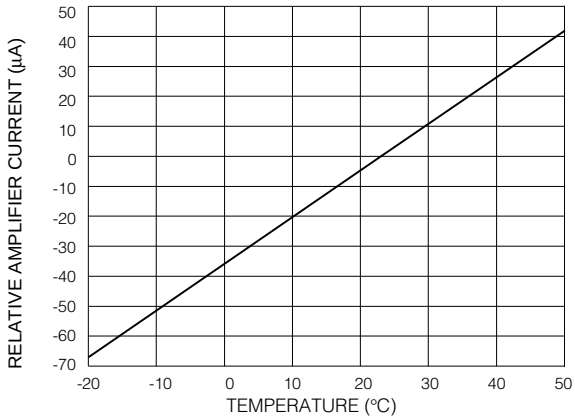


Fig. 9 Amplifier Current vs Temperature

REVISION NOTES:
Pb/Sn bump removed, V_{P8}=0 added to Electrical Characteristics,
I_{OUT} added to Test Circuit