ZiLOG

PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z89319/328

DIGITAL TELEVISION CONTROLLER IN-CIRCUIT EMULATOR (ICE) DEVICE

FEATURES

Part Number	ROM (Word)	RAM (Word)	Speed (MHz)
Z89319	0	0	12
Z89328	0	0	12

- 124-Pin Grid Array (PGA) Package (Z89319)
  100-Pin Quad Flat Pack (QFP) Package (Z89328)
- 4.5- to 5.5-Volt Operating Range
- Z89C00 RISC Processor Core
- 0°C to +70°C Temperature Range
- Direct Closed Caption Decoding
- TV Tuner Serial Interface
- Customized Character Set
- Character Control Mode
- Directly Controlled Receiver Functions

GENERAL DESCRIPTION

The Z89319 and Z89328 are ROMless versions of the Z89300 family of Zilog's Digital Television Controllers designed for use in emulators and development boards to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities.

The powerful Z89C00 RISC processor core allows users to control on-board peripheral functions and registers using the standard processor instruction set.

In closed caption mode, text can be decoded directly from the composite video signal and displayed on the screen with assistance from the processor's digital signal processing capabilities. The character representation in this mode allows for a simple attribute control through the insertion of control characters.

The character control mode provides access to the full set of attribute controls. The modification of attributes is allowed on a character-by-character basis. The insertion of control characters permits direction of other character attributes.

Display attributes, including underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency, are made possible through a fully customized 512 character set, formatted in two 256 character banks.

Serial interfacing with the television tuner is provided through the tuner serial port. Digital channel tuning adjustments may be accessed through the industry-standard I^2C port.

Additional hardware provides the capability to display two to three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Special circuitry can be activated to improve the visibiity of text by adding a right-sided shadow effect to the characters.

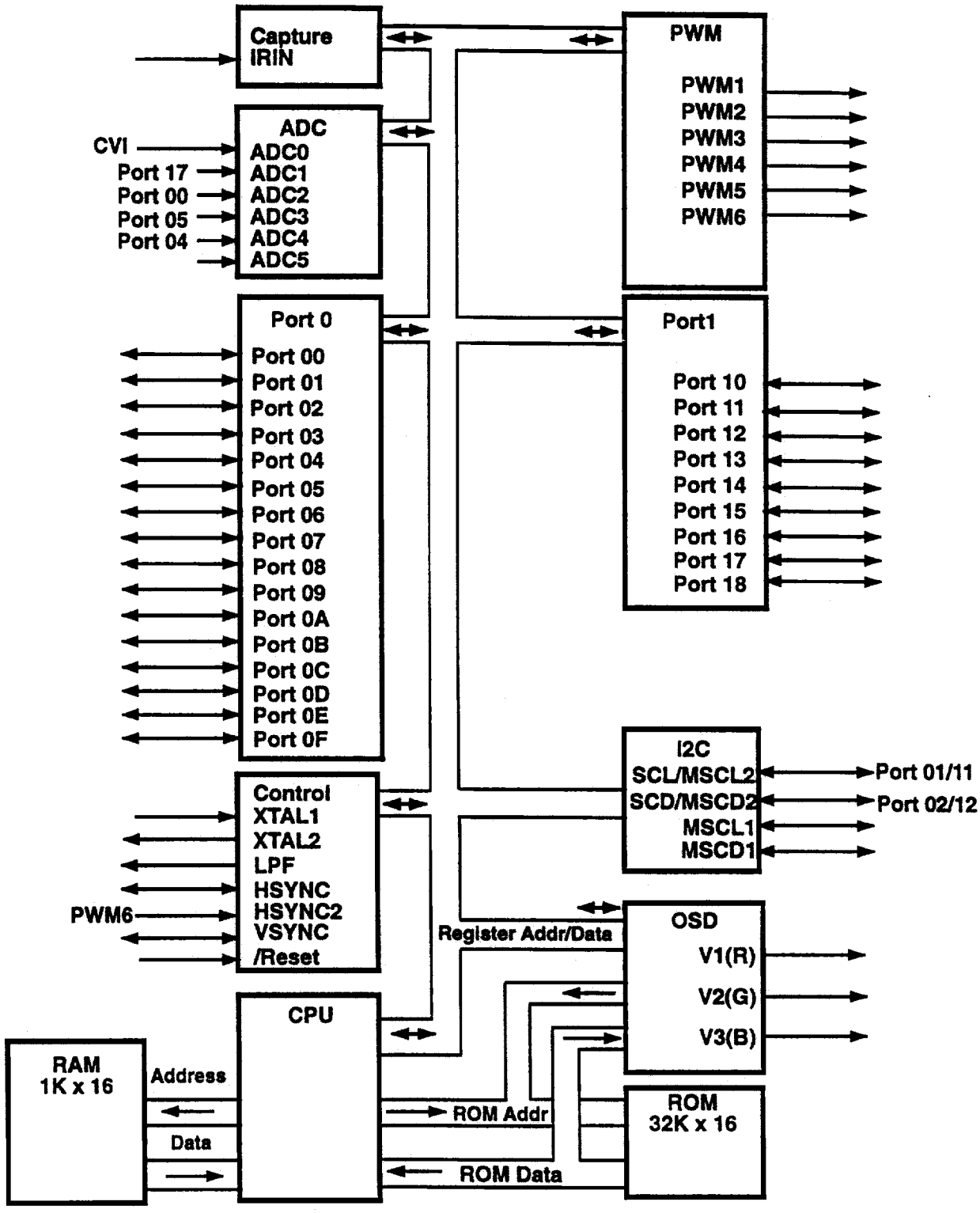
Receiver functions such as color and volume can be directly controlled by six 8-bit pulse width modulated ports.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

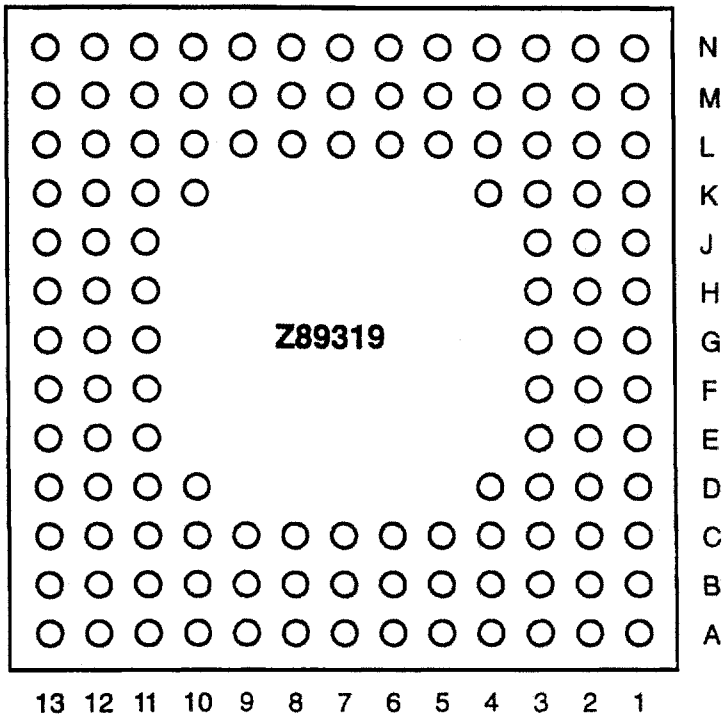
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

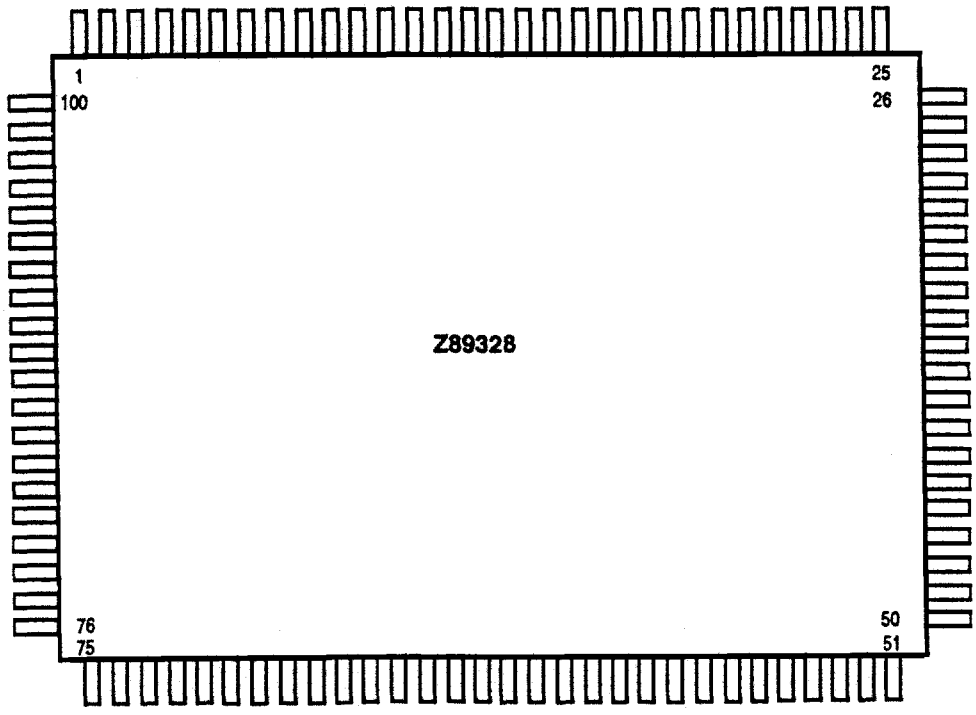


Functional Block Diagram

PIN DESCRIPTION



124-Pin PGA Configuration



100-Pin QFP Configuration

PIN DESCRIPTION (Continued)

Z89319/Z89328 Pin Identification Table

Number	Pin Name	124-Pin	100-Pin
1	P03	C3, 10	52
2	P01	B2, 11	53
3	V_{cc}	B1	
4	gnd	D3	
5	address12	C2	54
6	address11	C1	55
7	P02	D2, 12	56
8	address10	E3	57
9	address9	D1	58
10	address8	E2	59
11	address7	E1	60
12	address6	F3	61
13	CVI/ADC0	F2, 13	62
14	address5	F1	63
15	address4	G2	64
16	V_{cc}	G3	
17	gnd	G1	
18	address3	H1	65
19	LPF	H2, 14	66
20	address2	H3	67
21	address1	J1	68
22	address0	J2	69
23	IE	K1	70
24	R/W	J3	71
25	ANGNDF	K2, 15	72
26	sys_clk	L1	73
27	EA0	M1	74
28	EA1	K3	75
29	EA2	L2	76
30	ADC5	N1, 16	77
31	P04/ADC4	K4, 17	78

Number	Pin Name	124-Pin	100-Pin
32	P05/ADC3	L3, 18	79
33	gnd	M2	
34	P00/ADC2	N2, 19	80
35	int_bus0	L4	
36	P17/ADC1	M3, 20	81
37	int_bus1	N3	82
38	ANGND	M4, 21	83
39	int_bus2	L5	
40	ANVCC	N4, 22	84
41	int_bus3	M5	85
42	P0F/HB	N5, 23	86
43	V3 (B)	L6, 24	87
44	V_{cc}	M6	
45	V2 (G)	N6, 25	88
46	V1 (R)	M7, 26	89
47	gnd	L7	
48	Blank	N7, 27	90
49	HSync	N8, 28	91
50	int_bus4	M8	
51	VSync	L8, 29	92
52	P12/I2MSD2	N9, 30	93
53	int_bus5	M9	
54	P11/I2MSC2	N10, 31	94
55	int_bus6	L9	95
56	P0E	M10, 32	96
57	int_bus7	N11	97
58	I2MSD1	N12, 33	98
59	V_{cc}	L10	
60	I2MSC1	M11, 34	99
61	int_bus8	N13	100
62	/Reset	K10, 35	1

PIN DESCRIPTION (Continued)

Z89319/Z89328 Pin Identification Table (continued)

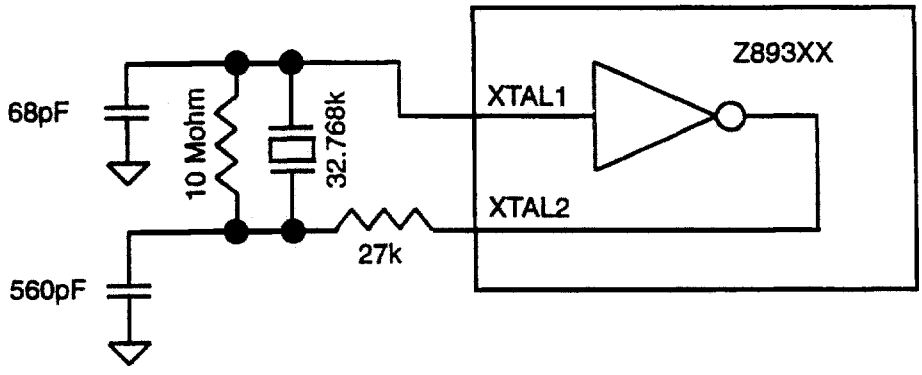
Number	Pin Name	124-Pin	100-Pin
63	XTAL1	L11, 36	2
64	XTAL2	M12, 37	3
65	int_bus9	M13	
66	gnd	K11	
67	data15	L12	4
68	data11	L13	5
69	GND	K12, 38	6
70	data10	J11	7
71	data14	K13	8
72	data13	J12	9
73	data12	J13	10
74	_pabus	H11	11*
75	V_{CC}/V_{DD}	H12, 39	12
76	_romless	H13	13*
77	data9	G12	14
78	data8	G11	15
79	data7	G13	16
80	stopwdt	F13	
81	ANGNDX	F12, 40	17
82	single-stop	F11	
83	data6	E13	18
84	data5	E12	19
85	data4	D13	20
86	data3	E11	21
87	PWM1	D12, 41	22
88	data2	C13	23
89	data1	B13	24
90	data0	D11	25
91	V_{CC}	C12	
92	PWM2	A13, 42	26
93	gnd	D10	
94	PWM3	C11, 43	27
95	PWM4	B12, 44	28
96	PWM5	A12, 45	29
97	int_bus10	C10	30
98	PWM6	B11, 46	31
99	int_bus11	A11	32
100	P10/4<0>	B10, 47	33
101	int_bus12	C9	34
102	P08/R<1>	A10, 48	35
103	VCC	B9	
104	P18/G<0>	A9, 49	36
105	P13/G<1>	C8, 50	37
106	gnd	B8	
107	P14/B<0>	A8, 51	38
108	P15/B<1>	B7, 52	39
109	int_bus13	C7	
110	P16/SCLK	A7, 1	40
111	int_bus14	A6	
112	IRIN	B6, 2	41
113	int_bus15	C6	
114	P0C	A5, 3	42
115	P0B	B5, 4	43
116	P0A	A4, 5	44
117	P19	C5	45
118	P09	B4, 6	46
119	V_{CC}	A3	
120	P0D	A2, 7	47
121	address14	C4	48
122	P07/CSync	B3, 8	49
123	address13	A1	50
124	P06/Cnter	D4, 9	51

V1, V2, V3 ANALOG OUTPUT
Specifications V_{CC} = 5.25 V

V_{CC} = 5.25 V	Condition	Limit
Output Voltage	Bit = 11	4.30 V ± 0.3 V
	Bit = 10	3.10 V ± 0.25 V
	Bit = 01	1.90 V ± 0.20 V
	Bit = 00	0 V ± 0.75 V
Setting Time	70% of DC Level, 10pf Load	< 50 ns

V1, V2, V3 ANALOG OUTPUT
Specifications V_{CC} = 4.75 V

V_{CC} = 4.75 V	Condition	Limit
Output Voltage	Bit = 11	3.90 V ± 0.30 V
	Bit = 10	2.80 V ± 0.25 V
	Bit = 01	1.70 V ± 0.20 V
	Bit = 00	0 V ± 0.65 V
Setting Time	70% of DC Level, 10pf Load	< 50 ns



32K Oscillator Recommended Circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Power Supply Voltage	0	7	V	
V_{ID}	Input Voltage	–0.3	V_{CC} +0.3	V	Digital Inputs
V_{IA}	Input Voltage	–0.3	V_{CC} +0.3	V	Analog Inputs (A/D0...A/D4)
V_O	Output Voltage	–0.3	V_{CC} +0.3	V	All Push-Pull Digital Output
I_{OH}	Output Current High		–10/–1[a]	mA	One Pin
I_{OH}	Output Current High		–100	mA	All Pins
I_{OL}	Output Current Low		20/1[b]	mA	One Pin
I_{OL}	Output Current Low		200	mA	All Pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	–65	150	°C	

Notes:
a) 1 mA max. when output pad impedance is 600 Ω.
b) 1 mA max. when output pad impedance is 600 Ω.

DC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to + 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	0.4	V	
V_{IH}	Input Voltage High	0.6 V_{CC}	V_{CC}	3.6	V	
V_{OL}	Output Voltage Low		0.4	0.16	V	@ I_{OL} = 1 mA
V_{OH}	Output Voltage High	V_{CC} –0.9		4.75	V	@ I_{OL} = 0.75 mA
V_{XL}	Input Voltage XTAL1 Low		0.3 V_{CC}	1.0	V	External Clock
V_{XH}	Input Voltage XTAL1 High	V_{CC} –2.0		3.5	V	Generator Driven
V_{HY}	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I_{IR}	Reset Input Current		150	90	µA	V_{RL} = 0 V
I_{IL}	Input Leakage	–3.0	3.0	0.01	µA	@ 0 V and V_{CC}
I_{CC}	Supply Current		100	60	mA	
I_{CC1}	Supply Current		300	100	µA	Sleep Mode @ 32 KHz
I_{CC2}	Supply Current		40	5	µA	Stop Mode

AC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units	Note
T_PC	Input Clock Period	16	100	32	µS	
T_RC, T_FC	Clock Input Rise and Fall			12	µS	
T_DPOR	Power On Reset Delay	0.8		1.2	s	Depends on Crystal

AC CHARACTERISTICS*

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units
T_WRES	Power-On Reset Min. Width		5TPC		µS
T_DH_S	H_Sync Incoming Signal Width	5.5	12.5	11	µS
T_DV_S	V_Sync Incoming Signal Width	0.15	1.5	1.0	mS
T_DE_S	Time Delay Between Leading Edge of V_Sync and H_Sync in Even Field	–12	+12	0	µS
T_DO_S	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	µS
T_WHV_S	H_Sync/V_Sync Edge Width		2.0	0.5	µS

Notes:
All timing of the I²C bus interface are defined by related specifications of the I²C bus interface.

Pre-Characterization Product:
The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

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