mosaic

Mosaic Semiconductor Inc.

256K x 2 DRAM

MD2258TC-8/10/12

DRAFT

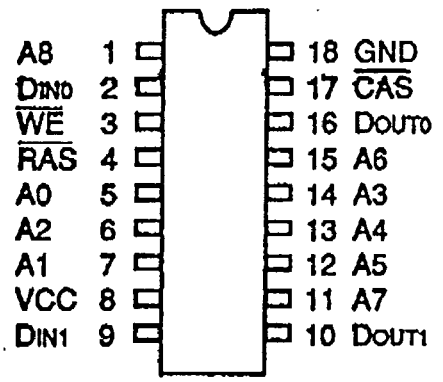
ADVANCE PRODUCT INFORMATION

262,144 X 2 CMOS High Speed Dynamic RAM

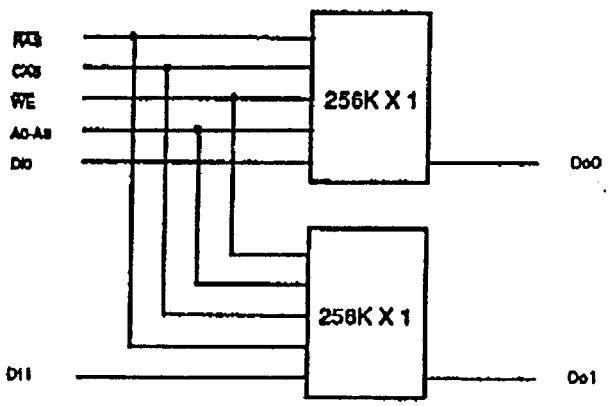
Features

- Row Access Times of 80/100/120 nS
- 2:1 Improvement in Density over DIL
- 5 Volt Supply ± 10%
- Uses two LCC Dynamic RAMs
- Standard 18 pin footprint
- Static Column Read/Write/Read Modify Write
- 256 Refresh Cycles
- RAS only Refresh
- Hidden Refresh
- CAS before RAS Refresh
- Extended RAS active time to facilitate multiple accesses within a RAS
- Directly TTL Compatible

Pin Definition



Block Diagram

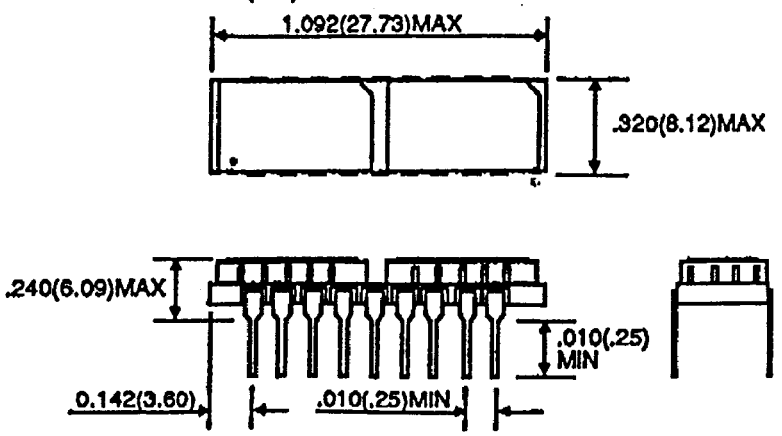


Pin Functions

A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column AddressStrobe
D_{IN0}-D_{IN1}	Data In
$D_{OUT}0$-D_{OUT1}	Data Out
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)

Package Details

Dimensions in inches (mm).



Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_t	-1 to +7	V
Power Dissipation	P_t	2	W
Storage Temperature	T_{stg}	-55 to +125	°C
Short circuit output current	I_{out}	50	mA

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{cc}	4.5	5.0	5.5	V
Input High Voltage	V_{ih}	2.4	-	$^*V_{cc}$+1	V
Input Low Voltage	V_{il}	-1.0	-	0.8	V
Operating Temperature	T_a	0	-	70	°C
	T_a Ind	-40	-	85	°C (MD2258 I)
	T_a mil	-55	-	125	°C (MD2258M,MB)

DC Electrical Characteristics

			-8		-10		-12		
Parameter	*Symbol*	*Test Condition*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Operating Current	I_{cc1}	$\overline{RAS}$,$\overline{CAS}$ Cycling: t_{RC}=min.(See Note 1)	-	140	-	120	-	100	mA
Vcc Power Supply Current (Active)	I_{cc2}	$\overline{RAS}$,$\overline{CAS}$≤V_{il} (max)	-	30	-	30	-	30	mA
Standby Current	I_{sb1}	All inputs stable at CMOS levels,$\overline{RAS}$≥(V_{cc}-0.4V)	-	5	-	5	-	5	mA
	I_{sb2}	All inputs stable at TTL levels $\overline{RAS}$≥2.4V	-	9	-	9	-	9	mA
	I_{sb3}	All inputs toggling between CMOS levels at 6.25MHZ, $\overline{RAS}$≥(V_{cc}-0.4V).	-	8	-	8	-	8	mA
	I_{sb4}	All inputs (except $\overline{RAS}$) toggling between TTL levels at 6.25MHZ.	-	11	-	11	-	11	mA
Input Leakage	I_{li}	0V≤V_{in}≤5.5V,others=0V	-20	20	-20	20	-20	20	µA
	I_{id}	Data inputs	-10	10	-10	10	-10	10	µA
Output Leakage	I_{lo}	Dout=Hi-Z, 0V≤Vout≤5.5V	-10	10	-10	10	-10	10	µA
Output Levels	V_{oh}	I_{out}=-5mA	2.4	-	2.4	-	2.4	-	V
	V_{ol}	I_{out}=5.0mA	-	0.4	-	0.4	-	0.4	V

Note 1: Icc depends on output loading condition when the device is selected,Icc max. is specified at the output open condition.

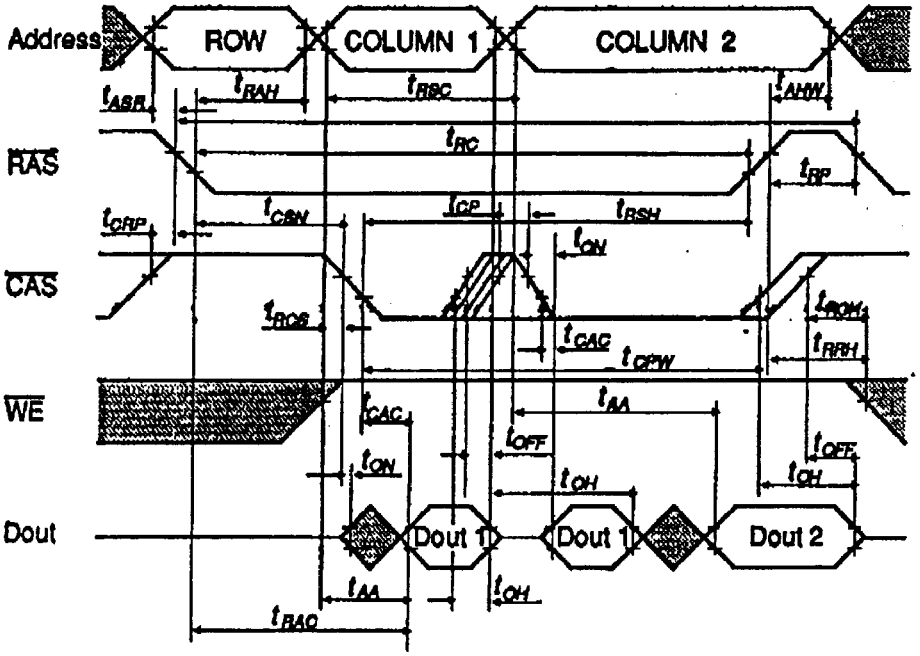
Capacitance

Parameter		*Symbol*	*typ*	*max*	*Unit*	*Notes*
Input Capacitance:	Address	C_{i1}	-	14	pF	1
	$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$	C_{i2}	-	20	pF	1
	Data In	C_{i3}	-	14	pF	1
Output Capacitance:		C_o	-	14	pF	1,2

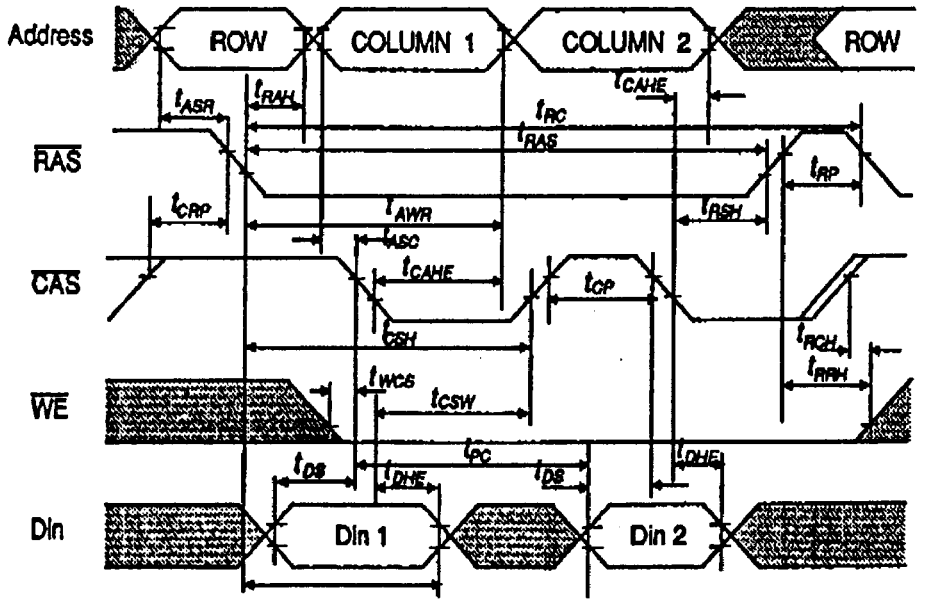
Notes: 1. Capacitance calculated, not measured.
2. $\overline{CAS}$=V_{ih} to disable Dout.

Timing Waveforms

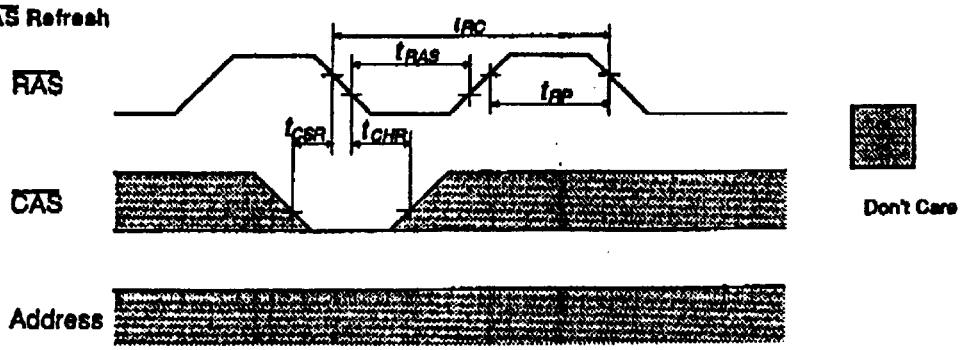
Read Cycle



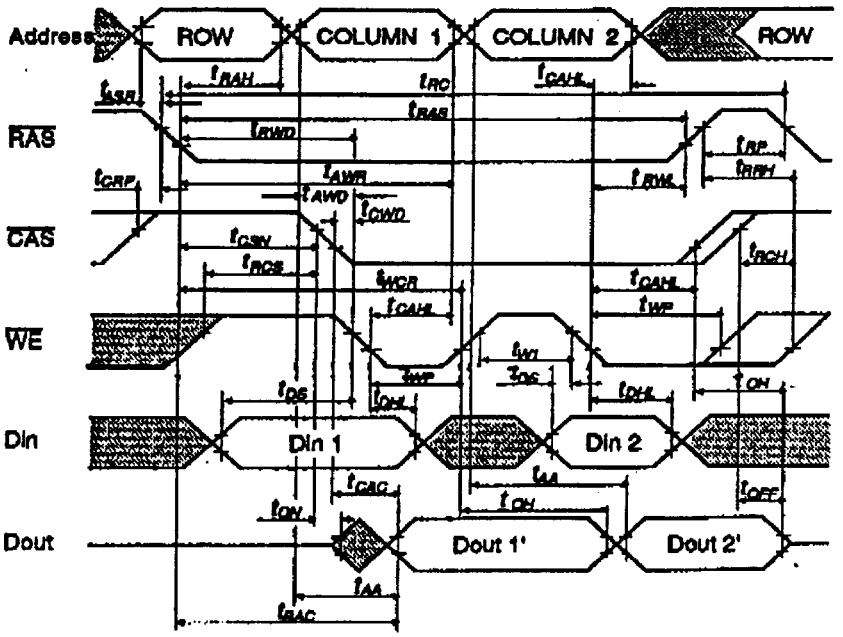
Early-Write Cycle



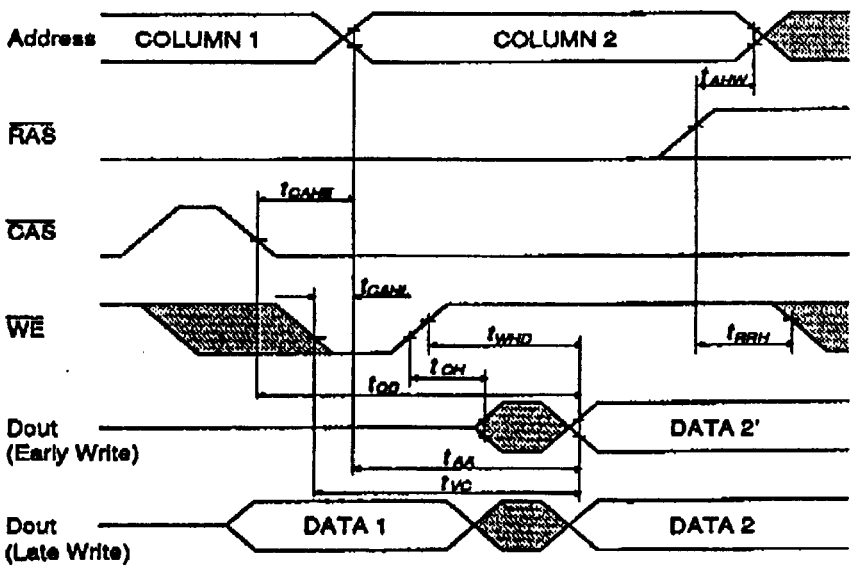
CAS Before RAS Refresh



Late-Write/Read-Modify-Write Cycle

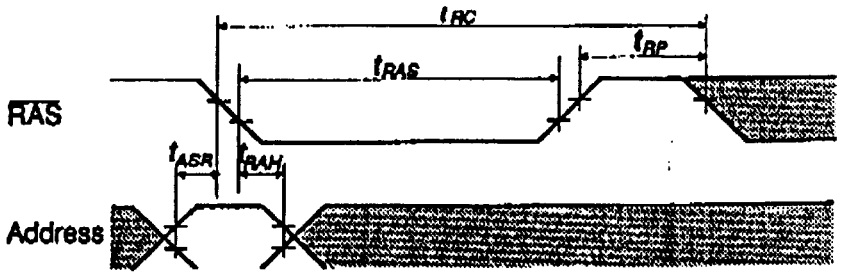


Write-Verify/Write-Read Cycle



(If Column Address 2=Column Address 1,Cycle is Write-Verify.)

RAS Only Refresh



Electrical Characteristics & Recommended AC Operating Conditions

Parameter	Symbol	-8 min	-8 max	-10 min	-10 max	-12 min	-12 max	Unit	Note
Access Time from $\overline{RAS}$	t_{RAC}	-	80	-	100	-	120	nS	
Access Time from $\overline{CAS}$	t_{CAC}	-	13	-	25	-	30	nS	
Output Buffer Turn-off Delay	t_{OFF}	-	15	-	25	-	25	nS	1
Transition Time (Rise & Fall)	t_T	2	50	3	50	3	50	nS	5,6
Random Read or Write Cycle Time	t_{RC}	151	-	200	-	230	-	nS	
$\overline{RAS}$ Precharge Time	t_{RP}	65	-	90	-	100	-	nS	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10^5	90	10^5	100	10^5	nS	
$\overline{CAS}$ Pulse Width (Read)	t_{CPW}	13	-	25	-	30	-	nS	
$\overline{CAS}$ Pulse Width (Write)	t_{CBW}	5	-	10	-	20	-	nS	
$\overline{CAS}$ Hold (Non-Refresh)	t_{CSH}	2	-	2	-	2	-	nS	
$\overline{CAS}$ to $\overline{RAS}$ Lead	t_{RSH}	20	-	25	-	30	-	nS	
$\overline{CAS}$ to $\overline{RAS}$ Set-up	t_{CRP}	2	-	2	-	2	-	nS	
Row Address Setup Time	t_{ASR}	2	-	2	-	2	-	nS	
Row Address Hold Time	t_{RAH}	2	-	15	-	15	-	nS	
Column Address Setup (Early $\overline{W}$)	t_{ASC}	0	-	0	-	0	-	nS	3
Column Address Hold (Early $\overline{W}$)	t_{CAHE}	8	-	10	-	15	-	nS	3
Early Write Setup	t_{WCS}	0	-	0	-	0	-	nS	4
Write Command Pulse Width	t_{WP}	5	-	15	-	20	-	nS	
$\overline{CAS}$ to $\overline{W}$ Delay (Read/Mod/Write)	t_{CWD}	13	-	25	-	30	-	nS	4
Data In Hold Time (Early Write)	t_{DHE}	8	-	15	-	15	-	nS	
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	nS	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	-	5	-	10	-	nS	2
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	nS	2
Refresh Period	t_{REF}	-	4	-	4	-	4	nS	
$\overline{CAS}$ to $\overline{RAS}$ Setup (Refresh)	t_{CSR}	2	-	20	-	25	-	nS	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	2	-	20	-	25	-	nS	
Address Cycle	t_{PAC}	46	-	50	-	60	-	nS	
Column Address Access	t_{AA}	-	40	-	45	-	55	nS	
Output Hold	t_{OH}	5	-	5	-	5	-	nS	1
$\overline{CAS}$ Precharge	t_{CP}	5	-	20	-	25	-	nS	
$\overline{CAS}$ to Data (Write-Verify)	t_{CD}	-	60	-	65	-	70	nS	
Page Read/Write Cycle	t_{PC}	-	40	-	50	-	60	nS	
Output Turn-on Delay	t_{ON}	0	-	0	-	0	-	nS	
Data Setup	t_{DS}	0	-	0	-	0	-	nS	3
Address Hold Without Data Change	t_{AHW}	0	-	0	-	0	-	nS	
Column Address Hold (Write)	t_{AWR}	45	-	80	-	90	-	nS	
$\overline{CAS}$ Hold (Early-Write)	t_{CSH}	45	-	80	-	95	-	nS	
Data Hold (Early-Write)	t_{DHR}	10	-	80	-	90	-	nS	
Write Command Hold (Ref. $\overline{RAS}$)	t_{WCR}	45	-	80	-	95	-	nS	
$\overline{RAS}$ to $\overline{W}$ Delay (Read/Mod/Write)	t_{RWD}	80	-	100	-	120	-	nS	
$\overline{W}$ High to Data (Write-Verify)	t_{WHD}	-	13	-	15	-	20	nS	
Write Precharge	t_{WT}	5	-	5	-	5	-	nS	
Column Address Hold (Late Write)	t_{CAHL}	5	-	10	-	15	-	nS	3
Data-In Hold (Late-Write)	t_{DHL}	7	-	10	-	15	-	nS	3
Write-Read Cycle (Write-Verify)	t_{WC}	-	74	-	95	-	115	nS	
Write to $\overline{RAS}$ Lead	t_{RWL}	15	-	25	-	30	-	nS	

Notes:

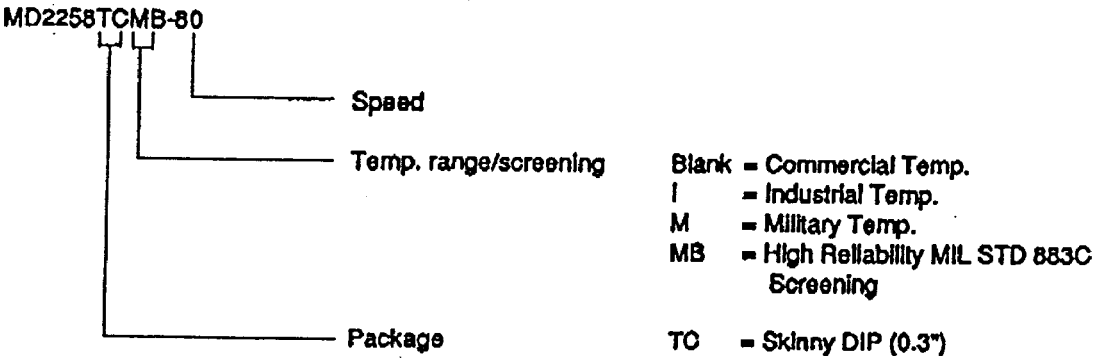
1. These values define the time it takes to achieve the open circuit condition.
2. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
3. Address and data set-up and hold times referenced to $\overline{CAS}$ (t_{ASC},t_{CAHE},t_{DS},t_{DHE}) are restrictive parameters for Early-Write operations only. Address and data set-up times referenced to $\overline{WE}$ (t_{ASC},t_{CAHL},t_{DS},t_{DHL}) are restrictive parameters for Late-Write and Read-Modify-Write cycle operations only.
4. t_{WCS},t_{CWD} and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify Write cycles only. If t_{WCS} is greater than or equal to t_{WCS} (min.), the cycle is an Early-Write cycle and data will remain open circuit unless $\overline{WE}$ goes high while $\overline{CAS}$ and $\overline{RAS}$ are both low. If t_{WCS} is greater than or equal to t_{WCS} (min.), t_{CWD} is greater than or equal to t_{CWD} (min.) and t_{AA} is greater than or equal to t_{AA} (min.), the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out is indeterminate at access time and remains so until either $\overline{CAS}$ or $\overline{WE}$ returns to V_{IH}.
5. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time is measured between V_{IH} (max.) and V_{IL} (min.).
6. 3nS rise and fall times (t_T) are used for cycle time specifications.

Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-In Electrical	Per Applicable device Specifications at Ta = +25°C (optional)	100%
Burn-In	Method 1015, Codition D, Ta = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-In at Ta=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information



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