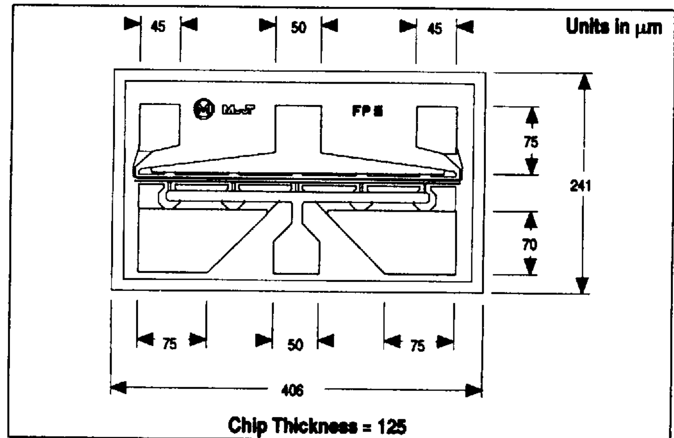
MICROWAVE TECHNOLOGY

MwT-5

26 GHz High Gain Dual GateGaAs FET



- 10.5 dB GAIN IN 6-18 GHz BALANCED CIRCUIT
- +14 dBm P1dB IN 6-18 GHz BALANCED CIRCUIT
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- DIAMOND-LIKE CARBON (DLC) PASSIVATION
- HIGH POWER ADDED EFFICIENCY
- 2 X 300 MICRON GATE WIDTH

DESCRIPTION

The MwT-5 is a dual gate GaAs MESFET device whose nominal quarter-micron gate length and 300 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 26 GHz frequency range. The straight gate geometry of the MwT-5 makes it equally effective for either wideband (ex. 2 to 26 GHz) or narrow-band applications (ex. 2.0 to 2.6 GHz). The chip is produced using MwT's reliable metal system and all devices are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for durability with no degradation in performance. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MwT-5 SG MIN	MwT-5 SG TYP	MwT-5 SG MAX	MwT-5 HG MIN	MwT-5 HG TYP	MwT-5 HG MAX
SSG	Small Signal Gain VDS=6.0V IDS=0.5 x IDSS	6-18 Bal.		9.0	9.5		10.0	10.5	
		12 GHz	dB	11.0	12.0		12.0	13.0	
P1dB	Output Power at 1dB Compression Point VDS=6.0V IDS=0.5 x IDSS	6-18 Bal.		13.0	15.0		15.0	18.0	
		12 GHz	dBm	13.0	15.0		15.0	18.0	
NF	Noise Figure VDS=6.0V IDS=30mA	6-18 Bal.			6.0			6.0	
		12 GHz	dB		4.0			3.5	
GA	Associated Gain at NF VDS=6.0V IDS=30mA	12 GHz	dB		10			11	
IDSS	Recommended IDSS Range for Optimum P1dB		mA		35-70			55-90	

AVAILABLE IN CHIP FORM ONLY

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MwT MicroWave Technology

DC SPECIFICATIONS AT Ta = 25 °C

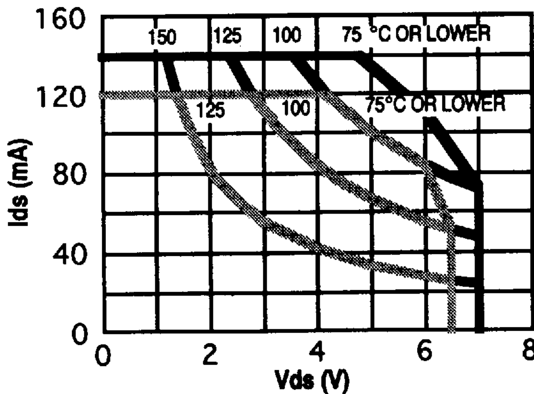
SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Idss	Saturated Drain Current Vds=4.0 V VG1S=VG2S=0.0 V	mA	30		110
Gm	Transconductance Vds=2.0 V VG2S=0.0 V IDS=50%IDSS	mS	23	40	
Vp	Pinch-off Voltage Vds=3.0 V VG2S=0.0 V IDS=2.0mA	V		-2.0	-4.5
BVGSO	Gate-to-Source & Gate 2 Breakdown Voltage IG1=-0.4mA, VG2S=0.0 V, IDS=0.0mA	V	-5.0	-8.0	
BVGDO	Gate2-to-Drain Breakdown Voltage IG2D=-0.4mA, IG1=IS=0.0mA	V	-7.0	-10.0	
Rth	Thermal Resistance MwT-5 Chip	°C/W		150	

MAXIMUM RATINGS AT Ta = 25 ° C

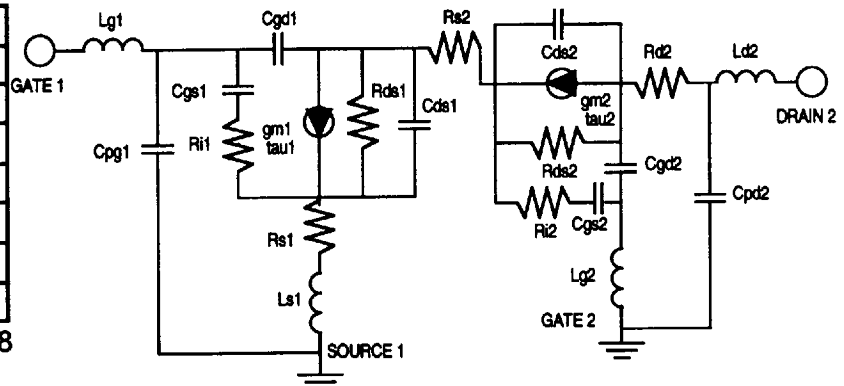
SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	95	145

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

SAFE OPERATING LIMITS vs. Case Temperature



DEVICE EQUIVALENT CIRCUIT MODEL

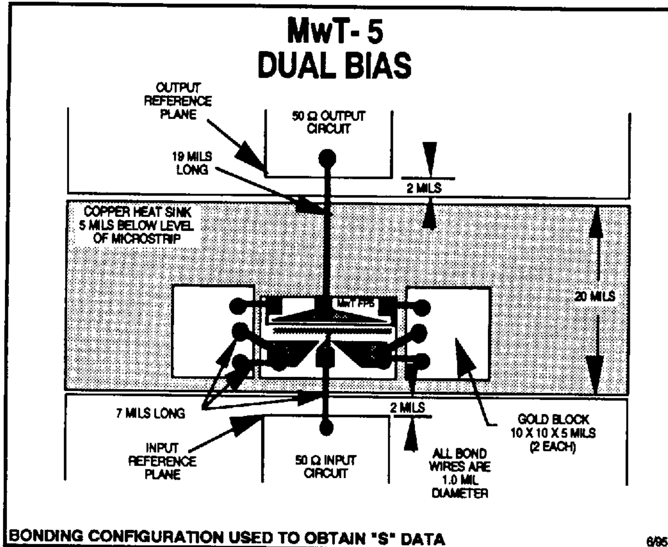


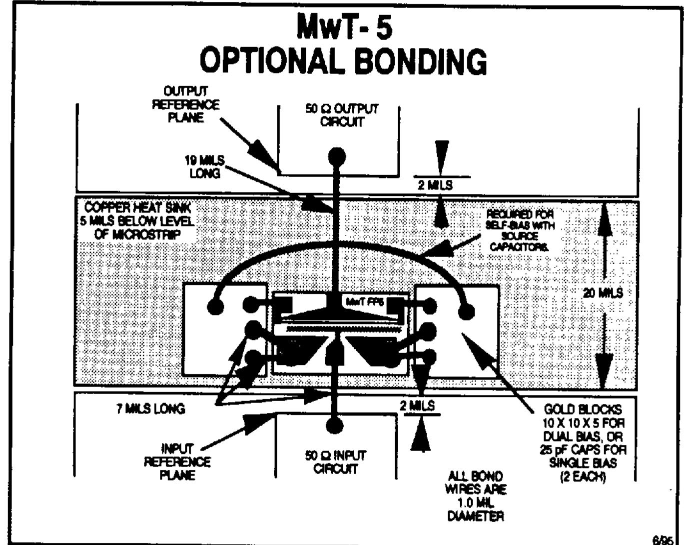
PARAMETER (1)		VALUE
Gate Bond Wire Inductance	Lg	.173 nH
Gate Pad Capacitance	Cpg	.01 pF
Gate-Source Capacitance	Cgs	.159 pF
Channel Resistance	Ri	4.37 Ω
Gate-Drain Capacitance	Cgd	.105 pF
Transconductance	gm	44 mS
Transit time	tau	2.0 psec
Source Resistance	Rs	0.7 Ω
Source Inductance	Ls	.04 nH
Drain-Source Resistance	Rds	100 Ω
Drain-Source Capacitance	Cds	.01 pF

PARAMETER (2)		VALUE
Gate Bond Wire Inductance	Lg	.120 nH
Gate-Source Capacitance	Cgs	.166 pF
Channel Resistance	Ri	5.7 Ω
Gate-Drain Capacitance	Cgd	.056 pF
Transconductance	gm	52 mS
Transit Time	tau	2.0 psec
Source Resistance	Rs	3.0 Ω
Drain-Source Resistance	Rds	205 Ω
Drain-Source Capacitance	Cds	.01 pF
Drain Resistance	Rd	4.3 Ω
Drain Bond Wire Inductance	Ld	.253 nH
Drain Pad Capacitance	pd	.01 pF

RECOMMENDED ASSEMBLY CONFIGURATION

Shown below is the assembly and bonding configuration used for S-Parameter measurements of the MwT-5 chip. This configuration is recommended for optimum performance. For single-bias applications the gold blocks may be replaced by capacitors. An additional interconnecting bond would then be required. Contact MwT for additional applications information.





BIN SELECTION

Every MwT-5 wafer has been probed for Idss and the data stored on computer disk. Customers may select from Idss values in any of 16 current bins, as shown below, to insure consistent performance in their circuit. The shaded bins are typically available in smaller quantity and caution is advised before designing these bins into high production applications. MwT's "Smart Wafer Picker" reads the stored Idss Data from the disk and devices from customer selected bins are quickly and automatically picked from the wafer and loaded into shipping containers.

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
IDSS (mA)	30-35	35-40	40-45	45-50	50-55	55-60	60-65	65-70	70-75	75-80	80-85	85-90	90-95	95-100	100-105	105-110

BIN ACCURACY

Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ after it has been attached to a proper heat sink and tested in an RF or DC circuit.

Because of the aforementioned effects, the IDSS distribution may deviate as much as +/- 1 bin within the range identified on the label of each die shipping container, and +/- 2 bins within the selected range.

TYPICAL COMMON SOURCE SCATTERING PARAMETERS

MwT-5 CHIP: VDS = 6.0 V, IDS = 0.6 IDSS = 35 mA

FREQUENCY (MHz)	S11 MAG	S11 ANG	S21 MAG	S21 ANG	S12 MAG	S12 ANG	S22 MAG	S22 ANG
1000	.995	-13.0	3.425	166.9	.005	81.4	.933	-5.1
2000	.981	-25.7	3.375	153.9	.009	72.9	.929	-10.2
3000	.960	-38.2	3.297	141.2	.013	64.7	.924	-15.2
4000	.934	-50.2	3.200	129.0	.016	57.0	.919	-20.2
5000	.906	-61.6	3.092	117.1	.018	49.7	.913	-25.1
6000	.877	-72.6	2.980	105.6	.020	42.9	.908	-30.0
7000	.848	-82.9	2.870	94.6	.022	36.6	.905	-35.0
8000	.822	-92.7	2.766	83.9	.022	30.9	.903	-40.2
9000	.799	-102.0	2.670	73.6	.022	25.6	.903	-45.4
10000	.780	-110.7	2.584	63.5	.021	21.0	.905	-50.9
12000	.751	-126.8	2.440	43.8	.017	14.3	.918	-62.8
14000	.736	-141.2	2.331	24.2	.012	16.1	.942	-76.1
16000	.734	-154.2	2.247	4.4	.007	58.9	.978	-91.3
18000	.744	-166.0	2.172	-16.3	.015	107.2	1.027	-108.5
20000	.766	-177.0	2.086	-38.1	.030	108.4	1.085	-127.7
22000	.794	172.4	1.963	-61.0	.048	98.7	1.139	-148.6
24000	.824	162.1	1.789	-84.8	.067	85.5	1.176	-170.2
26000	.848	152.1	1.569	-108.4	.084	71.4	1.183	168.8

DEVICE HANDLING PROCEDURE

1) Open package in clean room environment only.
2) GaAs FETs are sensitive to electrostatic discharge. Precautions should be taken in handling, die attachment, and bonding to assure that Maximum Ratings are not exceeded as a result of electrical discharge.
3) Chips have been cleaned and are ready for die attachment. DO NOT attempt to re-clean.
4) Assembly should be performed with parts no hotter than 300° C. All circuit components (such as resistors and capacitors) should be assembled completely before the FET is die attached. Assembly should be performed as quickly as possible. In general, no chip should be left at 300°C for over 2 minutes.
5) Die attach with clean AuSn alloy under forming gas at 280 to 300° C. Scrub chip down with tweezers. Thermal resistance is critically dependent on this operation.
6) Thermasonic wedge bonding is recommended. A .0015 in. bond flat wedge at 125 to 150° C should be used with a heater stage temperature of 200 to 225° C. Apply 15 to 20 grams of bond force to .001 in. diameter gold wire with an elongation of 2 to 5%.
7) Store in a clean, dry, inert environment such as nitrogen at room temperature.
8) CAUTION: Handling of chips other than as specified above may cause permanent damage.