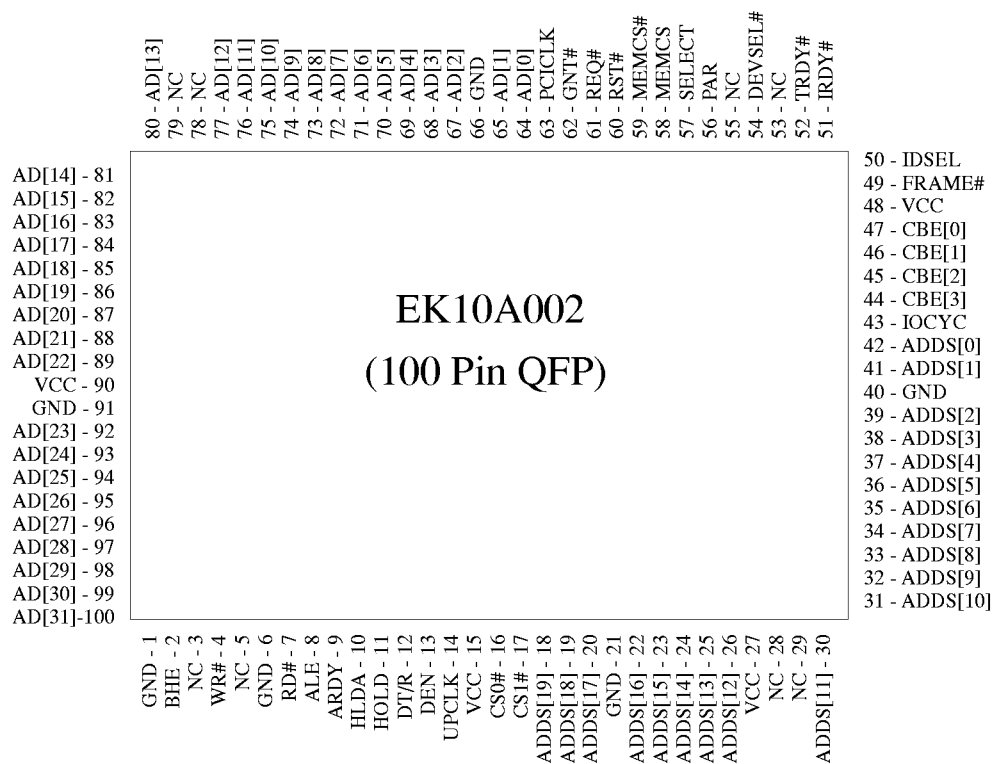


PCI/ISA Bridge Controller

Features

- Provide an interface between AMD80C186/186EM mP and Digital Semiconductor 21143 PCI device
- Single Word FIFO for accessing mP data
- Double Word FIFO for accessing Digital 21143 data
- Support memory burst read / write cycles
- Parity bit generated for address/data output, not checked on address/data input
- For unspecified functions, refer to PCI Local Bus Specification, Revision 2.0, and Revision 2.1
- Support Byte, Word and Double Word write/read command to access PCI device.
- Function as PCI master or target through automatic switching.
- 100 pin PQFP package

Pin Assignment



PIN DESCRIPTION

Reference to PCI Local Bus Specification and AMD80C186/186EM specification

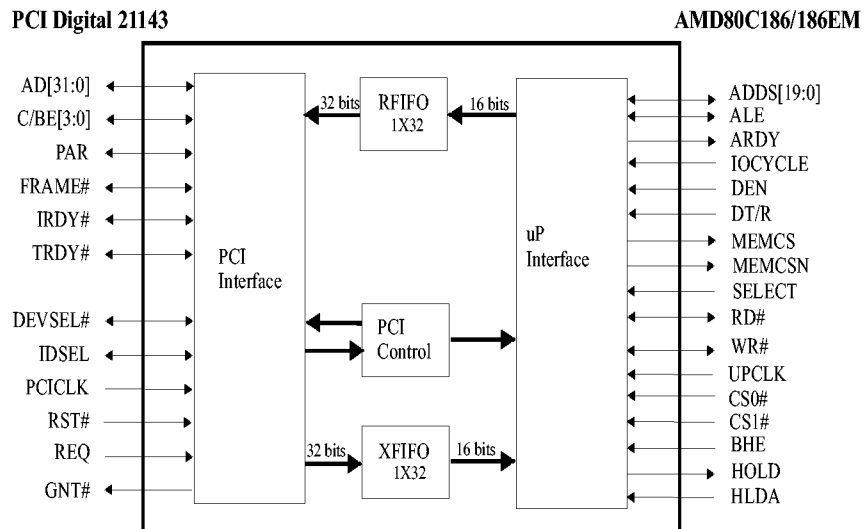
NO.	Symbol	I/O	Function
PCI interface			
44- 47	C/BE[3:0]	I/O	The Command/Byte Enable bus is driven by the master to indicate the byte to be transferred in the currently addressed doubleword and data paths to be used to transfer the data.
49	FRAME#	I/O	Cycle Frame is driven by the master, it indicates the start and duration of the transaction.
50	IDSEL	O	Initialization Device Select activates the PCI device during an access to one of the device's configuration registers.
51	IRDY#	I/O	Initiator Ready is driven by bus master.
52	TRDY#	I/O	Target Ready is driven by the currently addressed target.
54	DEVSEL#	I/O	Device Select is asserted by the target of the current bus access.
56	PAR	I/O	Even parity signal, PAR is set by the master one clock after the completion of an address phase (by Frame#) or data phase (by IRDY#) .
60	RST#	I	Power on Reset. When asserted, the reset signal forces all registers to an initial state.
61	REQ#	I	This indicates to the arbitrator that this agent desires use of the bus. Every master has its own GNT and REQ signal. (see Note.1)
62	GNT#	O	This indicates to the agent that access to the bus has been granted.
63	PCICLK	I	PCI system clock at 33MHz.
64-65,67-77, 80-89,92-100	AD[31:0]	I/O	AD[31:0] carries address and data in sequence
AMD Interface			
2	BHE	I	Byte High Enable, BHE is used to select command is Double word / word transfer table.
4	WR#	I/O	Write strobe. This pin indicates to EK10A002 that the data on the bus is to be written to it. (see Note. 1)
7	RD#	I/O	Read strobe. This pin indicates to EK10A002 that the μ P is performing a read cycle. (see Note. 1)
8	ALE	I/O	Address Latch Enable. (see Note. 2)
9	ARDY	O	When set HIGH, this pin indicates to the μ P that the FIFO data in EK10A002 is ready.
10	HLDA	I	The AMD80C186 generate HLDA (HIGH) in response to a HOLD request.
11	HOLD	O	The hold input is active HIGH. HOLD indicates that another bus master is requesting the local bus.
12	DT/R	I	Data Transmit or Receive. This pin indicates which direction data should flow through an external data-bus transceiver. When DT/R is asserted high , the μ P transmits data. When this pin is deasserted low, the μ P receives data. (see Note. 1)
13	DEN	I	Data Enable asserted low during a μ P read/write cycle. (see Note.1)
14	μ PCLK	I	AMD μ P clock
16	CS0#	I	CS0# is an active LOW select strobe input. When μ P does read / write, CS0# must be asserted.

NO.	Symbol	I/O	Function
AMD interface			
17	CS1#	I	CS1# is an active LOW select strobe input.
43	IOCYCLE	I	Setting μ P to do I/O read / write cycle or PCI configuration cycle.
57	SELECT	I	When SELECT=0, use AMD clock. for AMD186 Interface When SELECT=1, use PCI clock. (see Note.1)
58	MEMCS	O/T	Memory chip selected enable, pin HIGH active.
59	MEMCS#	O/T	Memory chip selected enable, pin LOW active.
41-42,30-39,22-26 18-20	ADDS[19:0]	I/O	ADDS[19:0] carries address and data in sequence
Others			
15-27,48,90	Vcc	I	Power 5V
1,6,21,40,66,91	GND	I	Ground
3, 5,28,29 53,55,78,79	NC		No connect

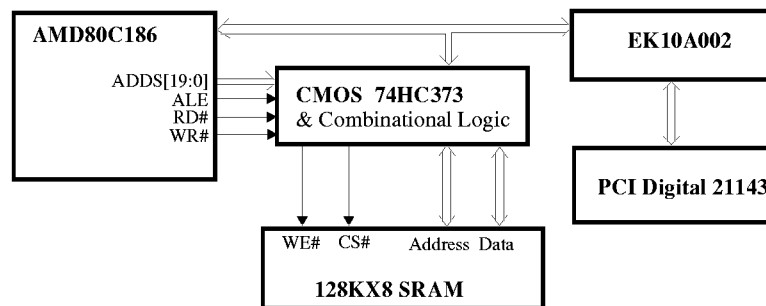
Note.1 : Internal pull up register is 50K.

Note.2 : Internal pull down register is 50K.

Block Diagram



Application Block Diagram



Operation Modes

PCI Cycle	IOCYCLE	WR	RD	Timing Diagram
Configuration Read	0	1	0	C/BE="A", DS="1", see Fig.1
Configuration Write	0	0	1	C/BE="B", DS="1", see Fig.2
I/O Read	1	1	0	C/BE="2", DS="0", see Fig.1
I/O Write	1	0	1	C/BE="3", DS="0", see Fig.2

1.Configuration : (IOCYCLE =0)

When IOCYCLE = 0 ,uP writes/reads command to/from EK10A002. It activates a PCI configuration read/write cycle with respect to Digital Semiconductor 21143 through EK10A002.

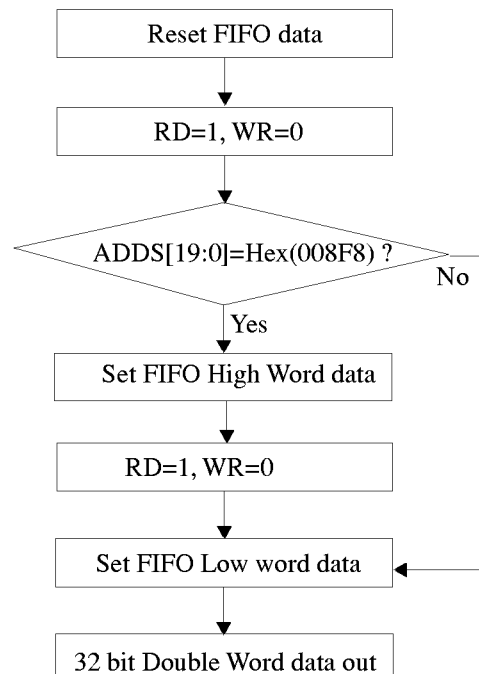
2.I/O OPERATION : (IOCYCLE = 1)

If RD=0, EK10A002 generates read command to Digital Semiconductor 21143 to start a PCI I/O read cycle .

If WR=0,EK10A002 generates write command to Digital Semiconductor 21143 to start a PCI I/O write cycle.

3.Double Word write operation

This is a special mode in which the high word data in the FIFO of EK10A002 can be written to mP in either a Configuration or an I/O operation. The following flow chart depicts this access sequence .



4.For detail of operation please refer to PCI Local Bus specification.

5.PCI Master/Target switching, EK10A002, according to REQ signal and mP HLDA signal , are asserted.

Fig.1 AMD186/186EM Read Cycle

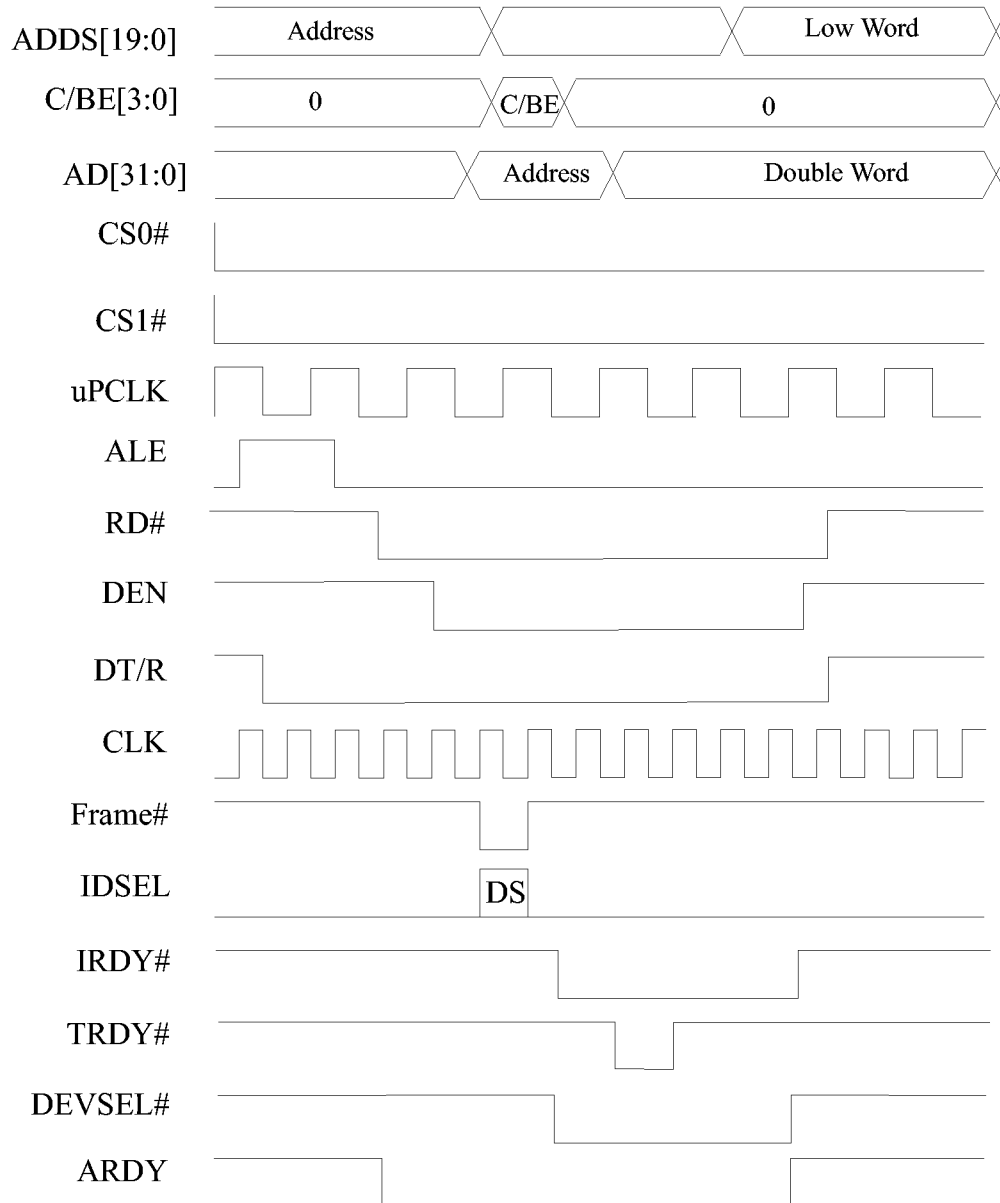


Fig.2 AMD186/186EM Write Cycle

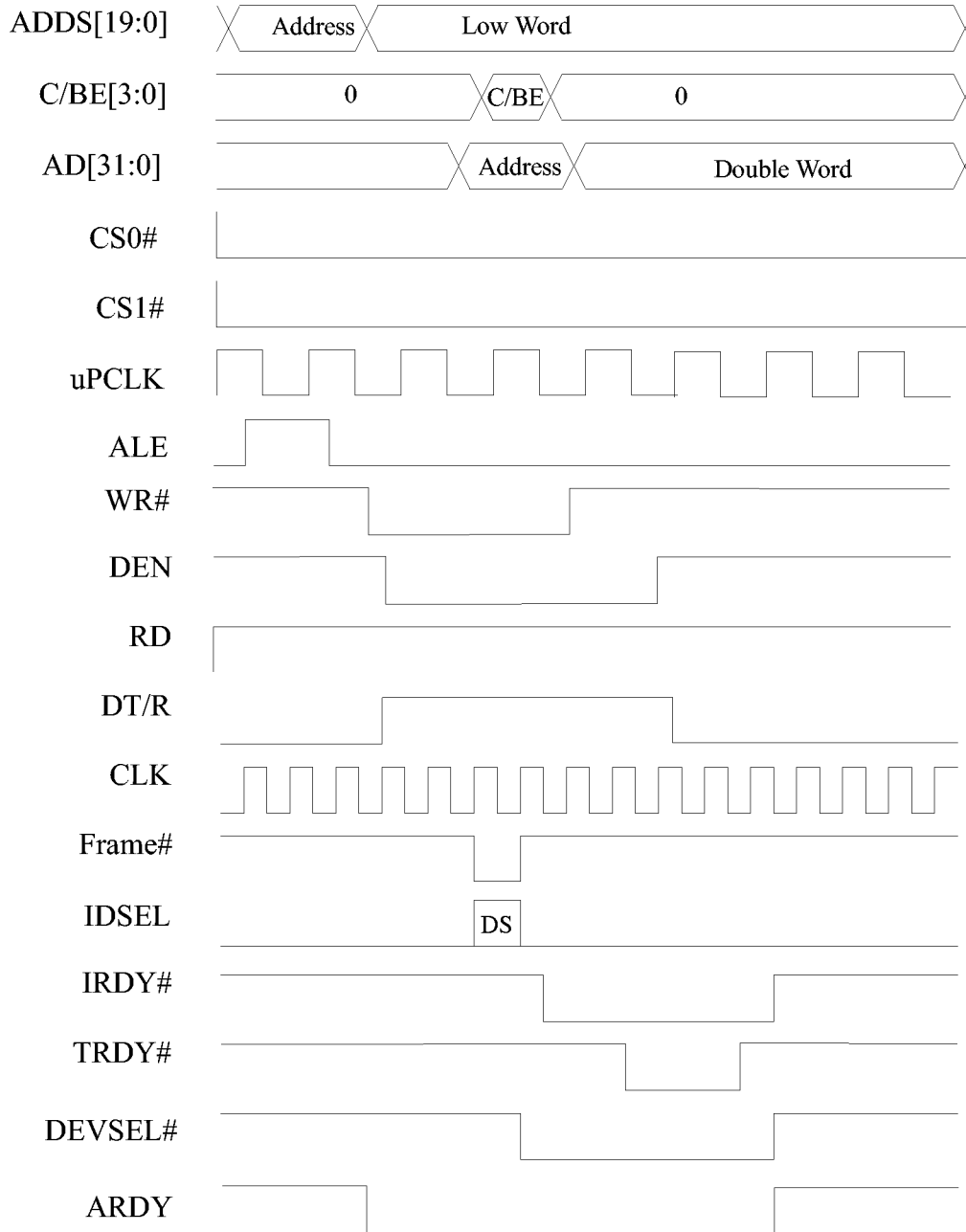


Fig.3 Memory Read Cycle

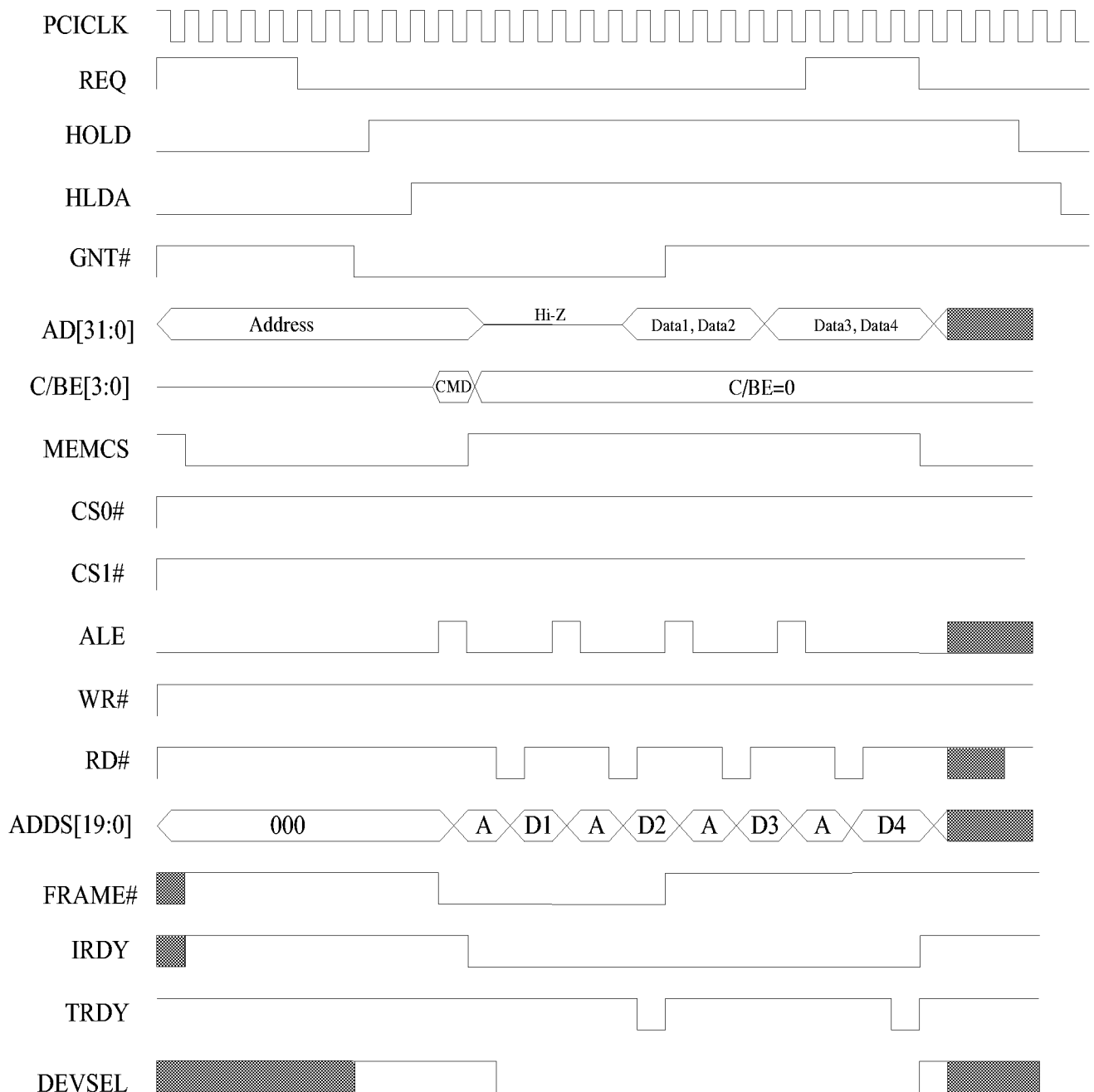


Fig.4 Memory Write Cycle

