

Recent Additions

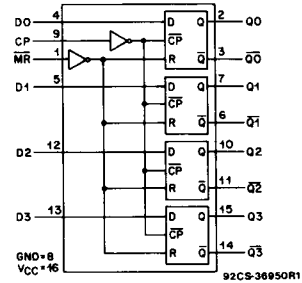
CD54AC175/3A

CD54ACT175/3A

Quad D Flip-Flop with Reset

The RCA CD54AC175 and CD54ACT175 are quad D flip-flops with reset that utilize the new RCA ADVANCED CMOS LOGIC technology. Information at the D input is transferred to the Q and \bar{Q} outputs on the positive-going edge of the clock pulse. All four flip-flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a LOW logic level independent of the clock.

The CD54AC/ACT175 are supplied in 16-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM

Package Specifications

(See Section 11, Fig. 11)

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS	
				+25		-55 to +125			
				MIN.	MAX.	MIN.	MAX.		
Quiescent Supply Current (MSI)	I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
D_n	0.58
\overline{MR}	0.67
CP	0.92

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections

Identical to CD54HC/HCT175/3A, page 5-78.

Recent Additions

CD54AC175/3A

CD54ACT175/3A

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V _{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Q, \bar{Q}	t_{PLH}	1.5	—	153	ns
	t_{PHL}	3.3*	3.1	17.1	
		5†	2.1	12.2•	
\overline{MR} to Q, \bar{Q}	t_{PLH}	1.5	—	169	ns
	t_{PHL}	3.3	3.5	18.9	
		5	2.3	13.5•	
Power Dissipation Capacitance	C _{PD} §	—			pF
Input Capacitance	C _I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V _{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: CP to Q, \bar{Q}	t_{PLH}	5†	2.3	13.5•	ns
	t_{PHL}	5	2.5	14.9•	
Power Dissipation Capacitance	C _{PD} §	—			pF
Input Capacitance	C _I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per flip-flop.

For AC, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$

For ACT, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

(Limits with black dots (•) are tested 100%.)

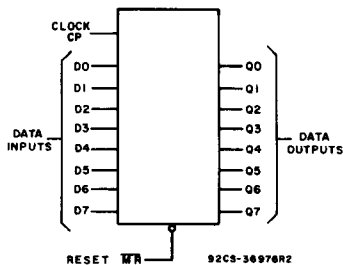
CD54AC273/3A

CD54ACT273/3A

Octal D Flip-Flop with Reset

The RCA CD54AC273 and CD54ACT273 are octal D flip-flops with reset that utilize the new RCA ADVANCED CMOS LOGIC technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and a common reset (\overline{MR}). Resetting is accomplished by a low-voltage level independent of the clock.

The CD54AC273 and CD54ACT273 are supplied in 20-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM

Package Specifications

(See Section 11, Fig. 13)