BURR-BROWN®

ADC674A/883B SERIES

ADC674ASD/883B ADC674ATD/883B

REVISION NONE
FEBRUARY, 1989

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE**
- **IMPROVED PERFORMANCE SECOND SOURCE FOR 674A-TYPE A/D CONVERTERS**
  Conversion Time: 15µs max
  Bus Access Time: 150ns max
  A_0 Input: Bus Contention During Read Operation Eliminated
- **28-PIN HERMETIC CERAMIC DIP**
- **FULLY SPECIFIED FOR OPERATION ON ±12V or ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE: –55°C to +125°C**

DESCRIPTION

The ADC674A/883B is a 12-bit, successive approximation, analog-to-digital converter utilizing state-of-the-art CMOS and laser-trimmed bipolar dice custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 15µs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC674A/883B requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin hermetic side-brazed ceramic DIP.

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PDS-917

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR

MICROPROCESSOR-COMPATIBLE, ANALOG-TO-DIGITAL CONVERTER

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a microprocessor-compatible, analog-to-digital converter.

1.2 Part Number. The complete part number is shown below.

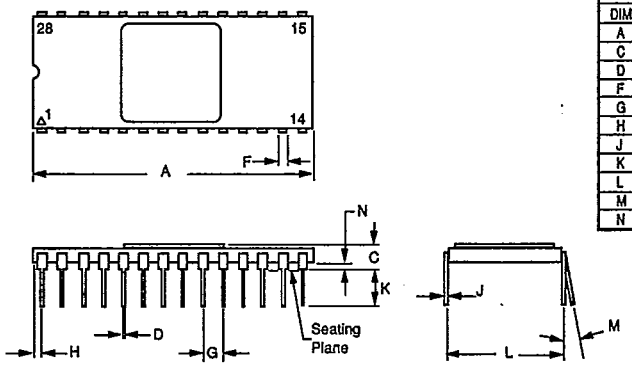
ADC674A	T	D	/883B
Basic Model Number	Grade (see 1.2.1)	Package (see 1.2.3)	Hi-Rel Product Designator (see 1.2.2)

1.2.1 Device Type. The device is a microprocessor-compatible, analog-to-digital converter. There are two electrical performance grades, which feature specifications and testing over the Military temperature range (–55°C to +125°C). Electrical specifications and tests are shown in Tables I and II.

1.2.2 Device Class. The device class is similar to the Class B product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level available as follows:

Hi-Rel Product Designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 Class B screening, with 10% PDA, plus Quality Conformance Inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed as required by MIL-STD-883.

1.2.3 Case Outline. The case outline is D-10 (28-lead, side-brazed ceramic DIP) as defined in MIL-M-38510, Appendix C and is shown in Figure 1.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.108	.166	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

FIGURE 1. Case Outline.

T-51-10-12

1.2.4 Absolute Maximum Ratings.

V_{CC} to Digital Common	0 to +16.5V
V_{EE} to Digital Common	0 to –16.5V
V_{LOGIC} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	–0.5V to V_{LOGIC} +0.5V
Analog Inputs (Ref In, BIP. OFF., $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
Ref Out	Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}; Ceramic	50°C/W

1.2.5 Recommended Operating Conditions.

Supply voltage:	V_{CC}:	+15V or +12
	V_{EE}:	–15V or –12
	V_{LOGIC}:	+5V
Ambient Temperature Range:	–55°C to +125°C	

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 — Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883 — Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail Specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, Construction, and Physical Dimensions.

3.2.1 Package, Metals, and Other Materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510.

3.2.2 Design Documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal Conductors and Internal Lead Wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead Material and Finish. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, Method 2003.

3.2.5 Die Thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical Dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein and are shown in Figure 1.

3.2.7 Circuit Diagram and Terminal Connections. The simplified circuit diagram and terminal connections are shown in Figures 2 and 3.

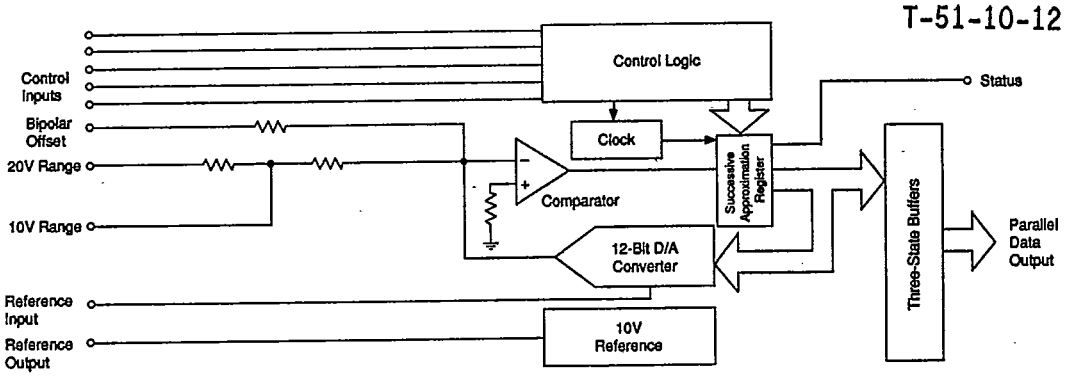


FIGURE 2. Simplified Circuit Diagram.

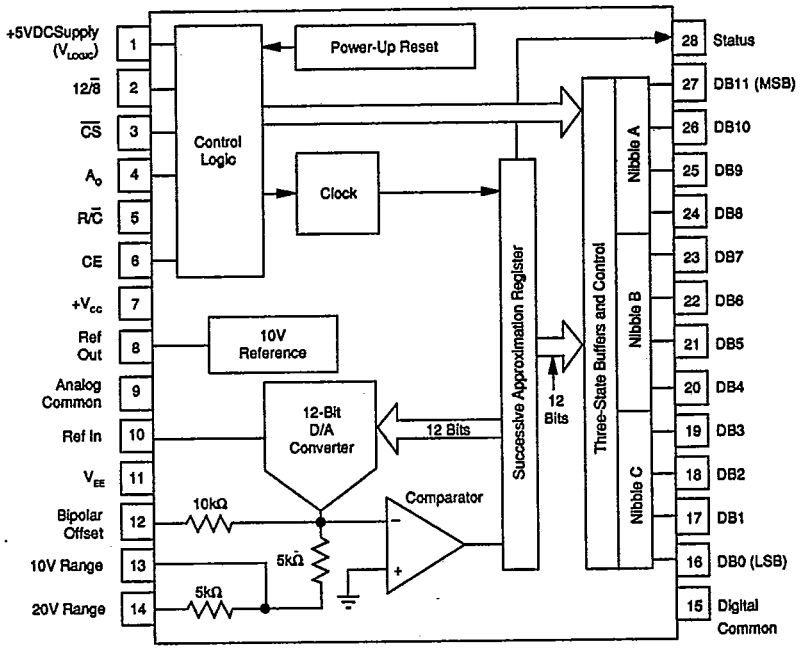


FIGURE 3. Terminal Connections.

3.2.8 Glassivation. The microcircuit die is glassivated.

3.3 Electrical Performance Characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of –55°C to +125°C unless otherwise specified.

3.4 Electrical Test Requirements. Electrical test requirements are shown in Table II. The subgroups of Table III, which constitute the minimum electrical test requirements for screening, qualification, and quality conformance inspection, are specified in Table II.

3.5 Marking. Marking is in accordance with MIL-STD-883. The following marking is placed on each microcircuit as a minimum:

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a. Part number (see paragraph 1.2).
b. Inspection lot identification code.(1)
c. Manufacturer's identification ( ).
d. Manufacturer's designating symbol (CEBS).
e. Country of origin.
f. Electrostatic sensitivity identifier (Δ).
g. Compliance identifier "C."

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanlike instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework Provisions. Rework provisions, including rebonding for the "/883B" product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the "/883B" product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and Process Change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process which may affect the performance, quality, or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, Method 5008, Class B, and as specified herein. All microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality Conformance Inspection. Quality Conformance Inspection (QCI) for the "/883B" product designation is in accordance with MIL-M-38510, and as specified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and Inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, Method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for Groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4 herein).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, Method 5008, Class B, and is conducted on all devices. The following criteria apply:

a. Interim and final test parameters are specified in Table II.
b. Burn-in test (MIL-STD-883, Method 1015) conditions:
   (1) Test condition B.
   (2) Test circuit is Figure 13.
   (3) T_A = +125°C minimum.
   (4) Test duration is 160 hours minimum.
c. Percent Defective Allowable (PDA). The PDA, for "/883B" product designation only, is 10% and includes both parametric and catastrophic failures. It is based on failures from Group A, Subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, Method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of Group A, Subgroup 1 after burn-in are used to determine the Percent Defective for each manufacturing lot, and the lot is accepted or rejected based on PDA.

(1) A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each unit.

d. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality Conformance Inspection. Groups A and B inspections of MIL-STD-883, Method 5008, Class B are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, Method 5008, Class B are performed as required by MIL-STD-883. A report of the most recent Group C and D inspections is available from Burr-Brown.

4.4.1 Group A Inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, Method 5008, and as specified in Table II herein.

4.4.2 Group B Inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, Method 5008, Class B.

4.4.3 Group C Inspection. Group C inspection consists of the subgroups and LTPD values shown in MIL-STD-883, Method 5008, and as follows:

a. Operating life test (MIL-STD-883, Method 1005) conditions:
   (1) Test condition B.
   (2) Test circuit is Figure 13.
   (3) T_A = +125°C minimum.
   (4) Test duration is 1000 hours minimum.
b. End point electrical parameters are specified in Table II.

4.4.4 Group D Inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, Method 5008.

4.4.5 Inspection of Packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of Examination and Test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced Test Methods of MIL-STD-883.

4.5.1 Voltage and Current. All voltage values given are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging Requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended Use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3. Ordering Data. The contract or purchase order should specify the following:
   a. Complete part number (see paragraph 1.2).
   b. Requirement for Certificate of Compliance, if desired.

6.4 Microcircuit Group Assignment. These microcircuits are assigned to technology Group G with a microcircuit group number of 93 as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic Sensitivity. Caution—these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

7. APPLICATION INFORMATION

7.1 Further Information. Further application information can be found in Burr-Brown's commercial data sheet for the ADC674. Request PDS-551.

TABLE I. Electrical Performance Characteristics.

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC674ASD/883B			ADC674ATD/883B			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			•	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: 0V to +10V, ±5V	4.7	5	5.3	•	•	•	kΩ
±10V, 0V to +20V	9.4	10	10.6	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2.0		+5.5	•		•	V
Logic 0	−0.5		+0.8	•		•	V
Current	−5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error: S, T Grades			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			•	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[1]							
(adjustable to zero)			±0.25			•	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error			±1			±1/2	LSB
Full-Scale Calibration Error Without Initial Adjustment[1]			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset			±5			±2.5	ppm/°C
Max Change			±2			±1	LSB
Bipolar Offset			±10			±5	ppm/°C
Max Change			±4			±2	LSB
Full-Scale Calibration			±50			±25	ppm/°C
Max Change			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
−16.5V < V_{EE} < −13.5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			•	LSB
CONVERSION TIME[4]							
8-Bit Cycle	6	8	10	•	•	•	µs
12-Bit Cycle	9	12	15	•	•	•	µs
OUTPUTS							
DIGITAL (DB11 – DB0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar		Unipolar Straight Binary (USB)					
Bipolar		Bipolar Offset Binary (BOB)					
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			•	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	•	•	•	µA
Capacitance		5			•		pF

TABLE I. Electrical Performance Characteristics.

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC674ASD/883B			ADC674ATD/883B			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	•	•	•	V
Source Current Available for External Loads[5]	2.0			•			mA
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	•		•	V
V_{EE}	−11.4		−16.5	•		•	V
V_{LOGIC}	+4.5		+5.5	•		•	V
Current: I_{CC}		3.5	5		•	•	mA
I_{EE}		15	20		•	•	mA
I_{LOGIC}		9	15		•	•	mA
Power Dissipation (±15V Supplies)		325	450		•	•	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specification	−55		+125	•		•	°C
Storage	−65		+150	•		•	°C

* Same specification as ASD.

NOTES: (1) With fixed 50Ω resistor from Ref Out to Ref In. This parameter is also adjustable to zero at +25°C (see Optional Full-Scale and Offset Adjustments section). (2) FS in this specification table means Full-Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. The term "Full-Scale" for these specifications instead of "Full-Scale Range" is used to be consistent with other vendors' 674 and 674A type specification tables. (3) Using internal reference. (4) See "Controlling the ADC674A" section for detailed information concerning digital timing. (5) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

TABLE II. Electrical Test Requirements.

MODELS	ADC674ASD/883B ADC674ATD/883B
MIL-STD-883 TEST REQUIREMENTS (HYBRID CLASS)	**SUBGROUPS**
Interim electrical parameters (preburn-in, Method 5008)	1
Final electrical test parameters (Method 5008)	1*, 2, 3, 4*, 5, 6
Group A test requirements (Method 5008)	1, 2,3, 4, 5, 6
Groups C and D end point electrical test (Method 5008)	1, 4

* PDA applies to subgroups 1 and 4.

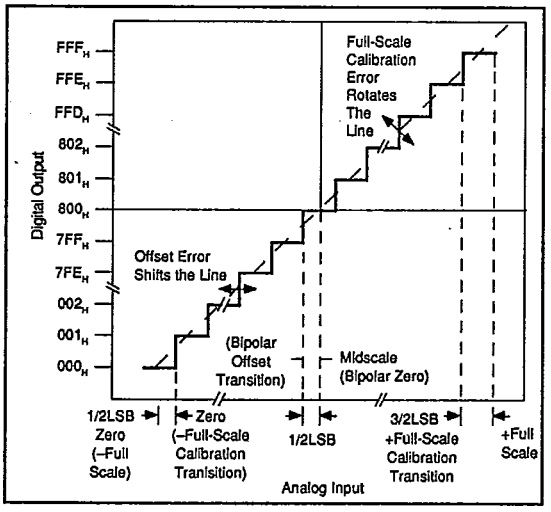

FIGURE 4. ADC674A Transfer Characteristic Terminology.

TABLE III. Group A Inspection.

			ADC674ASD		ADC674ATD		
SUBGROUP	PARAMETERS	CONDITIONS	MIN	MAX	MIN	MAX	UNITS
1 T_A = +25°C	Power Dissipation	±15V Supplies		450		450	mW
	Input Resistance	10V Span	4.7	5.3	4.7	5.3	kΩ
		20V Span	9.4	10.6	9.4	10.6	kΩ
	Reference Voltage		+9.9	+10.1	+9.9	+10.1	V
	I_{LIN} Logic Input Current		−0.5	+5.0	−0.5	+5.0	µA
	V_{OH} Logic Output High		+2.4		+2.4		V
	V_{OL} Logic Output Low			+0.4		+0.4	V
	3-State Output Leakage DB11 – DB0		−5.0	+5.0	−5.0	+5.0	µA
	Power Supply Currents						
	I_L			+15		+15	mA
	I_{CC}			+5		+5	mA
	I_{EE}			+20		+20	mA
	Power Supply Sensitivity	+13.5V < V_{CC} < 16.5V or +11.4V < V_{CC} < +12.6V		±2		±1	LSB
		+4.5V < V_{LOGIC} < +5.5V		±0.5		±0.5	LSB
		−16.5V < V_{EE} < −13.5V or −12.6V < V_{EE} < −11.4V		±2		±1	LSB
	Conversion Time	12-Bit Cycle	9	15	9	15	µs
2 T_A = +125°C	All test parameters, test conditions, and test limits in subgroup 2 are identical to those specified in Table III, subgroup 1.						
3 T_A = −55°C	All test parameters, test conditions, and test limits in subgroup 3 are identical to those specified in Table III, subgroup 1.						
4	Linearity Error		−1	+1	−0.5	+0.5	LSB
	Differential Non-Linearity (No Missing Codes Resolution)		11		12		LSB
	Unipolar Offset Error (Adjustable to Zero)		−2	+2	−2	+2	LSB
	Bipolar Offset Error (Adjustable to Zero)		−10	+10	−4	+4	LSB
	Full-Scale Calibration Error	Adjustable to Zero at +25°C	−0.3	+0.3	−0.3	+0.3	%FSR
5 T_A = +125°C	Unipolar Offset Drift		−2	+2	−1	+1	LSB
6 T_A = −55°C	Bipolar Offset Drift	No Adjustment at +25°C	−4	+4	−2	+2	LSB
	Full-Scale Calibration Error		−0.75	+0.75	−0.5	+0.5	%FSR
	Full-Scale Calibration Drift		−0.5	+0.5	−0.25	+0.25	%FSR

TABLE IV. Input Voltages, Transition Values, and Values.

Binary (BIN) Output		Input Voltage Range and LSB Values			
Analog Input Voltage Range	Defined As:	±10V	+5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values FFE_H to FFF_H $7FFF_H$ to 800_H 000_H to 001_H	+ Full-Scale Calibration	+10V – 3/2LSB	+5V – 3/2 LSB	+10V – 3/2LSB	+10V – 3/2LSB
	Midscale Calibration (Bipolar Offset)	0 – 1/2LSB	0 – 1/2LSB	+5V – 1/2LSB	±10V – 1/2LSB
	Zero Calibration (– Full-Scale Calibration)	−10V + 1/2LSB	−5V + 1/2LSB	0 to +1/2LSB	0 to +1/2LSB

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full-scale for bipolar operation) and plus full-scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 4).

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table IV).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

The ADC674ATD is guaranteed to have no missing codes to 12-bit resolution over its specification temperature range.

UNIPOLAR OFFSET ERROR

An ADC674A connected for unipolar operation has an analog input range of 0V to plus full-scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC674A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC674A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL-SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC674A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value of T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2SLB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC674A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter or on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common. Analog common (pin 9) typically carries +8mA.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full-scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC674A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10µF tantalum type capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC674A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48 V (5mV LSB) input range, insert a 120Ω 1% metal-film resistor in series with pin 13 for the 10.24V range, or a 240Ω 1% metal-film resistor in series with pin 14 for the 20.48V range. Offset and gain adjustments are still performed as described below. However, you must recalculate full-scale adjustment voltages proportionately. A fixed metal-film resistor can be used because the input impedance of the ADC674A is trimmed to less than ±6% of the nominal value.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC674A as shown in Figures 5 and 6 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If adjustment of unipolar offset and full-scale is not required, replace R_2 with a 50Ω, 1% metal-film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 5. Sweep the input through the endpoint transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full-scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

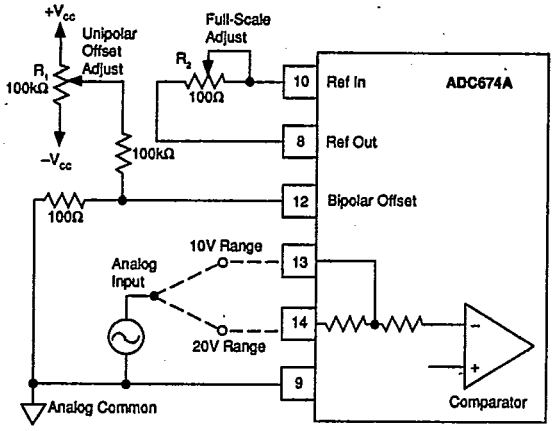

FIGURE 5. Unipolar Configuration.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal-film resistors.

If adjustments are required, connect the converter as shown in Figure 6. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R2 for DB0 to toggle ON and OFF with all other bits ON.

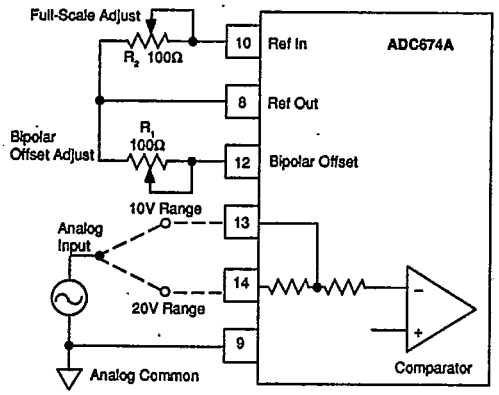

FIGURE 6. Bipolar Configuration.

TABLE V. ADC674A Control Line Functions.

DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When Short Cycle reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE VI. ADC674A Control Input Truth Table.

CE	CS	R/C	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

CONTROLLING THE ADC674A

The Burr-Brown ADC674A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting and 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table V. The control function truth table is listed in Table VI.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode, $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case, the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 7 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 8 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table VII lists timing specifications for stand-alone operation.

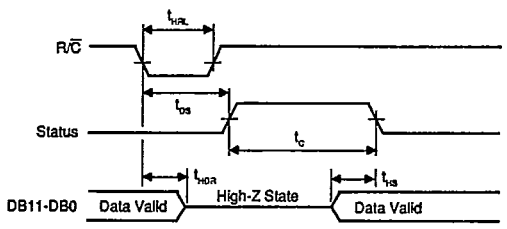

FIGURE 7. R/C Pulse Low—Outputs Enabled After Conversion.

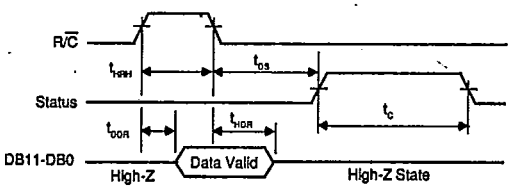

FIGURE 8. R/C Pulse High—Outputs Enabled Only While R/C is High.

TABLE VII. ADC674A Stand-Alone Mode Timing.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C Pulse Width	50			ns
t_{DS}	STS Delay from R/C			200	ns
t_{HDR}	Data Valid After R/C Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/C Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE VIII. ADC674A Timing Specifications.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	CS to CE setup	50	20		ns
t_{HSC}	CS low during CE high	50	20		ns
t_{SRC}	R/C to CE setup	50	0		ns
t_{HRC}	R/C low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time 12-bit cycle	9	12	15	µs
	8-bit cycle	6	8	10	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	CS to CE setup	50	0		ns
t_{SRR}	R/C to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	CS valid after CE low	0			ns
t_{HRR}	R/C high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid	100	300	600	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the three LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

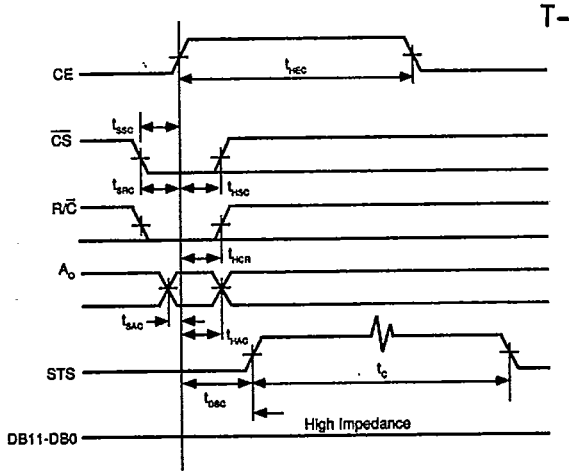

FIGURE 9. Conversion Cycle Timing.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table VI. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns before the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 9. The specifications for timing are contained in Table VIII.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time, the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion in initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 10 and Table VIII for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC674A to an 8-bit bus for transfer of data in a left-justified format is illustrated in Figure 11. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data work in two consecutive memory locations.

When A_0 is low, the byte addressed contains the eight MSBs. When A_0 is high, the byte addressed contains the four LSBs from the conversion followed by four logic zeroes which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 11. The design of the ADC674A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 12 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 750ns (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 10 for these timing relationships.

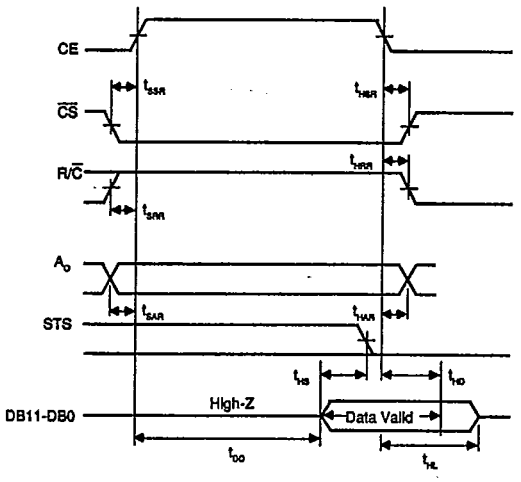

FIGURE 10. Read Cycle Timing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 11. 12-Bit Data Format for 8-Bit Systems.

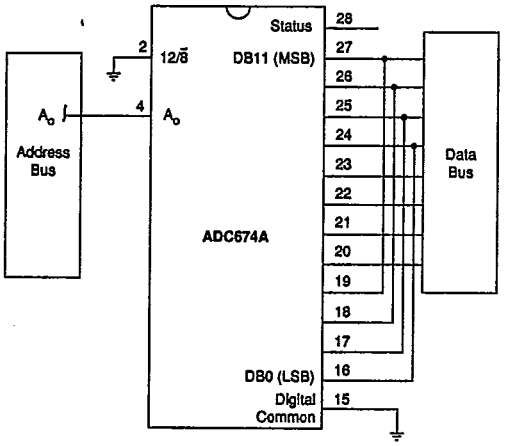

FIGURE 12. Connection to an 8-bit Bus.

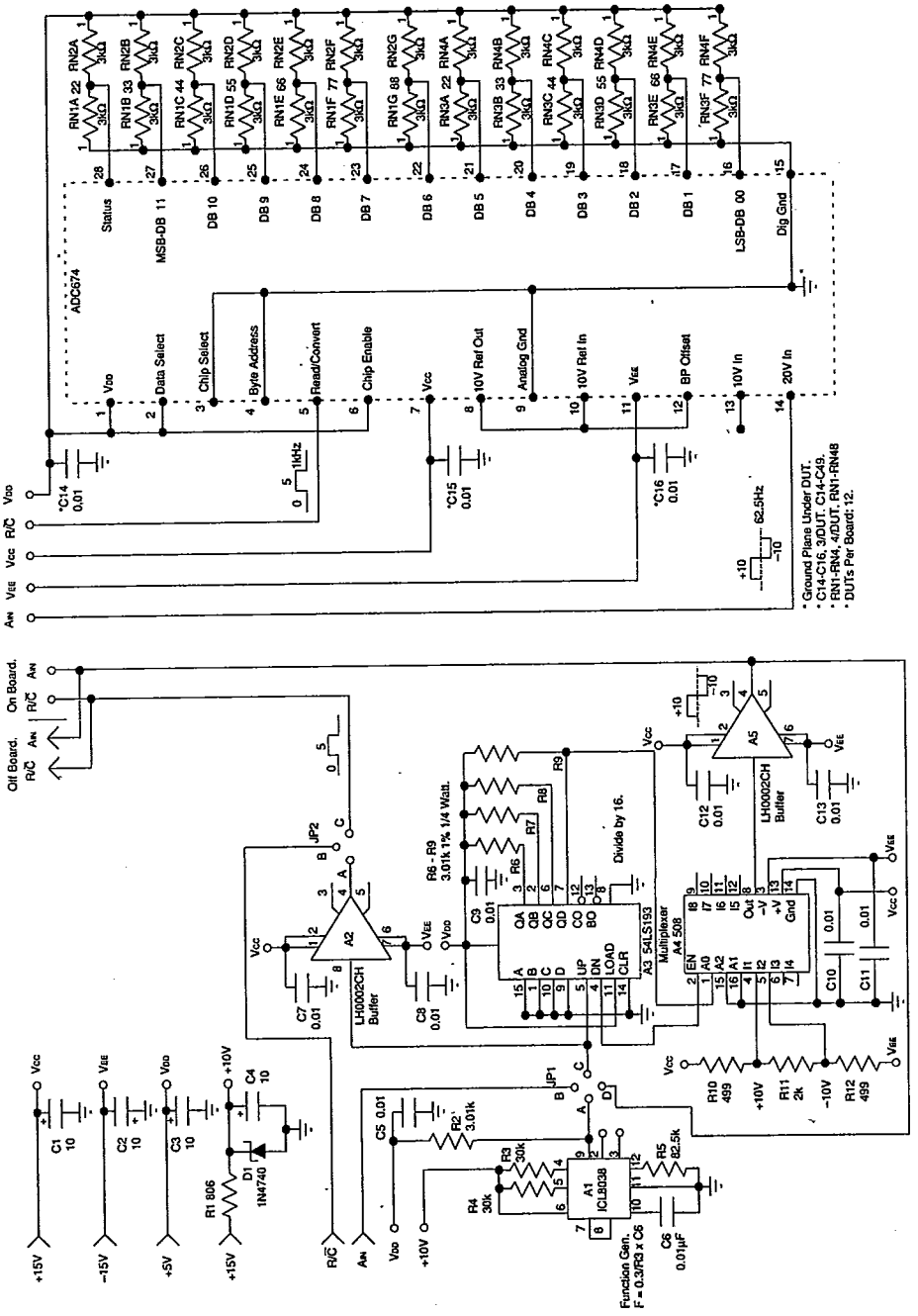

FIGURE 13. Test Circuit—Burn-in and Operating Life Test.