

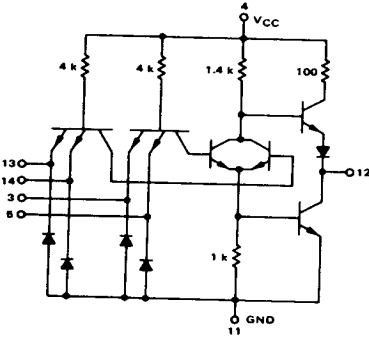
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DUAL 2-WIDE 2-INPUT
"AND-OR-INVERT" GATE

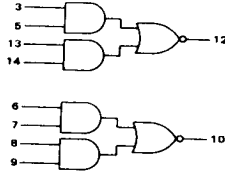
MTTL MC5400F/7400F series

MC5451F*
MC7451F*

1/2 OF CIRCUIT SHOWN



This device consists of two AND-OR-INVERT gates. Each gate is made up of two 2-input AND gates ORed together and inverted.



Positive Logic: $12 = (\overline{3 \cdot 5}) + (\overline{13 \cdot 14})$

Negative Logic: $12 = (\overline{3 + 5}) \cdot (\overline{13 + 14})$

Input Loading Factor = 1

Output Loading Factor = 10

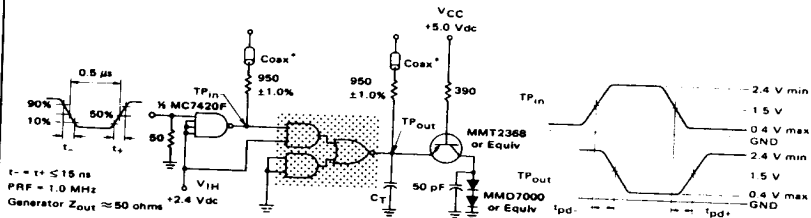
Total Power Dissipation = 28 mW typ/pkg

Propagation Delay Time = 13 ns typ

*F suffix = TO-8B ceramic package (Case 609).
See General Information section for package outline dimensions.

SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



Ground inputs to gates not under test.

$C_T = 15 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

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