

SMC82C59AC

CMOS PROGRAMMABLE INTERRUPT CONTROLLER

- Supports 8 Levels of Interrupt
- Many Functions for Interrupt
- Low Power

DESCRIPTION

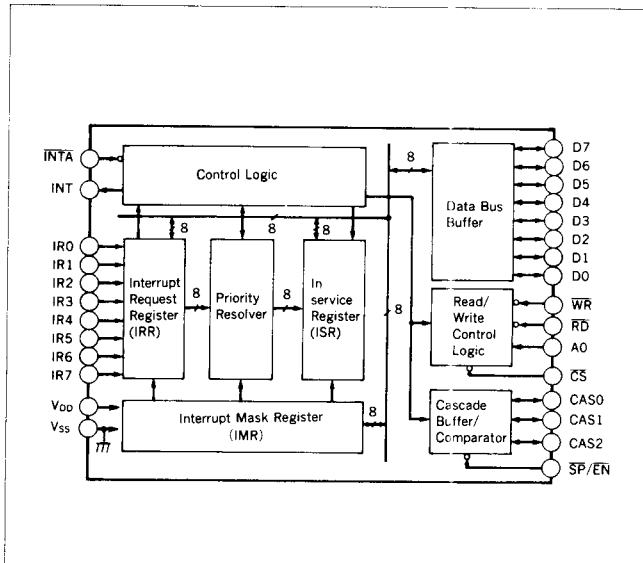
The SMC82C59AC is a CMOS Programmable Interrupt Controller. The device is designed to minimize the system software overhead required to handle multi-level interrupts. The device requires no clock inputs.

FEATURES

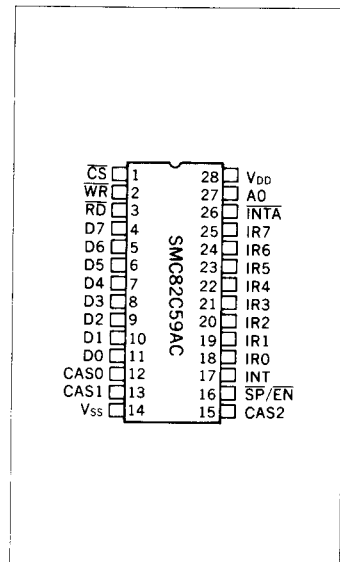
- Supports eight levels of interrupt
- Cascadable up to 64 levels
- Programmable
 - Priority
 - Mask Capability
 - Vectored Address
- Single 5V ($\pm 10\%$) power supply
- Package: 28-pin DIP
28-pin SOP*

*Under development

BLOCK DIAGRAM



PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$, $T_a=25^\circ C$)

Parameter	Symbol	Conditions	Ratings	Unit
Power-supply voltage	V_{DD}	With respect to V_{SS}	-0.3 to 7	V
Input voltage	V_I		-0.3 to $V_{DD}+0.3$	V
Output voltage	V_O		-0.3 to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	—	-20 to 75	$^\circ C$
Storage temperature	T_{stg}	—	-65 to 150	$^\circ C$
Soldering temperature and time	T_{sol}	—	260 $^\circ C$, 10s (lead)	—

■ RECOMMENDED OPERATING CONDITIONS

($T_a = -20$ to $75^\circ C$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5	5.5	V
Supply voltage	V_{SS}	—	—	0	—	V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

($T_a = -20$ to $75^\circ C$, $V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—	2	—	$V_{DD}+0.3$	V
Low-level input voltage	V_{IL}	—	-0.3	—	0.8	V
High-level output voltage	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	—	V
High-level output voltage, interrupt request output	$V_{OH(INT)}$	$I_{OH} = -100\mu A$	3.5	—	—	V
Low-level output voltage	V_{OL}	$I_{OL} = 2.2mA$	—	—	0.45	V
Standby supply current from V_{DD}	I_{DDs}	$V_{DD}=5V$, $V_I=V_{DD}$ or GND output open	—	—	10	μA
High-level input current	I_{IH}	$V_I = V_{DD}$	-10	—	10	μA
Low-level input current	I_{IL}	$V_I = 0V$	-10	—	10	μA
Off-state output current	I_{OZ}	$V_{SS} = 0$, $V_I = 0.45$ to $5.5V$	-10	—	10	μA
High-level input current, interrupt request inputs	$I_{IH(IR)}$	$V_I = V_{DD}$	—	—	10	μA
Low-level input current, interrupt request inputs	$I_{IL(IR)}$	$V_I = 0V$	-300	—	—	μA
Input capacitance	C_I	$V_{DD}=V_{SS}$, $f=1MHz$, $25mV_{rms}$, $T_a=25^\circ C$	—	—	10	pF
Input/output capacitance	$C_{I/O}$	$V_{DD}=V_{SS}$, $f=1MHz$, $25mV_{rms}$, $T_a=25^\circ C$	—	—	20	pF

● AC Electrical Characteristics

○ Timing Requirements

($T_a = -20$ to $75^\circ C$, $V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, unless otherwise noted)

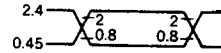
Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Write pulse width	$t_{W(W)}$	t_{WLWH}		200	—	—	ns
Address setup time before write	$t_{SU(A,W)}$	t_{AHWL}		0	—	—	ns
Address hold time after write	$t_{H(W,A)}$	t_{WHAX}		0	—	—	ns
Data setup time before write	$t_{SU(DQ,W)}$	t_{DVWH}		100	—	—	ns
Data hold time after write	$t_{H(W,DQ)}$	t_{WDHX}		0	—	—	ns
Read pulse width	$t_{W(R)}$	t_{RIRH}		200	—	—	ns
Address setup time before read	$t_{SU(A,R)}$	t_{AHLR}		0	—	—	ns
Address hold time after read	$t_{H(R,A)}$	t_{RHAX}		0	—	—	ns
Interrupt request input width, low-level time, edge triggered mode	$t_{W(IR)}$	$t_{JI JH}$		100	—	—	ns
Cascade setup time before INTA (slave)	$t_{SU(CAS-INTA)}$	$t_{C'IAL}$		55	—	—	ns
Write recovery time	$t_{rec(W)}$	t_{WHRL}		190	—	—	ns
Read recovery time	$t_{rec(R)}$	t_{RHRL}		160	—	—	ns

● Switching Characteristics

($T_a = -20$ to 75°C , $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Data output enable time after read	$t_{PZV(R-DQ)}$	t_{RLDV}		—	—	170	ns
Data output disable time after read	$t_{PVZ(R-DQ)}$	t_{RHDZ}		10	—	100	ns
Data output enable time after address	$t_{PZV(A-DQ)}$	t_{AHDV}		—	—	200	ns
Propagation time from read to enable signal output	$t_{PHL(R-EN)}$	t_{RLEL}		—	—	125	ns
Propagation time from read to disable signal output	$t_{PLH(R-EN)}$	t_{RHEH}		—	—	150	ns
Propagation time from interrupt request input to interrupt request output	$t_{PLH(IR-INT)}$	t_{JHIH}		—	—	350	ns
Propagation time from INTA to cascade output (master)	$t_{PLV(INTA-CAS)}$	t_{IALCV}		—	—	565	ns
Data output enable time after cascade output (slave)	$t_{PZV(CAS-DQ)}$	t_{CVDV}		—	—	300	ns

- *1 INTA signal is considered read signal
 \overline{CS} signal is considered address signal
 Input pulse level 0.45 to 2.4V
 Input pulse rise time 10ns
 Input pulse fall time 10ns
 Reference level Input $V_{IH} = 2V$, $V_{IL} = 0.8V$
 Output $V_{OH} = 2V$, $V_{OL} = 0.8V$
 Load capacitance $C_L = 100\text{pF}$, where $\overline{SP}/\overline{EN}$ pin is 15pF

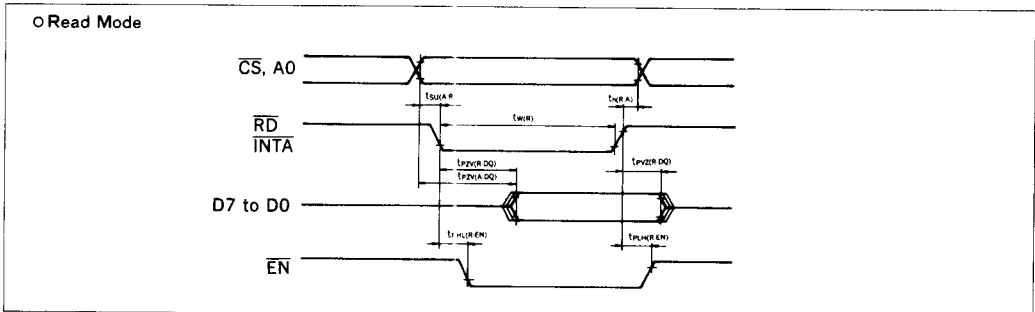
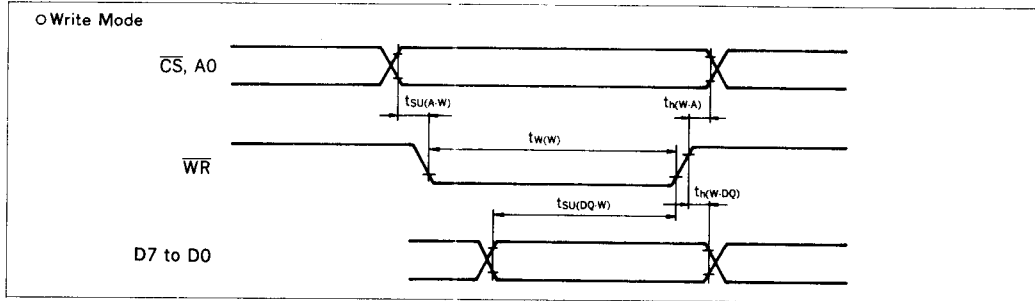


■ FUNCTIONS

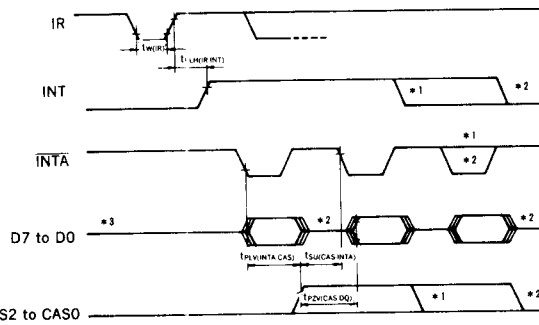
The SMC82C59AC is able to handle up to eight vectored priority interrupts for a CPU. The device is designed for real time use and thus reduces system software overhead. The priority and interrupt mask can be reconfigured as required by the system software.

When a peripheral requires servicing an interrupt is generated by the peripheral. The SMC82C59AC based on the mask and the priority of the interrupt will issue an interrupt request (INT) to the CPU. After the CPU acknowledges (\overline{INTA}) the interrupt; the SMC82C59AC can "point" the Program Counter to the service routine associated with the peripheral interrupt request. This "pointer" is a programmed vector address in the device and is released via the data bus.

● Timing Chart

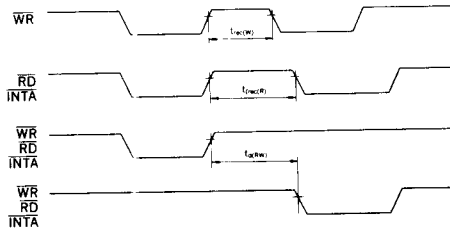


Interrupt Sequence



- *1 8086 mode
- *2 8085 mode
- *3 8086 mode is in high-impedance state, pointer is released during the next \overline{INTA} . When in single 8085 mode, data is released by all \overline{INTA} s. When master, CALL instruction is released during the first \overline{INTA} , high impedance state during the second and third \overline{INTA} . When slave, high impedance state during the first \overline{INTA} , vectored address is released during the second and third \overline{INTA} .

Other Timing



APPLICATION

The SMC82C59AC can be used as an interrupt controller for most CPUs and specifically the 80XX series microcomputers.

PACKAGE DIMENSIONS

