ADC-922

12-BIT, 3µs COMPLETE
A/D CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- **High Conversion Rate ..... ≤3µs**
- **+5 and ±12 to ±15V Operation**
- **Unipolar or Bipolar Inputs**
- **User Selectable Input Ranges**
- **On-Chip Clock**
- **High Accuracy 10.00V Reference**
- **Fast Bus Access Time 30ns**

APPLICATIONS

- **Digital Signal Processing**
- **Medical Diagnostics**
- **Avionics**
- **Process Control Equipment**

GENERAL DESCRIPTION

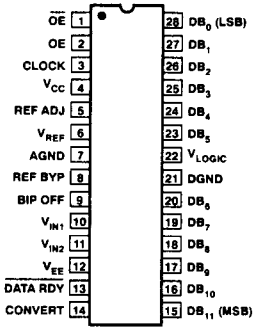
The ADC-922 is a complete, 12-bit, high-speed analog-to-digital converter that includes a precision 10V reference, unipolar and bipolar inputs and an internal clock that can be overridden externally. Input ranges are 0 to +10 or 0 to +20, ±10, and ±5 volts.

Separate CONVERT and OUTPUT ENABLE controls enable the user to access the data from the most recent conversion at any time. The CONVERT input can be synchronized with the clock to sample at precise intervals for DSP processing.

A 10.00V high-performance reference that is trimmed for voltage and temperature drift allows the designer to build high accuracy systems without the need for an external reference. The reference can be externally adjusted and has a tempco of only 5ppm/°C. A reference output is available so that several ADCs or DACs can be used in the same system and maintain tracking.

Designed in a low voltage bipolar process for improved radiation hardness and operating from ±12 to ±15 and +5V supplies, the ADC-922 dissipates less than 750mW.

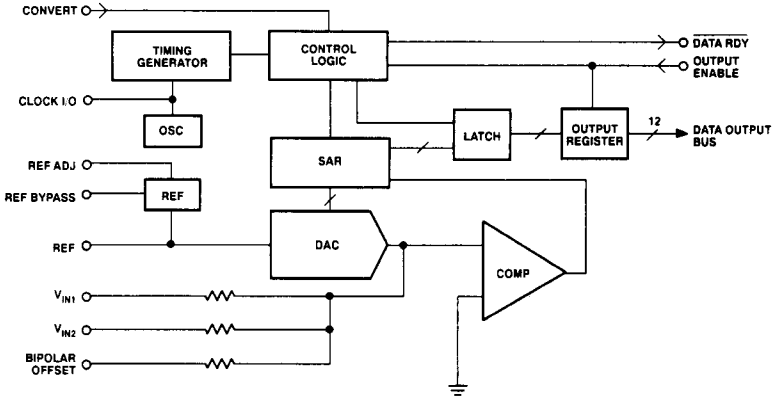
PIN CONNECTIONS



28-PIN CERDIP
(T-Suffix)

NOTE:
A 28-CONTACT LCC PACKAGE WILL BE AVAILABLE; CONTACT FACTORY FOR PINOUT.

FUNCTIONAL DIAGRAM



This preliminary product information is based on proposed specifications. Final specifications may vary. Please contact local sales office or factory for final data sheet.

ORDERING INFORMATION †

INL (LSB)	MILITARY* TEMPERATURE –55°C TO +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C TO +85°C
±1/2	ADC922AT††	ADC922ET††
±1	ADC922BT††	ADC922FT††
±1	ADC922BTC††	

* For devices processed in total compliance to MIL-STD-883, add /883 after the part number. Consult factory for 883 data sheet.

† Burn-in is available on extended industrial temperature range parts in CerDIP and plastic DIP packages. For ordering information, see PMI's Data Book.

†† For availability and burn-in information, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{CC} to AGND ..... –0.3V, +18.0V
V_{EE} to AGND ..... –0.3V, +18.0V
V_{LOGIC} to DGND ..... –0.3V, +7.0V
V_{IN1} or V_{IN2} to AGND ..... ±25V
Digital Input Voltage to DGND ..... –0.3V, V_{LOGIC} +0.3V
Digital Output Voltage to DGND..... –0.3V, +7.0V
AGND to DGND ..... ±800mV
Operating Temperature Range
ET,FT ..... –40°C to +85°C
AT, BT ..... –55°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Power Dissipation 1000mW
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
28-Pin Hermetic DIP (Z)	50	7	°C/W

NOTE:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

CAUTION:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than V_{EE} potential on any terminal except V_{REF}.
3. The digital inputs are zener protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
4. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at +12V ≤ V_{CC} ≤ 15V ±5%, –15V ≤ V_{EE} ≤ –12V, V_{LOGIC} = +5V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

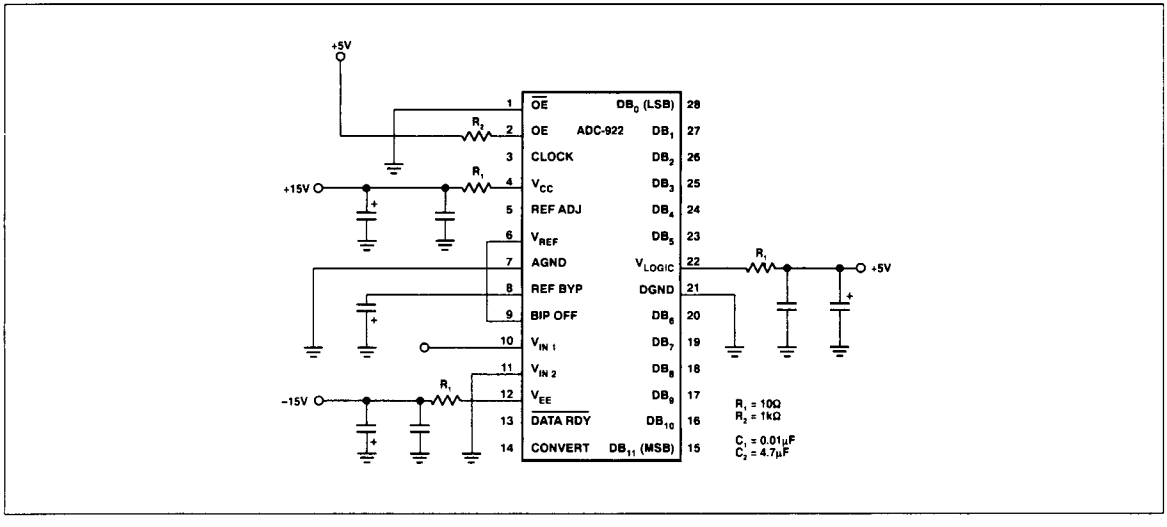
PARAMETER	SYMBOL	CONDITIONS	ADC-922 MIN	ADC-922 TYP	ADC-922 MAX	UNITS
Integral Linearity "A"	INL		–	–	±1/2	LSB
Differential Linearity "A"	DNL		–	–	±1/2	LSB
Integral Linearity "B"	INL		–	–	±1	LSB
Differential Linearity "B"	DNL		–	–	±0.9	LSB
Unipolar Offset Error			–	–	1	LSB
Gain Error			–	0.25	–	%FS
Input Resistance	R_{IN}	V_{IN1}, V_{IN2}, BIP OFF	–	–	5	kΩ
Reference Output Voltage	V_{REF}		–	10.00	–	V
Reference Output Current	I_{REF}		–	5	–	mA
Reference Tempco			–	10	–	ppm/°C
Power Supply Rejection Ratio	PSRR		–70	–	–	dB
Oscillator Frequency	f_{OSC}		–	16	–	MHz
Conversion Time	T_C		–	2	–	µs
Logic Input High Voltage	V_{INH}	T_A = +25°C	–	–	2.0	V
Logic Input Low Voltage	V_{INL}	T_A = +25°C	0.8	–	–	V
Logic Output High Voltage	V_{OH}	T_A = +25°C	2.4	–	–	V
Logic Output Low Voltage	V_{OL}	T_A = +25°C	–	–	0.45	V

ELECTRICAL CHARACTERISTICS at $+12V \le V_{CC} \le 15V \pm 5\%$, $-15V \le V_{EE} \le -12V$, $V_{LOGIC} = +5V$, $-40°C \le T_A \le +85°C$, unless otherwise noted. *Continued*

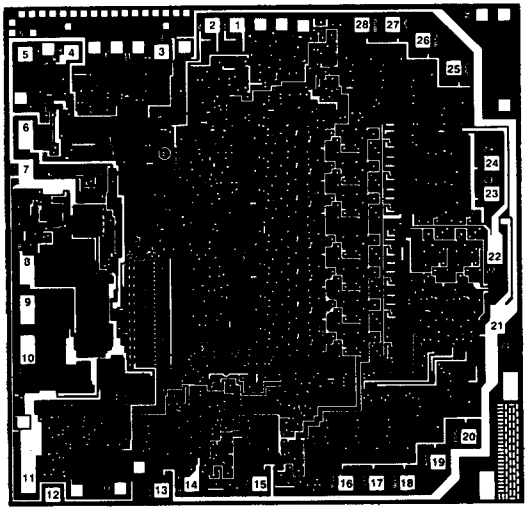
PARAMETER	SYMBOL	CONDITIONS	ADC-922 MIN	TYP	MAX	UNITS
Positive Supply Current	I_{CC}	$V_{CC} = +16.5V$	–	–	13	mA
Negative Supply Current	I_{EE}	$V_{EE} = -16.5V$	–	–	22	mA
Logic Supply Current	I_{LOGIC}	$V_{LOGIC} = +5.5V$	–	–	45	mA
Power Dissipation	P_d		–	–	750	mW
TIMING CHARACTERISTICS (Note 1)						
Output Rise Time	t_r	$Z_L = 50pF$	–	10	–	ns
Output Fall Time	t_f	$Z_L = 50pF$	–	10	–	ns
Release to High Z	t_z	$Z_L = 500\Omega$ to $+2.5V$	–	10	–	ns
Access Time	t_1		–	–	–	ns
Clock Width High	t_2		–	–	–	ns
Clock Width Low	t_3		–	–	–	ns
Output Enable Pulse Width	t_4		–	–	–	ns
Data Hold Time	t_5		–	–	–	ns
Output Enable to Data Ready	t_6		–	–	–	ns
Output Enable to Data	t_7		–	–	–	ns

NOTE:
1. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of 1.6V.

BURN-IN CIRCUIT "PROPOSED"



DICE CHARACTERISTICS



1. $\overline{OE}$
2. OE
3. CLOCK
4. V_{CC}
5. REF ADJ
6. V_{REF}
7. AGND
8. REF BYP
9. BIP OFF
10. V_{IN1}
11. V_{IN2}
12. V_{EE}
13. $\overline{DATA\ RDY}$
14. CONVERT
15. DB_{11} (MSB)
16. DB_{10}
17. DB_9
18. DB_8
19. DB_7
20. DB_6
21. DGND
22. V_{LOGIC}
23. DB_5
24. DB_4
25. DB_3
26. DB_2
27. DB_1
28. DB_0 (LSB)

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

DIE SIZE 0.168 x 0.172 inch, 28,896 sq. mils (4.267 x 4.369 mm, 18.64 sq. mm)

WAFER TEST LIMITS at V_{CC} = +15V, V_{EE} = –15V, V_{LOGIC} = +5V, V_{REF} = +10V, A_{IN} = 0V to +10V and T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-922G LIMITS	UNITS
Integral Nonlinearity	INL		±1	LSB Max
Differential Nonlinearity	DNL		±1	LSB Max
Offset Error	V_{ZSE}	Guaranteed by Design	±1	LSB Max
Gain Error	G_{FSE}		±1	LSB Max
Input Resistance	R_{IN}	V_{IN1}, V_{IN2}, BIP OFF	3.5/5	kΩ Min/Max
Logic Input High Voltage	V_{INH}		–	V Min
Logic Input Low Voltage	V_{INL}		–	V Max
Logic Input Current	I_{IN}		–	µA Max
Logic Output High Voltage	V_{OH}		–	V Min
Logic Output Low Voltage	V_{OL}		–	V Max
Positive Supply Current	I_{CC}		–	mA Max
Negative Supply Current	I_{EE}		–	mA Max
Logic Supply Current	I_{LOGIC}		–	mA Max

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

PIN DESCRIPTIONS

CLOCK: MULTIFUNCTION CLOCK INPUT/OUTPUT

This pin is connected to the internal clock oscillator. If left unconnected, the ADC internal clock will oscillate at a rate near the maximum speed. A small capacitor (internal capacitance is 10pF) connected here will slow the internal oscillator. The oscillator output voltages peaks are at about +1 and +2V, and therefore may be overridden by an externally supplied clock with standard TTL logic levels. The internal oscillator has very little drive capability, and must be amplified by a comparator if the user wishes to extract it for other uses in the system.

The clock frequency is divided by two, within a special glitch lockout circuit. This circuit immediately halts SAR operation when the outputs are enabled. The SAR operation does not resume until a short delay after outputs have been disabled. By providing the glitch lockout, the ADC-922 functional operation permits outputs to be read at any time, even if a conversion is in progress. Switching noise from the outputs will not distrurb the conversion accuracy, nor will the SAR attempt to transfer data to the output registers at the time they are actually being read.

OE, $\overline{OE}$: CHIP SELECTS

These inputs are TTL/CMOS compatible controlling the 3-state output with OE being active "High" and $\overline{OE}$ active "Low." The CS_1 input has an internal pull-up for users who do not use the select function. Both inputs must be active to enable the output. Note that this will also stop the clock.

V_{CC}: POSITIVE SUPPLY VOLTAGE

Positive supply for analog portions of the converter. This supply can be from +12 to +15V.

REF BYP: COMPENSATION

Capacitor connection for reference bias voltage stabilization. Recommended value is 10μF with 0.1μF connected as near to the pins as possible. Note: The voltage on this pin is approximately –11.8V. Be sure that the reference bypass capacitor polarity is correct.

REF ADJ: REFERENCE ADJUST

The internal reference is trimmed by connecting the REF ADJ pin to the tap of a 10kΩ potentiometer that is connected between the REF pin and analog ground (AGND). The adjustment is then accomplished by placing the desired full-scale voltage minus two LSBs, on the input and checking for the code change at codes 4094 to 4095.

BIP OFF: BIPOLAR OFFSET INPUT

This input is connected through a laser-trimmed, 4.995kΩ resistor to the summing node. The value of this resistor is trimmed to be slightly less than the resistors at V_{IN1} or V_{IN2} so that offset trimming is easily accomplished. (For more information, see section on bipolar input operation.)

V_{IN1}, V_{IN2}: ANALOG INPUTS

Connections to the summing node through identical laser-trimmed resistors with values of 5kΩ.

AGND: ANALOG GROUND

Internally, this pin connects to the reference, DAC, bias amplifier and comparator. Because the DAC switches current, this pin sees substantial current changes during the conversion cycle. For this reason, a good low impedance ground connected to this pin is essential to proper ADC operation.

V_{EE}: NEGATIVE SUPPLY

Negative supply for analog portions of the converter. This supply can be from –12 to –15V.

$\overline{DATA\ RDY}$: CONVERSION COMPLETE SIGNAL

An active "Low" TTL/CMOS compatible digital output that signals new data available in the output register. $\overline{DATA\ RDY}$ goes "Low" following the rising clock edge which defines the start of cycle T_{13}. $\overline{DATA\ RDY}$ is reset to "High" following the negative edge of OE. This input can be asynchronous with respect to CLOCK.

If the data is not read prior to the completion of another conversion, the data in the output register will be overwritten with the newest data.

CONVERT: RESET $\overline{DATA\ RDY}$ AND BEGIN CONVERSION

This is a TTL/CMOS compatible input. This input has hysteresis with 1 and 2V levels. Internally, there is a 30kΩ pull-up resistor so that leaving this pin unconnected will result in a logic "High" at this input.

A logic "High" on this input sets the conversion status latch and a new conversion will begin and continue until complete. Once the conversion status latch is set, the CONVERT input has no effect.

The conversion status latch is cleared during the reset cycle which follows data transfer, after conversion. SAR activity then stops until a new conversion is started by a logic "High" at CONVERT. This may occur at any time, subject only to minimum pulse width requirements.

Leaving the CONVERT input unconnected will result in continuous conversion.

DB_0 THROUGH DB_{11}: DIGITAL OUTPUTS

These are TTL/CMOS compatible 3-state digital outputs. DB_0 is the Least Significant Bit and DB_{11} is the Most Significant Bit.

V_{LOGIC}: +5 V SUPPLY

The power supply for the digital logic and output portions of the converter. Should be bypassed to DGND.

DGND: DIGITAL SUPPLY GROUND

ADC-922 OPERATION

CLOCK

The internal clock of the ADC-922 is an RC oscillator with an internal capacitance of approximately 10pF and a laser-trimmed resistor to set the maximum clock rate at 14MHz (Min). This clock is internally divided by two to generate the timing for the SAR and ADC control logic. The clock is then divided into 14 states that control the conversion rate as given in the following equation:

Conversion Rate = $f_{CLOCK}/14$

To run the clock at a slower speed, an external capacitor can be placed on the CLOCK pin. The clock speed will be proportional to the ratio of the internal capacitor (approximately 10pF) to the sum of the external and internal capacitors as given in the following equation:

$f_{CLOCK} = 14 \times 10^6 Hz * 10pF/(C_{EXT} + 10pF)$

To generate a timing signal based on the ADC-922's internal clock, a comparator can be connected to the CLOCK pin as shown in Figure 2. This connection should be designed for minimum stray capacitance to avoid loading the clock. Any stray capacitance will result in the slowing of the clock as described in the above equation for f_{CLOCK}.

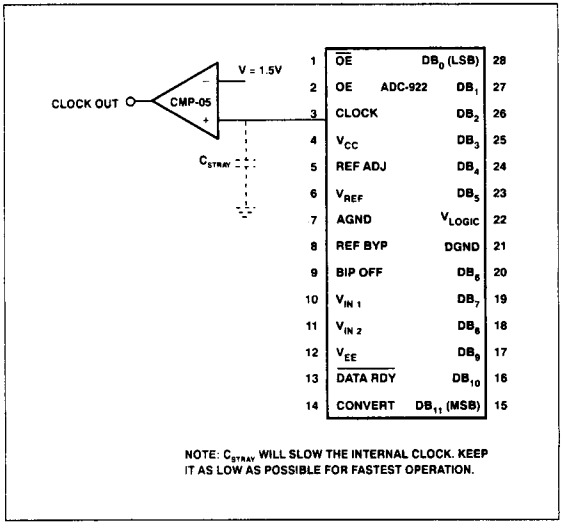


FIGURE 1: *Using Clock to Drive External Loads*

This technique can be used to synchronize two or more ADCs by connecting the comparator output from one ADC to other ADCs. Another way to implement a synchronized group of ADCs would be to drive them all from a single external clock.

Driving the clock from an external source is also possible because the internal clock swings are between +1 and +2V so that either TTL or CMOS logic levels will be capable of controlling the clock by overdriving the internal clock levels.

CONVERSION CYCLE

The ADC-922 uses a successive approximation technique with a total of 14 cycles for a complete conversion. Conversion always begins in the T_0 state. This state is unique in that the converter is always repeating the T_0 state until the CONVERT signal is given. Therefore, the MSB is being continuously tested. A conversion is initiated by a rising edge on the CONVERT input, the conversion process then begins on the next rising clock edge of the CLOCK. After 12 cycles, the conversion is complete. On the 13th cycle, data is transferred to the output register and the $\overline{DATA\ RDY}$ bit is set valid. During T_{13}, the SAR is reset so another conversion may begin.

A summary of the ADC-922's cycles starting with T_0 are as follows:

T_0: Test the MSB (DB_{11}). Note: T_0 is performed indefinitely until the CONVERT edge rises.

T_1: Test the next data bit, DB_{10}. Continue this process through T_{11} which is the LSB DB_0.

T_{12}: Transfer the results of the conversion from the SAR to the output register and set $\overline{DATA\ RDY}$.

T_{13}: Internal reset. Return to state T_0.

REFERENCE

A high-performance bandgap reference is used in the ADC-922. This reference is trimmed to 10V for both absolute value and temperature coefficient. By connecting the REF ADJ pin as shown in Figure 2, the full-scale value can be adjusted by approximately ±200 mV about 10V.

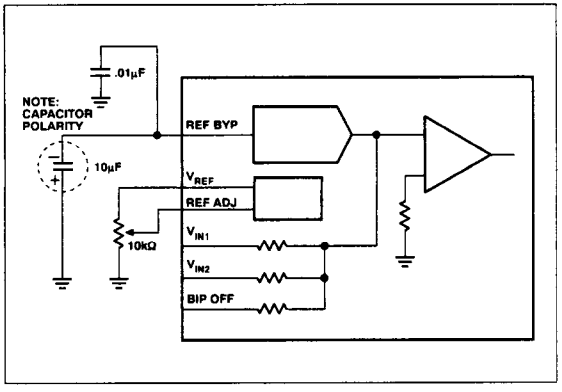


FIGURE 2: *Reference Adjust Circuit*

High-speed converters have high-speed clocks and switches that put heavy demands on the references. For the optimum performance, the ADC reference must be adequately bypassed. This will require a large electrolitic capacitor in parallel with a small ceramic capacitor. Best results will be obtained when the ADC is soldered into the board and a chip capacitor is mounted next to the REF BYP pin.

An external reference can be connected to the REF pin to set the full scale from an external reference (see Figure 3). In order to connect an external reference, the REF ADJ pin must be connected to V_{CC} to disable the internal reference.

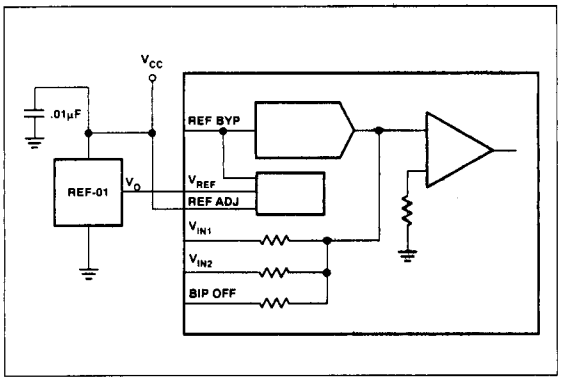


FIGURE 3: *Using an External Reference*

The REF pin can also be used as an output to provide a single reference for other ADCs or DACs in the system. Reference output current is limited to 5mA, so for loads greater than this, the output should be buffered. Care must be taken during power-up to avoid stressing this output.

INPUT RANGES

A wide variety of input ranges are easily configured with the ADC-922 because of the applications resistors that are available on-chip. By using these internal resistors rather than external resistors required by many other A/D converters, excellent temperature performance is possible. For this reason, it is recommended that the internal resistors be used whenever possible. Note that the internal input resistors are slightly less than 5kΩ, so be sure that the source resistance driving each of these pins has a low enough source impedance to prevent a DC error source.

Standard input ranges that can be configured without additional components are 0 to +10V, –10 to +10V, –5 to +5V and 0 to +20V. These ranges will be modified by the use of an external reference that is not set to 10V. Figures 4a through 4d show the connections for these inputs ranges.

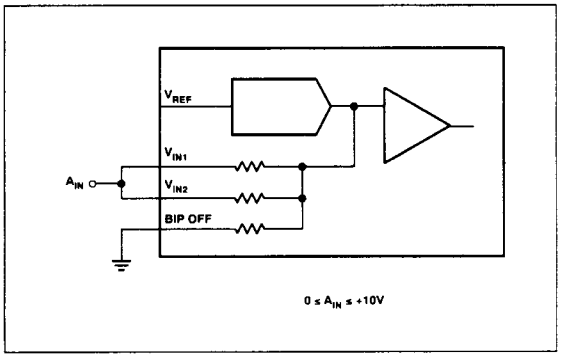


FIGURE 4a: *Unipolar 10V Input*

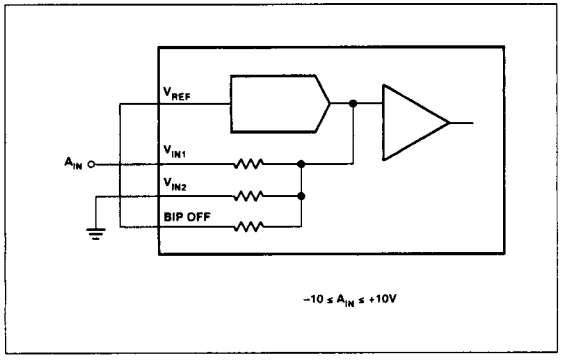


FIGURE 4b: *Bipolar ±10V Input*

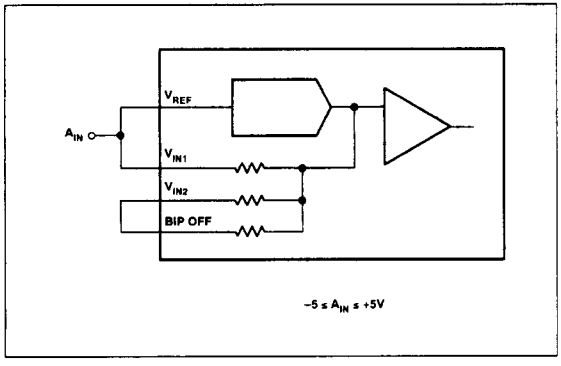


FIGURE 4c: *Bipolar ±5V Input*

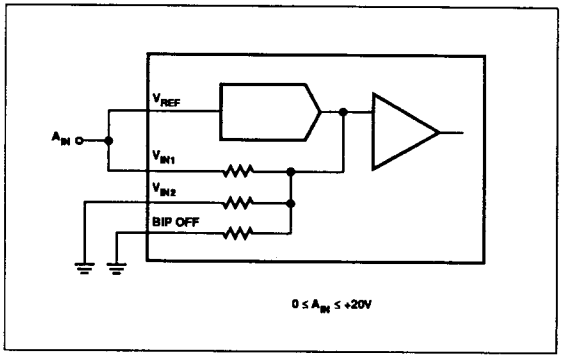


FIGURE 4d: *Unipolar +20V Input*

ANALOG INPUTS

The ADC-922 is a very high-speed converter with the inputs going through 5kΩ resistors (these can be paralleled in some applications for 2.5kΩ) to an internal comparator. This comparator is clamped by diodes so that the swing at this node is limited to $\pm V_{BE}$. The DAC output connected to this node can sink up to 4mA when the MSB switches causing large current spikes at the input pins to the ADC-922. For this reason, the input to the ADC should be driven by a wide bandwidth amplifier with low output resistance for high-speed performance. PMI's OP-64 is an excellent device for this application.

CONVERSION MODES

Three conversion modes are available: continuous conversion, externally triggered conversion, and single shot. To continuously convert, the CONVERT input is left unconnected forcing, by means of an internal pull-up resistor, an active "High" at this input. This forces the converter to go directly from cycle T_0 to T_1 without repeating the T_0 cycle. Thus, after the result of a conversion has been transferred to the output register, the ADC-922 automatically proceeds to a new conversion, whether or not the outputs have been read. Output register data will remain valid until the register is again updated during the following T_{12} cycle.

Single shot operation is achieved by connecting the $\overline{\text{DATA RDY}}$ output to the CONVERT input. When the results of the conversion are transferred to the output register, the $\overline{\text{DATA RDY}}$ = "Low" and this prevents a new conversion from starting by bringing CONVERT "Low" (remember the conversion is initiated by a rising edge on the CONVERT input). By reading the data by taking Output Enable "True," the $\overline{\text{DATA RDY}}$ will be reset to "High" and a new conversion will be allowed to begin. The read signal now becomes not only the output enable, but also the start conversion command.

To externally trigger a conversion, the CONVERT input may be independently controlled by an address decoder, using a processor "WRITE" command to create a pulse. Or, CONVERT may be made entirely independent of the processor by deriving CONVERT from an external asynchronous event. In this case, the ADC-922 $\overline{\text{DATA RDY}}$ signal may be used as part of a handshake operation with the external hardware.

READ OPERATION

The read operation is controlled by the inputs OE and $\overline{\text{OE}}$. They are asynchronous with respect to the CLOCK conversion signal. Data may be read at any time, including during a conversion allowing easy asynchronous interface with microprocessors. $\overline{\text{DATA RDY}}$ need not be active to access data, though if it is active, it will be reset to "High."

The asynchronous read operation of the ADC-922 is accomplished by stopping the convert CLOCK internally until the data "READ" is completed by bringing either OE or $\overline{\text{OE}}$ inactive. This operation is transparent to the user. If a track-and-hold is used, the timing must take this into account.

DIGITAL OUTPUTS

The ADC-922 is a high-performance converter designed to interface to the fastest processors available. Its access time is less than 30ns and its outputs are capable of driving 120pF loads at full speed. However, driving heavy loads requires large currents from the +5V power supply. In order to keep the required supply voltages on the supply lines, good supply bypassing techniques (Figure 5) must be followed.

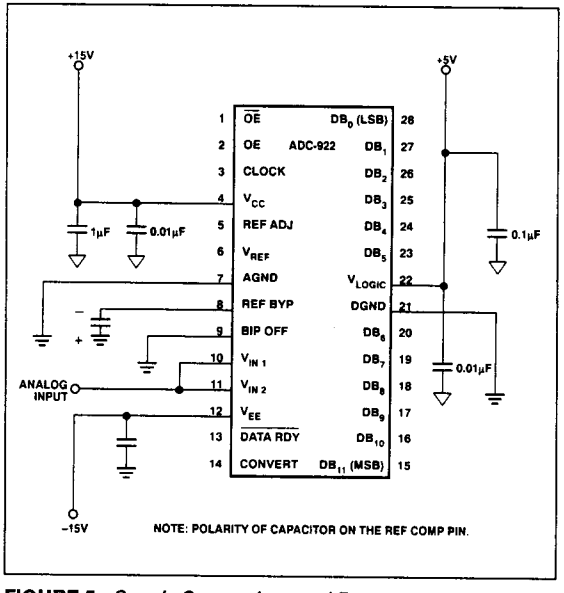


FIGURE 5: *Supply Connections and Bypassing*

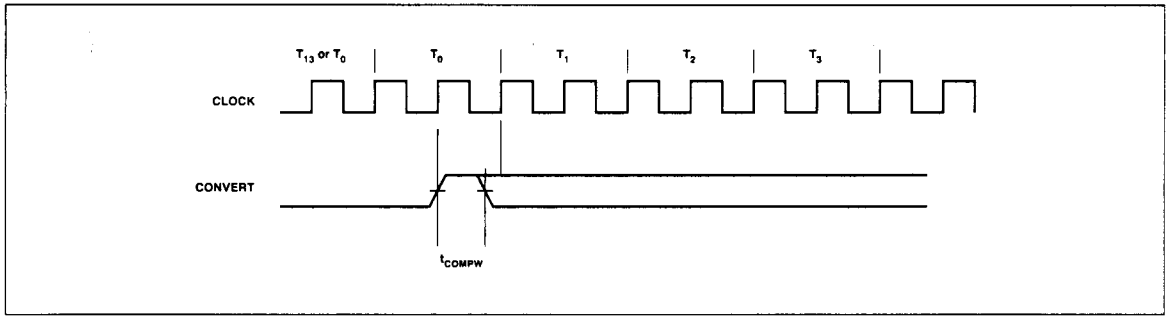


FIGURE 6: *Conversion Start Timing Diagram*

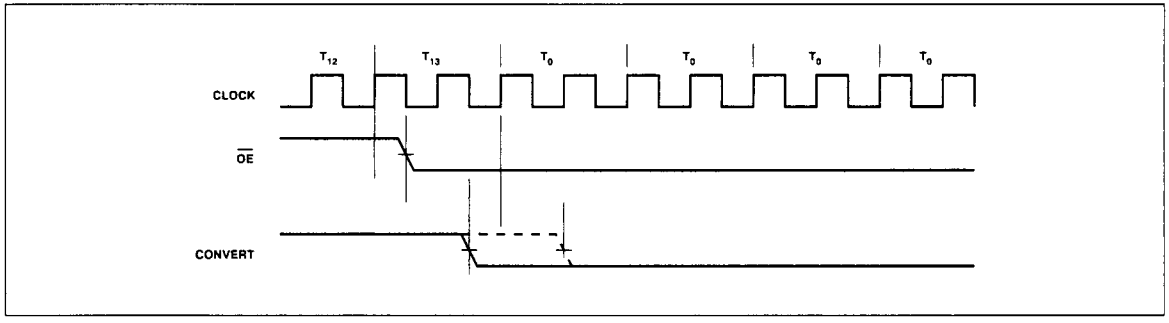


FIGURE 7: *Conversion Halt Timing Diagram*

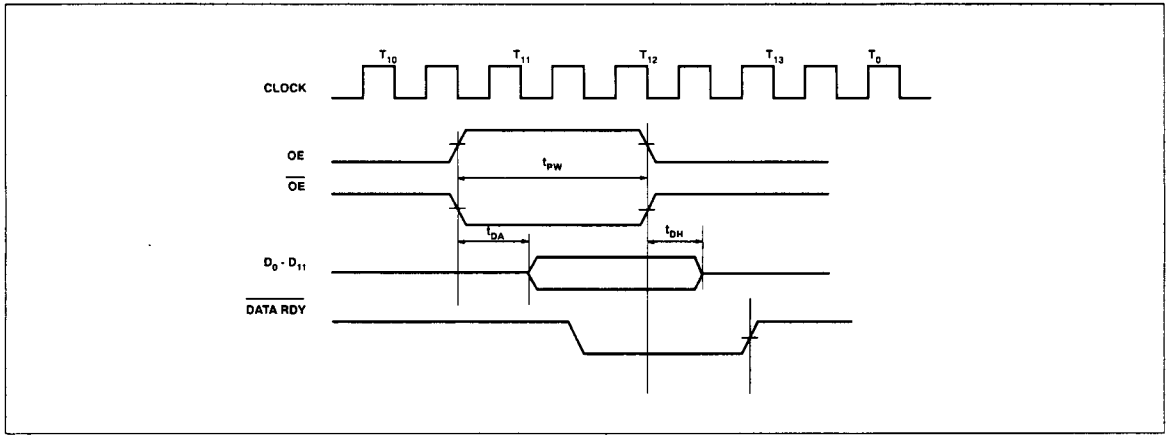


FIGURE 8: *Read Timing Diagram*