54F/74F194

4-Bit Bidirectional Universal Shift Register

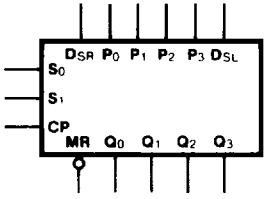
Description

The 'F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'F194 is similar in operation to the 'F195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

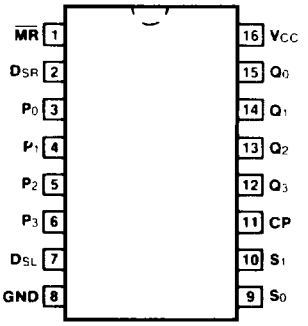
- **Typical Shift Frequency of 150 MHz**
- **Asynchronous Master Reset**
- **Hold (Do Nothing) Mode**
- **Fully Synchronous Serial or Parallel Data Transfers**

Ordering Code: See Section 5

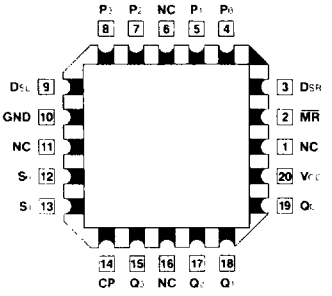
Logic Diagram



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0, S_1	Mode Control Inputs	0.5/0.375
P_0-P_3	Parallel Data Inputs	0.5/0.375
D_{SR}	Serial Data Input (Shift Right)	0.5/0.375
D_{SL}	Serial Data Input (Shift Left)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
Q_0-Q_3	Parallel Outputs	25/12.5

Functional Description

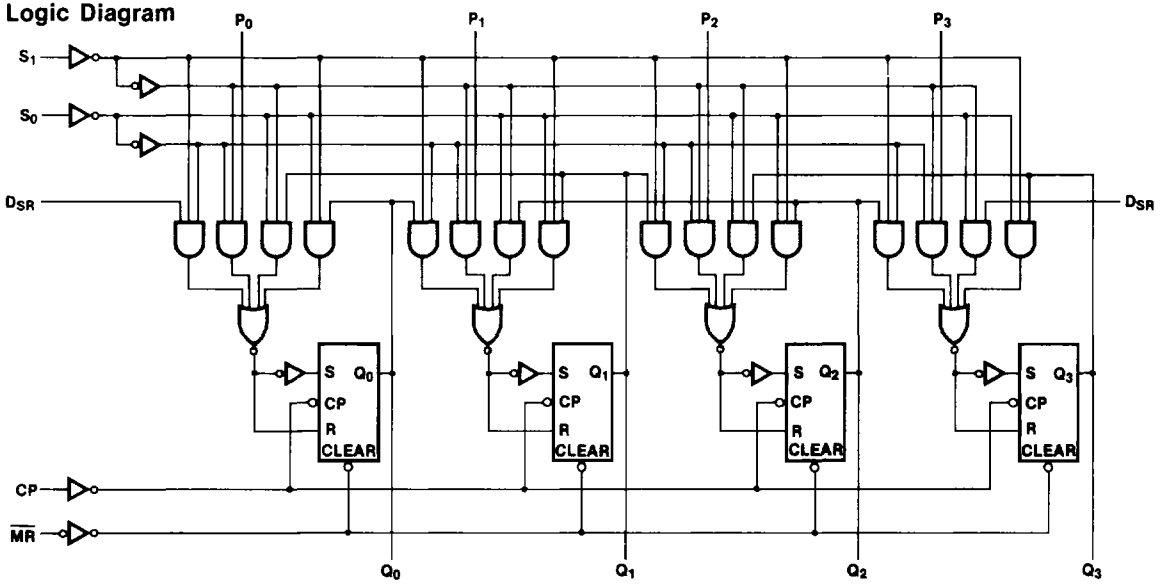
The 'F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0, S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P_0-P_3) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ($\overline{MR}$) overrides all other inputs and forces the outputs LOW.

Mode Select Table

Operating Mode	Inputs						Outputs			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

H = HIGH Voltage Level
L = LOW Voltage Level
$p_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		33	46	mA	V_{CC} = Max S_n, $\overline{MR}$, D_{SR}, D_{SL} = HIGH P_n = Gnd, CP = ⌐

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	105	150		90		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.5 3.5	5.2 5.5	7.0 7.0	3.0 3.0	8.5 8.5	3.5 3.5	8.0 8.0	ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	4.5	8.6	12.0	4.5	14.5	4.5	14.0	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n or D_{SR} or D_{SL} to CP	4.0 4.0			4.0 4.0		4.0 4.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n or D_{SR} or D_{SL} to CP	0 0			1.0 1.0		1.0 1.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S_n to CP	8.0 8.0			9.5 8.0		9.0 8.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S_n to CP	0 0			0 0		0 0			
$t_w(H)$	CP Pulse Width, HIGH	5.0			5.5		5.5		ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.0			5.0		5.0		ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP	7.0			9.0		8.0		ns	3-11