VITESSE

VSC7124
Datasheet

Quad Port Bypass Circuit

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FEATURES

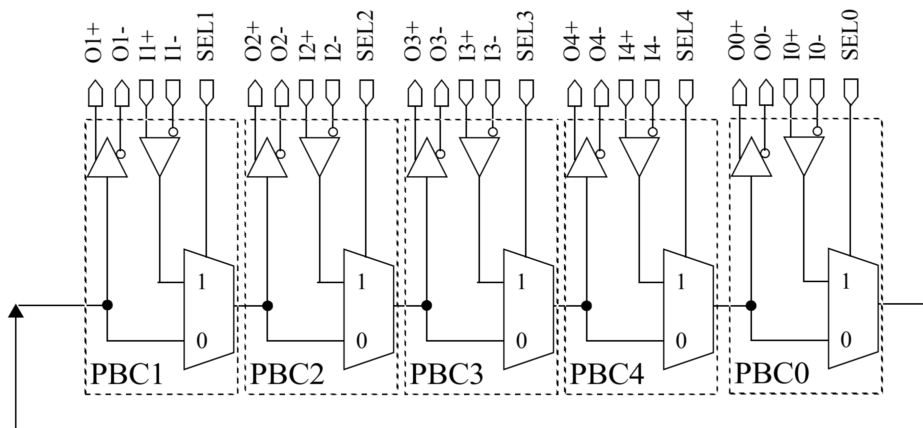
- ANSI X3T11 Fibre Channel-compliant at 1.0625 Gbps
- IEEE 802.3z GbE-compliant at 1.25 Gbps
- Five-port bypass circuits (PBCs)
- On-chip transmit termination
- 3.3 V, 0.25 W typical power
- 0.35 micron CMOS, a velocity family member
- 44-Pin, 10 mm PQFP package

GENERAL DESCRIPTION

The VSC7124 contains five cascaded Port Bypass Circuits (PBCs) used to steer serial signals. This part is typically used in distributing Fibre Channel signals to an array of disk drives in an FC-AL loop as illustrated in Figure 1. The VSC7124 can be used with any of the Vitesse JBOD circuits to implement FC-AL JBODs of virtually any size. In Figure 2, page 2, the first VSC7127 CRU is configured as a repeater to attenuate jitter. The VSC7124 does not contain a CRU to reduce power and cost. The second VSC7127 CRU is configured as a retimer so that the output of the device is a jitter compliance point.

Each PBC is a multiplexer that is controlled by the corresponding SELx line, which if high, selects the external input or if low, selects the output of the previous PBC.

Figure 1. Block Diagram



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Application Example

A 12-port JBOD is shown in the following figure. This dual loop application uses one VSC7127R, one VSC7127T and one VSC7124 on each loop in order to configure the FC-AL disk array. Functional drives are included in the FC-AL loop while nonfunctional or missing drives (numbers 2, 7, 9) are excluded.

Figure 2. 12-Drive FC-AL JBOD Application

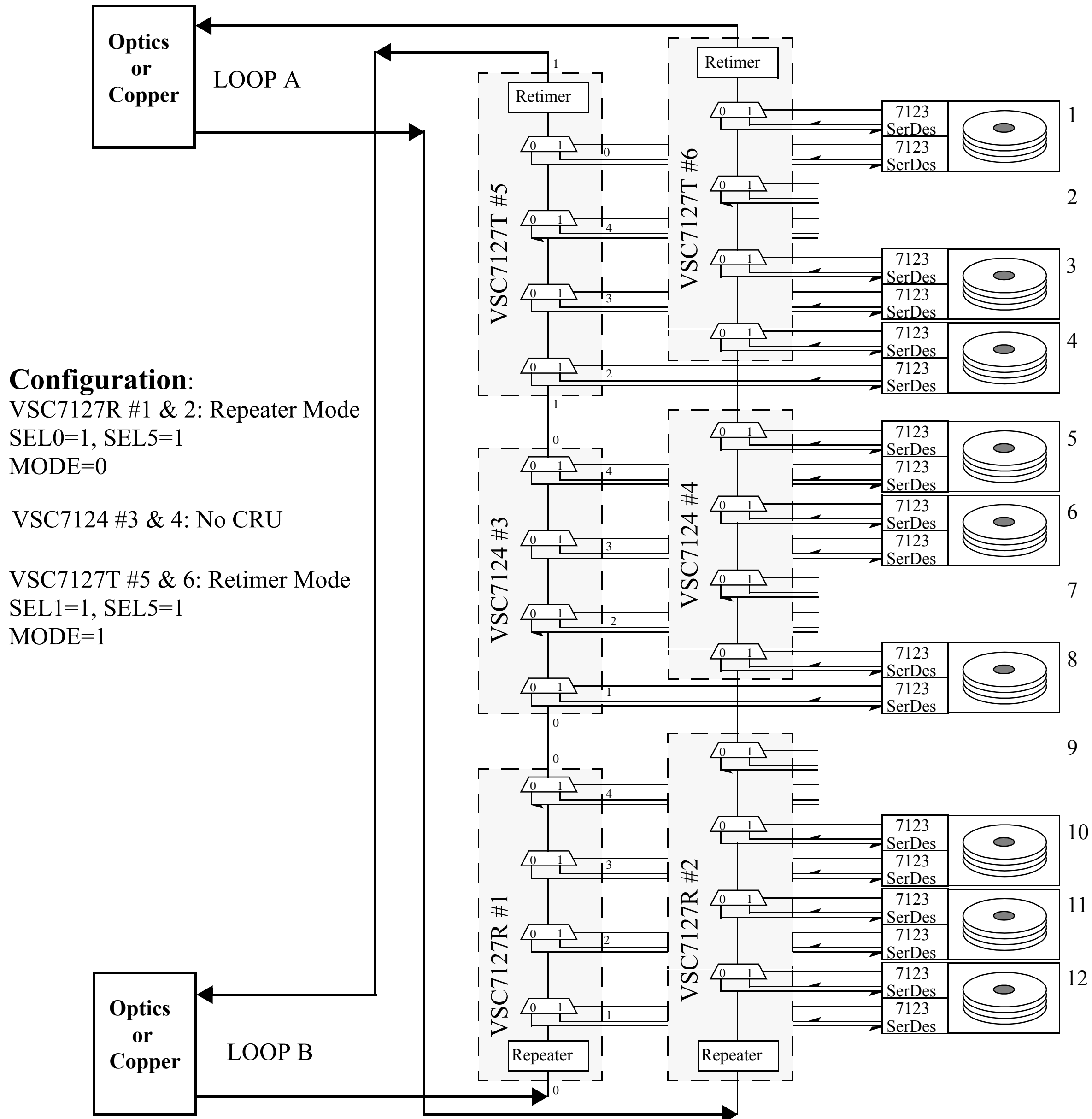

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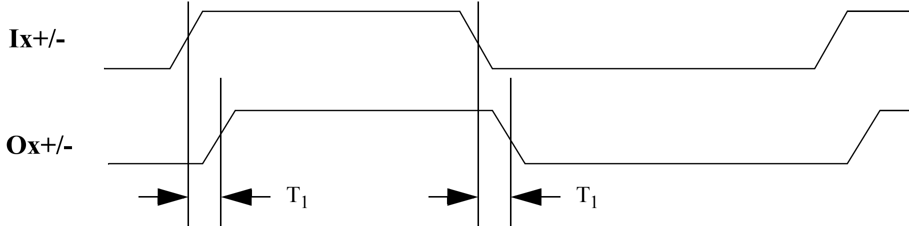
Figure 3. Timing Waveforms



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Electrical Specifications

DC Characteristics

Figure 4.

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{OH}	Output high voltage (TTL)	2.4			V	$I_{OH} = -1.0$ mA
V_{OL}	Output low voltage (TTL)			0.5	V	$I_{OL} = 1.0$ mA
V_{IH}	Input high voltage (TTL)	2.0		5.5	V	
V_{IL}	Input low voltage (TTL)	0		0.8	V	
I_{IH}	Input high current (TTL)		50	500	µA	$V_{IN} = 2.4$ V
I_{IL}	Input low current (TTL)			-500	µA	$V_{IN} = 0.5$ V
ΔV_{OUT75}[1]	TX output differential peak-to-peak voltage swing	1200		2200	mVp-p	75 Ω to V_{DD} − 2.0 V
ΔV_{OUT50}[1]	TX output differential peak-to-peak voltage swing	1000		2200	mVp-p	50 Ω to V_{DD} − 2.0 V
ΔV_{IN}[1]	Receiver differential peak-to-peak input sensitivity RX	400		2600	mVp-p	Internally biased to V_{DD} / 2
V_{DD}	Supply voltage	3.14		3.47	V	3.3 V ±5%
P_D	Power dissipation		250	555	mW	Outputs open, $V_{DD} = V_{DD}$ maximum ±2%
I_{DD}	Power supply current		76	160	mA	Outputs open, $V_{DD} = V_{DD}$ maximum

1. For more information about differntial voltage measurement, see Application Note AN-37.

AC Characteristics

Table 1. AC Characteristics

Symbol	Parameter	Maximum	Units	Condition
T_1	Propagation Delay	7.0	ns	Delay with all circuits bypassed.
T_R, T_F	Serial Data Rise and Fall Time	300	ps	At ΔV_{IN} minimum levels
$T_{j(PBC)}$	Data Jitter Accummulation	120	ps	Peak-to-peak on Ox+/Ox–

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Operating Conditions

The functional and parametric operations of the device are guaranteed under the recommended operating conditions except where noted in "DC Characteristics," page 4 and "AC Characteristics," page 4.

Table 2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Power supply voltage	3.14	3.47	V
T	Operating temperature(1)	0	95	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

Maximum Ratings

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	TTL power supply voltage	.5	4	V
V_{INP}	PECL DC input voltage	–.5	V_{DD} + 5	V
V_{INT}	TTL DC input voltage	–.5	5.5	V
V_{IN_TTL}	DC voltage applied to outputs for high output state	–.5	V_{DD} + 5	V
I_{OUT_TTL}	TTL output current (DC, output high)		50	mA
I_{OUT_PECL}	PECL output current (DC, output high)	–50		mA
T_S	Storage temperature	–65	150	°C

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

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PACKAGE INFORMATION

The VSC7124 device is available in the following package types, including lead-free packages:

- VSC7124QM is a 44-pin, thermally enhanced, plastic quad flat package (QFP) with a 10 mm × 10 mm body size, 2 mm body thickness, and 0.8 mm pitch. VSC7124XQM is the lead-free package.
- VSC7124RY is a 44-pin, thermally enhanced, plastic thin quad flat package (TQFP) with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, and 0.8 mm pitch. VSC7124XRY is the lead-free package.

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the thermal specifications and characteristics, moisture sensitivity rating, and package drawings for the VSC7124 device.

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 4. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC7124RY	6.3	75	68	66
VSC7124XRY	6.3	75	68	66

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

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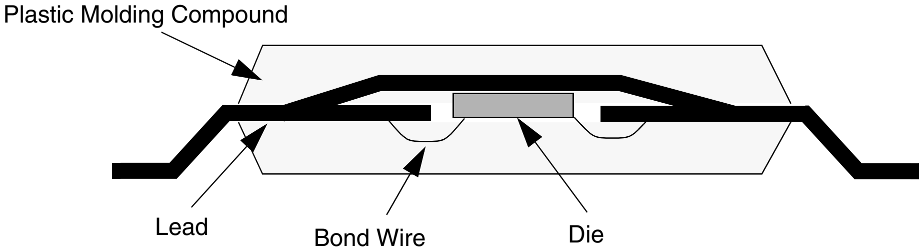
Package Thermal Characteristics

The VSC7124QM package construction is shown in the following illustration. For more information about the thermal properties, see Table 4, page 6.

Figure 5. VSC7124QM Package Cross Section



Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Package Drawings

The following illustrations show the package drawings for the VSC7124 device.

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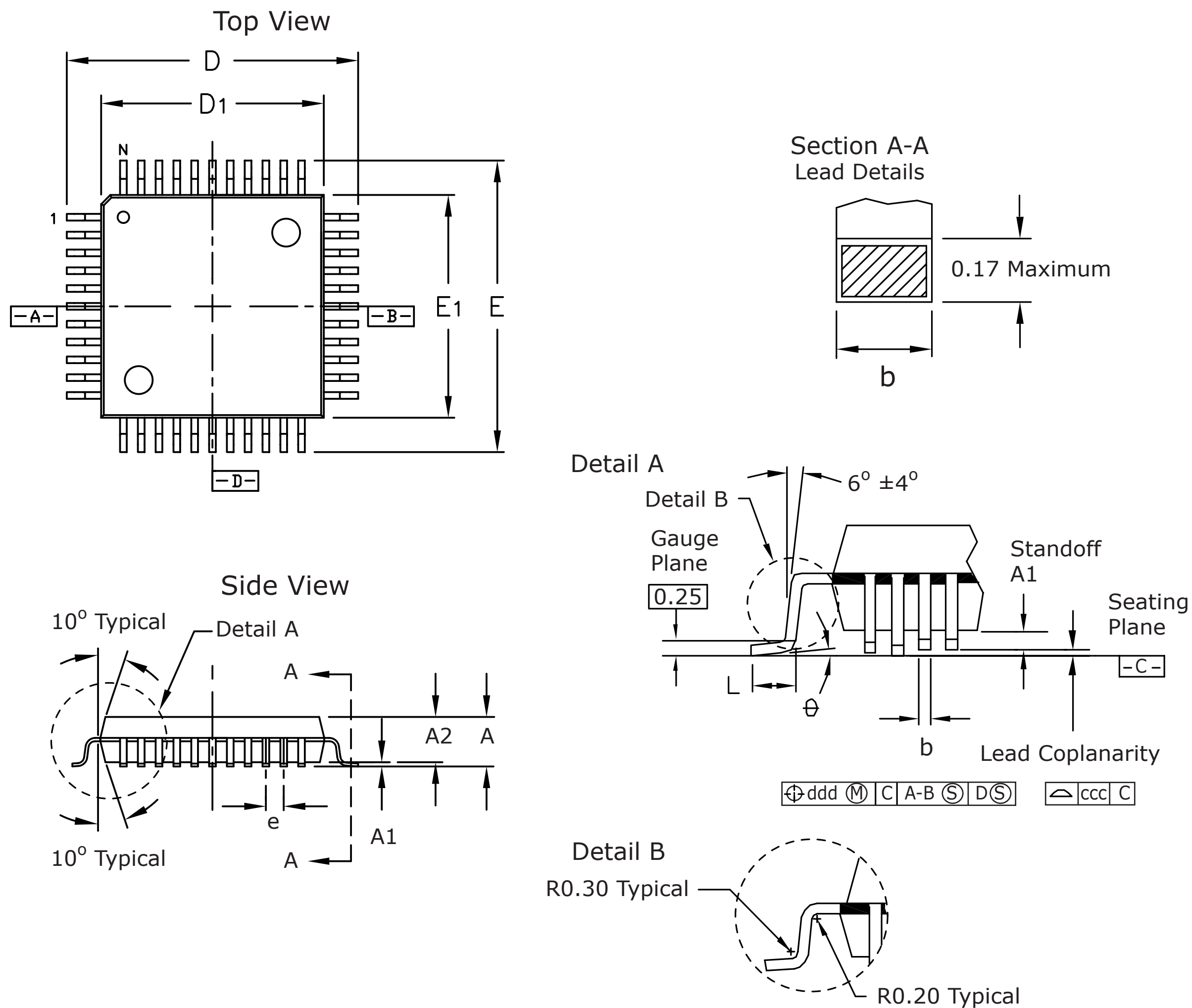
Figure 6. Package Drawing for VSC7124QM and VSC7124XQM



Notes
1. All dimensions in millimeters.
2. Dimensions shown are nominal with tolerances indicated.
3. Foot length L is measured at gauge plane 0.25 mm above seating plane.
4. N is the total number of leads.
5. This outline conforms to JEDEC MS-022, variation BC-1.

Reference	Minimum	Nominal	Maximum
A			2.45
A1	0.25		0.50
A2	1.95	2.00	2.10
D	12.95	13.20	13.45
D1	9.90	10.00	10.10
E	12.95	13.20	13.45
E1	9.90	10.00	10.10
L	0.78	0.88	1.03
N		44	
e		0.80	
b	0.30	0.35	0.40
θ		0° ~ 7°	
ddd		0.20	
ccc			0.10

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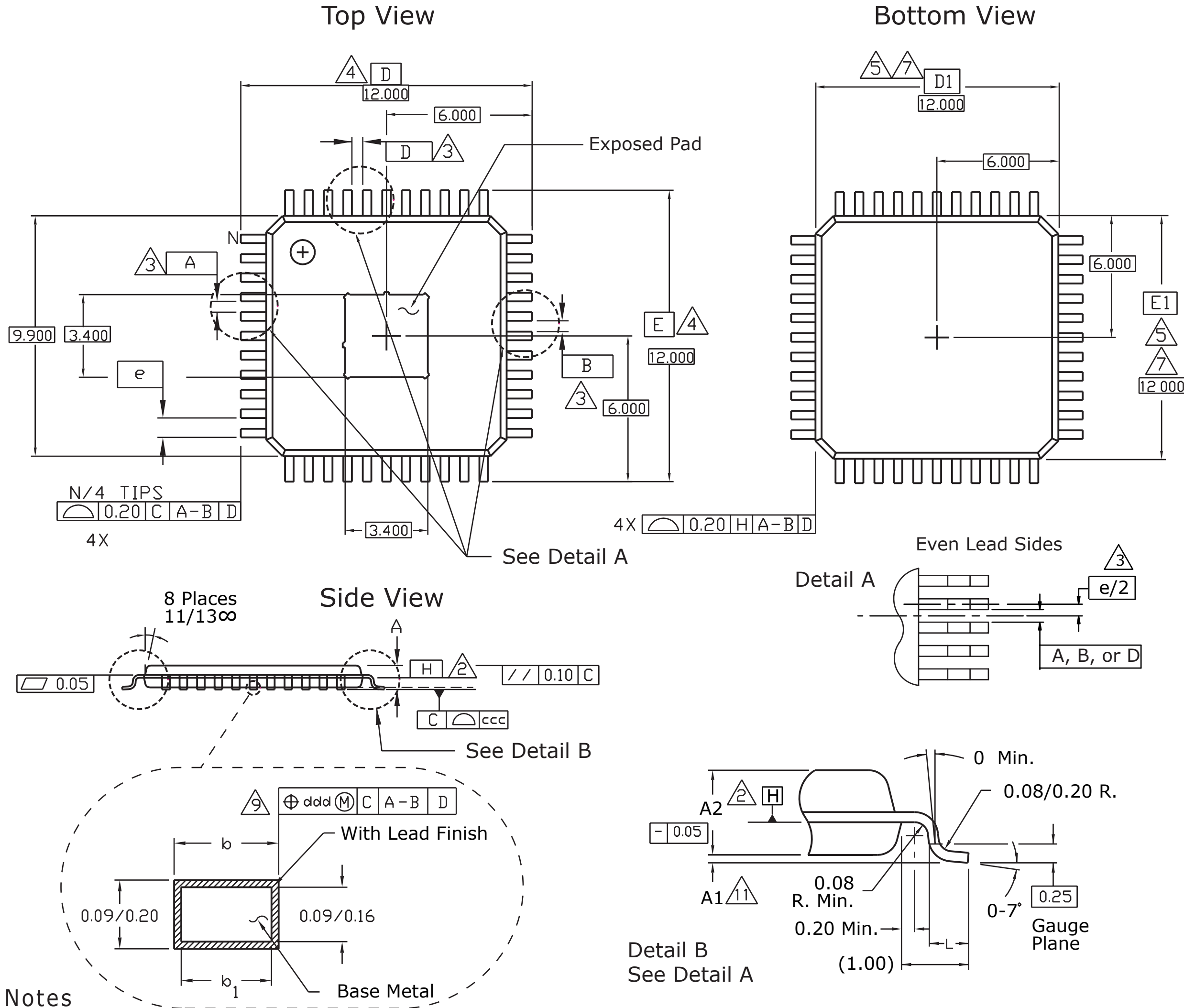
Figure 7. Package Drawing for VSC7124RY and VSC7124XRY



Notes

1. All dimensions and tolerances in millimeters.
2. Datum plane H located at mold parting line and coincident with lead where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. N is the total number of terminals.
7. To be determined at datum plane H.
8. Package top dimensions are smaller than bottom dimensions by 0.15 mm.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion is 0.08 mm total in excess of the b dimension at maximum material condition.
10. This outline conforms to JEDEC MS-026, variation ACB.
11. A1 is defined as the distance from the seating plane to the lowest point of the package body.
12. Exposed die pad is coplanar with bottom of package within 0.05 minimum.

Reference	Minimum	Nominal	Maximum
A			1.20
A1	0.05		0.15
A2	1.95	1.00	1.05
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
L	0.45	0.60	0.75
N		44	
e		0.80	
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
ddd			0.10
ccc			0.20

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PIN DESCRIPTIONS

Figure 8. Pin Diagram

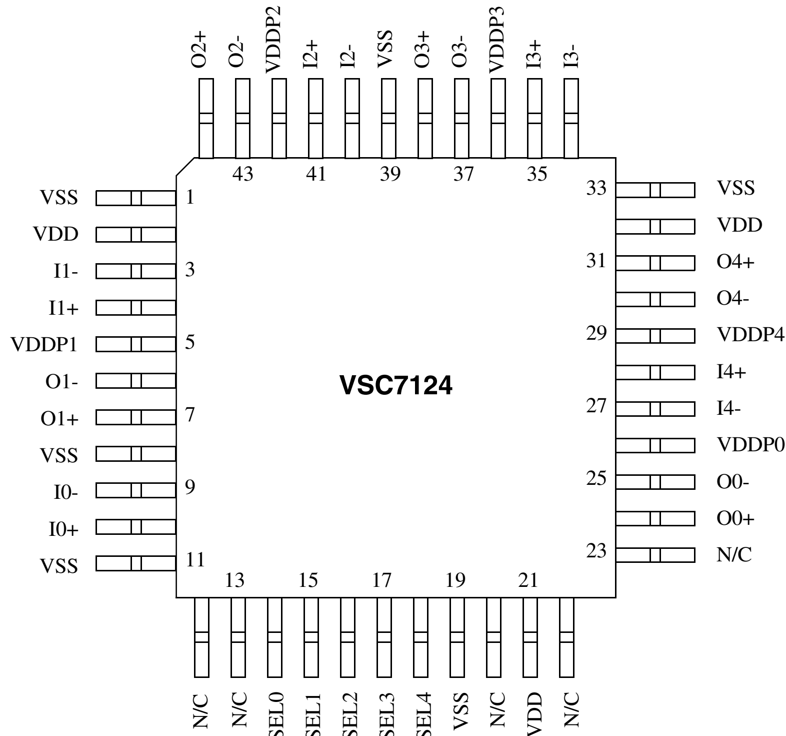

Table 5. Pin Identifications

Pin #	Name	Description
4, 3, 41, 40 35, 34, 28, 27 10, 9	I1+, I1-, I2+, I2- I3+, I3-, I4+, I4- I0+, I 0-	INPUT - Differential, internally biased to V_{DD} / 2. Ix+/Ix– is the serial input to PBCx.
15, 16, 17, 18 14	SEL1, SEL2 SEL3, SEL4 SEL0	INPUT - TTL. Port bypass mux select lines. High selects Ix. Low selects the output of the previous internal device.
7, 6, 44, 43 38, 37, 31, 30 24, 25	O1+, O1-, O2+, O2- O3+, O3-, O4+, O4- O0+, O0-	OUTPUT - Differential. Ox+/Ox– is the serial output from PBCx.
2, 21, 32	VDD	Digital logic power supply.
5 42 36 29 26	VDDP1 VDDP2 VDDP3 VDDP4 VDDP0	Power supply (3.3 V) for O1+/O1–. If unused, connect to VSS. Power supply (3.3 V) for O2+/O2–. If unused, connect to VSS. Power supply (3.3 V) for O3+/O3–. If unused, connect to VSS. Power supply (3.3 V) for O4+/O4–. If unused, connect to VSS. Power supply (3.3 V) for O0+/O0–. If unused, connect to VSS.
12, 13, 20, 22, 23	N/C	Not connected.
1, 8, 11, 19, 33, 39	VSS	Ground.

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ORDERING INFORMATION

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The following table lists the ordering information for the VSC7124 device.

Table 6. Ordering Information

Part Order Number	Description
VSC7124QM	44-pin, thermally enhanced, plastic QFP with a 10 mm × 10 mm body size, 2 mm body thickness, and 0.8 mm pitch
VSC7124XQM	Lead-free, 44-pin, thermally enhanced, plastic QFP with a 10 mm × 10 mm body size, 2 mm body thickness, and 0.8 mm pitch
VSC7124RY	44-pin, thermally enhanced, plastic TQFP with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, and 0.8 mm pitch
VSC7124XRY	Lead-free, 44-pin, thermally enhanced, plastic TQFP with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, and 0.8 mm pitch

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