HD153201

NRZ to CMI Code Converter

The HD153201 is a code converter (CODEC) IC which converts NRZ signals to CMI code and vice versa. Since both TTL and ECL input/output levels are available, this device is suitable for use in high speed, low power data transmission systems.

Features

- Encoder/Decoder for conversion between NRZ and CMI code
- High speed data transfer rate of 32 Mbps
- Either TTL or ECL input/output levels available for interface
- Low power dissipation of 540 mW typical
- Error bit output provided for illegal code conversion
- 5 V single power supply (at TTL interface)
- Two packages supported: MSP-44 and DIP-42S

Functions

- NRZ signal to CMI code conversion
- CMI code to NRZ signal conversion
- Carrier detection
- Error detection
- Frame signal superimposition

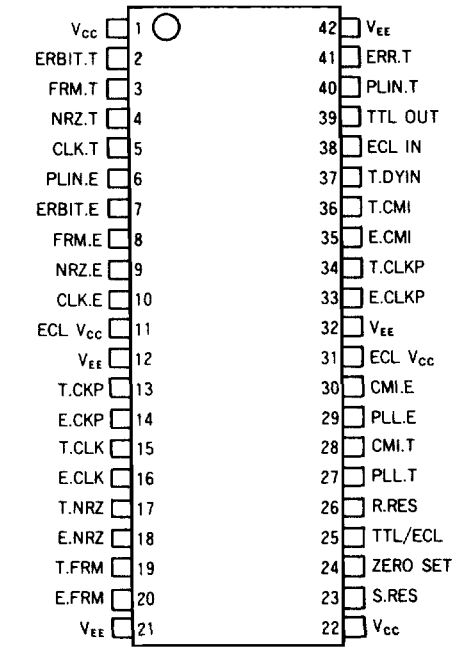
NRZ: Non Return to Zero
CMI : Coded Mark Inversion

Ordering Information

Type No.	Data Transmission Rate	Package
HD153201PS16	16 Mbps max	42 pin Plastic Shrink DIP
HD153201PS32	32 Mbps max	
HD153201MP16	16 Mbps max	44 pin MSP
HD153201MP32	32 Mbps max	

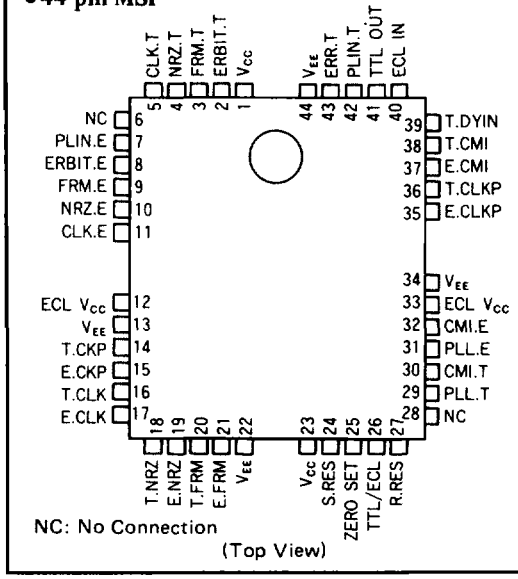
Pin Arrangement

●42 pin plastic shrink DIP



(Top View)

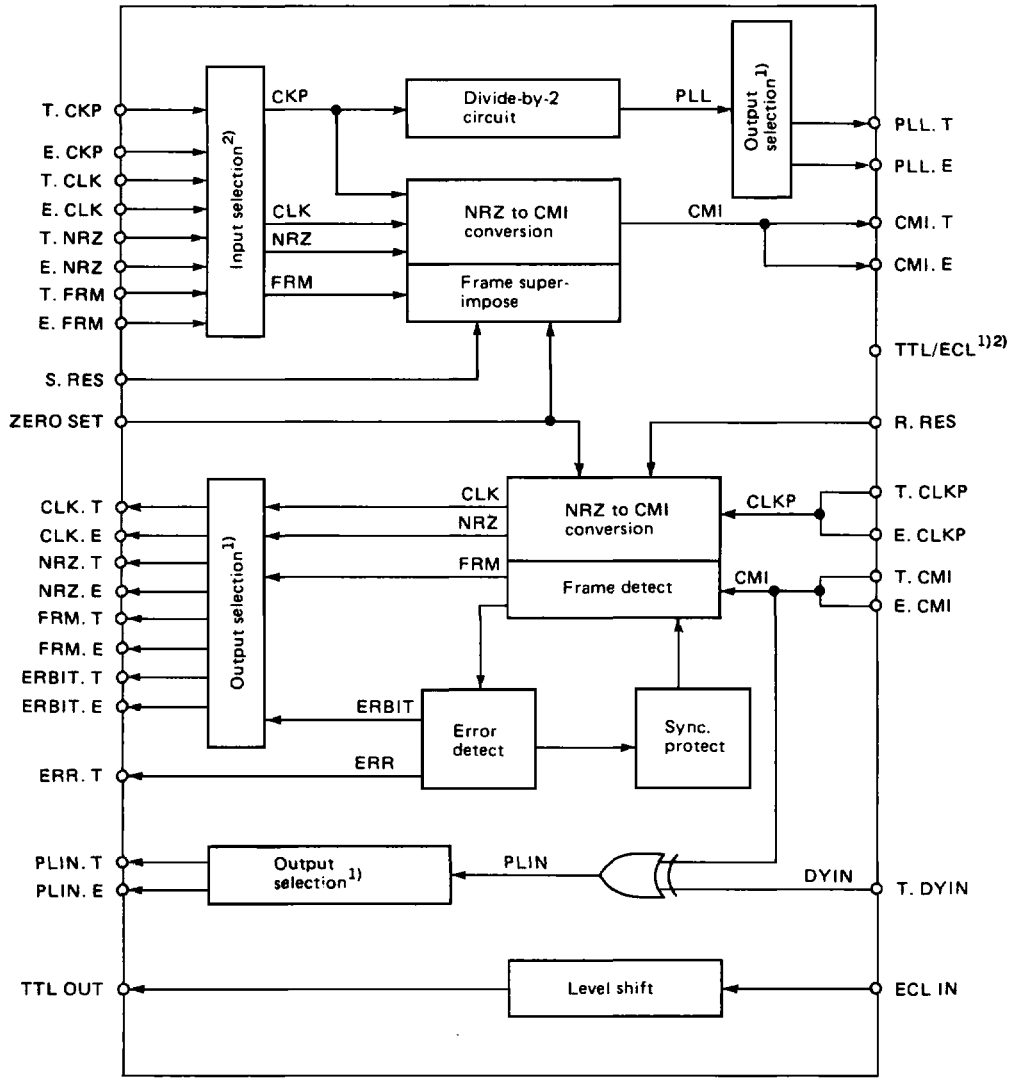
●44 pin MSP



NC: No Connection

(Top View)

Block Diagram



Notes: 1 The output select circuit is controlled by the TTL/ECL pin. However, the ECL output cannot be controlled.
2 The input select circuit performs a switching between the TTL and ECL input pins through the TTL/ECL pin.
3 "T. –" and "E. –" indicate the TTL and ECL inputs, respectively, while "–. T" and "–. E" represent their outputs.

Signal Description in the Block Diagram

	Input		Output	
	Signal	**Description**	**Signal**	**Description**
Transmit function	CKP	2fo: Frequency double the reference clock	CMI	Transmitted CMI code converted from NRZ and FRM signals
	CLK	fo: Reference clock	PLL	CKP-divide-by-2 signal
	NRZ	Transmitted NRZ signal		
	FRM	Frame signal for superimpose		
Receive function	CMI	Received CMI code	CLK	Reproduced reference clock, fo
			NRZ	NRZ signal reproduced from CMI code
	CLKP	2fo: Frequency double the transmission rate	FRM	Frame signal detected from CMI code
			ERBIT	Signal for detecting illegal received CMI code
	DYIN	Delayed received CMI code	PLIN	Signal having a frequency double the received CMI code
			ERR	Signal for detecting 2 error bits in the 16-bit received CMI code

Pin Description

Pin No.	Pin Name	IN/OUT	Function	
			TTL interface	ECL interface
1, 22 (1), (23)	V_{CC}	Power	Supplies +5V power. Connects to V_{CC} (Both V_{CC} pins must be directly connected without shorting.)	Connects to ground (0V).
12, 21, 32, 42 (13), (22), (33), (44)	V_{EE}	Power	Connect to ground (0V). (All V_{EE} pins must be directly connected without shorting.)	Supplies –5.2V power
11, 31 (12), (33)	ECL V_{CC}	Power	This pin must be open.	Both pins must be directly connected to ground (0V) without shorting with V_{CC}.
15 (16)	T. CLK	IN	Provides the fo reference clock signal for transmitted signals. This clock frequency is the transmission rate.	This pin must be open or pulled up or down with a 2–5k ohm resistor.
13 (14)	T. CKP	IN	Supplies the 2fo clock signal which is double that of and synchronous with the reference clock signal fo. 2fo can be easily generated using Hitachi's PLL (HD153202).	This pin must be open or pulled up or down with a 2–5k ohm resistor.
17 (18)	T. NRZ	IN	Provides NRZ data to be transmitted synchronously with the reference clock signal.	This pin must be open or pulled up or down with a 2–5k ohm resistor.
19 (20)	T. FRM	IN	Provides frame signals synchronously with the reference clock signal. When T. FRM is set to high, the frame signal is superimposed on the CMI output.	This pin must be open or pulled up or down with a 2–5k ohm resistor.
16 (17)	E. CLK	IN	This pin must be open or pulled up or down with a 2–5k ohm resistor.	Provides reference clock signal fo for transmitted signals. The frequency of this clock signal is the transmission rate.
14 (15)	E. CKP	IN	This pin must be open or pulled up or down with a 2–5k ohm resistor.	Provides clock signal 2fo which is double of and synchronously with the reference clock signal. The 2fo signal can be easily generated using Hitachi's PLL (HD153202).

Parenthesized pin numbers are for the MP-44 package.

(to be continued)

Pin No.	Pin Name	IN/OUT	Function	
			TTL interface	ECL interface
18 (19)	E. NRZ	IN	This pin must be open or pulled up or down with a 2–5k ohm resistor.	Inputs NRZ data to be transmitted synchronously with the reference clock signal.
20 (21)	E. FRM	IN	This pin must be open or pulled up or down with a 2–5k ohm resistor.	Provides frame signals synchronously with the reference clock signal. When this signal is set to high, a frame signal is superimposed on the CMI output signal. When not being used, this pin must be pulled down to V_{EE} (–5.2V) with a 2–5k ohm resistor or a low level signal must be applied.
23 (24)	S. RES	IN	Resets transmitted signal outputs. A low level S. RES forces both CMI and PLIN outputs to be set to low. A high level allows data to be transmitted.	Resets transmitted signal outputs. A low level S. RES forces both CMI and PLIN outputs to be set to low. A high level allows data to be transmitted. The input signal with a high level > –3.2V and low < –4.4V must be applied at V_{EE} = –5.2V.
25 (26)	TTL/ECL	IN	Switches between TTL and ECL interfaces. This pin is pulled down to V_{EE} level with a 2–5k ohm resistor.	Switches between TTL and ECL interfaces. This pin is pulled up to V_{CC} level with a 2–5k ohm resistor.
24 (25)	ZERO SET	IN	Determines whether CMI code 0 is converted into 01 or 10; a high level on this pin selects 01 and a low level 10.	Determines whether CMI code 0 is converted into 01 or 10; a high level (>–3.2V) on this pin selects 01 and a low level (<–4.4V) selects 10 (at V_{EE} = –5.2V)
36 (38)	T. CMI	IN	Inputs the CMI signal to be received.	This pin must be pulled up with a 2–5k ohm resistor.
34 (36)	T. CLKP	IN	Inputs a clock signal having a frequency double of the transmission rate synchronously with the received CMI signal. This clock signal can be easily generated using Hitachi's PLL (HD153202).	This pin must be pulled up with a 2–5k ohm resistor.

Parenthesized pin numbers are for the MP-44 package.

(to be continued)

Pin No.	Pin Name	IN/OUT	Function	
			TTL interface	ECL interface
35 (37)	E. CMI	IN	This pin must be pulled up to V_{CC} level with a 2–5k ohm resistor.	Inputs the received CMI signal.
33 (35)	E. CLKP	IN	This pin must be pulled up to V_{CC} level with a 2–5k ohm resistor.	Supplies signals having a frequency double of the transmission rate, synchronously with the CMI signal to be received. This clock signal can be easily generated using Hitachi's PLL (HD153202).
26 (27)	R. RES	IN	Resets received output signals. When this is set to low, all outputs of CLK, NRZ, FRM and ERBIT go to low. A high level on this pin allows data to be received.	Resets received output signals. When this is set to low, all outputs of CLR, NRZ, FRM, ERBIT and PLIN go to low. A low level on this pin allows data to be received. The input signal with a high level > –3.2V and low level < –4.4V must be applied at V_{EE}=–5.2V.
37 (39)	T. DYIN	IN	Inputs the delayed CMI signal. The resulting output appears on the PLIN. T pin at a frequency double of the CMI signal. When combined with Hitachi's PLL (HD153202), this pin must be open or pulled up/down using a 2–5k ohm resistor.	Inputs the delayed CMI signal with a high level > –3.2V and low level < –4.4V at V_{EE} = –5.2V. The resulting output appears on PLIN. E at a frequency double of the CMI signal. When combined with Hitachi's PLL (HD153202), this pin must be open or pulled up or down with a 2–5k ohm resistor.
38 (40)	ECL IN	IN	Converts signals having a 0.9 Vp-p (3.2 to 4.1V) swing into the TTL level; input signal with high > 4.04V and low < 3.15V must be applied at V_{CC} = 5V.	When the CMI signal is input to this pin, output with an amplitude of –4.4 to –3.2V necessary for T. DYIN can be obtained.
39 (41)	TTL OUT	OUT	When a signal with 0.9 Vp-p and 3.2-to-4.1V swing is input to the ECL IN pin, this pin provides an output with TTL-level voltage swing. When not being used, this pin must be open.	Outputs a signal to be input to the ECL IN pin with an amplitude of –4.4 to –3.2V.
28 (30)	CMI. T	OUT	Outputs TTL-level CMI code converted from the T. NRZ and T. FRM signals.	This pin must be open.

Parenthesized pin numbers are for the MP-44 package.

(to be continued)

Pin No.	Pin Name	IN/OUT	Function	
			TTL interface	ECL interface
27 (29)	PLL. T	OUT	Outputs a signal at a frequency half of T. CKP. This output must be fed back to the PLL to produce the 2fo clock signal with a frequency double of the reference clock signal. When used with Hitachi's PLL, this pin must be open.	This pin must be open.
30 (32)	CMI. E	OUT	This pin must be open.	Outputs ECL-level CMI code converted from E. NRZ and E. FRM signals.
29 (31)	PLL. E	OUT	This pin must be open.	Provides a signal at a frequency half of E. CLK, which is fed back to produce clock signal 2fo double of the reference clock signal. This pin must be open when used with Hitachi's PLL (HD153202).
4 (4)	NRZ. T	OUT	Reproduces TTL-level NRZ signal which was converted from CMI code according to the conversion rule.	This pin must be open.
3 (3)	FRM. T	OUT	Reproduces TTL-level FRM signal when frame signals are superimposed on the CMI code.	This pin must be open.
5 (5)	CLK. T	OUT	Reproduces reference clock fo according to CMI and CLKP signals. NRZ. T, FRM. T and ERBIT. T are output synchronously with this clock.	This pin must be open.
2 (2)	ERBIT. T	OUT	Outputs signals with the same waveform as CLK. T's if illegal CMI code is input or if frame signal is superimposed on CMI code.	This pin must be open.

Parenthesized pin numbers are for the MP-44 package.

(to be continued)

Pin No.	Pin Name	IN/OUT	Function	
			TTL interface	ECL interface
40 (42)	PLIN. T	OUT	Used to generate T. CLKP (double clock signal 2fo) for reproduction; CMI and delayed CMI (input from T. DYIN) are Exclusive ORed to output signal having a frequency double of CMI. This pin must be open when used with Hitachi's PLL (HD153202).	This pin must be open.
9 (10)	NRZ. E	OUT	This pin must be open.	Reproduces ECL-level NRZ signal which was converted from CMI based on the conversion rule.
8 (9)	FRM. E	OUT	This pin must be open.	Reproduces ECL-level FRM signal when frame signals are superimposed on CMI code.
10 (11)	CLK. E	OUT	This pin must be open.	Reproduces reference clock signal fo based on CMI and CLKP signal. NRZ. E, FRM. E and ERBIT. E are output synchronously with this signal.
6 (7)	PLIN. E	OUT	This pin must be open.	This signal is used to generate E. CLKP (double clock signal fo) for reproduction; CMI and delayed CMI (input from T. DYIN) are Exclusive ORed to output signal having a frequency double of CMI. When used with Hitachi's PLL (HD153202) this pin must be open.
7 (8)	ERBIT. E	OUT	This pin must be open.	Outputs signal having the same waveform as CLK. E's when illegal CMI code is input or if frame signals are superimposed on CMI code.
41 (43)	ERR. T	OUT	If 2 bits or more in the 16 bits of the received CMI signal are in error, provides a high level signal during the subsequent 16-bit output.	If 2 bits or more in the 16 bits of the received CMI signal are in error, provides a high level signal with an amplitude of −4.4 to −3.2V during the subsequent 16-bit output.

Parenthesized pin numbers are for the MP-44 package.

Functional Description

1. Data transmission

(1) Converts NRZ signal to CMI code.
An NRZ signal synchronous with reference clock signal CLK is converted into CMI code.

(2) Two types of CMI code selectable for CMI 0 data
NRZ 0 can be converted into either 01 or 10 code for CMI 0 data; the high level Zero Set pin selects 01 and the low level Zero Set pin selects 10, as shown in Table 1 on the right.

(3) Superimposes frame signals which are synchronous with the CLK reference signal on CMI code. The value of CMI code with the frame superimposed is the reverse of the value when the frame is not superimposed.

2. Data Reception

(1) Converts CMI code to an NRZ signal.

(2) Detects frames
Detects frame signals which are superimposed on CMI code, and outputs them through the FRM. T or FRM. E pin.

(3) Detects error bits
Outputs an error bit signal to the ERBIT. T or ERBIT. E when an illegal conversion is performed or a frame signal is superimposed.

(4) Detects carrier
Outputs high level data via the ERR. T pin during a 16-bit period when the CMI code has a 2-bit-or-more error in 16 bits due to input break or other reasons.

(5) Protects synchronization
Inverts the phase of the reproduced reference clock (CLK) for synchronizing with the phase of CMI input signal, when the phase of CLK is different from that of CMI.

3. Code conversion examples

(1) NRZ-to-CMI conversion
As shown in table 2, NRZ signals are converted into CMI code according to the conversion table shown in Table 1. Output data have the delay times shown in figure 3.

(2) CMI-to-NRZ conversion
Examples of CMI-to-NRZ conversion are shown in table 3. Output data have the delay times shown in figure 4.

Table 1 CMI Data Conversion

ZERO SET	NRZ 0	NRZ 1
High	01	11 or 00
Low	10	11 or 00

CMI data 1 is converted alternately into 11 and 00.

Table 2 NRZ-to-CMI code conversion

Input	NRZ	1	0	0	1	1	1	0	0	0	1	0	0	1	1
	FRM	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Output	CMI *	11	01	01	00	00	11	01	01	01	00	01	01	11	00
	CMI **	11	10	10	00	00	11	10	10	10	00	10	10	11	00

* ZERO SET = High
** ZERO SET = Low

Table 3 CMI-to-NRZ code conversion

Input	CMI	11	01	01	00	00	11	01	01	01	00	01	01	11	00
Output	NRZ	1	0	0	1	1	1	0	0	0	1	0	0	1	1
	FRM	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	ERBIT	00	00	00	00	10	00	00	00	00	00	00	00	00	00

(Zero Set = High)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{CC}	7.0	V	For TTL interface
	V_{EE}	−7.0	V	For ECL interface
Input voltage	V_I	−0.5 to 5.5	V	For TTL interface
		0 to V_{EE}	V	For ECL interface
Power dissipation	P_d	830	mW	
Output current	I_O	−50	mA	ECL output
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−65 to +150	°C	

Electrical Characteristics

DC Characteristics-1 (for TTL interface)

[V_{EE} = 0 V, T_a = −20 to +75°C]

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}	–	–	140	mA	V_{CC} = 5.25V
Input voltage*1	V_{IH}	2.2	–	–	V	V_{CC} = 4.75V
	V_{IL}	–	–	0.7	V	V_{EE} = 5.25V
Output voltage*1	V_{OH}	2.7	–	–	V	V_{CC} = 4.75V, I_{OH} = −400 μA
	V_{OL}	–	–	0.5	V	V_{CC} = 4.75V, I_{OL} = 8 mA
Input current*1	V_{IH}	–	–	20	μA	V_{CC} = 5.25V, V_I = 2.7V
	V_{IL}	–	–	−400	μA	V_{CC} = 5.25V, V_I = 0.4V

Note *1 These apply to TTL inputs and outputs.

DC Characteristics-2 (for ECL interface)

[V_{CC} = 0 V, T_a = −20 to +75°C]

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	
Supply current	I_{EE}	–	–	130	mA	V_{EE} = −5.46V
Input voltage*2	V_{IH}	−0.5	–	−0.3	V	V_{EE} = −5.2V, Ta = 25°C
	V_{IL}	−2.5	–	−2.0	V	V_{EE} = −5.2V, Ta = 25°C
Output voltage*2	V_{OH}	−1.0	–	–	V	V_{EE} = −5.2V, V_{TT} = −2V 50Ω termination, Ta = 25°C
	V_{OL}	–	–	−1.6	V	V_{EE} = −5.2V, V_{TT} = −2V 50Ω termination, Ta = 25°C

Note *2 These apply to ECL inputs and outputs.

AC Characteristics (T_a=25°C)

Item	Symbol	32Mbps Version			16Mbps Version			Unit	Test Conditions
		min.	typ.	max.	min.	typ.	max.		
Maximum transmission rate	R_T	–	–	32	–	–	16	Mbps	
Transmitted signal delay*1	t_{CLK1}	–	1	–	–	1	–	bit	Fig. 3
	t_{DDS}	–	–	20	–	–	20	ns	Fig. 3
Transmitted signal set up time	t_{CSS}	8	–	–	8	–	–	ns	Fig. 1
Transmitted signal hold time	t_{CSH}	5	–	–	5	–	–	ns	Fig. 1
Received signal delay*2	t_{CLK2}	–	2	–	–	2	–	bit	Fig. 4
	t_{DDR}	–	–	20	–	–	20	ns	Fig. 4
Received clock delay	t_{CD}	–	–	20	–	–	20	ns	Fig. 4
Frame signal delay*3	t_{FD}	–	–	20	–	–	20	ns	Fig. 4
Error bit signal delay*4	t_{ED}	–	–	20	–	–	20	ns	Fig. 4
Error detection signal delay*5	t_{ERD}	–	–	20	–	–	20	ns	Fig. 5
Error detection signal output time	t_{ERR}	–	16	–	–	16	–	bit	Fig. 5
Received signal set up time	t_{CRS}	8	–	–	8	–	–	ns	Fig. 2
Received signal hold time	t_{CRH}	5	–	–	5	–	–	ns	Fig. 2

Notes) 1. Delay time taken for input signal is $t_{CSS} + t_{CLK1} + t_{DDS}$.
2. Delay time taken for input signal is $t_{CRS} + t_{CLK2} + t_{DDR}$.
3. Delay time taken for input signal is $t_{CRS} + t_{CLK2} + t_{FD}$.
4. Delay time taken for input signal is $t_{CRS} + t_{CLK2} + t_{ED}$.
5. Delay time taken for input signal is $t_{CRS} + t_{CLK2} + t_{ERD}$.

Timing chart

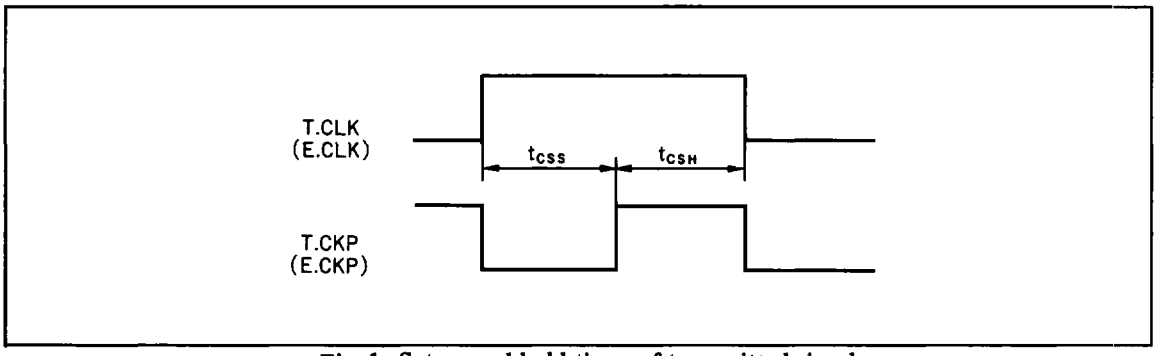


Fig. 1 Set up and hold times of transmitted signals

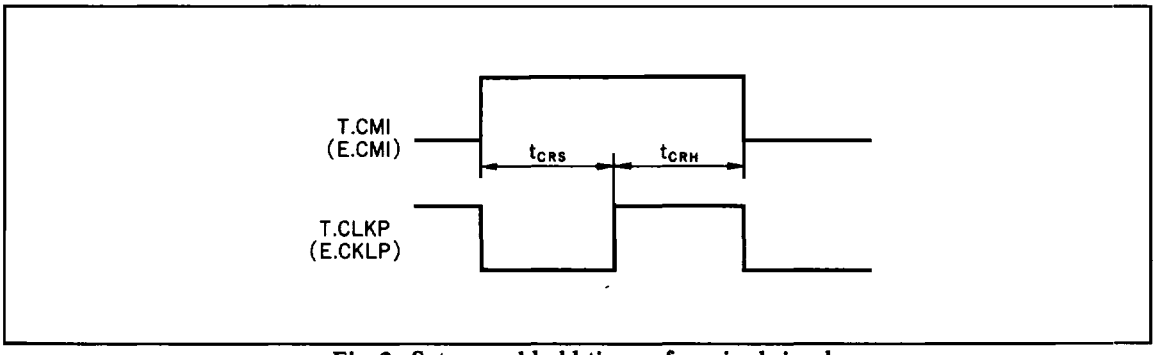


Fig. 2 Set up and hold times of received signals

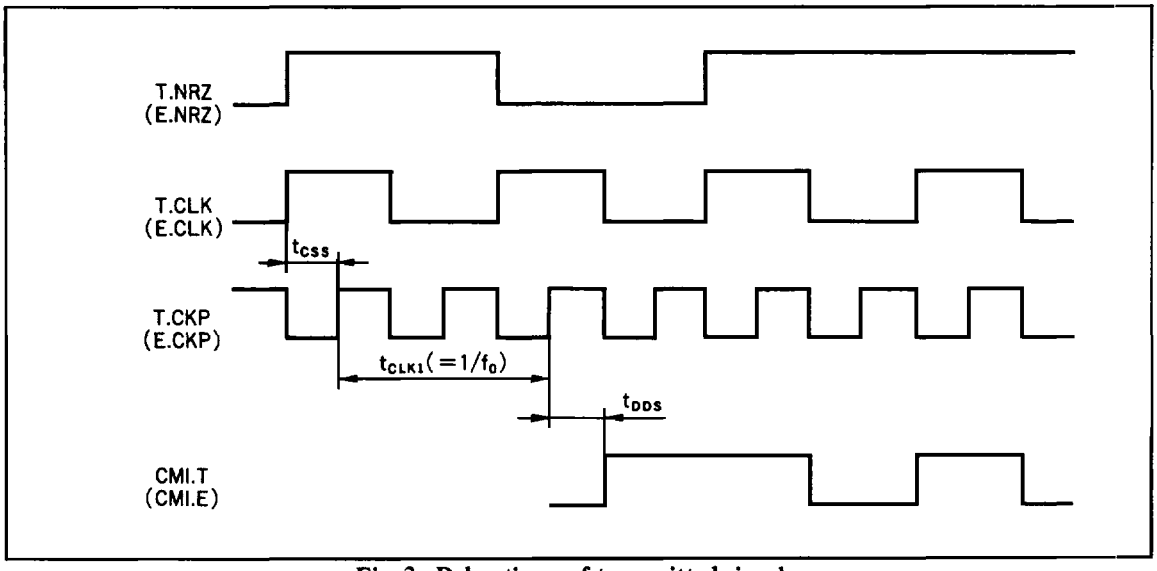


Fig. 3 Delay times of transmitted signals

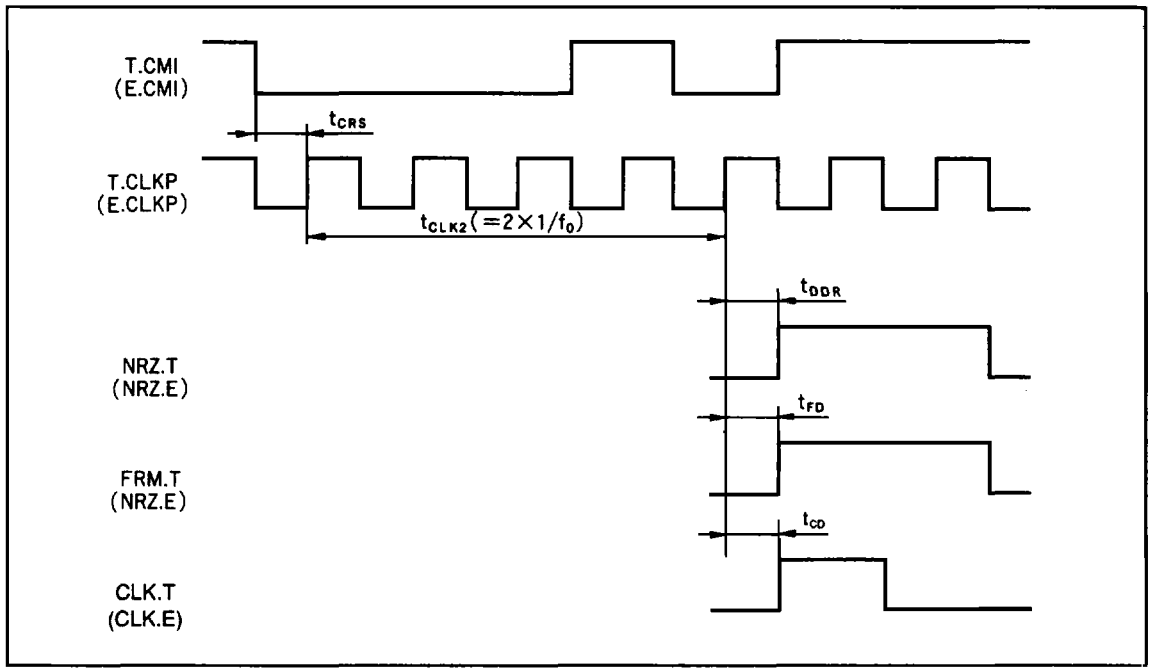


Fig. 4 Delay times of transmitted signals

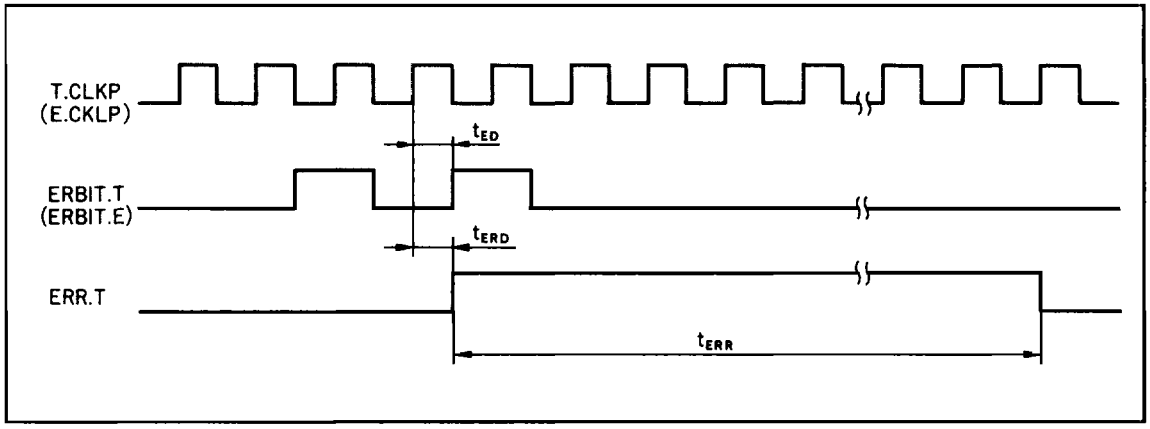
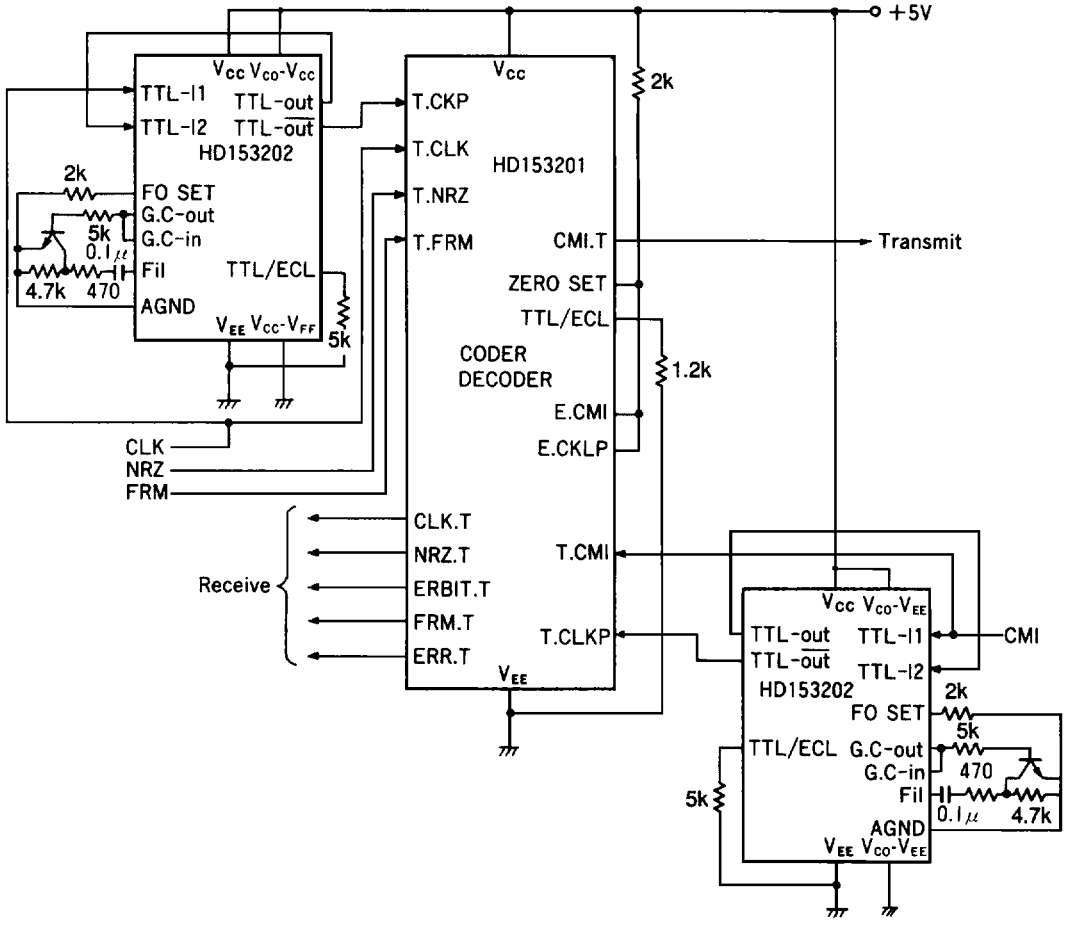


Fig. 5 ERR detect time

Example of connection with Hitachi PLL HD153202 (using TTL interface)



Note: The unused pins, which are not shown here, must be open.