ProSLIC® Single-Chip FXS Solution with Integrated Serial Interface (ISI)

Si32172/3/5 Features

- Complete FXS solution in 5 x 7 mm
- 3-wire ISI combines PCM, SPI, and interrupt data
- Performs all BORSCHT functions
- Ideal for short to medium loops
- Global programmability
- Internal balanced or unbalanced ringing
- Patented low power ringing
- Simplified configuration and diagnostics
- Supported by ProSLIC API
- Ultra low power consumption
- Integrated tracking dc-dc controller with direct connection to MOSFET
- Wideband voice support (Si32172/3)
- On-hook transmission
- Loop or ground start operation
- Smooth polarity reversal
- A-Law/μ-Law companding, linear PCM
- Software-programmable parameters:
  - Ringing frequency, amplitude, cadence, and waveshape
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (10-45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
- DTMF generation
- DTMF detection (Si32175)
- Pulse metering
- 3.3 V operation
- Support for 1.8 V I/O
- Maximum battery up to –140 V
- Pb-free/RoHS-compliant packaging

Applications

- Customer Premise Equipment (CPE)
- VoIP DSL Gateways and Routers
- Wireless Local Loop (WLL)
- Integrated Access Devices (IAD)
- Analog Terminal Adapters (ATA)
- Small Office/Home Office PBX

Description

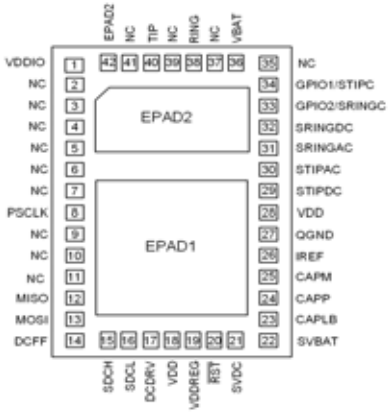
The Si32172/3/5 devices are pin-compatible single-channel ProSLIC products that implement a complete foreign exchange station (FXS) telephony interface solution in accordance with all relevant LSSGR, ITU, and ETSI specifications. The Si32172/3/5 ProSLIC ICs operate from a 3.3 V supply and use Silicon Labs' proprietary three-wire digital Integrated Serial Interface (ISI) with 3.3 V or 1.8 V I/O to connect to SoCs with the ISI pre-integrated. The Si32172/3/5 integrated dc-dc controller automatically generates the optimal battery voltages required for each linestate. Si32172/3/5 ICs are available with voltage ratings of –110 V or –140 V to support a wide range of ringing voltages. See the Ordering Guide for the voltage rating of each Si32172/3/5 version. The Si32172/3/5 devices are available in a 5x7 mm 42-pin QFN package.

Ordering Information

See page 37.

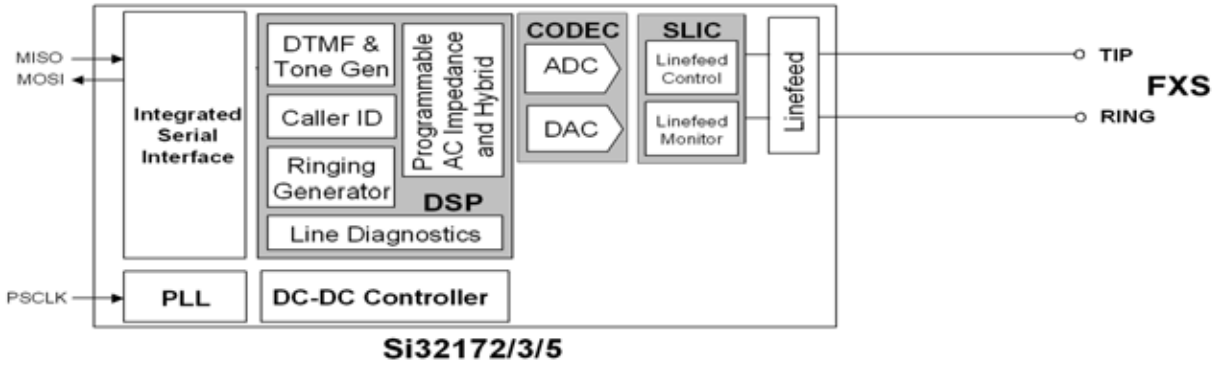
Pin Assignments

Si32172/3/5



Patents pending

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
		G-grade	–40	25	85	°C
Silicon Junction Temperature, QFN-42	T_{JHV}	Linefeed Die	—	—	145	°C
Supply Voltage, Si32172/3/5	V_{DD}		3.13	3.3	3.47	V
Battery Voltage, Si32172/5[2]	V_{BAT}		–110	–95	–15	V
Battery Voltage, Si32173[2]	V_{BAT}		–140	–130	–15	V
3.3 V IO Supply Voltage	V_{DDIO}		3.13	3.3	3.47	V
1.8 V IO Supply Voltage	V_{DDIO}		1.71	1.8	1.89	V

Notes:
1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Operation at minimum voltage dependent upon loop conditions and dc-dc converter configuration.

Table 2. Power Supply Characteristics

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Currents: Reset	I_{DD}	V_T and V_R = Hi-Z , RST = 0	—	6.3	—	mA
	I_{VBAT}		—	0	—	mA
Supply Currents: High Impedance, Open	I_{DD}	V_T and V_R = Hi-Z	—	20.8	—	mA
	I_{VBAT}		—	0.6	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V, Automatic Power Save Mode enabled	—	10.8	—	mA
	I_{VBAT}		—	0.6	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V, Automatic Power Save Mode disabled	—	31.2	—	mA
	I_{VBAT}		—	2.1	—	mA
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V V_R or V_T = Hi-Z, Automatic Power Save Mode enabled	—	10.9	—	mA
	I_{VBAT}		—	0.4	—	mA

Notes:
1. All specifications are for a single channel of Si3217x with a tracking flyback dc-dc converter.
2. I_{LOOP} is the dc current in the subscriber loop during the off-hook state.

Table 2. Power Supply Characteristics (Continued)

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V V_R or V_T = Hi-Z, Automatic Power Save Mode disabled	—	30.6	—	mA
	I_{VBAT}		—	1.3	—	mA
Supply Currents: Forward/Reverse OHT, On-hook	I_{DD}	V_{TR} =48 V,	—	43.8	—	mA
	I_{VBAT}		—	2.9	—	mA
Supply Currents: Forward/Reverse Active, Off-hook	I_{DD}	I_{LOOP} = 20 mA R_{LOAD} = 200 Ω,	—	44.6	—	mA
	I_{VBAT}		—	21.3	—	mA
Supply Currents: Ringing	I_{DD}	V_{TR} =55V_{RMS} + 0 V_{DC}, balanced, sinusoidal, f = 20 Hz, RLOAD = 5 REN = 1400 Ω	—	35.8	—	mA
	I_{VBAT}		—	37.5	—	mA

Notes:
1. All specifications are for a single channel of Si3217x with a tracking flyback dc-dc converter.
2. I_{LOOP} is the dc current in the subscriber loop during the off-hook state.

Table 3. AC Characteristics for FXS

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Level		2.5	—	—	V_{PK}
Overload Compression	2-Wire – PCM	Figure 3	—	—	
Single Frequency Distortion[1]	2-Wire – PCM or PCM – 2-Wire: 200 Hz to 3.4 kHz	—	—	–40	dB
	PCM – 2-Wire – PCM: 200 Hz – 3.4 kHz, 16-bit Linear mode	—	—	–63	dB
Signal-to-(Noise + Distortion) Ratio[2]	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any Z_T	Figure 2	—	—	

Notes:
1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as V_{TIP} – V_{RING}. Assumes ideal line impedance matching.
3. The quantization errors inherent in the μ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DD}, V_{DDIO} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
6. 0 dBm 0 is equal to 0 dBm into 600 Ω.

Table 3. AC Characteristics for FXS (Continued)

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Test Condition	Min	Typ	Max	Unit
Audio Tone Generator Signal-to-Distortion Ratio[2]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy[2]	2-Wire to PCM or PCM to 2-Wire 1014 Hz, Any gain setting	–0.2	—	0.2	dB
Attenuation Distortion vs. Frequency	0 dBm 0[6]	See Figure 16 and 17			
Group Delay vs. Frequency		See Figure 18 and 19			
Gain Tracking[3]	1014 Hz sine wave, reference level –10 dBm Signal level:	—	—	—	—
	3 dB to –37 dB	—	—	0.25	dB
	–37 dB to –50 dB	—	—	0.5	dB
	–50 dB to –60 dB	—	—	1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
2-Wire Return Loss[4]	200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance[4]	300 Hz to 3.4 kHz	26	30	—	dB
Noise Performance					
Idle Channel Noise[5]	C-Message weighted	—	8	12	dBrnC
	Psophometric weighted	—	–82	–78	dBmP
PSRR from V_{DD}, V_{DDIO} @ 3.3 V	RX and TX, 200 Hz to 3.4 kHz	—	55	—	dB
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 Hz to 1 kHz	58	60	—	dB
	1 kHz to 3.4 kHz	53	58	—	dB
Metallic/PCM to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current Capability	Active off-hook 60 Hz Reg 73 = 0x0B	—	25	—	mA

Notes:

1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DD}, V_{DDIO} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
6. 0 dBm 0 is equal to 0 dBm into 600 Ω.

Table 4. Linefeed Characteristics for FXS

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Loop Resistance	R_{LOOP}	$R_{DC,MAX}$ = 430 Ω I_{LOOP} = 18 mA, V_{BAT} = –52 V, R_{PROT} = 0 Ω	—	—	2000	Ω
DC Feed Current		Differential	—	—	45	mA
		Common Mode	—	—	30	mA
		Differential + Common Mode	—	—	45	mA
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	—	640	Ω
DC On-Hook Voltage Accuracy—Ground Start	V_{OHTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground, V_{RING} = –51 V	—	—	4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	160	—	640	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	400	—	—	kW
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ring Trip Threshold Accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80mA	—	—	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	—	—	1	mA
		DC Detection, 48 V DC offset, R_{loop} = 1500 Ω	—	—	3	mA
Ringing Amplitude*	$V_{RINGING}$	Si32172/5 Open circuit, V_{BAT} = –110 V	108	—	—	V_{PK}
		Si32173 Open circuit, V_{BAT} = –140 V	132	—	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}	Si32172/5 : 60 V_{RMS}, 15 V_{OFFSET}, 0–5 REN	—	1	—	%
		Si32173 : 55 V_{RMS}, 48 V_{OFFSET}, 0–5 REN				
Ringing Frequency Accuracy		f = 16 Hz to 60 Hz	—	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	50	ms
Loop Voltage Sense Accuracy		$V_{TIP} – V_{RING}$ = 48 V	—	2	4	%

Table 4. Linefeed Characteristics for FXS (Continued)

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Current Sense Accuracy		I_{LOOP} = 18 mA	—	7	10	%
Power Alarm Threshold Accuracy		Power Threshold = 1.0 W V_{BAT} = –56 V, I_{LDDD} = 40 mA, R_{LOAD} = 600 Ω	—	15	—	%
Test Load Impedance	R_{TEST}	HVIC_STATE_SPARE[23] = 1; $\lvert V_{T/R} \rvert \leq 50$ V	—	2.2	—	kΩ
Test Load Voltage	V_{TL}	HVIC_STATE_SPARE[23] = 1	±5		±50	V
***Note:** Ringing amplitude is set for 108 or 128 V peak and measured at TIP-RING using no series protection resistance.						

Table 5. Digital I/O Characteristics

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DDIO}	—	V_{DDIO}	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}	V
High Level Output Voltage*	V_{OH}		V_{DDIO} – 0.6	—	—	V
Low Level Output Voltage*	V_{OL}	I_O = 4 mA	—	—	0.4	V
$\overline{RST}$ Internal Pullup Current			33	42	65	µA
Input Leakage Current	I_L		—	—	10	µA

Table 6. Charge Pump Characteristics

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage (DCDRV, DCFF)	V_{CP}		2 x V_{DD} – 1	—	2xV_{DD}	V
Output Current	I_{CP}		—	—	3*	mA
***Note:** Peak drive current capability is >60 mA.						

Table 7. Switching Characteristics—General Inputs*

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, $\overline{RST}$	t_r	—	—	5	ns
$\overline{RST}$ Pulse Width	t_{rl}	396/ PSCLK	—	—	µs

***Note:** All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_{DD} – 0.4$ V, $V_{IL} = 0.4$ V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.

Table 8. Switching Characteristics—ISI

T_A = 0 to 70 °C (F grade) or –40 to +85 °C (G grade) unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Setup Time, MOSI to PSCLK Fall	t_{su}	7.5	—	—	ns
Hold Time, MOSI to PSCLK Fall	t_h	5	—	—	ns
Delay Time, PSCLK Rise to MISO	t_d	—	—	16	ns
PSCLK Period	t_p	—	40.69	—	ns
PSCLK Duty Cycle		40	50	60	%

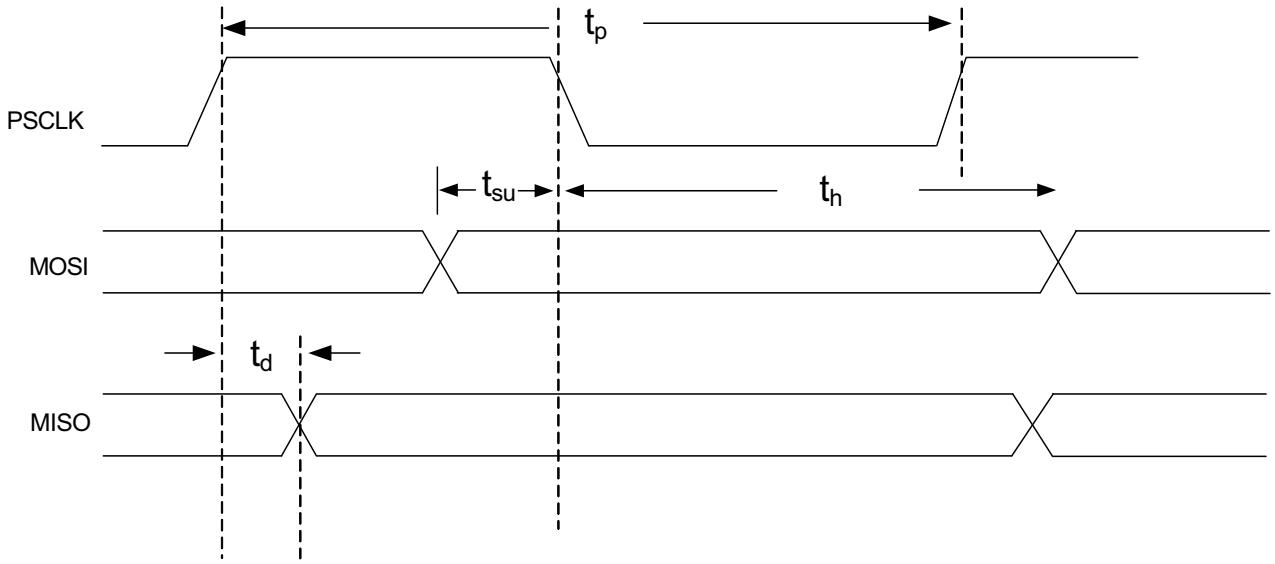


Figure 1. ISI Timing Diagram

Table 9. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		–55 to 150	°C
Thermal Resistance, Typical[1] QFN-42	θ_{JA} θ_{JB} θ_{JC}		53 33 39	°C/W
Continuous Power Dissipation[2,3] QFN-42	P_D	T_A = 85 °C	0.75	W
Maximum Junction Temperature, QFN-42 (Linefeed Die)	T_{JHV}	Continuous	145	°C
Maximum Junction Temperature QFN-42 (Low Voltage Die)	T_{JLV}		125	°C

Notes:
1. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane. Thermal resistance values are empirical measurements taken from Silicon Labs EVBs.
2. Operation above 125 °C junction temperature may degrade device reliability. Thermal resistance values are empirical measurements taken from Silicon Labs EVBs.
3. The linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold should normally be set to 145 °C; when in the ringing state with cadence the thermal shutdown may be set to 200 °C. For optimal reliability long term operation of the linefeed above 150 °C junction temperature should be avoided.

Table 10. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Value	Unit
Supply Voltage	V_{DD}, V_{DDIO}		–0.5 to 4.0	V
Digital Input Voltage	V_{IND}		–0.3 to 3.6	V
Battery Supply Voltage[2], Si32172/5	V_{BAT}		+0.4 to –115	V
Battery Supply Voltage[3], Si32173	V_{BAT}		+0.4 to –142	V
Tip or Ring Voltage, Si32172/5[3]	V_{TIP}, V_{RING}		–130	V
Tip or Ring Voltage, Si32173[3]	V_{TIP}, V_{RING}		–142	V
TIP, RING Current	I_{TIP}, I_{RING}		±100	mA

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.
2. The dv/dt of the voltage applied to the VBAT pins must be limited to 10 V/µs.
3. Specification requires circuit for surge event as shown in typical application circuit.

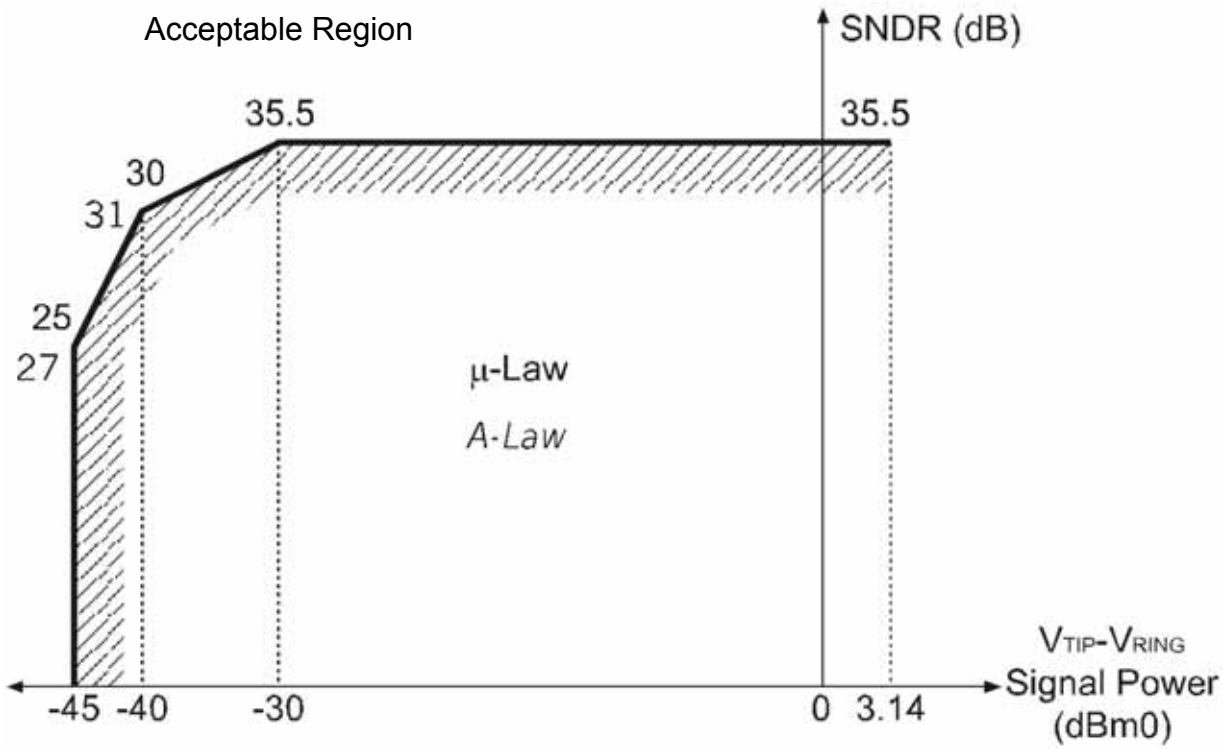


Figure 2. Transmit and Receive Path SNDR

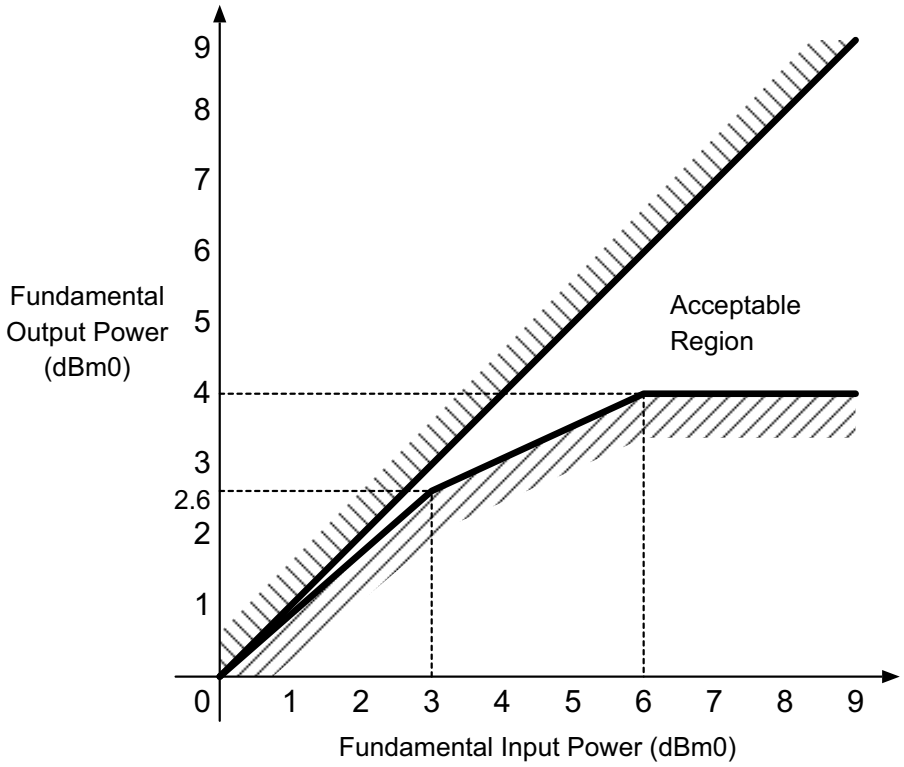


Figure 3. Overload Compression Performance

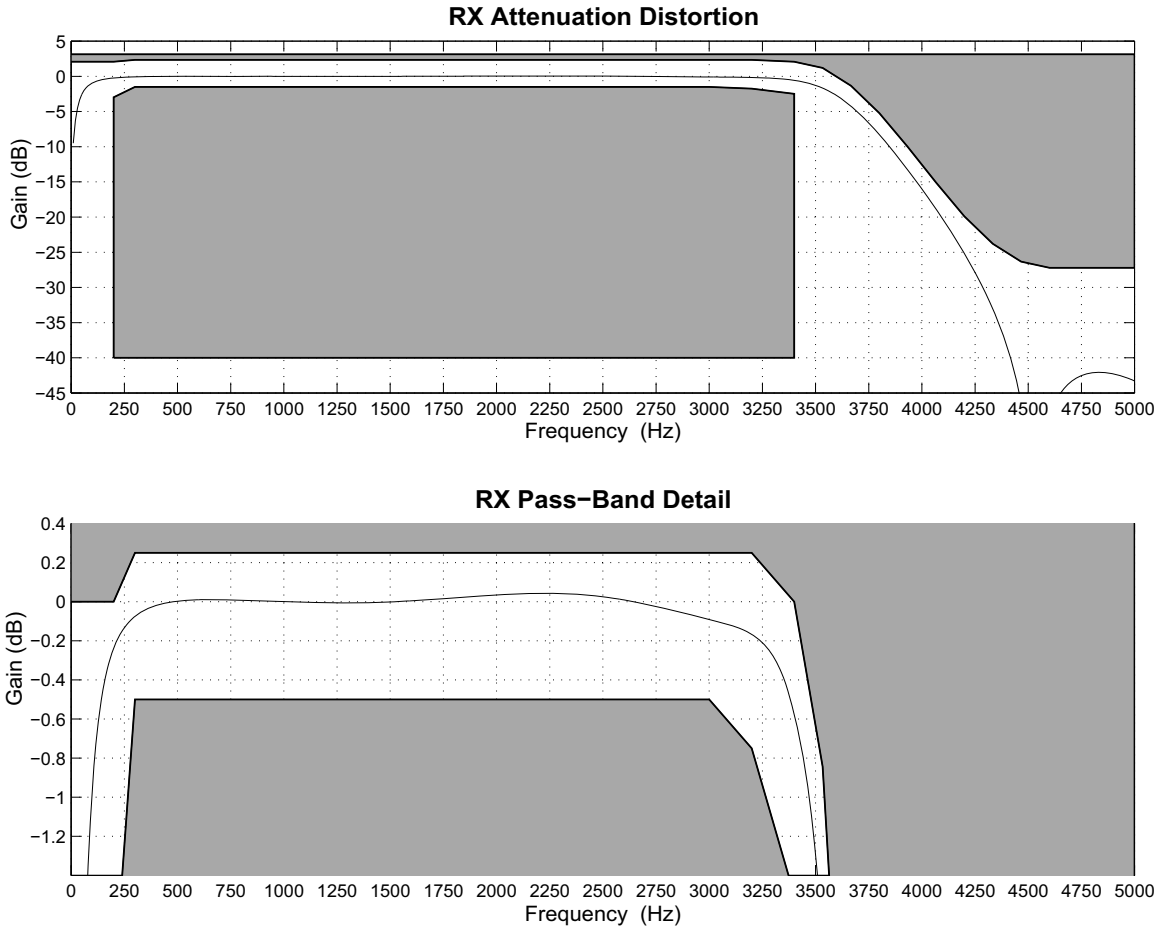


Figure 4. Receive Path Frequency Response

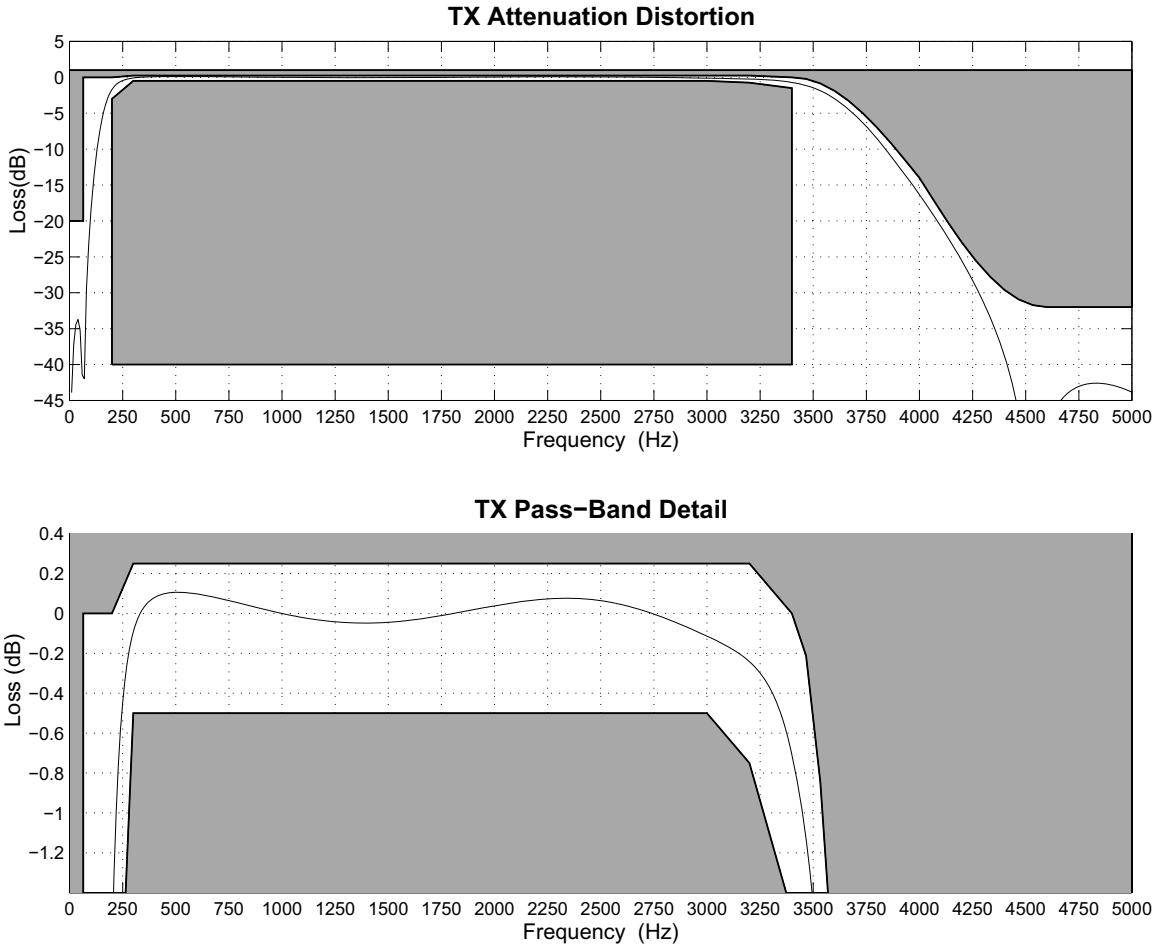


Figure 5. Transmit Path Frequency Response

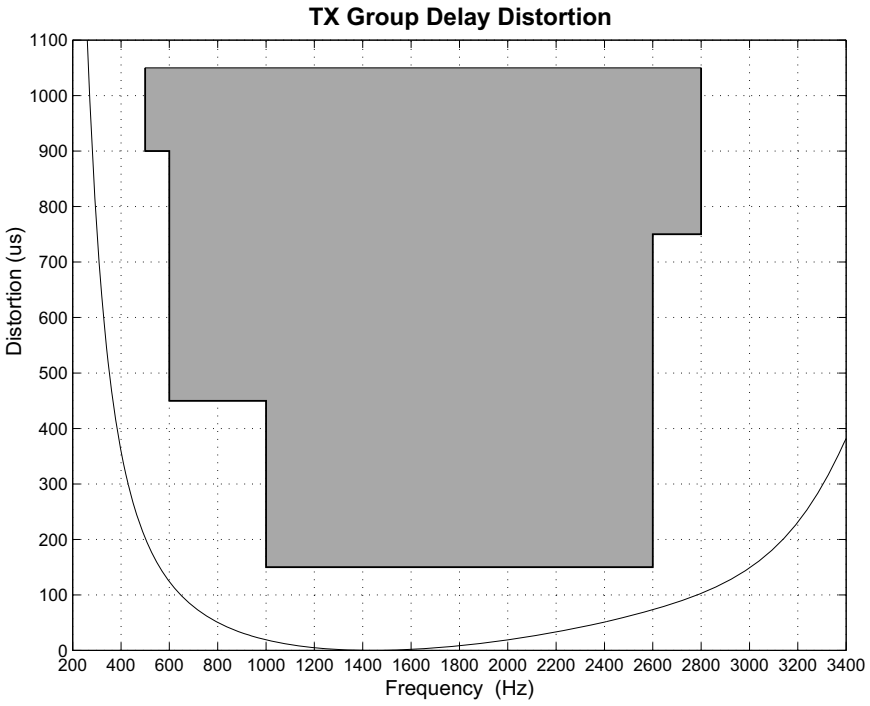


Figure 6. Transmit Group Delay Distortion

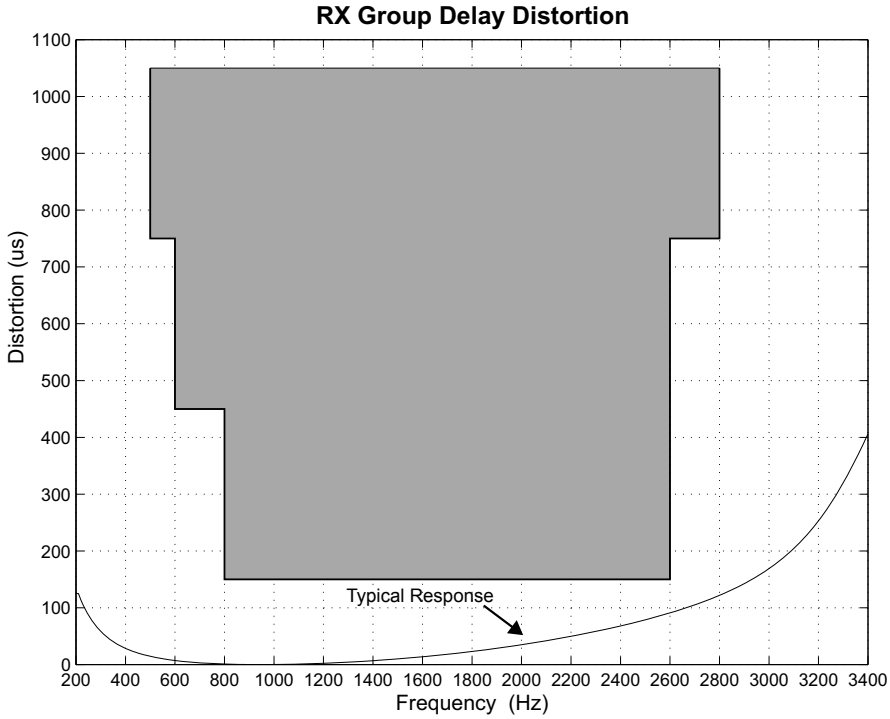


Figure 7. Receive Group Delay Distortion

2. Schematics

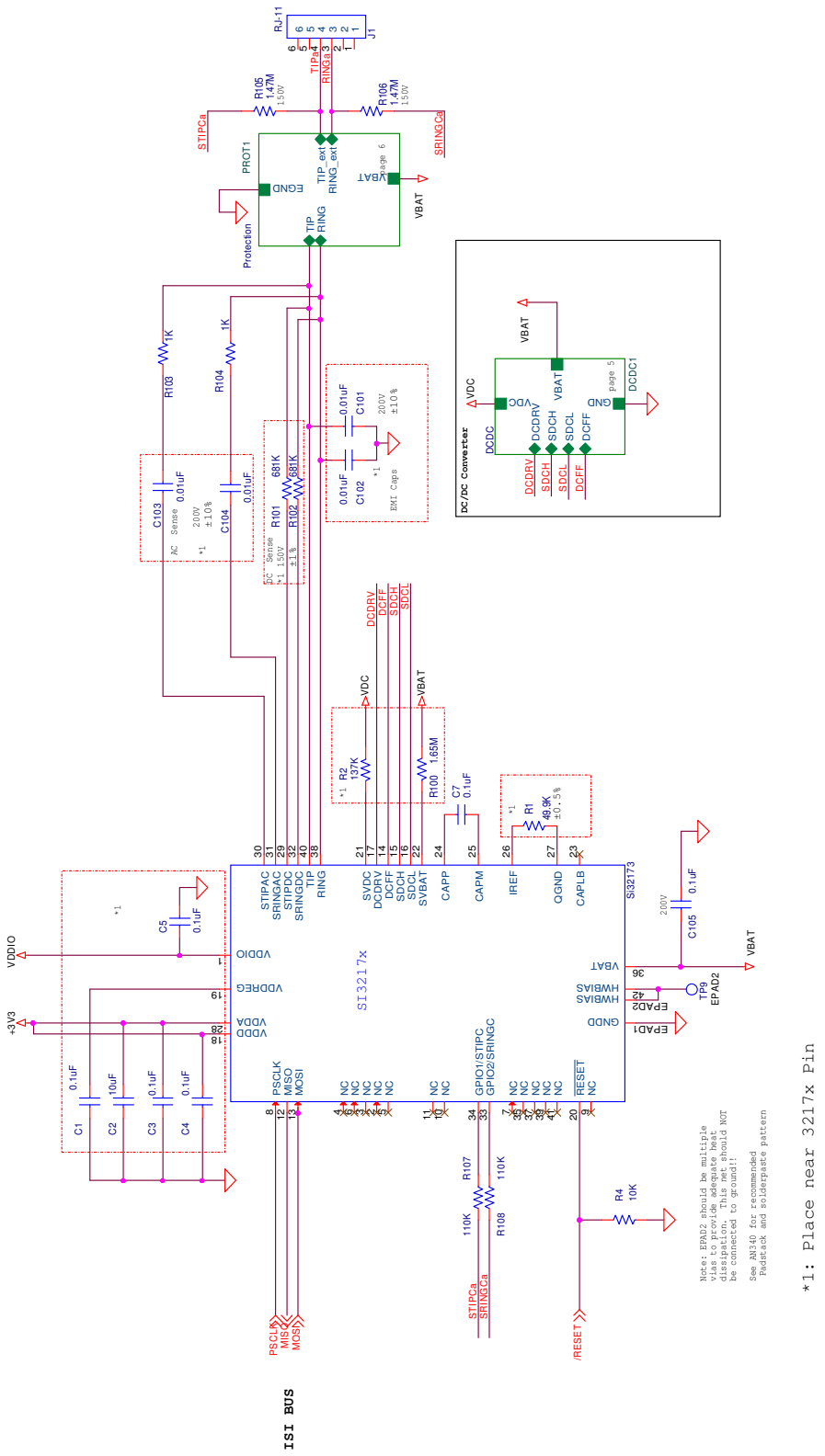


Figure 8. Top Level Schematic

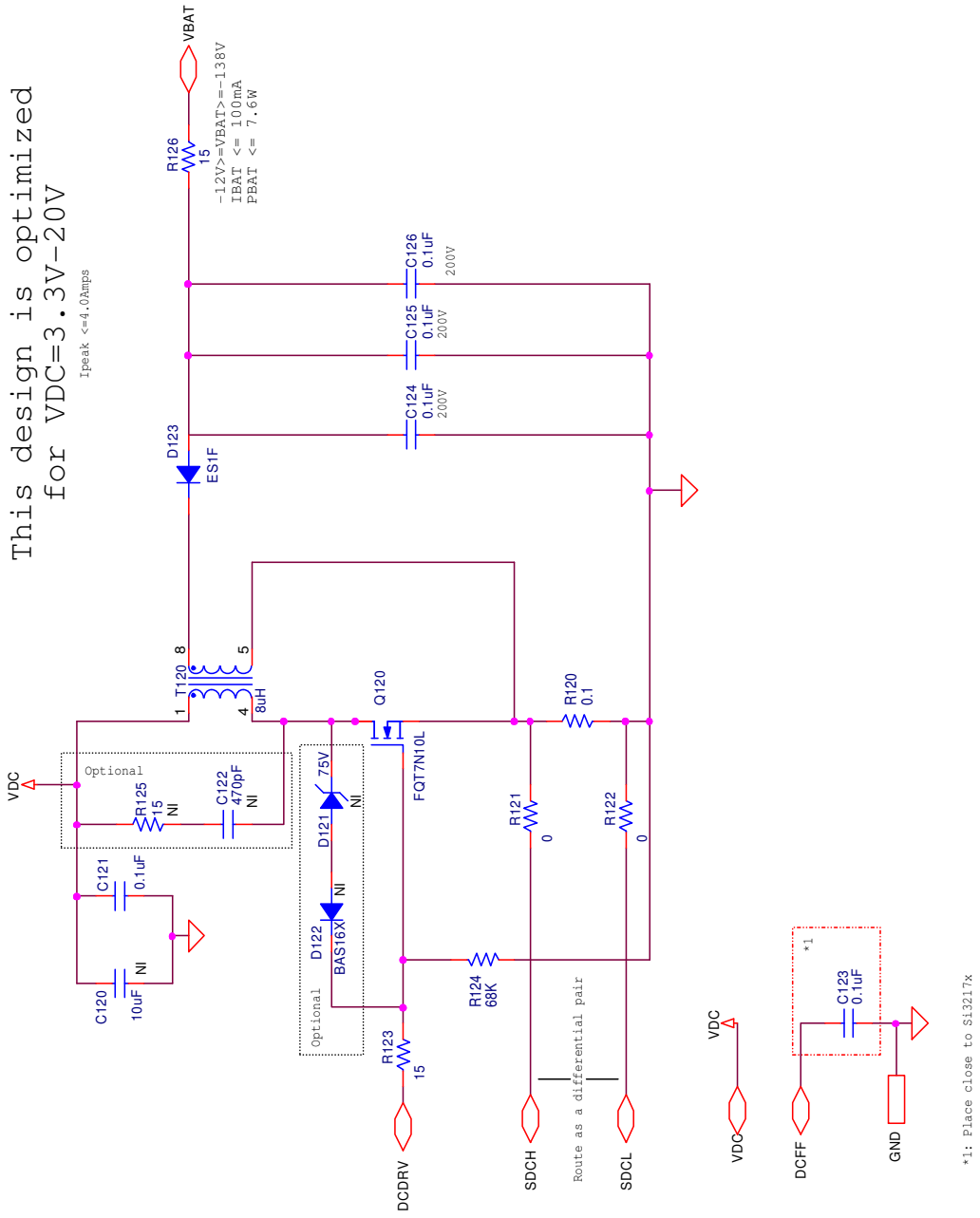


Figure 9. Flyback DC DC Option

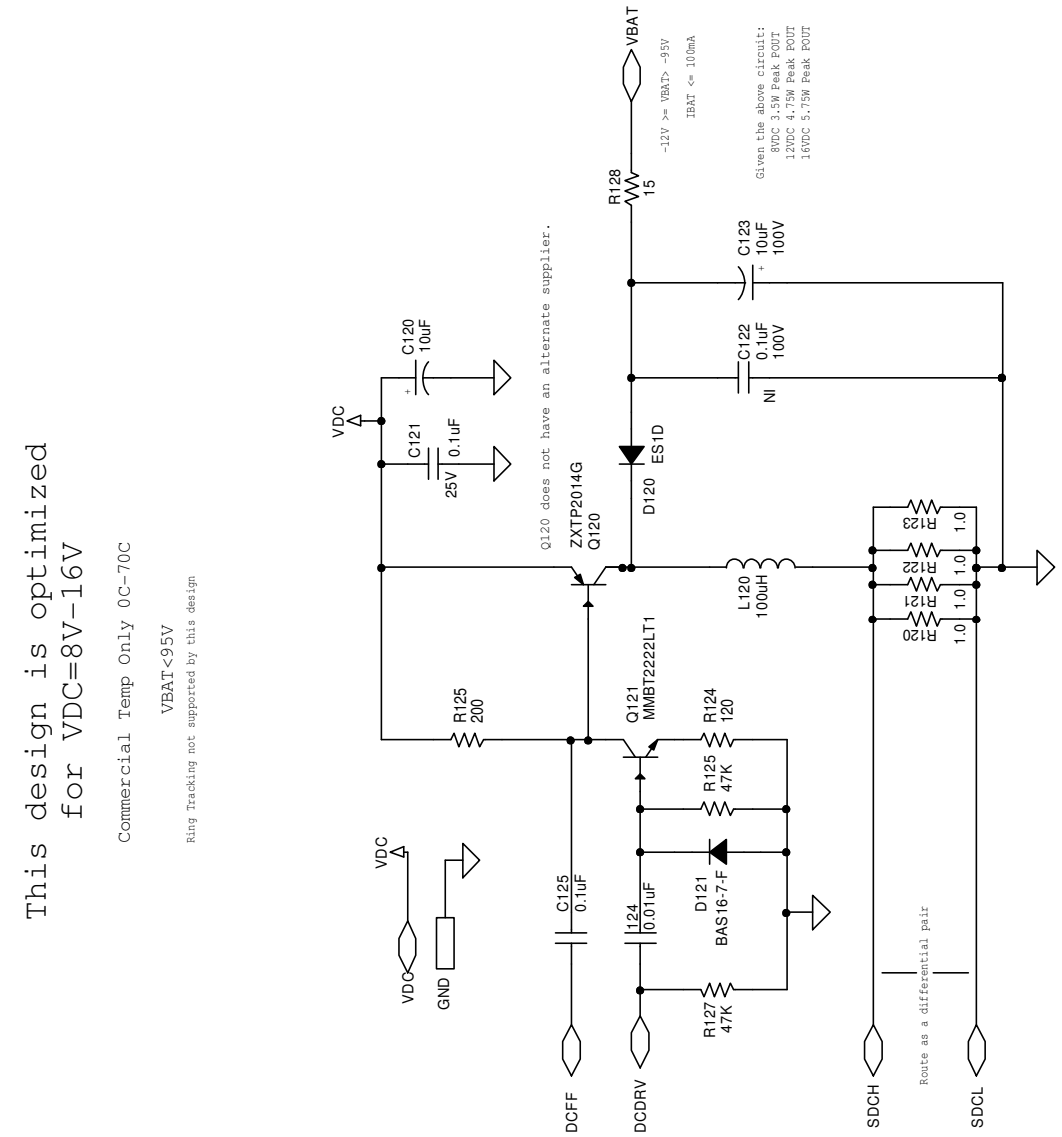


Figure 10. BJT Buck Boost DC-DC Option

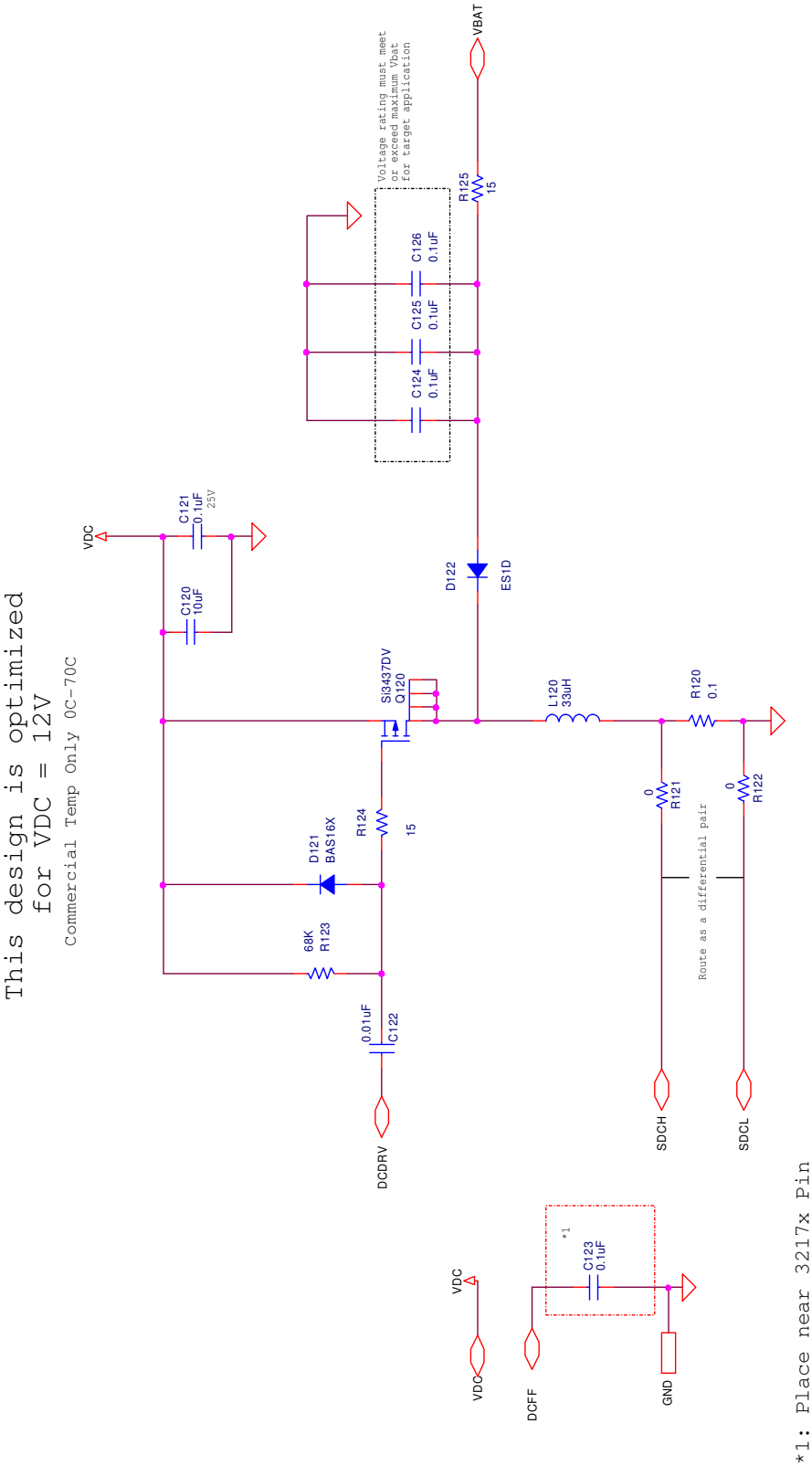


Figure 11. PMOS Buck Boost DC-DC Option

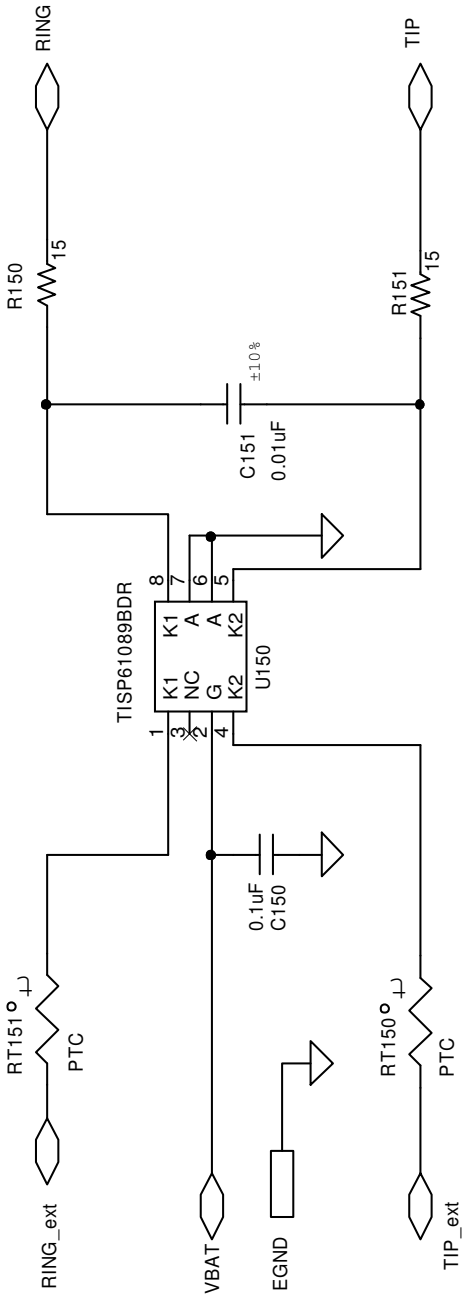


Figure 12. Protection

3. Bill of Materials

Table 11. Top Level Bill of Materials

Reference	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C1 C3 C4 C5 C7	0.1 µF		10V	±10%	X7R	C0402	C0402X7R100-104K	Venkel
C2	10 µF		6.3V	±20%	X5R	C0603	C0603X5R6R3-106M	Venkel
C101 C102 C103 C104	0.01 µF		200V	±10%	X7R	C0805	C0805X7R201-103K	Venkel
C105	0.1 µF		200V	±20%	X7R	C1206	C1206X7R201-104M	Venkel
R1	49.9K	1/16W		±0.5%	ThickFilm	R0603	CR0603-16W-4992D	Venkel
R2	137K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-2673F	Venkel
R3 R4	10K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-103J	Venkel
R100	1.65M	1/10W		±1%	ThickFilm	R0805	CR0805-10W-1654F	Venkel
R101 R102	681K	1/10W		±1%	ThickFilm	R0805	CR0805-10W-6813F	Venkel
R103 R104	1K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-1001F	Venkel
R105 R106	1.47M	1/8W		±1%	ThickFilm	R1206	CR1206-8W-1474F	Venkel
R107 R108	110K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-1103F	Venkel
U1	Si32173		140V		MCM	LGA42M5X 7P0.5	Si32173-C-GM1	SiLabs

Table 12. Flyback Bill of Materials

Reference	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C120 (Not Installed)	10 µF		25	±20%	X7R	C1210	C1210X7R250-106M	Venkel
C122 (Not Installed)	470 pF		100	±10%	X7R	C0603	C0603X7R101-471K	Venkel
C127 (Not Installed)	0.1 µF		200	±20%	X7R	C1206	C1206X7R201-104M	Venkel
D121 (Not Installed)	75 V	200mW	75		Zener	SOD-323	BZX384C75-V	Vishay
D122 (Not Installed)	BAS16X	200mA	75		Switch	SOD-523	BAS16XV2T1G	On Semi
R125 (Not Installed)	15	1/2W		±5%	ThickFilm	R1210	CR1210-2W-150J	Venkel
C121	0.1 µF		50	±10%	X7R	C0603	C0603X7R500-104K	Venkel
C123	0.1 µF		10	±10%	X7R	C0402	C0402X7R100-104K	Venkel
C124 C125 C126	0.1 µF		200	±20%	X7R	C1206	C1206X7R201-104M	Venkel
D123	ES1F	1.0A	300		Fast	DO-214AC	ES1F	Fairchild
Q120	FQT7N10L	1.7A	100		N-CHNL	SOT223-GDS	FQT7N10L	Fairchild
R120	0.1	1/2W		±1%	ThickFilm	R1210	LCR1210-R100F	Venkel
R121 R122	0	1A			ThickFilm	R0402	CR0402-16W-000	Venkel
R123	15	1/16W		±1%	ThickFilm	R0402	CR0402-16W-15R0F	Venkel
R124	68K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-683J	Venkel
R126	15	1/2W		±5%	ThickFilm	R1210	CR1210-2W-150J	Venkel
T120	8 µH	4A				XFMR-UTB01701s	UTB01890s	UMEC

Table 13. BJT Buck Boost Bill of Materials

Reference	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C122	0.1 uF		100	±20%	X7R	C0603	C0603X7R101-104M	Venkel
C120 C123	10 uF		100	±20%	Alum_Elec	C2X5MM-RAD	ECA2AM100	Panasonic
C121 C125	0.1 uF		25	±20%	X7R	C0603	C0603X7R250-104M	Venkel
D120	ES1D	1.0A	200		Single	DO-214AC	ES1D	Diodes Inc.
D121	BAS16-7-F	300mA	75		Single	SOT23-AXK	BAS16-7-F	Diodes Inc.
L120	100 uH	3.64A		±20%	Shielded	IND-SPD	DR127-101-R	Cooper Bussman
Q120	ZXTP2014G	4A	140		PNP	SOT223-BCE	ZXTP2014G	Zetex
Q121	MMBT2222LT1	600mA	30		NPN	SOT23-BEC	MMBT2222LT1	On Semi
R120 R121 R122 R123	1	1/16W		±1%	ThickFilm	R0402	CR0402-16W-1R00F	Venkel
R124	120	1/10W		±1%	ThickFilm	R0603	CR0603-10W-1200F	Venkel
R125 R127	47K	1/16W		±1%	ThickFilm	R0402	CR0402-16W-4702F	Venkel
R125	200	1/10W		±1%	ThickFilm	R0603	CR0603-10W-2000F	Venkel
R128	15	1/10W		±1%	ThickFilm	R0805	CR0805-10W-15R0F	Venkel
C124	0.01uF		10	±20%	X7R	C0402	C0402X7R100-103M	Venkel

Table 14. PMOS Buck Boost Bill of Materials

Reference	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C120	10 µF		16	±10%	X5R	C0805	C0805X5R160-106K	Venkel
C121	0.1 µF		25	±20%	X7R	C0603	C0603X7R250-104M	Venkel
C122	0.01 µF		25	±10%	X7R	C0402	C0402X7R250-103K	Venkel
C123	0.1 µF		10	±10%	X7R	C0402	C0402X7R100-104K	Venkel
C124 C125 C126	0.1 µF		200	±20%	X7R	C1206	C1206X7R201-104M	Venkel
D121	BAS16X	200mA	75		Switch	SOD-523	BAS16XV2T1G	On Semi
D122	ES1D	1.0A	200		Fast	DO-214AC	ES1D	Diodes Inc.
L120	33 µH	1.4A		±20%	Shielded	IND-NR6045	NR 6045T 330M	Taiyo Yuden
Q120	Si3437DV	1.4A	–150		P-CHNL	TSOP6N2.85P0.95	Si3437DV	Vishay
R120	0.1	1/2W		±1%	ThickFilm	R1206	LCR1206-R100F	Venkel
R121 R122	0	1A			ThickFilm	R0402	CR0402-16W-000	Venkel
R123	68K	1/16W		±5%	ThickFilm	R0402	CR0402-16W-683J	Venkel
R124	15	1/16W		±1%	ThickFilm	R0402	CR0402-16W-15R0F	Venkel
R125	15	1/10W		±1%	ThickFilm	R0805	CR0805-10W-15R0F	Venkel

Table 15. Protection Bill of Materials

Reference	Value	Rating	Volt	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
C150	0.1 µF		200	±20%	X7R	C1206	C1206X7R201-104M	Venkel
C151	0.01 µF		200	±10%	X7R	C0805	C0805X7R201-103K	Venkel
RT150 RT151	PTC	3A	250		TelCom	PTC-MF-SM013/250V	MF-SM013/250V	Bourns
R150 R151	15	1/10W		±1%	ThickFilm	R0805	CR0805-10W-15R0F	Venkel
U150	TISP61089BDR		–150		SLIC	SO8N6.0P1.27	TISP61089BDR	Bourns

4. Functional Description

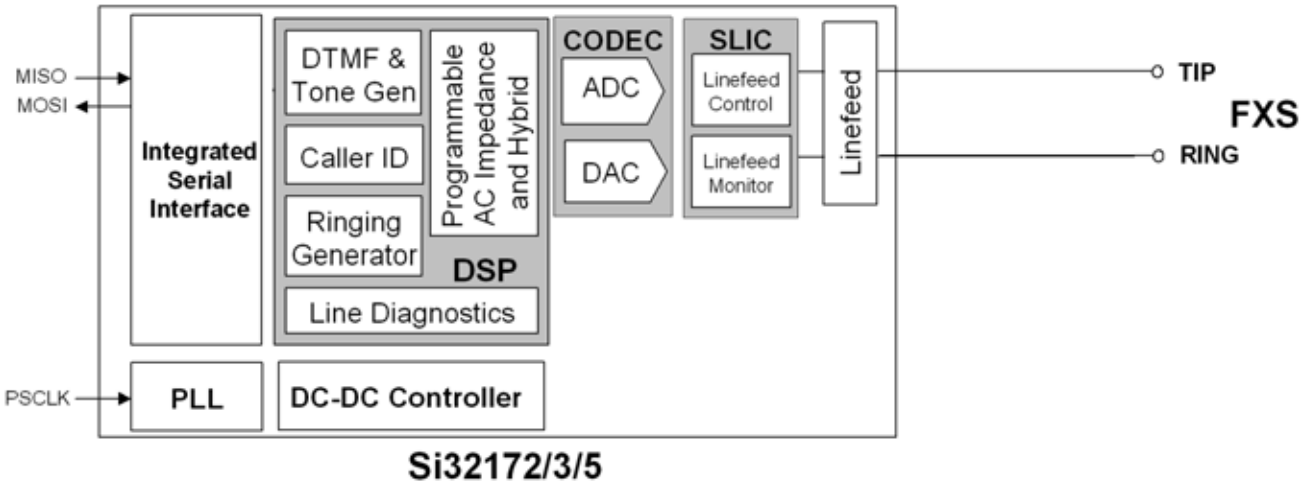


Figure 13. Si32172/3/5 Functional Block Diagram

The Si32172/3/5 series provides all SLIC, codec, DTMF detection, and signal generation functions needed for one complete analog telephone interface. The Si32172/3/5 performs all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions; it also supports extensive metallic loop testing capabilities.

The Si32172/3/5 provides a standard voice-band (200 Hz–3.4 kHz) audio codec and, optionally, an audio codec with both wideband (50 Hz–7 kHz) and standard voice-band modes. The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality while the standard voice-band mode provides standard telephony audio bandwidth. The Si32172/3/5 incorporates a programmable dc-dc converter controller that reacts to line conditions to provide the optimal battery voltage required for each line-state. Si32172/3/5 ICs are available with voltage ratings of –110 V or –140 V to support a wide range of ringing voltages; see "9. Ordering Guide," on page 37 for the voltage rating of each Si32172/3/5 version.

Programmable on-hook voltage, programmable off-hook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission are supported. Loop current and voltage are continuously monitored by an integrated monitoring ADC.

The Si32172/3/5 supports balanced 5 REN ringing with or without a programmable dc offset. The available voltage offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements.

5. FXS Features

5.1. DC Feed Characteristics

ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics.

When in the active state, the ProSLIC operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in Figure 14. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

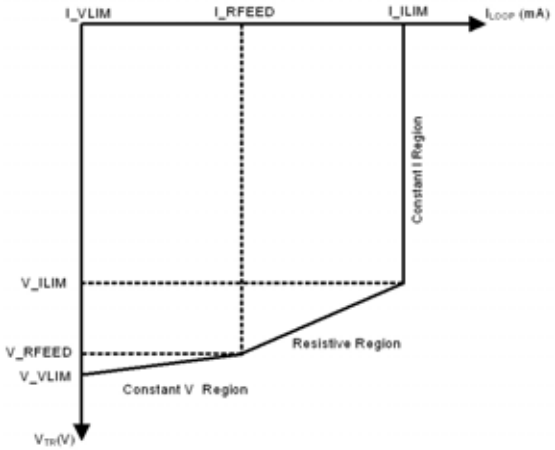


Figure 14. Dual ProSLIC DC Feed Characteristics

5.2. Linefeed Operating States

The linefeed interface includes eight different register-programmable operating states as listed in Table 16. The Open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

5.3. Line Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip ADC and stores the resulting values in individual RAM locations. Additionally, the loop voltage (V_{TIP}–V_{RING}), loop current, and longitudinal current values are calculated based on the TIP and RING measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

6. Power Monitoring and Power Fault Detection

The Si32172/3/5 line monitoring functions are used to continuously protect against excessive power conditions. The Si32172/3/5 contains an on-chip, analog sensing diode that provides real-time temperature data and turns off the device when a preset threshold is exceeded.

If the Si32172/3/5 detects a fault condition or overpower condition, it automatically sets that device to the open state and generates a "power alarm" interrupt.

The interrupt can be masked, but masking the automatic transition to open is not recommended since it is used to protect the Si3217x HVIC under excessive power conditions.The various power alarms and linefeed faults supporting automatic intervention are described below.

1. Total power exceeded.
2. Excessive foreign current or voltage on TIP and/or RING.
3. Thermal shutdown event.

6.1. Thermal Overload Shutdown

If the die temperature exceeds the maximum junction temperature threshold, TJmax, of 145 °C or 200 °C, the device has the ability to shut itself down to a low-power state without user intervention. The thermal shutdown circuit contains a sufficient amount of hysteresis and/or turn-on delay time so as to remain shut down during a power cross event, where 50 Hz or 60 Hz, 600 V, is connected to TIP and/or RING.

Table 16. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance, and all line supervision functions are powered down. Audio is powered down. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high impedance state during linefeed testing. A power fault condition may also force the device into the open state.
Forward Active Reverse Active	Linefeed circuitry and audio are active. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead. Loop closure and ground key detect circuitry are active.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.
TIP Open	Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (>400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
RING Open	Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (>400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto TIP and RING leads with or without dc offset.
Line Diagnostics	The channel is put into diagnostic mode. In this mode, the channel has special diagnostic resources available.

6.2. Loop Closure Detection

The Si32172/3/5 provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

6.3. Ground Key Detection

The Si32172/3/5 provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

6.4. Ringing Generation

The Si32172/3/5 provides the ability to generate a programmable sinusoidal or trapezoidal ringing waveform, with or without dc offset. The ringing frequency, wave shape, cadence, and offset are all register-programmable. Three ringing modes are supported: balanced, unbalanced, and low-power ringing (LPR). Figure 15 illustrates the fundamental differences between the three ringing modes.

6.5. Polarity Reversal

The Si32172/3/5 supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

6.6. Two-Wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Si32172/3/5 to the reference impedance. Most real or complex two-wire impedances can be generated with appropriate register coefficients.

6.7. Transhybrid Balance Filter

The trans-hybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path.

6.8. Tone Generators

The Si32172/3/5 includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

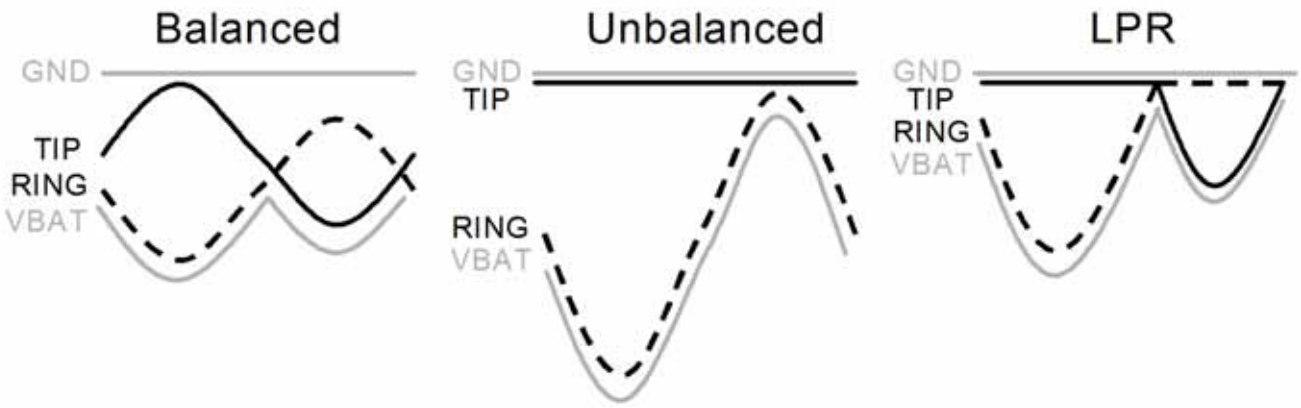


Figure 15. Ringing Modes

6.9. DTMF Detection (Si32175 Only)

In DTMF, two tones generate a DTMF digit. One tone is chosen from four possible row tones, and one tone is chosen from four possible column tones. The sum of these tones constitutes one of 16 possible DTMF digits.

6.10. Pulse Metering (Si32175 Only)

The pulse metering system for the Si32175 is designed to inject a 12 or 16 kHz billing tone into the audio path with maximum amplitude of 0.5 V_{RMS} at TIP and RING into a 200 Ω ac load impedance. The tone is generated in the DSP via a table lookup that guarantees spectral purity by not allowing drift. The tone will ramp up until it reaches a host-programmed threshold, at which point it will maintain that level until instructed to ramp down, thus creating a trapezoidal envelope.

The amplitude is controlled by an automatic gain control circuit (AGC). While the tone is ramping up, the AGC takes the feedback audio and applies it to a band pass filter, which is programmed for the 12 or 16 kHz frequency of interest. When the peak is detected, the ramp is stopped.

See AN340 section 2.3.9 for additional details and considerations on Pulse Metering.

6.11. DC-DC Controller

The Si32172/3/5 devices integrate a dc-dc controller to control an external tracking dc-dc converter which generates the high voltage supply (VBAT) to the SLIC. The tracking VBAT voltage generated from a single positive dc input is optimized to minimize power consumption by closely tracking the SLIC state, even tracking the ringing waveforms.

The dc-dc controller output DCDRV is driven by an internal charge pump which allows it to connect directly to the gate of the MOSFET switch of the dc-dc converter. This eliminates the need for the MOSFET predrive circuit that is typically required when other SLICs are used with a MOSFET with VTH greater than VDD. See Table 7.

6.12. Wideband Audio

Select Si32172/3 ICs support a software-selectable wideband (50 Hz–7 kHz) and narrowband (200 Hz–3.4 kHz) audio codec. The wideband mode provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. Wideband audio samples are transmitted and received on the PCM interface using two consecutive 8 kHz frames.

6.13. In-Circuit and Metallic Loop Testing (MLT)

A rich set of features is provided for in-circuit testing of the FXS system and the connected telephone line (MLT):

- Tone generators
- Audio diagnostic filters
- Digital and analog loop-back modes
- Internal test load
- Monitor ADC
- DSP algorithms

Using these facilities, it is possible to test the Si32172/3/5's dc-dc converter, codec, line-feed, ISI bus interface, DSP, and call progress state-machine as well as testing the connected telephone line and external protection circuitry.

The audio diagnostic filters on the FXS are intended to provide programmable filtering of the TX digital audio signal and calculate the peak and/or average signal power of the filters' outputs. The signal powers are then compared to programmable thresholds. The programmable filters can be used to band-pass filter a certain tone or notch out certain tones, so that the signal power measurements are frequency selective. This filtering is useful in a telephony system because it can measure harmonic distortion, intermodulation, noise, etc.

The Si32172/3/5 incorporates an internal test load with a 2.2 kΩ nominal value that can be connected across Tip/Ring (Figure 16). The audio diagnostics system and built-in test load can be used to test the FXS interface (Si32172/3/5) itself without requiring an external load, a connected line, or any relays. This facility can be used for production and in-service testing of such things as:

- Dial tone draw/break
- Audio quality measurements
- Pulse digit detection
- DC feed
- Ringtrip
- Polarity reversal
- Transmission loss

MLT, e.g., GR-909, is facilitated by the built-in DSP, monitor ADC, and test load. They provide the ability to detect multiple fault conditions within the CPE as well as on the Tip/Ring pair (T-R). Thirteen different measured and/or calculated parameters are reported by the Monitor ADC. Host software for use in conjunction with the ProSLIC API is available from Silicon Labs. Typical MLT tests include:

- Hazardous Potential Test – This checks for ac voltage > 50 V_{RMS} or dc voltage > 135 V between Tip and Ground (T-G) or Ring and Ground (R-G).
- Foreign Electromotive Force Test – Checks T-G or R-G for ac voltage > 10 V_{RMS} or dc voltage > 6 V. Uses same threshold as for hazardous voltage test.
- Resistive Faults Test – Checks for dc resistance from T-R, T-G or R-G. Any measurement < 150 kΩ is considered a resistive fault.
- Receiver-Off-Hook Test – Distinguishes between a T-R resistive fault and an off-hook condition.
- Ringers Test – Measures the magnitude of the connected ring load (REN) across T-R. Results are > 0.175 REN and < 5 REN for a valid load
- AC Line Impedance (line length) – T-R, T-G, and R-G. Generates a tone at several specific frequencies (audio band) and measures the reflected signal amplitude (complex spectrum) that comes back (with transhybrid balance filter disabled). The reflected signal is then used to calculate the line impedance based on certain assumptions of wire gauge, etc.
- Line Capacitance – T-R, T-G, R-G. Generates a linear ramp function with polarity reversal, and measures the time constant.

Diagnostic information is available even in the presence of fault conditions that cause the system's protection devices (fuses, PTCs, etc.) to open. A high-impedance sensing path (pins SRINGC and STIPC) can be used to measure the conditions on Tip/Ring even when the FXS system is effectively disconnected from the line. No relay is required and this sensing path inherently meets Dielectric Withstand per GR-49 (> 1000 V).

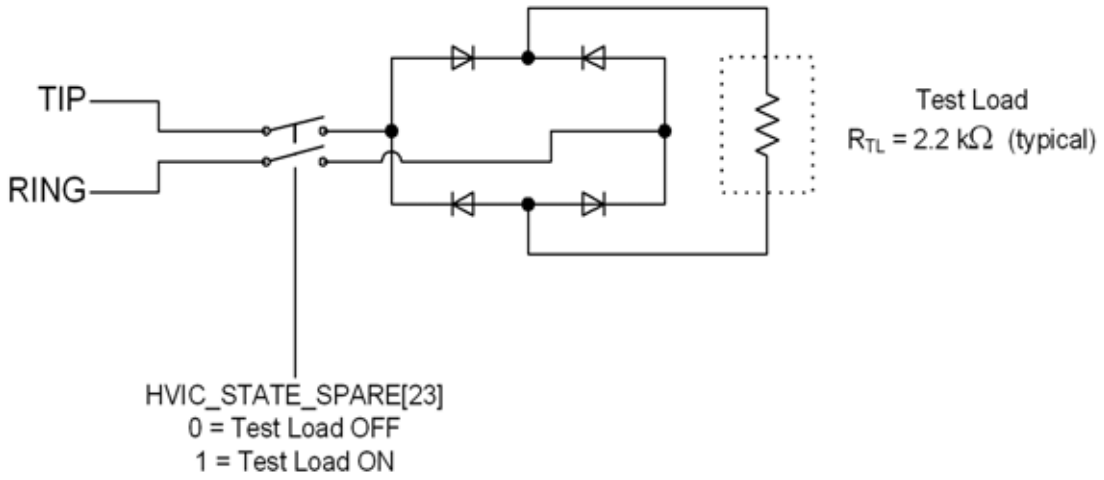


Figure 16. Internal Test Load Circuit

7. System Interfaces

7.1. Integrated Serial Interface

The Si32266/7/8/9 devices' integrated serial interface (ISI) is a three-wire proprietary interface which serializes SPI and PCM communications and interrupts, reducing the SoC interface from nine wires to three (PSCLK, MISO, MOSI). SPI communications and PCM data transfers are embedded in the serial data. The host side of the ISI is integrated onto selected SoCs from several vendors.

ISI is a point to point interface, it is not possible to daisy chain more than one ISI ProSLIC device.

Both µ-255 Law (µ-Law) and A-law companding formats are supported in addition to 16-bit linear data mode with no companding.

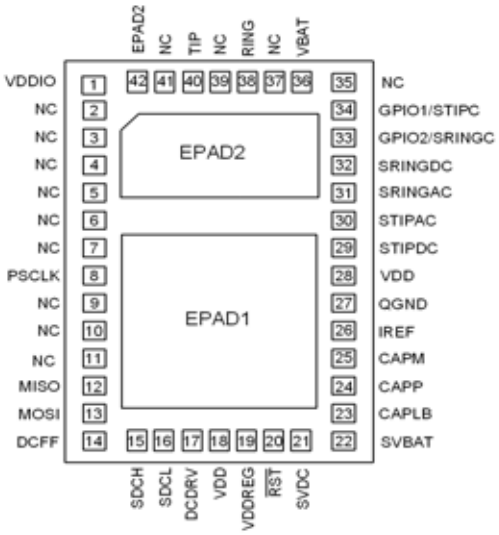
7.2. Input/Output Voltage Selection

Revision C devices have the ability to gluelessly interface directly to 1.8 V devices via the ISI and $\overline{\text{RST}}$ pins (PSCLK, MISO, MOSI, $\overline{\text{RST}}$). The I/O voltage selection is made by attaching the desired voltage (3.3 V or 1.8 V) to the VDDIO pin (pin 1).

To avoid power supply sequencing issues, VDDIO should be connected to the same supply as VDD in 3.3 V interface designs and VDDIO should be connected to VDDREG in 1.8 V interface designs.

Other voltages between 1.8 V and 3.3 V can also be used for VDDIO (for example 2.5 V), but steps must be taken to ensure that the VDDIO supply comes up after the VDD supply if VDDIO is not connected to VDD or VDDREG.

8. Pin Descriptions: Si32172/3/5



Pin #	Pin Name	Description
1	VDDIO	**IO Voltage Supply (3.3 V or 1.8 V)**
2	NC	**No Connection.** Do not connect.
3	NC	**No Connection.** Do not connect.
4	NC	**No Connection.** Do not connect.
5	NC	**No Connection.** Do not connect.
6	NC	**No Connection.** Do not connect.
7	NC	**No Connection.** Do not connect.
8	PSCLK	**ISI Clock Input** Clock input for ISI bus timing.
9	NC	**No Connection.** Do not connect.
10	NC	**No Connection**
11	NC	**No Connection**
12	MISO	**ISI Data Output** Output data to ISI.
13	MOSI	**ISI Data Input** Input data from ISI.

Pin #	Pin Name	Description
14	DCFF	**DC Feed-Forward/High Current General Purpose Output** Feed-forward drive of external bipolar transistors to improve dc-dc converter efficiency
15	SDCH	**DC Monitor** DC-DC converter monitor input used to detect overcurrent situations in the converter
16	SDCL	**DC Monitor** DC-DC converter monitor input used to detect overcurrent situations in the converter.
17	DCDRV	**DC Drive/Battery Switch** DC-DC converter control signal output which drives external bipolar transistor.
18	VDD	**IC Voltage Supply** 3.3 V supply for internal circuitry.
19	VDDREG	**Regulated Core Power Supply**
20	$\overline{\text{RST}}$	**Reset Input** Active low input. Hardware reset used to place all control registers in the default state.
21	SVDC	**DC-DC Input Voltage Sensor** Senses V_{DC} input to dc-dc converter.
22	SVBAT	**VBAT Sense** Analog current input used to sense voltage on dc-dc converter output voltage lead.
23	CAPLB	**Calibration Capacitor**
24	CAPP	**SLIC Stabilization Capacitor** Capacitor used in low pass filter to stabilize SLIC feedback loops.
25	CAPM	**SLIC Stabilization Capacitor** Capacitor used in low pass filter to stabilize SLIC feedback loops.
26	IREF	**Current Reference Input** Connects to an external resistor used to provide a high accuracy reference current.
27	QGND	**Quiet Ground Reference Input**
28	VDD	**IC Voltage Supply** 3.3 V supply for internal circuitry.
29	STIPDC	**TIP DC Sense** Analog current input used to sense voltage on the TIP lead.
30	STIPAC	**TIP AC Sense Input** Analog ac input used to detect voltage on the TIP lead.
31	SRINGAC	**RING AC Sense Input** Analog ac input used to detect voltage on the RING lead

Pin #	Pin Name	Description
32	SRINGDC	**RING DC Sense Input** Analog current input used to sense voltage on the RING lead.
33	GPIO2 SRINGC	**General Purpose I/O** RING Coarse Sense Input. Voltage sensing outside protection circuit.
34	GPIO1 STIPC	**General Purpose I/O** TIP Coarse Sense Input. Voltage sensing outside protection circuit.
35	NC	**No Connect** This pin should be left unbiased.
36	VBAT	**Battery Voltage Supply** Connect to battery supply from dc-dc converter.
37	NC	**No Connect** This pin should be left unbiased.
38	RING	**RING Terminal** Connect to the RING lead of the subscriber loop.
39	NC	**No Connect** This pin should be left unbiased.
40	TIP	**TIP Terminal** Connect to the TIP lead of the subscriber loop.
41	NC	**No Connect** This pin should be left unbiased.
42	NC	**No Connect** This pin is internally connected to EPAD2 and should be left unbiased.
—	EPAD1	**Exposed Paddle** Connect to ground.
—	EPAD2	**Exposed Paddle** Connect to electrically-isolated low thermal impedance inner layer and/or backside thermal plane using multiple thermal vias.

9. Ordering Guide

Table 17. Si32172/3/5 Ordering Guide

P/N	Description	Package Type	Max V_{BAT}	Temperature
Si32172-C-FM1	Wideband capable FXS, Integrated Serial Interface	LGA[2]	–110 V	0 to 70 °C
Si32172-C-GM1	Wideband capable FXS, Integrated Serial Interface	LGA[2]	–110 V	–40 to 85 °C
Si32173-C-FM1	Wideband capable FXS, Integrated Serial Interface	LGA[2]	–140 V	0 to 70 °C
Si32173-C-GM1	Wideband capable FXS, Integrated Serial Interface	LGA[2]	–140 V	–40 to 85 °C
Si32175-C-FM1	Narrowband FXS, Integrated Serial Interface DTMF detection, pulse metering	LGA[2]	–110 V	0 to 70 °C
Si32175-C-GM1	Narrowband FXS, Integrated Serial Interface DTMF detection, pulse metering	LGA[2]	–110 V	–40 to 85 °C

Notes:
1. Adding the suffix "R" to the part number (e.g., Si32172-B-FM1R) denotes tape and reel.
2. LGA—Land Grid Array.

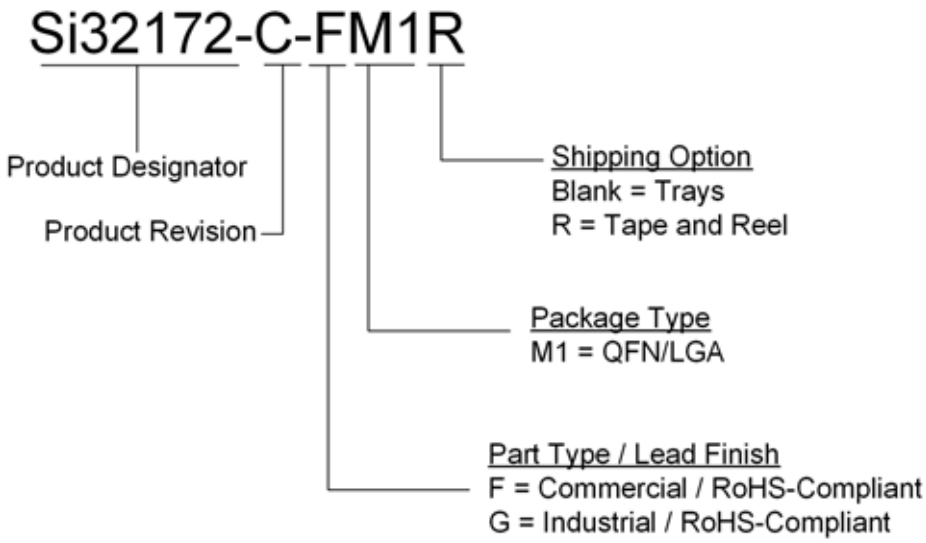
Table 18. Evaluation Kit Ordering Guide

Part Number	Description	V_{BAT} Max
Si32171CFB10SL0EVB	Wideband capable FXS with DTMF detection and pulse metering, 110 V Flyback (MOSFET transformer based) dc-dc converter EVB	–110 V
Si32176CPB10SL0EVB	Wideband FXS, 110 V PMOS buck-boost (PMOS FET and inductor based) dc-dc converter EVB for V_{DC} in the range 9.0 to 20.0 V	–110 V
Si32176CPB10SL3EVB	Wideband FXS, 85 V PMOS buck-boost (PMOS FET and inductor based) dc-dc converter EVB for V_{DC} in the range 3.3 to 5.5 V	–85 V
Si32176CBB10SL0EVB	Wideband FXS, 100 V buck-boost (BJT inductor based) dc-dc converter EVB	–100 V
Si32177CFB10SL0EVB	Wideband FXS, 138 V flyback (MOSFET transformer based) dc-dc converter EVB	–138 V

10. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



11. Package Outline

11.1. 42-Pin QFN/LGA

Figure 17 illustrates the package details for the Si32172/3/5. Table 19 lists the values for the dimensions shown in the illustration.

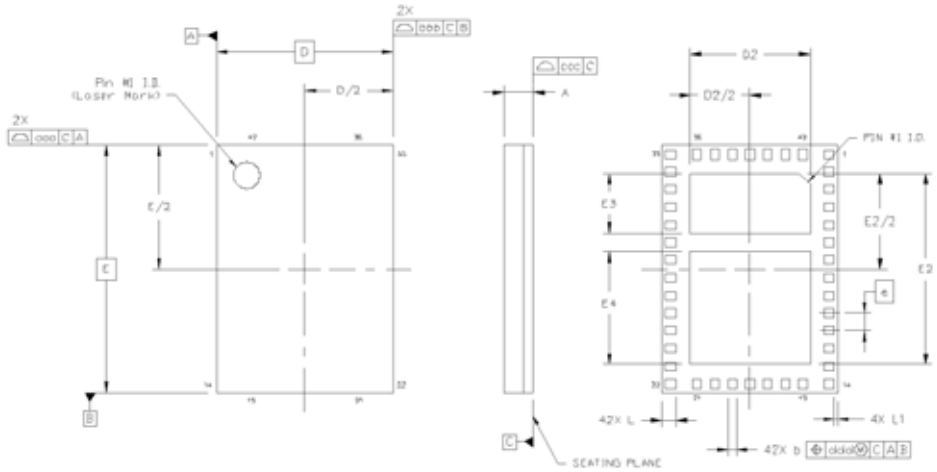


Figure 17. 42-Pin QFN/LGA Package

Table 19. 42-Pin QFN/LGA Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
b	0.20	0.25	0.30
D		5.00 BSC	
D2	3.35	3.40	3.45
e		0.50 BSC	
E		7.00 BSC	
E2	5.35	5.40	5.45
E3	1.65	1.70	1.75
E4	3.15	3.20	3.25
L	0.35	0.40	0.45
L1	0.05	0.10	0.15
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

12. PCB Land Pattern

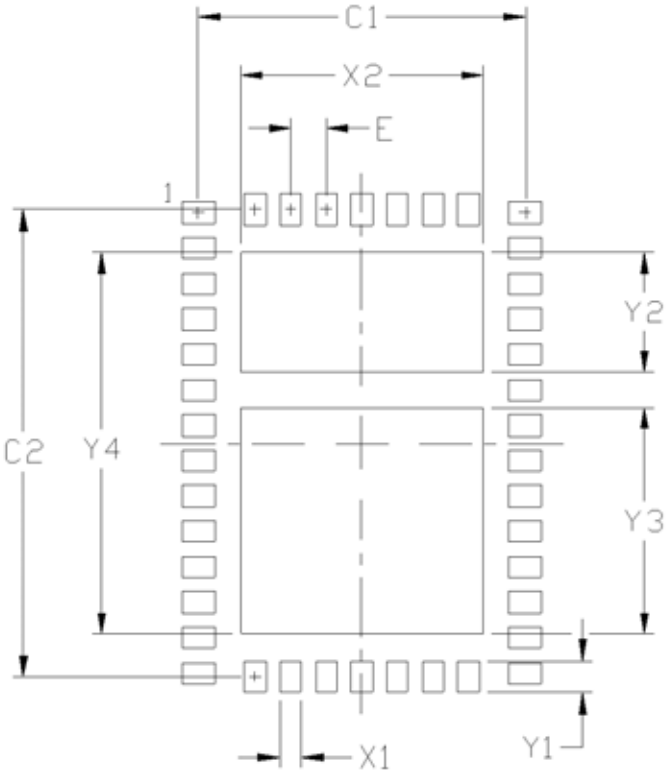


Table 20. PCB Land Pattern

Dimension	mm
C1	4.60
C2	6.60
E	0.50
X1	0.30
X2	3.45
Y1	0.45
Y2	1.75
Y3	3.25
Y4	5.45

Notes:
General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

12.1. QFN PCB Design

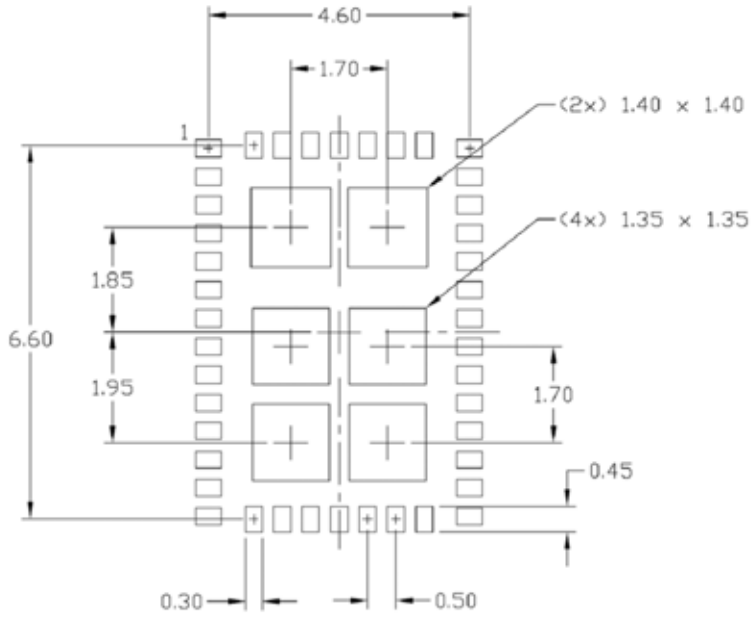
1. PCB design must ensure sufficient thermal relief for high power operation of the device. See layout guidelines in application note AN340 for further details.
2. A minimum of four vias are required under each E-Pad. Eight or more vias are recommended.
3. Via diameter should be between 0.20 and 0.31 mm.
4. Vias should either be filled or tented on the top side of the board to prevent solder thieving under the device.

12.2. QFN Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

12.3. QFN Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 1x2 array of 1.40 mm square openings on 1.7 mm pitch should be used for the top center pad and a 2x2 array of 1.35 mm square openings on 1.7 mm pitch should be used for the bottom center pad (as shown below).

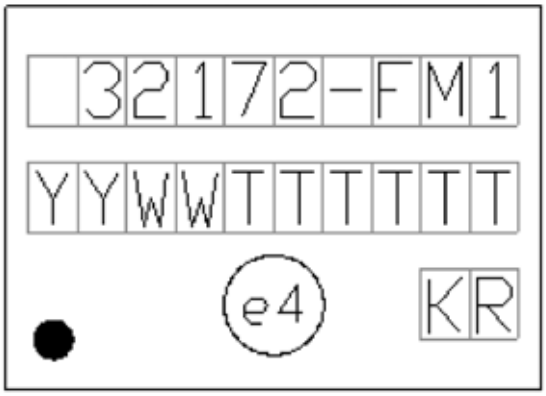


12.4. QFN Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

13. Top Markings

13.1. Top Marking



13.2. Top Marking Explanation

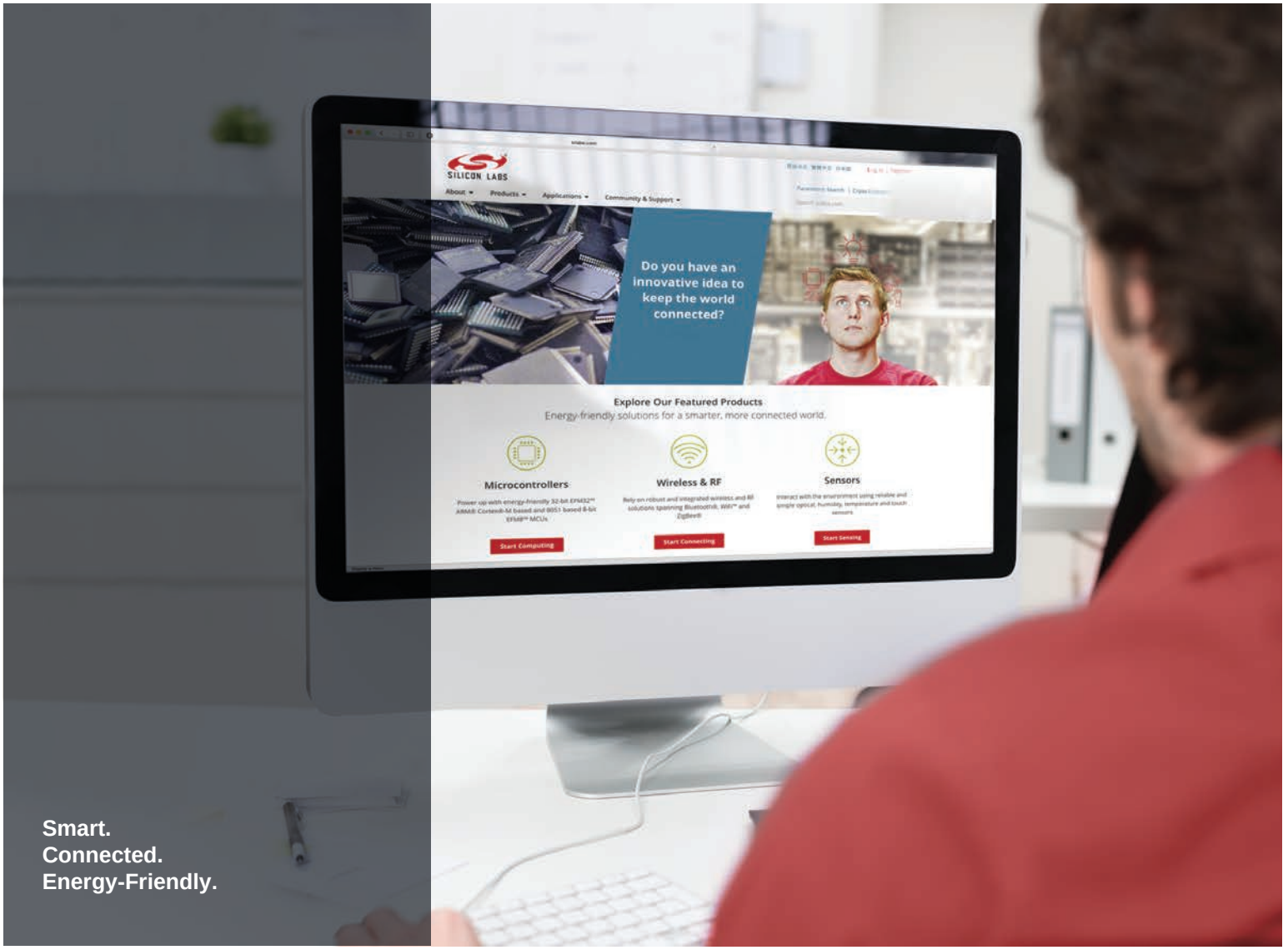
Line 1 Marking:	**Device Part Number**	**e.g., 32172-FM1**
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 0.5 mm Diameter Lower Left-Justified	Pin 1 Identifier
	Circle = 1.3 mm Diameter Center-Justified	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	e.g., KR

Document Change List

Revision 0.1 to Revision 1.0

- Reversed the order of Table 2 and Table 3 for consistency with other ProSLIC data sheets
- Added supply current measurements to Table 2 and corrected text formatting
- Added additional thermal resistance values θ_{JB} and θ_{JC}
- Changed test load resistor value to 2.2 kΩ (typical), was 5.3 kΩ in rev B
- Updated EVB ordering guide with new part numbers for revision C evaluation boards
- Corrected single frequency distortion (8-bit) values in Table 3 to show a maximum of –40 dB
- Deleted Table 5 (Monitor ADC Characteristics for FXS) to be consistent with Si3226x data sheets

NOTES:



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