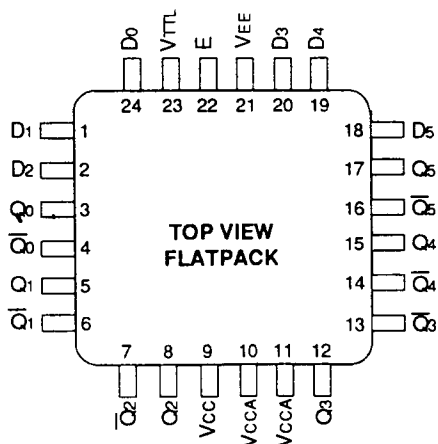
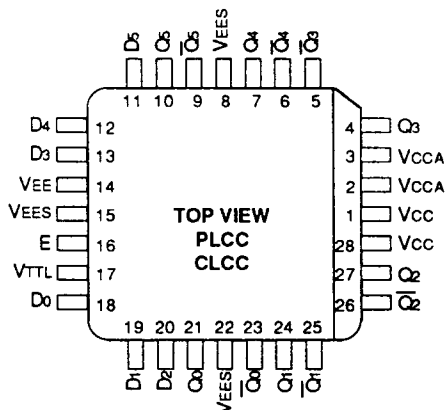
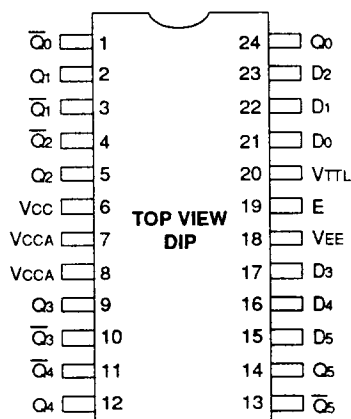


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FEATURES

- Max. Propagation Delay of 1.5ns.
- IEE min. of -55mA.
- ESD protection of 2000V.
- Industry standard 100K ECL levels.
- Extended supply voltage option:
SY100S324: VEE = -4.5V
SY101S324: VEE = -5.2V
- Differential outputs.
- Voltage and Temperature compensation for improved noise immunity.
- Twice as fast as National or Signetics.
- Approximately 35% lower power than National or Signetics.
- Function and pinout compatible with National and Signetics.
- Available in CERDIP, CERPACK, PLCC and CLCC packages.

PIN CONFIGURATIONS



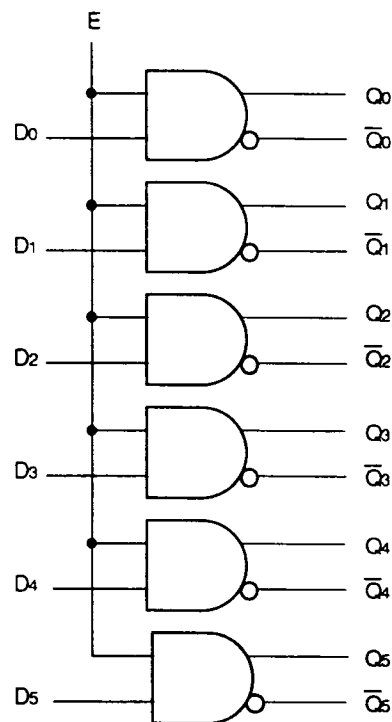
DESCRIPTION

The SY100/101S324 is a hex translator, designed to convert TTL logic levels to 100K ECL levels. The inputs are TTL compatible with differential outputs that can either be used as an inverting/non-inverting translator or as differential line drivers. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all non-inverting outputs LOW.

When used in the differential mode, due to its high common mode rejection, it overcomes voltage gradients between the TTL and ECL ground systems.

The SY100/101S324 meets the standard 100K ECL signal levels at both -4.5V (100K) and -5.2V (101K) supply levels and features on-chip voltage and temperature compensation. The SY101S324 meets standard 100K I/O levels, but at -5.2V supply.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
D ₀ - D ₅	Data Inputs
E	Enable Inputs
Q ₀ - Q ₅	Data Outputs
\bar{Q}_0 - \bar{Q}_5	Complementary Data Outputs

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.7V$ unless otherwise specified, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$, $T_c = 0^\circ C$ to $+85^\circ C$

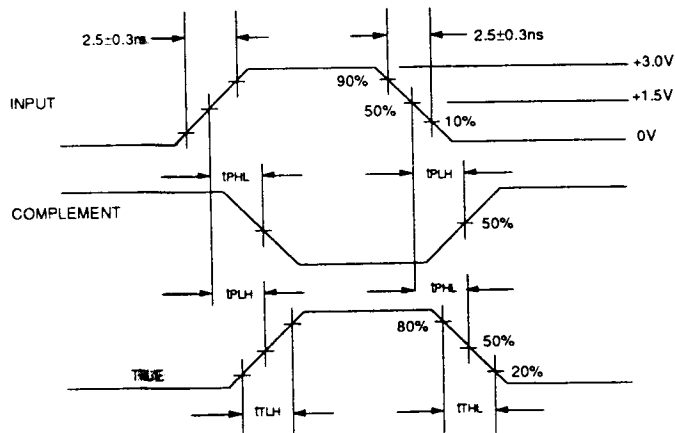
Symbol	Parameter	Min.	Sim	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	-1025	-986	-880	mV	$V_{IN} = V_{IH} (Max.)$ Loading with 50Ω
V_{OL}	Output LOW Voltage	-1810	-1674	-1620	mV	$V_{IN} = V_{IL} (Min.)$
V_{OHC}	Output HIGH Voltage	-1035	—	—	mV	$V_{IN} = V_{IH} (Min.)$ Loading with 50Ω to $-2V$
V_{OLC}	Output LOW Voltage	—	—	-1610	mV	$V_{IN} = V_{IL} (Max.)$
V_{IH}	Input High Voltage	2.0	—	5.0	V	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	0	—	0.8	V	Guaranteed LOW Signal for All Inputs
V_{CD}	Input Clamp Diode Voltage	-1.5	—	—	V	$I_{IN} = -10mA$
I_{IH}	Input HIGH Current Data Enable	— —	— —	20 120	μA	$V_{IN} = +2.4V$, All Other Inputs $V_{IN} = GND$
I_{IH}	Input HIGH Current Breakdown Test, All Inputs	—	—	1.0	mA	$V_{IN} = +5.5V$, $V_{TTL} = Max.$, All Other Inputs $V_{IN} = GND$
I_{IL}	Input LOW Current Data Enable	-1.2 -6.7	— —	— —	mA	$V_{IN} = +0.4V$, All Other Inputs $V_{IN} = V_{IH}$
I_{EE}	V_{EE} Power Supply Current	-55	-35	-28	mA	All Inputs $V_{IN} = +4.0V$
I_{TTL}	V_{TTL} Power Supply Current	—	14	25	mA	All Inputs $V_{IN} = GND$

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.7V$ unless otherwise specified, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$,

Symbol	Parameter	Min.	Sim	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.5	0.84	1.5	ns	See Switching Wave Form Figures
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	—	1.80	ns	

SWITCHING WAVEFORM



Propagation Delay and Transition Times

ORDERING INFORMATION

