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ECL Products	

10114
Line Receiver

Triple Differential Line Receiver

FEATURES

- **Typical propagation delay: 2.4ns**
- **Typical supply current ($-I_{EE}$): 28mA**

DESCRIPTION

The 10114 is a Triple Differential Line Receiver with low-impedance emitter-follower complementary outputs. With translated emitter-follower inputs and an active current source, it features a peak common-mode rejection voltage of ± 1V.

Furthermore, the OR outputs keep a Low logic level whenever the inputs are left floating. Intended primarily to receive data from balanced twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation.

It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit, as a high-speed comparator and, having an internal reference bias voltage (V_{BB}) output, it can operate as a Schmitt trigger.

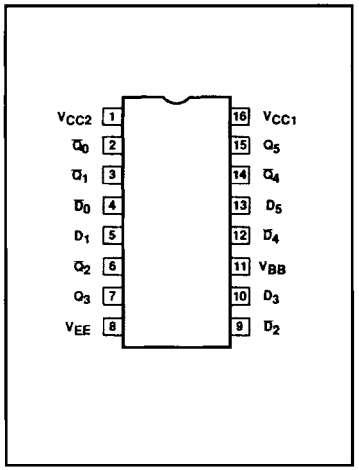
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10114N
16–Pin Ceramic DIP	10114F

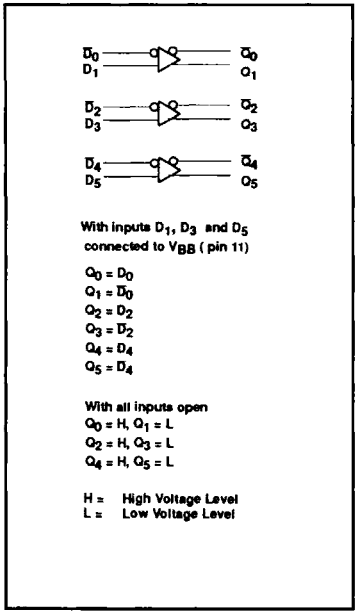
PIN DESCRIPTION

PINS	DESCRIPTION
$\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$; D_1, D_3, D_5	Data Inputs
Q_1, Q_3, Q_5	Data Outputs (OR)
$\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$	Data Outputs (NOR)
V_{BB}	Reference Bias Voltage Output

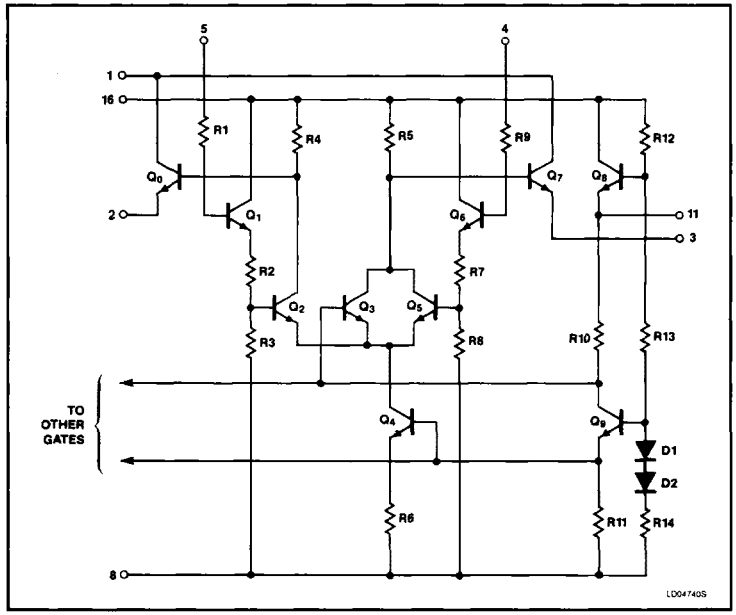
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		+5.0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC OPERATING CONDITIONS FOR COMMON–MODE REJECTION TEST $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{IHH}	V_{IHMAX} + 1.0V	$T_A = -30°C$			+110	mV
		$T_A = +25°C$			+190	mV
		$T_A = +85°C$			+300	mV
V_{IHL}	V_{IHMAX} – 1.0V	$T_A = -30°C$			–1890	mV
		$T_A = +25°C$			–1810	mV
		$T_A = +85°C$			–1700	mV
V_{ILH}	V_{ILMIN} + 1.0V	$T_A = -30°C$	–890			mV
		$T_A = +25°C$	–850			mV
		$T_A = +85°C$	–825			mV
V_{ILL}	V_{ILMIN} – 1.0V	$T_A = -30°C$	–2890			mV
		$T_A = +25°C$	–2850			mV
		$T_A = +85°C$	–2825			mV

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{IHMAX} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other	–1060		–890	mV
		$T_A = +25°C$	inverting inputs and V_{BB} applied to all non–inverting inputs. For Q_n outputs, apply V_{ILMIN} to each	–960		–810	mV
		$T_A = +85°C$	inverting input, one at a time, with V_{BB} applied to all non–inverting inputs and w/ V_{IHMAX} applied to all other inverting inputs.[4]	–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{IHT} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other inverting	–1080			mV
		$T_A = +25°C$	inputs and V_{BB} applied to all non–inverting inputs. For Q_n outputs, apply V_{ILT} to each inverting input,	–980			mV
		$T_A = +85°C$	one at a time, with V_{BB} applied to all non–inverting inputs and w/ V_{IHMAX} applied to all other inverting inputs.[4]	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{ILT} to each inverting input, one at a time, w/ V_{BB} applied to all non–inverting			–1655	mV
		$T_A = +25°C$	inputs and V_{IHMAX} applied to all other inverting inputs. For Q_n outputs, apply V_{IHT} to each inverting			–1630	mV
		$T_A = +85°C$	input, one at a time, with V_{BB} applied to all non–inverting inputs and V_{ILMIN} applied to all other inverting inputs.[4]			–1595	mV

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OL}	Low level output voltage	T_A = –30°C	For $\overline{Q}_n$ outputs, apply V_{ILMIN} to each inverting input, one at a time, w/ V_{BB} applied to all non–inverting	–1890		–1675	mV
		T_A = +25°C	inputs and V_{IHMAX} applied to all other inverting inputs. For Q_n outputs, apply V_{IHMAX} to each inverting	–1850		–1650	mV
		T_A = +85°C	input, one at a time, with V_{BB} applied to all non–inverting inputs and V_{ILMIN} applied to all other inverting inputs.[4]	–1825		–1615	mV
I_{IH}	High level input current	T_A = –30°C	Apply V_{IHMAX} to each inverting input under test, one at a time, w/ V_{ILMIN} applied to all other inverting			70	µA
		T_A = +25°C	inputs and V_{BB} applied to all non–inverting inputs. Apply V_{IHMAX} to each non–inverting input under test,			45	µA
		T_A = +85°C	one at a time, with V_{ILMIN} applied to all other non–inverting inputs and V_{BB} applied to all inverting inputs.[4]			45	µA
$-I_{EE}$	V_{EE} supply current	T_A = –30°C	Apply V_{ILMIN} to all inverting			39	mA
		T_A = +25°C	inputs. Apply V_{BB} to all		28	35	mA
		T_A = +85°C	non–inverting inputs.			39	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V
V_{BB}	Reference voltage	T_A = –30°C	All inverting or all non–inverting	–1420		–1280	mV
		T_A = +25°C	input pins are tied to the V_{BB} pin	–1350	–1290	–1230	mV
		T_A = +85°C	during measurement.	–1295		–1150	mV
V_{OH}	High level output voltage for Common–Mode Rejection Test	T_A = –30°C	For $\overline{Q}_n$ outputs, apply V_{IHH} to inverting inputs and	–1060		–1280	mV
		T_A = +25°C	V_{ILH} to non–inverting inputs. For Q_n outputs, apply	–960		–810	mV
		T_A = +85°C	V_{ILL} to inverting inputs and V_{IHL} to non–inverting inputs.	–890		–700	mV
V_{OL}	Low level output voltage for Common–Mode Rejection Test	T_A = –30°C	For $\overline{Q}_n$ outputs, apply V_{ILH} to inverting inputs and	–1890		–1675	mV
		T_A = +25°C	V_{IHH} to non–inverting inputs. For Q_n outputs, apply	–1850		–1650	mV
		T_A = +85°C	V_{IHL} to inverting inputs and V_{ILL} to non–inverting inputs.	–1825		–1615	mV
$-I_{CBO}$	Input leakage current	T_A = –30°C	Apply V_{EE} to each inverting input under test, one at			1.5	µA
		T_A = +25°C	a time, w/ V_{ILMIN} applied to all other inverting inputs			1.0	µA
		T_A = +85°C	and V_{BB} applied to all non–inverting inputs.[4]			1.0	µA

NOTES:

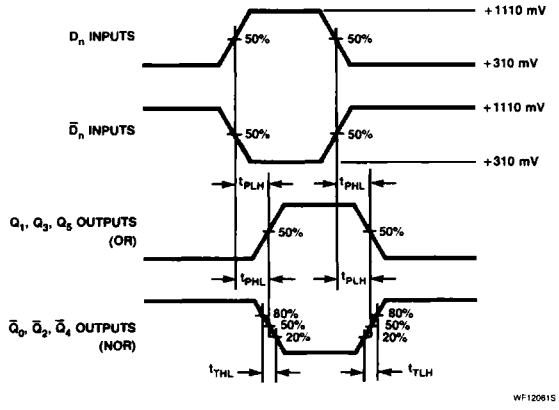
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. Refer to DC Test Circuit.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	4.40 4.40	1.00 1.00	2.40 2.40	4.00 4.00	0.90 0.90	4.30 4.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{D}_n$ to $\overline{Q}_n$		1.00 1.00	4.40 4.40	1.00 1.00	2.40 2.40	4.00 4.00	0.90 0.90	4.30 4.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.50 1.50	3.80 3.80	1.50 1.50	2.10 2.10	3.50 3.50	1.50 1.50	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

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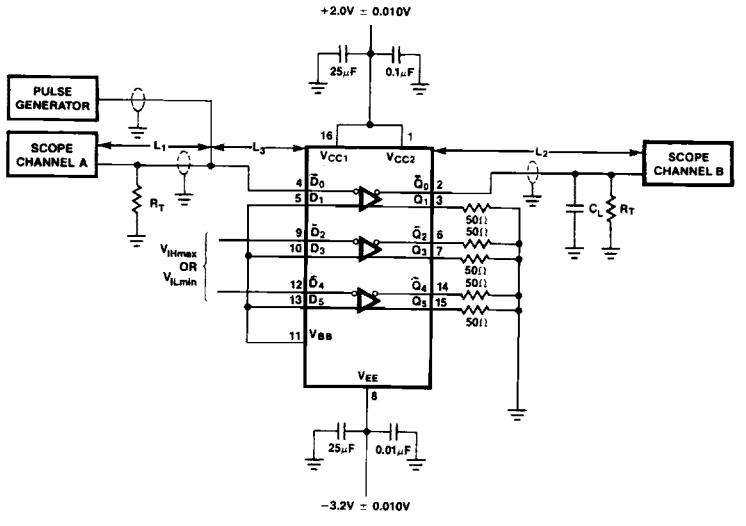
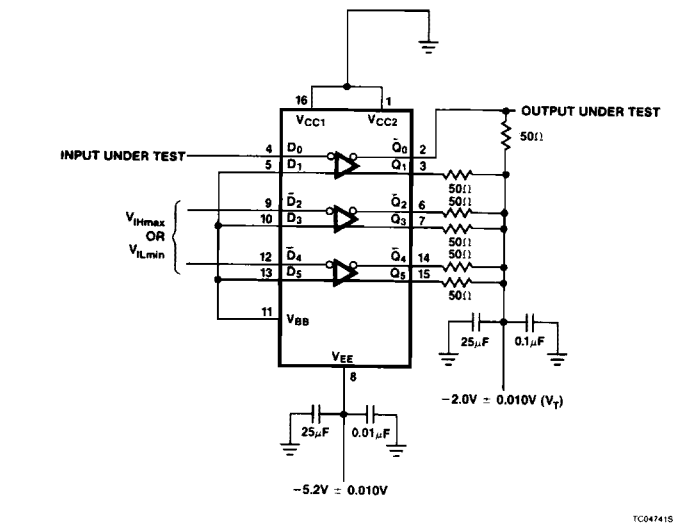
AC TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 equal length 50Ω impedance lines. L_3 the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

DC TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = 0V$ (GND), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to V_{EE}, 0.1μF and 25μF from GND to V_T (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT, and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to V_T.
5. All 50Ω resistors should have tolerance of ± 1% or better.