DS2098-1.0

SL373

SUBSCRIBER LINE INTERFACE CIRCUIT

The SL373 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing, supports line testing and detects Ground Key or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks.

The SL373 is fabricated using bipolar technology

FEATURES

- Low Power Line Feed via Regulator
- Programmable Constant Current Feed Independent of Battery to Line
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ground Key and Ring Trip Detection
- Programmable Off-Hook Detection
- Disconnect and Low Power Standby Modes
- A-Leg Disconnect, B-Leg Standby Mode
- Normal or Reversed Line Polarity Operation
- Ring and Test Relay Drivers
- Thermal Shut-Down Protection

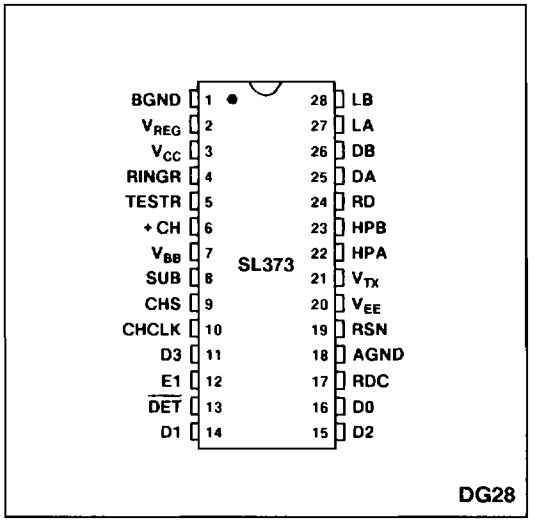


Fig. 1 Pin connections - top view

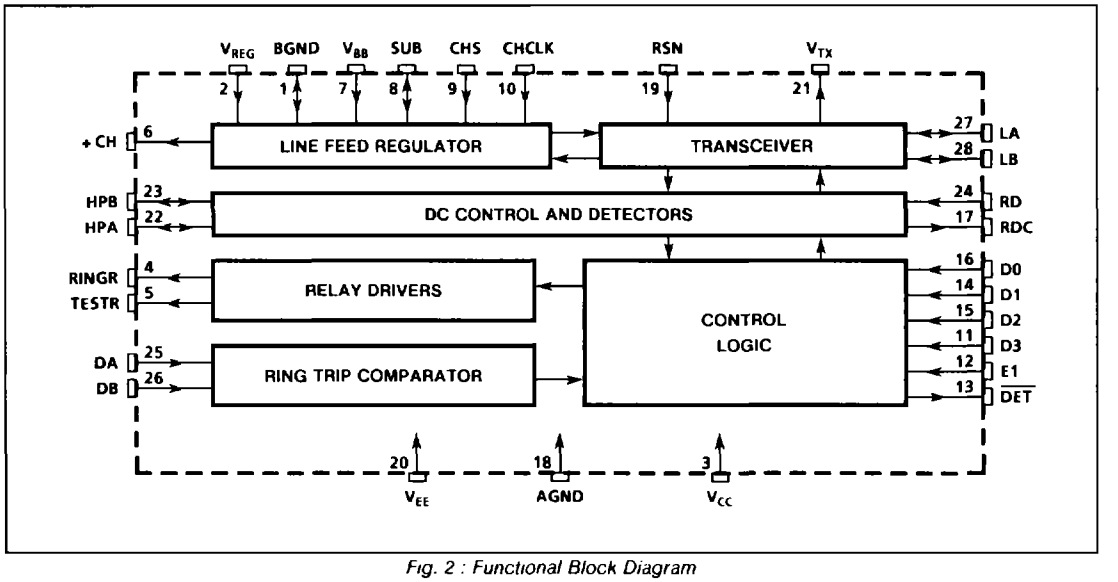


Fig. 2 : Functional Block Diagram

FUNCTIONAL OVERVIEW

The SL373 Subscriber Line Interface Circuit (SLIC), together with some external components, provides most of the line interface functions for ordinary or PABX line connections in a telephone network. It performs the interface between the two wire line and an ALAP (Analogue Line Audio Processor)/COMBO, such as the GEC Plessey Semiconductors MV3010 PSLAC (Plessesy Subscriber Line Audio Circuit) DSP device.

The SLIC circuit contains several functional blocks to achieve the design aims (Fig.2). Firstly, the Transceiver consists of the two wire port, pins LA and LB. These pins are fed from the 4 wire input (RSN) controlling AC conditions, and from the Line Feed Regulator and DC Control blocks, controlling DC conditions. The 2 wire transverse AC signal is fed onto the 4 wire transmit output, VTX.

Power dissipation is minimised, under varying line conditions, by the Line Feed Regulator which adjusts the internal high voltage supply to that required for line feed. It consists of a switching regulator which can be synchronised to a 256kHz clock.

DC line conditions at the 2 wire interface are determined by the DC Control block. These DC conditions (modes of operation) are set by the Control Logic, which also monitors line status (On/Off-Hook) via the DC Control block detectors (Loop/Ground Key/Ring Trip comparator). The control logic also controls the Ring Relay Driver for Ringing mode of operation and an undedicated Test relay driver.

A brief outline of the device functionality is given below, before a more detailed discussion of the SLIC circuitry in the Functional Description section.

LINE FEED

Line loop (pins LA &LB) feeding is obtained from the battery supply (pin 7) by means of an internal power circuit, which can be set to different modes of operation (refer to table 2). These modes are as follows:

Standby Mode

Standby mode is the SLIC's low power mode in which the battery feed circuit limits the DC loop current to a level just sufficient to enable the SLIC to detect current above the On/Off-Hook threshold. This mode is used when the subscriber is Off-Hook and no call is in progress, or if On-Hook, to save power. Both the Loop and Ground Key detectors work in this mode.

Disconnect A and B Leg

This mode programs the SLIC such that the A and B leg output amplifiers are turned off, preventing current flow to the line.

Disconnect A, Standby B Leg

This is the SLIC Standby mode with the A Leg amplifier turned off, so that current can only flow in the B Leg. In this state it is only possible to detect the application of a ground to the B Leg.

Active Mode

This is the normal operating mode with a call in progress. The SLIC is used as a constant current feed device, with the feed current being set by external resistors.

Polarity reversal

The polarity of the feeding voltage at the SLIC can be reversed on command, in Active and Standby modes. All Active and Standby conditions apply equally to the respective reverse conditions. In these conditions the polarity of any DC parameter is reversed.

Ringing

This mode enables the Ring Relay output and selects the Ring Trip comparator. It does not provide DC line feed or AC ringing voltage which must be supplied externally (via the ring relay).

Test Mode

Testing of the line is not performed by the SLIC. This mode enables external access to the telephone line by directly driving the test relay.

SUPERVISION

The SLIC provides an Off-Hook (or loop) Detector (OHD), Ring Trip Detector (RTD) and a Ground Key Detector (GKD). These are described below, in addition to the SLIC on-chip thermal protection.

Off-Hook Detector

The Off-Hook Detector recognises the loop status by means of a threshold circuit The OHD operates in Standby and Active modes (with or without polarity reversal), and in the presence of longitudinal currents. The detector threshold is nominally the same in Standby and Active modes, the actual level being externally programmable.

Ring Trip Detector

This detects when a subscriber goes off-hook during the application of a ringing signal (normally 25Hz) within a maximum delay of 150ms (determined by external components - see Applications section). The detector is active when the Ring Relay Driver is activated.

Ground Key Detector

The GKD circuit detects a current path from the A or B Leg to ground. It can be used in Standby, Active and Disconnect A Standby B modes.

Thermal Protection

In conditions which cause the chip junction temperature to rise above a critical level (around 170°C), the thermal protection will operate. This switches off the line current and therefore reduces the power dissipation.

TRANSMISSION

The signal transmission functions include 2 to 4-wire and 4 to 2- wire conversions.

The 2-wire termination impedance of the SLIC is programmed by external components. Transmit and Receive Gain are fixed and are nominally both unity (0dB), with the 2- wire port terminated in a matched load.

All the transmission parameters apply when the SLIC is operating in the presence of longitudinal currents, as specified in the Electrical Characteristics.

CONTROL

The SLIC is provided with a digital interface for controlling the 2-wire line status and passing line status information to the line card/system hardware. The operating characteristics can be selected by hardware with external components (see Digital Interface).

METERING

Injection of high amplitude high frequency meter pulses is not supported by the SL373. If this function is required, then the GPS SL376 Metering SLIC can be used instead (refer to separate Data Sheet).

RINGING

The application of the ringing voltage to the subscriber line can be via a relay or suitable high voltage crosspoint, external to the SLIC. This component is driven by the on-chip Ring Relay Driver. The relay is connected between RINGR and V_{BAT}.

When the SLIC is set to RING mode, the Ring Relay Driver output will be activated to energise the ring relay. The relay should be connected so as to cause the line to be disconnected from the SLIC and connected to a suitable ringing supply (continuous) voltage. Ring cadence can then be obtained by de-energising and re-energising the relay as required.

OVERVOLTAGE PROTECTION

Overvoltage protection is required to protect the SLIC from such line phenomena as lightning strikes, and induced AC signals from, or direct contact with, power lines. This protection can be realised with components external to the SLIC (refer to SL373/SL376 Application Note AN82).

INTERFACES

The SLIC has three main interfaces to external circuitry. These are the 2-wire, 4-wire and Digital interfaces which are described below.

Subscriber Line Interface (2-wire port)

Pins LA and LB form the Subscriber Line Interface providing line feed, signalling supervision and voice transmission between the subscriber's apparatus and exchange. It exhibits very good balance about ground to minimise the crosstalk between adjacent pairs in the local cable and noise from longitudinal interference. The termination impedance is set externally by Z_{TX} (see Fig. 3 and Functional Description).

The 2-wire port is designed to offer a low impedance to any longitudinal signals that appear on the subscriber line and the resulting signal level at the 4-wire output port is minimised.

It is able to handle longitudinal currents on the subscriber line in all modes of operation, except Disconnect mode, Ringing and Disconnect A Standby B when the SLIC 2-wire port is no longer connected to the line.

Analog 4-wire interface

Two pins of the SLIC (V_{TX} and RSN), together with associated grounds, provide the 4 wire interface to an ALAP or COMBO device. Both the transmit (V_{TX}) and receive (RSN) signals are unbalanced and have fixed gain settings. The V_{TX} pin has a low output impedance, whilst the RSN pin is a low impedance virtual earth input. The input current is normally a combination of the receive voice signal from the ALAP, line feed current programmed by the RDC pin (see Applications section) and termination of the V_{TX} pin.

Hybrid Balancing is not provided on the SLIC. This can be done by an ALAP such as the MV3010 PSLAC which uses DSP techniques, including an Adaptive Echo Cancellation feature.

Digital Interface

This is a parallel interface providing control of all the SLIC operating modes and indication of line status information. It consists of the 6 pins as listed in Table 1, the functions of which are described in Table 2.

Pin designation	Pin description
D0	Data Input
D1	Data Input
D2	Data Input
D3	Test Select Input
E1	Detector Select Input
$\overline{DET}$	Detector Data Output

Table 1 Digital interface pin designation

Mode	D3	D2	D1	D0	$\overline{DET}$ output status (Note 2)		Test relay
					E1 = 0	E1 = 1	
Disconnect A & B Legs	X	0	0	0	(Invalid)	(Invalid)	-
Ringing	X	0	0	1	Ring Trip (Note 3)	-	-
Active(Non-ringing)	X	0	1	0	Loop Detect	Ground Key	-
Standby	X	0	1	1	Loop Detect	Ground Key	-
Disconnect A,Standby B	X	1	0	0	(Invalid)	Ground Key	-
Reserved	X	1	0	1	-	-	-
Active, Polarity Reversed	X	1	1	0	Loop Detect	Ground Key	-
Standby, Polarity Reversed	X	1	1	1	Loop Detect	Ground Key	-
Line Test (Note 1)	0	X	X	X	-	-	Enabled
	1	X	X	X	-	-	Disabled

NOTES

1. D2, D1, D0 still change SLIC status even though Line outputs will be disconnected from line.
2. $\overline{DET}$ = 1 for On-Hook (high line impedance), $\overline{DET}$ = 0 for Off-Hook (low line impedance).
3. $\overline{DET}$ = 1 for Voltage DA > DB , $\overline{DET}$ = 0 for Voltage DA < DB.

Table 2 Digital interface functional description.

FUNCTIONAL DESCRIPTION

VOICE TRANSMISSION AND RECEPTION

It is conventional to assign the signal directions from the point of view of the served telephone set. The receive direction is towards the served telephone and the transmit direction is from it.

The basic voice circuit for the device is shown in Fig.3. The current which flows on the line, into LA and out of LB, is 1000 times the current which flows into RSN and through the device to AGND.

The AC voice current flowing into RSN is composed of the current from V_{RX} through Z_{GR}, which controls the signal received at the remote telephone and a current from V_{TX} through Z_{TX} which controls the termination impedance. There is also a DC current at RSN which is analysed later in the discussion on DC line feed.

The 2 wire termination impedance is $Z_{AB} = (Z_{TX} \div \alpha)$ where α (= 1000) is the current gain between RSN and I_L (see Fig.3). This can be checked by setting V_{RX} to zero.

The Receive Gain, for normal voice signals (at V_{RX}), is inversely proportional to Z_{GR}. The actual value, which is negative, can be obtained by setting $(V_L)_{ac}$ equal to zero in Fig.3. This gives:-

AC voltage between LA and LB $(V_{LA}-V_{LB})_{ac}$

$$= (V_{LA} - V_{LB}) - (V_{HPA} - V_{HPB})$$

$$= (I_L)_{ac} \times \{Z_{AB} \| Z_L\}$$

$$= -\left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)\frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}$$

i.e. minus the ratio of the line and terminating impedances (Z_L and $Z_{TX} \div \alpha$) in parallel, to the receive impedance divided by the current gain ($Z_{GR} \div \alpha$). This expression simplifies to :-

$$= \frac{-V_{RX}\alpha Z_L Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

In the transmit direction, the voltage at V_{TX} is the superposition of the voltage from the line, with the voltage produced on the line from V_{RX}, i.e:-

$$V_{TX} = \left[\left(\frac{\frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)V_L - \left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)\frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}\right]$$

This expression simplifies to :-

$$V_{TX} = \frac{[Z_{GR}(V_L)_{ac} - \alpha Z_L V_{RX}]Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

This equation can be used to determine the transmit gain, from $(V_L)_{ac}$ to V_{TX}, by setting $V_{RX} = 0$ which gives $+Z_{TX} \div (\alpha Z_L + Z_{TX})$. The 4 wire-4 wire gain, V_{RX} to V_{TX}, is also given by this equation when setting $(V_L)_{ac} = 0$, which gives us the alternative result $-\alpha Z_L Z_{TX} + [(\alpha Z_L + Z_{TX})Z_{GR}]$. If fuse resistors are included in the 2 wire loop, then Z_L is modified to become $(Z_L + 2R_{FUSE})$ in the above equations.

The transmission circuitry also contains a longitudinal feedback circuit, such that the SLIC appears as typically 25Ω resistors from LA and LB to a bias voltage (see DC Line feed section). This bias voltage comes from the DC feed circuitry. The feedback circuit attenuates longitudinal signals from the transmit path, and has no effect on transverse signals.

DC LINE FEED (Active Mode)

DC line feed (loop) current $I_L = \frac{1}{2}(|I_A - I_B|)$ is provided by the device when it is in non-ringing modes. In RING mode, DC line feed and AC ringing voltage are normally applied through the ring relay which is controlled by the device. The line feed current is reduced during standby operation.

In Active mode, Power feed is controlled by the resistance R_{DC} (= $R_{DC1} + R_{DC2}$) between the R_{DC} pin and the RSN pin (Fig.4). Again, the current in the 2 wire loop will be 1000 times the current into RSN. Operation of the DC feed circuitry is described with reference to Fig.4, which shows a conceptual model.

For the normal line feed region, a voltage V_{DC}, of magnitude 2.5V is produced at the R_{DC} pin. The sign of V_{DC} determines normal or reverse polarity operation. If negative, normal polarity is established and if positive, reverse polarity will occur (polarity is set by control logic - see Table 2). This normal line feed region exists when $|V_{BAT}| - |V_{DCT}| \geq V_{SG}$ (V_{SG} = 15V nominally, $V_{DCT} = |V_{LA} - V_{LB}|$), else the Saturation Guard circuit is active (described later).

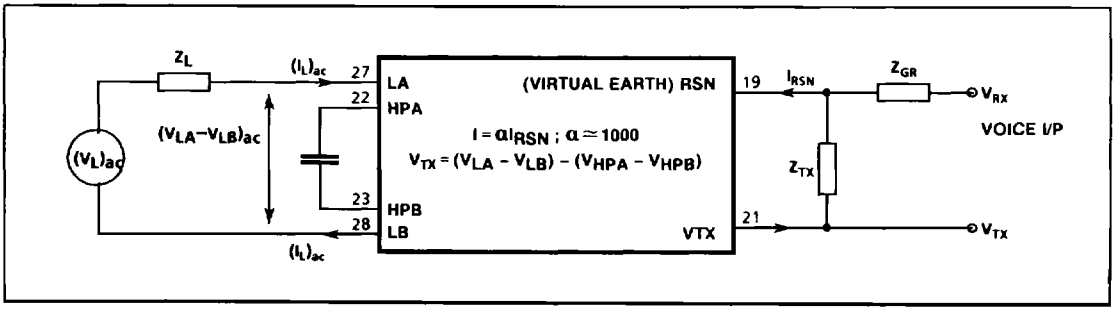


Fig.3 Voice circuit

Note that the internal resistors, R_{HP}, and external capacitor, C_{HP}, form a low pass filter network (see discussion on C_{HP} in SL373/SL376 Application Note AN82 Applications General Considerations Section). During the action of reversing polarity, the resistors R_{HP} are momentarily short-circuited to reduce the time taken for the DC voltage on C_{HP} to change sign

The ×1000 virtual earth input current amplifier means that the feed current is determined by R_{DC}, i.e:-

$$I_{FEED} = 2500 \div R_{DC} \text{ (Saturation Guard inactive)}$$

If fuse resistors are included in the 2-wire loop, the feed current will not be affected. However, the fuse resistors will affect the line current in the saturation guard region (desribed later)

As an example, to set $I_{FEED} = 40mA$, then.-

$$R_{DC} = (R_{DC1} + R_{DC2}) = 2500 \div I_{FEED} = 62\ 5k\Omega$$

The values of R_{DC1} and R_{DC2} should be kept nearly equal, forming a low pass filter network with C_{DC} to reduce chopper noise from the RDC pin (see also discussion in AN82 Applications General Considerations Section). The time constant of this network (C_{DC} and $R_{DC1} \| R_{DC2}$) also affects the time taken for a polarity reversal, and it is normally ≈1 5ms.

The remaining circuitry models the action of the saturation guard circuit This operates to reduce the voltage at the RDC pin when - $|V_{BAT}|-|V_{DCT}| < V_{SG}$. V_{SG} is a notional threshold voltage which is the headroom between the value of V_{DCT} and the battery voltage at the point where saturation guard becomes active (this includes the diode drop in series with the V_{BAT} supply, D_2 figure 7). Thus, when the comparator determines this condition, the magnitude of the difference is used to reduce the voltage at RDC.

The total line feed characteristic is shown graphically in Figs. 6a and 6b. The nearly constant voltage region is due to the action of the saturation guard circuit, and is affected by the value of R_{FUSE} as shown in Fig. 6a. Fig. 6b plots the loop current value as a function of line resistance R_L. The example shown is that of a 40mA ($R_{DC} = 62.5K\Omega$) feed current, the graphs being obtained by using the simple models of Figs 5a and 5b (0Ω fuse resistors). Figs 6a and 6b also show the action of V_{BB} on the line characteristics.

With the Saturation Guard inactive, normal line feed conditions apply such that the feed current and line/loop resistance determine V_L by the following relationship:-

$$V_L = I_L \times R_L$$

This gives the characteristic shown in Fig 6a, which is the vertical line section of the graph

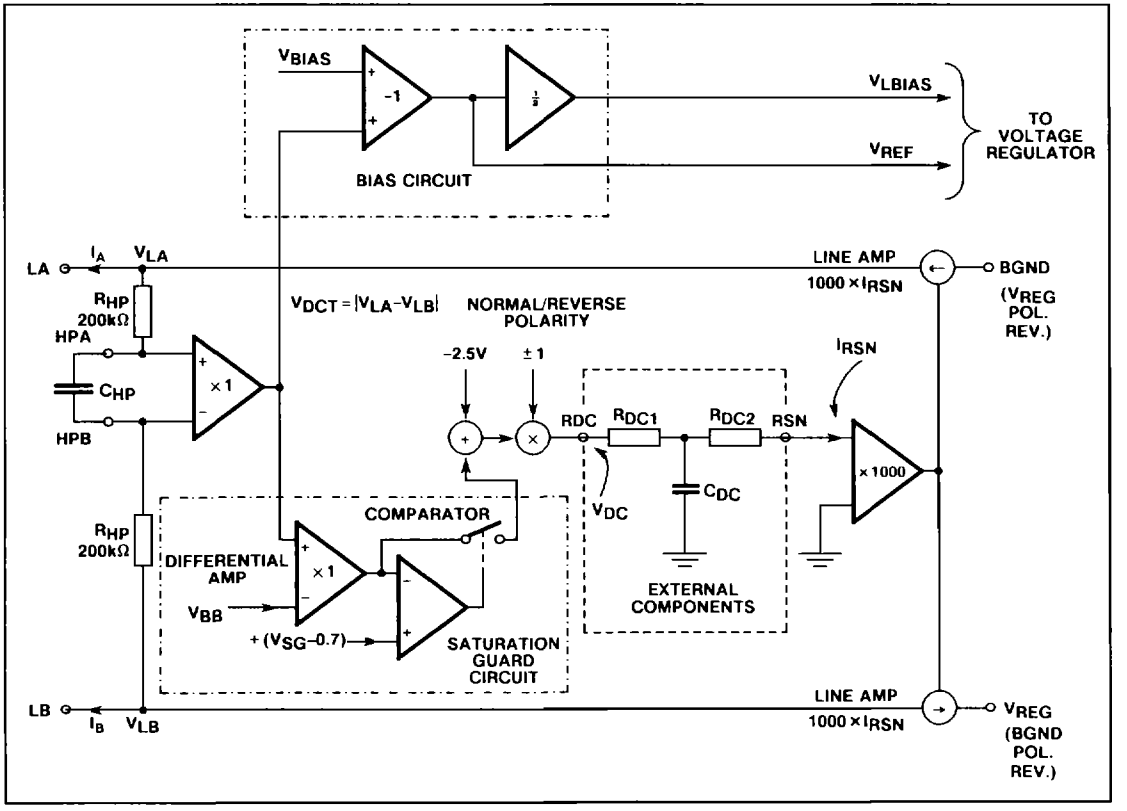


Fig.4 DC power feed circuit model.

When the saturation guard is active, then the line voltage is effectively held constant due to the reduction of the voltage at the RDC pin. Thus, line conditions are set by the following:

$$I_L = [(|V_{BAT}| - V_{SG}) \div (R_L + 2R_{FUSE})]$$

To determine the line resistance (R_{LSG}) and Line voltage (V_{LSG}) at which the saturation guard becomes active, these parameters are obtained by equating the two expressions for normal and saturation guard regions. Thus,

$$R_{LSG} = [(|V_{BAT}| - V_{SG}) \times (R_{DC} + 2500)] - 2R_{FUSE}$$
$$V_{LSG} = |V_{BAT}| - V_{SG} - [2R_{FUSE} \times (2500 \div R_{DC})]$$

The resultant line voltage (V_{LSG}) that occurs depends on the ohmic relationship of I_{LSG} and R_{LSG} (see Fig. 6a) which will equal $|V_{BAT}| - V_{SG}$ when $2R_{FUSE} = 0\Omega$. The open circuit voltage, $V_{LOC} \approx |V_{BAT}| - V_{SG}$ at $R_L = \infty\Omega$, will always be greater than V_{LSG}, even when $2R_{FUSE} = 0\Omega$. This change in voltage between V_{LSG} and V_{LOC} will be greater at lower battery voltages. Fig. 6a shows the nominal effect.

DC LINE FEED (Standby Mode)

For Standby mode, the DC current is limited to a value just sufficient for the loop Detector to sense Off-Hook.

Normally this threshold (I_{DET}) is set externally by a resistor, R_{TH} (see Control and Signalling section). The limited loop current (I_{LIM}) is also determined by R_{TH} via a conversion factor K_{LIM} (nominally 1.7, see Electrical Characteristics) such that :-

$$I_L \leq I_{LIM} = K_{LIM} \times I_{DET}$$

The shape of this characteristic is almost a constant current, as shown in Fig. 6a. Since $K_{LIM} > 1$, the current level is still sufficient to detect the Off-Hook threshold (see Control and Signalling section).

LINE POLARITY

Normal polarity (Active/Standby) consists of the LA pin voltage near BGND and the LB pin voltage near V_{BB}. Under these conditions $I_L = +\frac{1}{2}|I_A - I_B|$ and the voltage at the RDC pin is negative. Reverse polarity will give LA voltage near V_{BB}, LB voltage near BGND, $I_L = -\frac{1}{2}|I_A - I_B|$ and the voltage at the RDC pin is positive.

BIAS CIRCUIT

The Bias circuit (Fig. 4) produces two reference voltages, both referred to ground. These are V_{REF}, being related to the 2-wire transverse DC voltage and V_{LBIAS} approximately half V_{REF}.

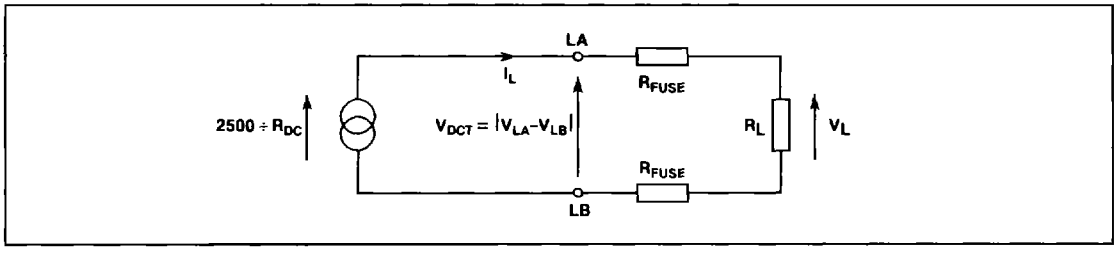


Fig. 5a Simple power feed model (normal line feed)

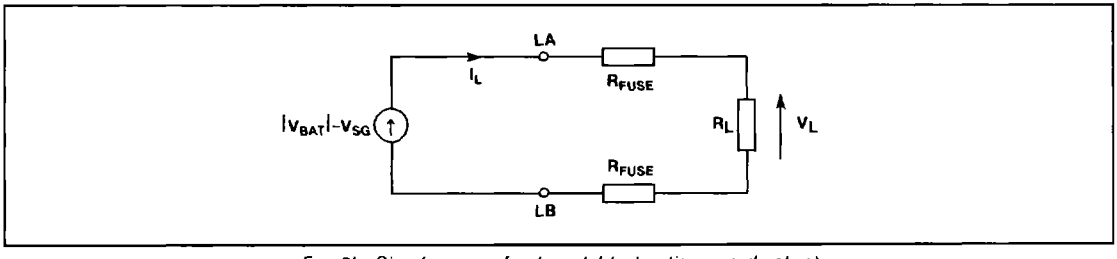


Fig. 5b Simple power feed model (saturation guard active)

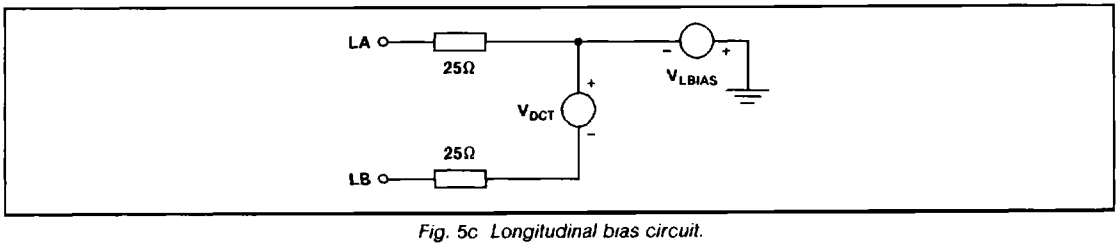
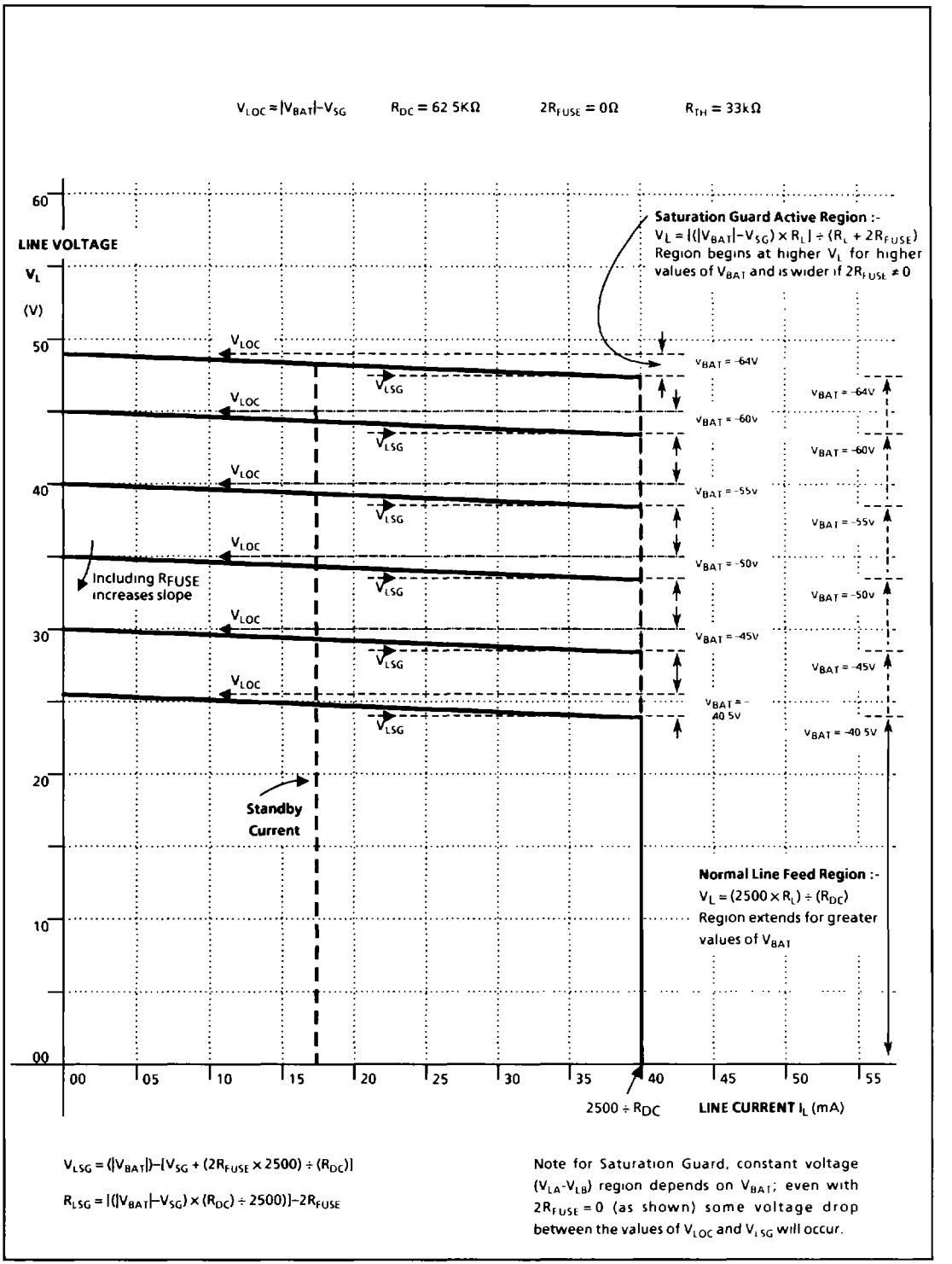


Fig. 5c Longitudinal bias circuit.



$V_{LSG} = (|V_{BAT}|) - [V_{SG} + (2R_{FUSE} \times 2500) \div (R_{DC})]$

$R_{LSG} = [(|V_{BAT}| - V_{SG}) \times (R_{DC}) \div 2500)] - 2R_{FUSE}$

Note for Saturation Guard, constant voltage (V_{LA}-V_{LB}) region depends on V_{BAT}; even with $2R_{FUSE} = 0$ (as shown) some voltage drop between the values of V_{LOC} and V_{LSG} will occur.

Fig. 6a Line feed characteristic, V_L vs I_L.

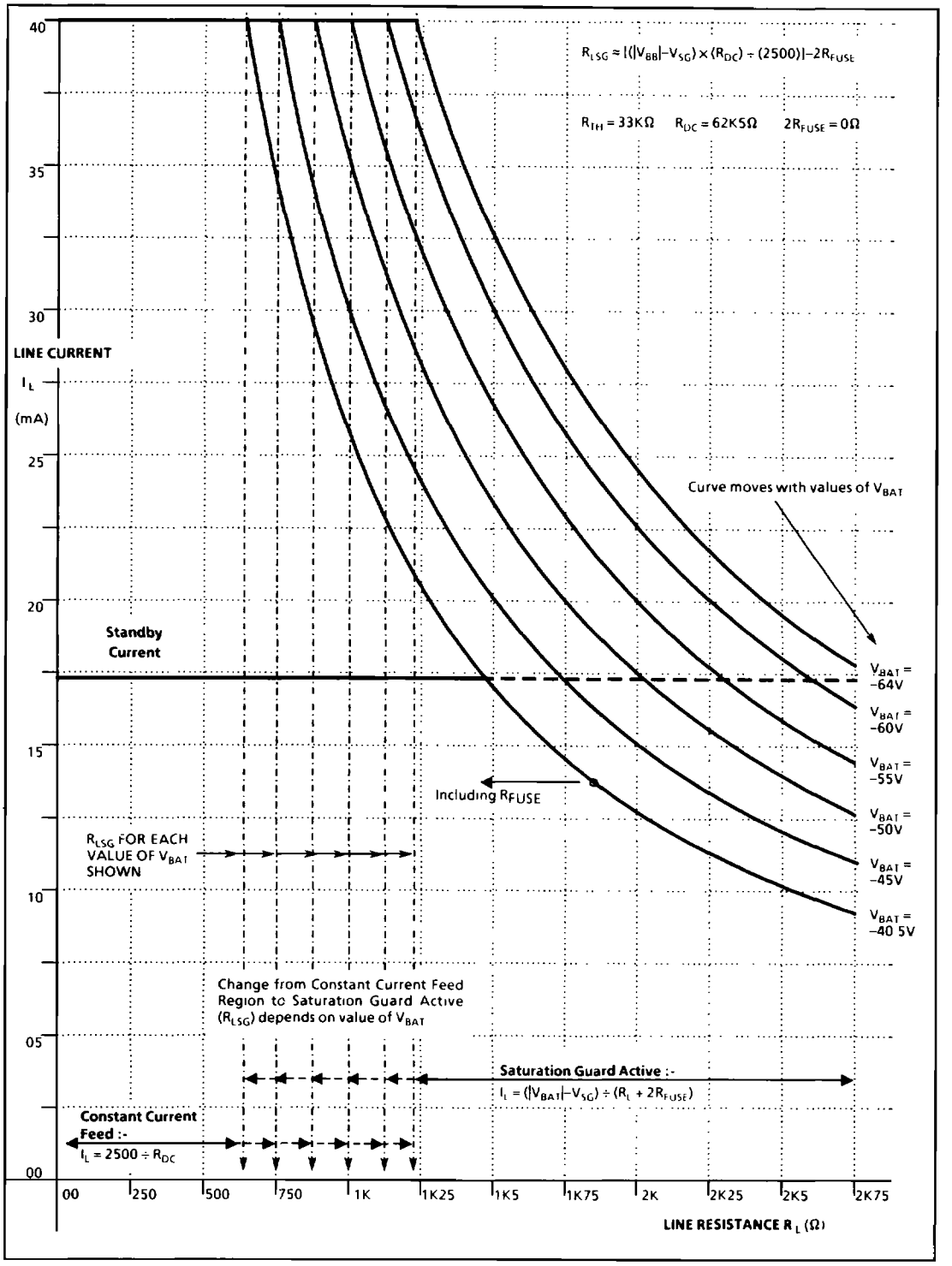


Fig. 6b Line feed characteristic, I_L vs R_L.

V_{REF} controls the line feed regulator and V_{LBIAS} sets the 2-wire feed balance voltage (centre point voltage of the lines). The longitudinal control loop achieves an input impedance of approximately 25Ω per line for longitudinal signals, as shown in Fig 5c

LINE FEED REGULATOR

The DC voltage between LA and LB will vary with the DC loop resistance. Unless the voltage supplied to the SLIC can be varied to match that on the line there will be a voltage drop across the chip along the path taken by the feed current. This could cause significant power dissipation. The purpose of the line feed regulator is to minimise this power dissipation by regulating the voltage supplied to the Line Amplifiers

Regulated voltage is supplied to the Line Amplifiers on V_{REG} and unregulated voltage is supplied on V_{BB}. The chip switches V_{BB} onto +CH when more power is required at the V_{REG} pin V_{REG} is the voltage used by the device to power the 2-wire interface, and it is adjusted to follow a reference voltage V_{REF} (from Power Feed) This reference voltage is determined as follows:

$$V_{REF} = -\{ | V_{DCT} | + V_{BIAS} \}$$

and is such to set V_{REG} to the minimum required to power the line interface. This then ensures a minimum power dissipation. The voltage V_{BIAS} is needed to keep the amplifier response linear when audio signals are transmitted

Fig. 7 shows the external components associated with the power supply aspect of the voltage regulator. +CH is the positive terminal of the regulator switch that connects to V_{BB}. When the switch is turned on, current in L_1 and C_1 increases, thus increasing stored energy. When the switch turns off, this stored energy sustains L_1 current which flows in D_1. The voltage at +CH is thus a square wave of up to 50V p-p making this node sensitive to PCB layout. Note that the inductor should be capable of taking twice the line current without saturating The regulator will work with a wide range of inductor resistance, although if this is too large, long line drive capability and regulator efficiency will be reduced. Since there are large current fluctuations from V_{BB} through the switch, C_2 provides filtering of the VBB pin, whilst D_2 isolates the V_{BAT} supply should the LA/LB pins be taken negative of the V_{BAT} supply.

The chip senses the voltage at V_{REG}, compares it to its requirements and switches power from V_{BB} to +CH, using the variable mark/space method, to give appropriate matching The rate of switching can be governed by CHCLK (pin 10) or allowed to free run, its stability ensured by the network on CHS (pin 9) , i.e. C_3, R_1, C_5. Since noise is produced by the switching, a decoupling node is provided at SUB (pin 8)

CONTROL AND SIGNALLING

The mode of operation of the SL373 is determined by the Digital Interface pins, as described in Tables 1 and 2. These pins enable Ringing or Non-Ringing modes of operation, controlling line status, line polarity, Relay Driver and selection of line detector.

The line status is selected by use of the D2..D0 pins, Table 2, to determine the modes as listed. The function of these modes has already been described in the 'Overview' and 'DC Line Feed' sections; more detail of the device detectors is given here (refer to Fig. 8)

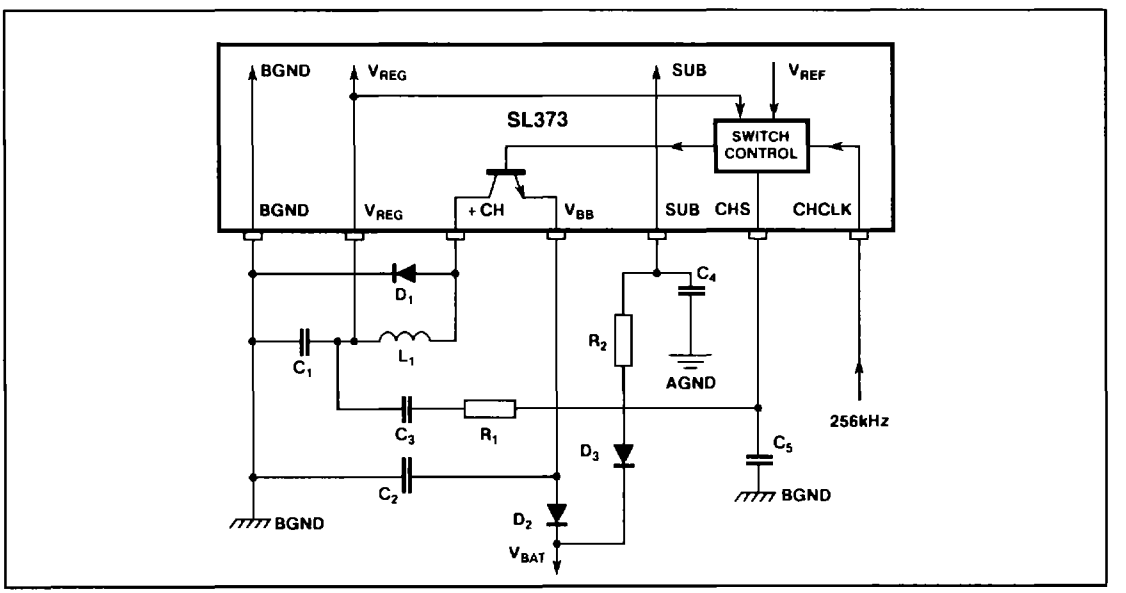


Fig.7 Voltage regulator power supply circuit.

Loop Detect

This detector is used in Active and Standby modes (with/without polarity reversal). The loop current at which the detector indicates the Off-Hook condition, is set by the comparator at pins 24 (RD) and 20 (V_{EE}). Normally a resistor, R_{TH}, is connected between these pins, such that Off-Hook line current threshold (I_{DET}) is set by.

$$I_{DET} = 350 \div R_{TH}$$

This is due to the fact that the current out of the RD pin is equal to the loop current $I_L = (\frac{1}{2}|I_A - I_B|)$ divided by ~280. This will create a voltage across R_{TH} at the RD pin Off-Hook is given by a logic low at the $\overline{DET}$ output pin (detector selected) when this voltage rises above the internal 1.25V reference.

Ground Key Detector

This detector is selected by the E1 pin of the Digital Interface. It can be used in Active and Standby modes (with/without polarity reversal), as well as Disconnect A Standby B mode.

Operation of the detector is via an internal threshold and the longitudinal current $I_{LL} = I_A + I_B$ of the 2-wire loop. Ground Key detection is indicated when either the midpoint of the A and B legs is connected to ground, or the B leg (A leg, polarity reversed) is connected to ground. The resistance values for which Ground Key detection is valid are given in the Electrical Characteristics section.

Ring Trip Detector

This consists of a comparator connected to the DA and DB pins, and indicates Ring Trip when the voltage at DA < DB. Selection of Ringing mode operates the Ring Relay and enables the Ring Trip Detector. The external ringing supply must consist of DC line feed in addition to the AC ringing voltage. In order that the Ring Trip Detector senses Ring Trip in ringing mode, a resistance bridge network is used in association with pins DA, DB, line and ring source. This network is described in the Applications section and discussed further in AN82.

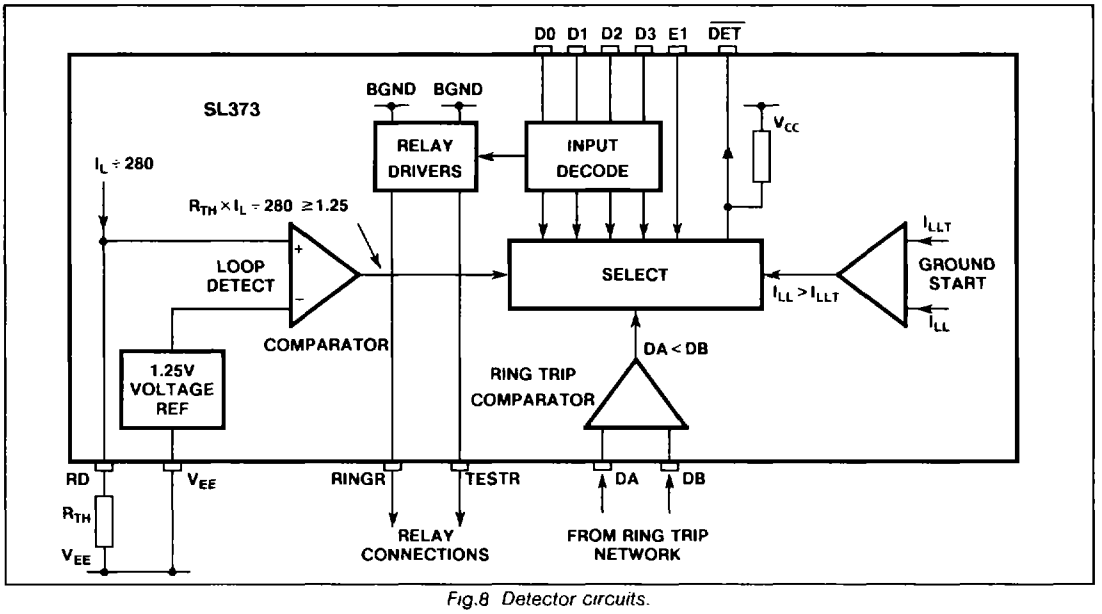


Fig.8 Detector circuits.

FUNCTIONAL PARAMETER SUMMARY

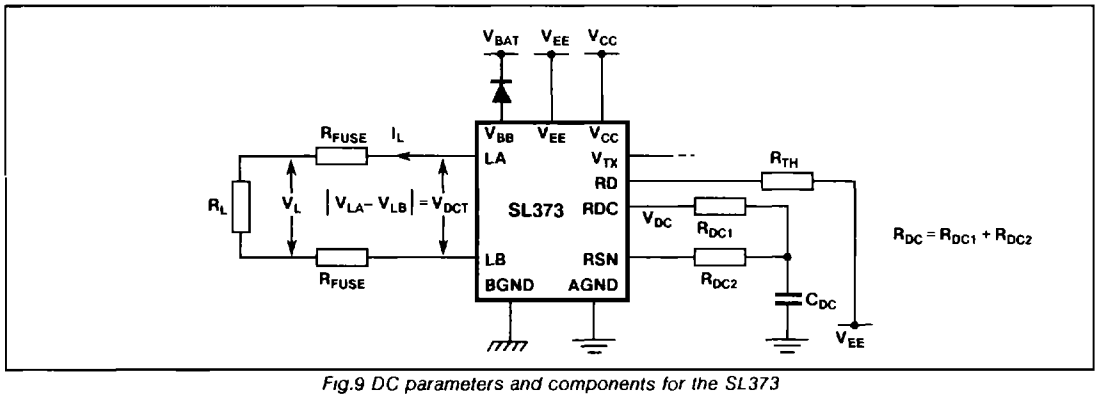


Fig.9 DC parameters and components for the SL373

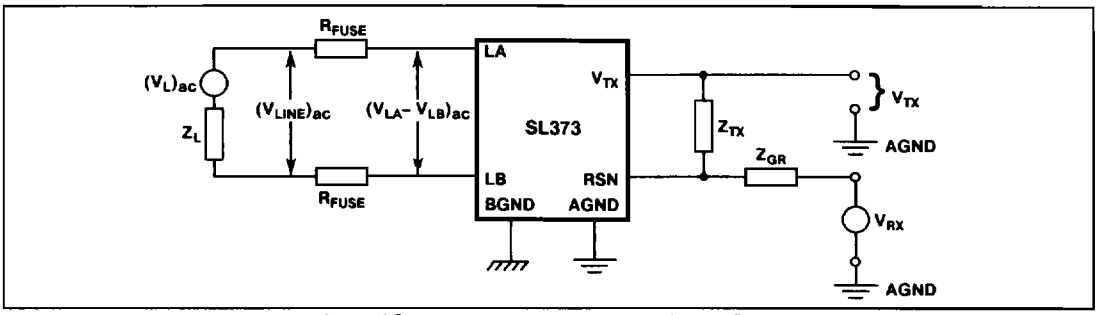


Fig.10 AC parameters and components for the SL373

LIST OF DEFINITIONS

1. Loop Current is defined as :- $I_L = \pm \frac{1}{2}|I_A - I_B|$

   I_A = current out of LA pin, I_B = current out of LB pin, + ⇒ normal line polarity and −⇒ reverse line polarity.

2. Longitudinal Current is defined as :- $ILL = (I_A + I_B)$

   I_A = current out of LA pin, I_B = current out of LB pin

3. Normal Line Feed Region when $|V_{BAT}|-|V_{DCT}| > V_{SG}$ with $I_L = I_{FEED} = (2500 \div R_{DC})$

4. Saturation Guard Threshold when $|V_{BAT}|-|V_{DCT}| = V_{SG} = 15.0V$ such that :-

   $V_L = V_{LSG} = |V_{BAT}|-V_{SG}-[2R_{FUSE} \times (2500 \div R_{DC})]$ which will equal $|V_{BAT}|-V_{SG}$ with $2R_{FUSE} = 0$ and
   $R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 2500)]-[2R_{FUSE}]$

5. Saturation Guard feed Region when $|V_{BAT}|-|V_{DCT}| < V_{SG}$ with $I_L = [|V_{BAT}|-V_{SG}] \div [R_L + 2R_{FUSE}]$

6. Note that V_{LSG} is referred to as the value of the line voltage, V_L, at the point where Saturation Guard becomes active. This will differ from the value of $|V_{LA}-V_{LB}|$ (i.e. V_{DCT}) if $2R_{FUSE} \neq 0$. V_{SG} is used as a notional threshold voltage which is the internal headroom between the $|V_{LA}-V_{LB}|$ voltage and the battery supply, at this same point.

7. Open Circuit Line Voltage V_{LOC} at $R_L = \infty\Omega$ such that :- $V_L = V_{LOC} - [|V_{BAT}|-V_{SG}]$

   V_{LOC} will be $\geq V_{LSG}$ even with $2R_{FUSE} = 0$. The voltage drop from V_{LOC} to the defined V_{LSG} point will be greater at lower values of V_{BAT}.

8. Standby Mode DC Feed Current $I_L \leq I_{LIM} = K_{LIM} \times I_{DET} \sim 600 \div R_{TH}$

9. 2 Wire Termination Impedance $Z_{AB} = (Z_{TX} \div \alpha) = (Z_{TX} + 1000)$

   Note that Z_{TX} is normally set to $[\alpha(Z_L + 2R_{FUSE})]$ where Z_L is the desired termination impedance.

10. Recieve Gain from V_{RX} to $(V_{LA}-V_{LB})_{ac}$ or $(V_{LINE})_{ac}$ is set by Z_{GR} after setting Z_{TX}. Thus, with $(V_L)_{ac} = 0$:-

    $$\frac{(V_{LA}-V_{LB})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L) + Z_{TX}]Z_{GR}} \quad \text{with } 2R_{FUSE} = 0 \; ; \quad \frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}} \quad \text{with } 2R_{FUSE} \neq 0$$

11. Resultant Transmit Gain is then :- $$\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]} \quad \text{with } V_{RX} = 0$$

12. Resultant 4 Wire-4 Wire Gain is then :- $$\frac{V_{TX}}{V_{RX}} = \frac{-\alpha(Z_L + 2R_{FUSE})Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}} \quad \text{with } (V_L)_{ac} = 0$$

13. Off-Hook Threshold is set by R_{TH} at :- $I_L = I_{DET} = 350 \div R_{TH}$

14. Ring Trip Threshold is set by the bridge associated with pins 25 .. 28 and the 2 Wire Line, thus :-

    $R_L = R_{LTH} = R_{B4}(2R_F) \div (R_{B4}-R_{B1})$ assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and $R_{FEED1} = R_{FEED2}$ for the bridge components (balanced ringing). $R_{B1}..R_{B4} \sim$ a few 100KΩ and $R_{FEED1} \sim$ a few 100Ω.

15. AC ringing voltage at DA (DB by the same amount) is reduced by a factor of :- $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$

    f_r is the ringing frequency and t_r is determined by the bridge components including C_B, thus :- $t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$

    for Balanced Ringing.

APPLICATIONS

The requirements for the subscriber line interface vary considerably from one telephone administration to another. The SL373 is designed to have the flexibility to meet these varying requirements. For simplicity, only a single example is given to illustrate how the device is connected. Fig. 11 shows the circuit which can be used to evaluate the device. Further applications information is given in the SL373/SL376 Application Note AN82 (page 7-18).

The DA and DB pins are connected to a resistance bridge network (R_{C1} to R_{B4}). This allows the change in line resistance to be sensed when the remote telephone goes off-hook during ringing (Ring Trip). The details of this network (and C_B) are given later (see Ring Trip section). The resistors R_{FEED1} and R_{FEED2} provide feeding of the ringing source onto the line during ringing mode. The Ring and Test Relay Drives are connected through current limiting resistors.

Connections to the LA and LB pins are shown, and include the resistors R_{FUSE} in addition to the ring relay. These resistors have a value around 20 to 30 ohms, depending on the application, and provide current line protection.

Overvoltage and protection circuitry may consist of slew-limiting inductors between the pins and the line itself and a thyristor or zener protection network at the line. In many applications, especially in PBXs, the amount of protection circuitry can be reduced. The capacitors between LA, LB and ground, allow noise from the regulator to be decoupled.

The capacitor C_{HP} between HPA and HPB (pins 22 and 23) is used to filter out the AC component of the signal on the line. The voltage difference between the two pins should be effectively DC. The SL373/SL376 Application Note AN82 contains a further discussion on this

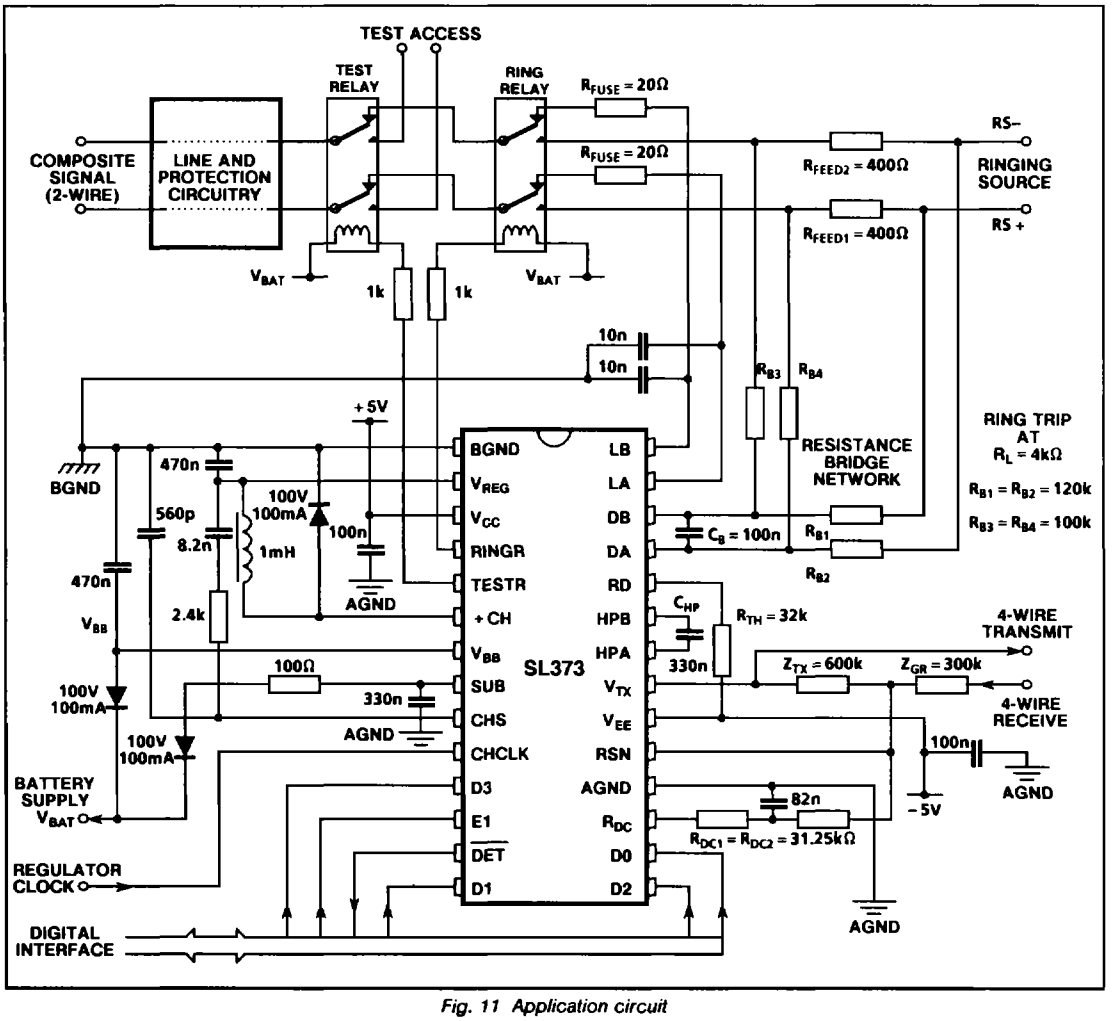


Fig. 11 Application circuit

The resistor, R_{TH}, between RD (Pin 24) and V_{EE} (pin 20) programs the threshold current for the loop detector. A capacitor in parallel can be added to reduce the effect of the AC component of the line current, but this can cause instability in standby operation with highly inductive lines if it is too large. The value of R_{TH} sets the current I_{DET} according to the relationship :

$$I_{DET} = 350 \div R_{TH}$$

The CHS pin (Pin 9) is connected to BGND through a capacitor and to V_{REG} by a capacitor and resistor in series. This stabilises the regulator control loop. Operation of the regulator has been described earlier in the Functional Description section (pins 2,6 & 7).

It is recommended that the substrate (SUB) pin be decoupled to AGND. However, BGND may be used if this is sufficiently quiet, otherwise some degradation in noise performance may be experienced.

DC current flows between the RDC (pin 17) and RSN (pin 19). This is used to set the line feed current. Any minor AC fluctuations are reduced by dividing the resistance RDC equally such that $R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC}$ and connecting a capacitor from the junction of R_{DC1} and R_{DC2} to AGND.

The Receive Gain is set by the network (Z_{GR}) which controls the receive current flowing into RSN. This can be a complex impedance network to allow for complex impedance terminations.

The network (Z_{TX}) between V_{TX} and RSN controls the 2 wire terminating impedance (Z_T). This can also be a complex impedance. The value of Z_{TX} can be calculated from the relationship :-

$$Z_{TX} = (\text{Required } Z_T) \times (\text{Receive Current Gain})$$

Connections for both Ring and Test relays are also shown in Fig. 11. Note that the 1kΩ resistors provide current limit through the relay coils when the driver outputs are on.

Control and status pins are TTL compatible. They are designed to give a simple interface to digital circuits and are directly compatible with the MV3010 PSLAC.

RING TRIP

Ring Trip detection operates by comparing the voltages on DA and DB and providing the output on $\overline{DET}$ when this function is enabled by the status input pins of the Digital Interface. A resistance bridge (R_{B1} to R_{B4}) must be connected to the line and the ringing voltage sources to cause the differential voltage between DA and DB to change sign when the line resistance falls below the level associated with Ring Trip. Note that it is simplified by use of $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ (see discussion in AN82)

Ringing voltage is normally applied to the line through the Ring Relay which is activated by RINGR. The ringing voltage sources, including line feed, are connected to the line via ringing feed resistors, R_{FEED1} and R_{FEED2}. The resistance bridge operates by allowing the DC voltage dropped across the ringing feed resistors (R_F) in the Off-Hook condition to reverse the polarity of the voltage on DA and DB (DA < DB). Since the AC ringing voltage is greater than the DC feed, the capacitor C_B (Fig. 12) will filter this out at the comparator inputs. The connection shown is suitable for balanced ringing only. For unbalanced ringing, separate capacitors from DA (C_{B1}) and DB (C_{B2}) to ground will be required to achieve the same result.

Fig. 12 shows how the resistance bridge is connected when used with balanced ringing. The circuit can operate correctly provided there is a DC feed in addition to the AC ringing voltage.

If R_{LTH} is the line resistance corresponding to the Ring Trip threshold (DA = DB), this can be determined from the values of R_F ($R_{FEED1} = R_{FEED2} = R_F$), R_{B1} and R_{B4} ($R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$) as:-

$$R_{LTH} = \frac{R_{B4}(2R_F)}{(R_{B1} - R_{B4})}$$

R_{B1} and R_{B4} should be a few hundred kΩ.

The amplitude of the AC ringing voltage at DA (DB by the same amount) is reduced by a factor of $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$ where f_r is the ringing AC frequency and t_r is set by:-

$$t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$$

for balanced ringing. For $f_r \approx 20$Hz, t_r should be ≈ 50ms. For unbalanced ringing C_B will become $C_{B1}C_{B2} \div (C_{B1} + C_{B2})$ in the above equation. More detail on Balanced and Unbalanced ringing is given in AN82.

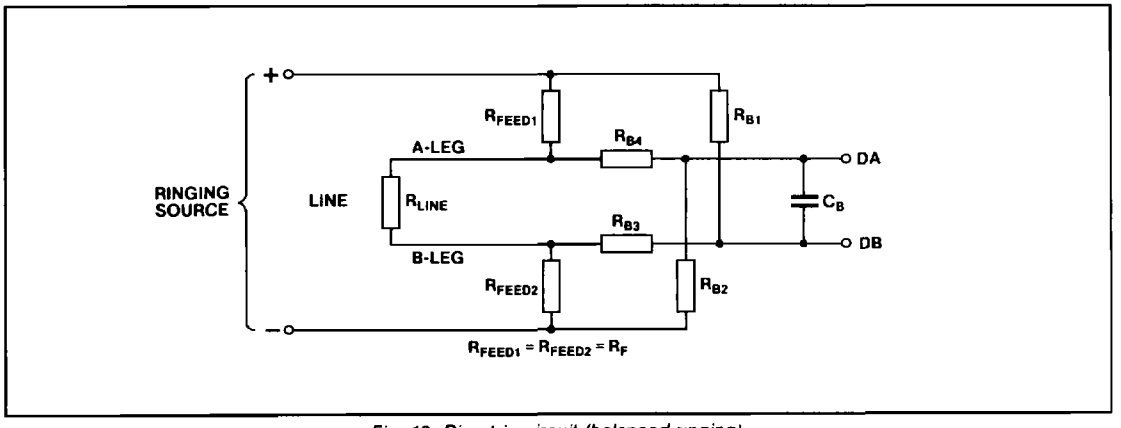


Fig. 12 Ring trip circuit (balanced ringing).

PIN DESCRIPTIONS

Symbol	Pin no.	Pin name and description
BGND	1	**Battery Ground (Power Input).** 0 Volts.
V_{REG}	2	**Regulated Voltage (Negative Power Input).** The voltage at this pin is compared to that required for line feed, and the result is used to control the voltage regulator.
V_{CC}	3	**Positive Supply (Power Input).** +5 Volts.
RINGR	4	**Ring Relay Driver Output (Pull-up Output).** This output is designed to drive a relay, when used together with the V_{BAT} supply.
TESTR	5	**Test Relay Driver Output (Pull-up Output).** This output is designed to drive a relay, when used together with the V_{BAT} supply.
+CH	6	**Switching Regulator (Chopper) Output (Negative Power Output).** Chopper switch transistor collector. An internal regulator controls the mark/space ratio of the switching waveform to maintain V_{REG} (pin 2) at the required voltage.
V_{BB}	7	**Battery Voltage (Negative Power Input).** This is the –50 Volt battery supply pin which connects to the V_{BAT} supply via an external diode. It is connected to the chopper switch emitter.
SUB	8	**Substrate (Decoupling Node).** An external decoupling capacitor (0.33µF) should be connected between this pin and AGND.
CHS	9	**Line Feed Regulator (Chopper) Stabilising Network.** This is the input to the voltage comparator which is used to control the switching regulator.
CHCLK	10	**Line Feed Regulator (Chopper) Clock (Digital Input).** This is the positive edge triggered, 256kHz clock input for the voltage regulator, which will free run in the absence of an input signal.
D3	11	**Control Input (Digital Input).** Enables the Test relay driver output pin.
E1	12	**Control Input (Digital Input).** Selects the line status detector (Loop or Ground Key).
$\overline{DET}$	13	**Detector Data output (Digital Output).** This pin outputs the status of the detector which has been selected by D0 - D3.
D1 D2 D0	14 15 16	**Control Input (Digital Input)** **Control Input (Digital Input)** **Control Input (Digital Input)** — These inputs determine the SLIC operating mode, and control the ring relay, selection of ringing and non-ringing modes, line polarity, line status and line detector.
RDC	17	**DC Reference Voltage (Voltage Output).** A reference voltage of ±2.5 Volts (± depending on line polarity), is output at this pin, excepting Saturation Guard operation.
AGND	18	**Analog Ground (Analog Reference Node).** This is the ground reference pin for the analog signals. It also provides a ground reference for the Digital Interface. Signal reference and decoupling connections should be separately run to this pin.
RSN	19	**Receive Summing Node (Current Input).** The current which is input on this pin is used to control the transverse current at LA and LB
V_{EE}	20	**Negative Supply (Power Input).** – 5 Volts.
V_{TX}	21	**Transmit Voltage (Voltage Output).** The voltage output at this pin is equal to the difference between the voltage (V_{LA}–V_{LB}) and the differential DC voltage (V_{HPA}–V_{HPB}), multiplied by the 2 to 4 wire voltage gain.
HPA HPB	22 23	**High Pass A, High Pass B - AC/DC separation (Voltage Inputs).** These inputs sense the DC feed voltages on the LA and LB pins respectively. Under normal operation they are connected to LA and LB respectively by internal resistors and should be connected as shown in Fig. 11.
RD	24	**Loop Detection Control (Current Output / Voltage Input).** This pin outputs a current which equals the transverse loop current through LA and LB divided by 280. Off-Hook is indicated via the $\overline{DET}$ pin when the voltage at this pin is $\geq (V_{EE} + 1.25)$ Volts.
DA DB	25 26	**Ring Trip Detector A, Ring Trip Detector B (Voltage Inputs).** These are the A and B inputs to the internal ring trip comparator. The output of the comparator controls the ring trip output on $\overline{DET}$.
LA LB	27 28	**A Line Transceiver, B Line Transceiver (Current Outputs / Voltage Inputs).** These two pins form the 2 wire port connecting to the subscriber loop.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Range - see page 3-21)

Test conditions (unless otherwise stated)

V_{CC} = +5.0V, V_{EE} = –5.0V, V_{BAT} = –50V (see note 3), $V_{AGND} = V_{BGND}$, T_{AMB} = +25°C, V_{IL} = 0.7V and V_{IH} = 2.0V. Test circuit Fig. 24. Voltages are measured with respect to analog ground (V_{AGND}). Typical figures are for design aid only; they are not guaranteed and are not subject to production testing.

Supply Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply (V_{CC}) current, disconnect mode	I_{CC1}			4	mA	
Positive supply (V_{CC}) current, standby mode	I_{CC2}			10	mA	On / Off-Hook, $I_L = 0$
Positive supply (V_{CC}) current, active mode	I_{CC3}			10	mA	On / Off-Hook, $I_L = 0$
Negative supply (V_{EE}) current, disconnect mode	I_{EE1}			2	mA	
Negative supply (V_{EE}) current standby mode	I_{EE2}			3	mA	On / Off-Hook, $I_L = 0$
Negative supply (V_{EE}) current active mode	I_{EE3}			3	mA	On / Off-Hook, $I_L = 0$
Battery supply (V_{BB}) current disconnect mode	I_{BB1}			1	mA	
Battery supply (V_{BB}) current standby mode	I_{BB2}			5	mA	On-Hook, $I_L = 0$
Battery supply (V_{BB}) current active mode	I_{BB3}			6	mA	On-Hook, $I_L = 0$
Positive supply (V_{CC}) rejection ratio (supply to 2-wire transverse)	P_{SRT}		17		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Positive supply (V_{CC}) rejection ratio (supply to 2-wire longitudinal)	P_{SRL}		17		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Negative supply (V_{EE}) rejection ratio (supply to 2-wire transverse)	N_{SRT}		17		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Negative supply (V_{EE}) rejection ratio (supply to 2-wire longitudinal)	N_{SRL}		17		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Battery supply (V_{BB}) rejection ratio (supply to 2-wire transverse)	B_{SRT}		27		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Battery supply (V_{BB}) rejection ratio (supply to 2-wire longitudinal)	B_{SRL}		27		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Power dissipation, active state	P_{WA}			1.00	W	$Z_L = 600\Omega$
Power dissipation, standby state, on-hook	P_{WD1}			0.35	W	$I_L = 0$

NOTES

1. Non production test; figures are guaranteed by characterisation.
2. Figures will degrade when saturation guard is active, i.e. when $|V_{BAT}| - |V_{DCT}| < V_{SG}$. V_{DCT} is voltage between pins LA and LB and $V_{SG} \approx 15.0V$.
3. Battery voltage V_{BAT} is generally defined. The corresponding V_{BB} voltage is assumed to be 0.7V more positive than V_{BAT} allowing for the diode drop in D_2, see Fig. 24.

Analog Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
2-wire port, low frequency overload level	V_{OAB}	– 3.1		+ 3.1	V (pk)	Refer Fig. 13, note 4: V_R = 1000 Hz, E_L = 0V
2-wire port,longitudinal impedance	Z_{LL}			35	Ω/wire	Refer Fig. 14: f < 100 Hz Z_L = 600Ω
Longitudinal current limit, active state	I_{LLA}	17.5			mA/wire (rms)	Refer Fig. 15, note 5: E_R = – 10dBm 700-1100Hz, Z_L = 600Ω
Longitudinal current limit, standby state	I_{LLS}	3.6			mA/wire (rms)	Refer Fig. 15, note 5: E_R = – 10dBm 700-1100Hz, Z_L = 600Ω
Longitudinal current limit, active state, B leg	I_{LLB}	63			mA	I_{LLB} is Current in B leg with B leg = 0V and A leg O/C
4-wire transmit port, overload level	V_{OT}	– 3.1		+ 3.1	V (pk)	Refer Fig. 13, note 4: f = 1000 Hz, V_R = 0V 4-wire load ≥ 25kΩ
4-wire transmit port, offset voltage	V_{TOFF}	– 30		+ 30	mV	Refer Fig. 13: V_R = 0
4-wire transmit port,output impedance	Z_T			20	Ω	Refer Fig. 13: E_L = 0V
Transmit (2 to 4-wire) voltage gain	G_T	– 0.1		+ 0.1	dB	Refer Fig. 13: E_L = 0dBu (see note 6), 1kHz, V_R = 0
4-wire receive port, low frequency voltage gain	G_{RL}	– 0.2		+ 0.2	dB	Refer Fig. 16: V_R = 2.6dBu, 1kHz
4-wire receive port, current gain	G_{RI}	59.8	60.0	60.2	dB	Refer Fig. 13:
4 to 4-wire voltage gain	$G_R \times G_T$	– 0.2		+ 0.2	dB	Refer Fig. 16: R3 = 600kΩ, V_R = 2.6dBu, 1000Hz
2-wire to 4-wire frequency response	F_{24}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 7: V_R = 0, E_L = 0dBu, 200-3400Hz,
4-wire to 2-wire frequency response	F_{42}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 7: E_L = 0, V_R = 0dBu, 200-3400Hz
4 to 4-wire frequency response	$F_{44} = F_{24} \times F_{42}$	– 0.1		+ 0.1	dB	Refer Fig. 13, note 7: E_L = 0, V_R = 0dBu, 200-3400Hz
Gain linearity, 2-wire to 4-wire	G_{L24-1}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 8: V_R = 0, E_L = + 7 to – 30 dBu, 1kHz
Gain linearity, 2-wire to 4-wire	G_{L24-2}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 1: V_R = 0, E_L = –30 to – 59 dBu, 1kHz
Gain linearity, 4-wire to 2-wire	G_{L42-1}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 8: E_L = 0, V_R = + 3 to –30 dBu, 1kHz
Gain linearity, 4-wire to 2-wire	G_{L42-2}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 1: E_L = 0, V_R = –30 to –64 dBu, 1kHz

NOTES
4. Overload occurs when distortion is 2% of total signal in the range 300-3400Hz.
5. E_{LL} = 50Hz. Amplitude of I_{LL} when signal-to-distortion ratio at $V_T \leq 30$dB.
6. dBu is defined thus: 0dBu is equivalent to the voltage at 0dBm when loaded with 600Ω ($0.775V_{RMS}$).
7. Response is measured with respect to 1kHz.
8. Linearity is measured with respect to gain at 0dBu.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
4-wire idle channel noise (psophometric weighted)	N_{P4}			-75.0	dBup	Refer Fig. 13: $E_L = V_R = 0V$
2-wire idle channel noise (psophometric weighted)	N_{P2}			-75.0	dBup	Refer Fig. 13: $E_L = V_R = 0V$
2-wire differential noise (wide band)	N_{D2}		Fig. 19			Refer Fig. 13, note 1; $E_L = V_R = 0V$
2-wire longitudinal noise (wide band)	N_{L2}		Fig. 20			Refer Fig. 18, note 1; $E_R = 0V$
Regulator noise, 4-wire receive, single frequency	N_{R4}			-55.0	dBu	Refer Fig. 21, note 1
Regulator noise, 2-wire transverse, single frequency.	N_{RT}			-50.0	dBu	Refer Fig. 21, note 1; measure V_{A-B}.
Regulator noise, 2-wire longitudinal, single frequency.	N_{RL}			-50.0	dBu	Refer Fig. 21, note 1; measure V_{LL}.
Longitudinal balance, longitudinal to transverse	B_{L-T1}	50	60		dB	Refer Fig. 14, note 11: $Z_L = 600\Omega, V_R = 0$, E_{LL} = +2dBu 40-4000Hz
Longitudinal balance, longitudinal to transverse	B_{L-T2}	35.5 40.0 45.0	40.0 45.0 50.0		dB dB dB	Ref Fig. 14: $V_R = 0, Z_L = 1.6k\Omega$ E_{LL} = +2dBu 40-400Hz E_{LL} = +2dBu 400-1000Hz E_{LL} = +2dBu 1000-4000Hz
Longitudinal balance, transverse to longitudinal + longitudinal to transverse	B_{T-L+} B_{L-T1}	98			dB	Refer Fig. 14 & Fig. 17: $Z_L = 600\Omega$, $V_R = 0$, E_{LL} = +2dBu 300-800Hz
Longitudinal balance, transverse to longitudinal + lonitudinal to transverse	B_{T-L+} B_{L-T2}	90			dB	Refer Fig. 14 & Fig. 17: $Z_L = 1600\Omega$, $V_R = 0$, E_{LL} = +2dBu 300-800Hz
Longitudinal signal rejection, longitudinal to 4-wire	$RJ_{L4\ A}$	50	60		dB	Refer Fig. 14: $Z_L = 600\Omega$, $V_R = 0$, E_{LL} = +2dBu 40-4000Hz
Longitudinal signal rejection, longitudinal to 4-wire	$RJ_{L4\ BL}$ $RJ_{L4\ BH}$	35 45	40 50		dB dB	Refer Fig. 14: $Z_L = 1600\Omega$, $V_R = 0$, E_{LL} = +2dBu 40-300Hz E_{LL} = +2dBu 300-4000Hz
Longitudinal signal generation, 4-wire to longitudinal	GN_{4-L}	40			dB	Refer Fig. 18; $Z_L = 600$ or $1.6k\Omega$ E_R = 2.6dBu 300-800Hz,
Harmonic distortion, 4 to 2-wire	T_{HD1}			-50.0	dB	Refer Fig. 13, note 9: V_R = 0dBu, 1000Hz
Intermodulation distortion	ID_{A-B1}			-40.0	dB	Refer Fig. 13, note 10: $V_R = f_1 + f_2$, $f_1 = f_2$ = -4 to -21dBu
50Hz intermodulation distortion	ID_{A-B2}			-49.0	dB	Refer Fig. 13, note 1: $V_R = f_1 + f_2$, f_1 = -9dBu 300-3400Hz, f_2 = -23dBu 50Hz

NOTES
9. Distortion measured in the bandwidth 300-3400Hz.
10. f_1 & f_2 in the range 300-3.4kHz, $f_1 \div f_2$ = Non-integer. Measure $(2f_1-f_2)$ relative to f_1 or f_2 level.
11. Parameter will degrade for some values of V_{BAT}

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Loop current, active state constant current region	I_{ACT1}	38	40	42	mA	Refer Fig. 24, note 12 : $Z_L = 600\Omega, R_{DC} = 62.5k\Omega$
Loop current, active state	I_{ACT2}	23			mA	Refer Fig. 24, note 12 : $Z_L = 2k\Omega, R_{DC} = 62.5k\Omega$
Loop current limit conversion factor K_{LIM} (see DC line feed section)	K_{LIM}	1.25		1.70	-	Standby mode
2-wire current, disconnected state	I_{DCT}			1.0	mA	LA to LB or Ground, or both LA and LB to Ground
2-wire current, disconnect A standby B mode	I_{DASB}			1.0	mA	$Z_L = 600\Omega$
Loop current, standby state, normal(+) or reverse(–)	I_{LIM}	14.7	17.3	22.0	(±)mA	Refer Fig. 24, note 13: $Z_L = 600\Omega$
Regulator voltage, pin 2	V_{REG1}	– 31.1 – 38.3		 – 32.2 – 39.1	V V V V	V_{LA}-V_{LB} = 18 9 Refer to V_{LA}-V_{LB} = 22 5 Fig. 13; V_{LA}-V_{LB} = 26.9 V_{BAT} = –63V V_{LA}-V_{LB} = 30.5
Loop detector, current threshold	I_{TH}	I_{TH} – 15%	I_{TH}	I_{TH} + 15%	A	Refer Fig. 24 · $I_{TH} = 350 \div R_{TH}$
Ring trip detector offset voltage	V_{RTO}	– 50		+ 50	mV	Refer Fig. 22 : R = 200kΩ $V_{BB} < V_{CMM} < -2V$
Ring trip detector bias current	I_{RTB}	–1.0			µA	Refer Fig. 22 : $I_{RTB} = \frac{1}{2}(I_{RTDA} + I_{RTDB})$
Ground key active mode $\overline{DET} = 0$	R_{G10}			900	Ω	Refer Fig. 23, note 14: SW1 Closed, RW = 300Ω
Ground key active mode $\overline{DET} = 1$	R_{G11}	10			kΩ	Refer Fig. 23, note 14: SW1 Closed, RW = 300Ω
Earthcall active mode $\overline{DET} = 0$	R_{G20}			1.7	kΩ	Refer Fig. 23, note 14: SW1 Open, RW = 300Ω
Earthcall active mode $\overline{DET} = 1$	R_{G21}	10			kΩ	Refer Fig. 23, note 14: SW1 Open, RW = 0Ω
Earthcall disconnect A standby B mode, $\overline{DET} = 0$	R_{G30}			1.7	kΩ	Refer Fig. 23, note 14: SW1 Open, RW = 300Ω
Earthcall disconnect A standby B mode, $\overline{DET} = 1$	R_{G31}	10			kΩ	Refer Fig. 23, note 14: SW1 Open, RW = 0Ω
Relay drivers, saturation voltage (active)	V_{SAT}	– 2			V	I = 25mA Connected to BGND
Relay drivers, leakage current (non-active)	I_{LK}			0.1	mA	V_{OUT} = Voltage at pin 8
Relay drivers, clamp voltage	V_{CLMP}	V_{BAT} – 2.0			V	I = 25mA into pin 4 or 5

NOTES
12. Applied V_{BAT} = – 63V.
13. Constant current in Standby mode approximately $600 \div R_{TH}$.
14. For Polarity Reversed State, connections to LA and LB are reversed.

Digital Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input low voltage (D_0-D_3, E_1, CHCLK)	V_{IL}			0.7	V	
Input high voltage (D_0-D_3, E_1, CHCLK)	V_{IH}	2.0			V	
Input low current (D_0-D_3, E_1, CHCLK)	I_{IL}			-0.25	mA	V_{IL} = 0.4V
Input high current (D_0-D_3, E_1, CHCLK)	I_{IH}			0.04	mA	V_{IH} = 2.4V
$\overline{DET}$ output low voltage	V_{OL}			0.4	V	I_{OL} = 0.8mA
$\overline{DET}$ output high voltage	V_{OH}	2.4			V	I_{OH} = 0.1mA
$\overline{DET}$ output, internal pull-up	R_{OUT}	10		20	kΩ	
Propagation delay, E_1 to $\overline{DET}$	t_{PD}			4	μs	$\overline{DET}$ 6.2kΩ to V_{CC}, 15pF to BGND
Loop detector make response time	t_{LM}			5	ms	Z_L = 2kΩ (V_{OL} < 0.45)
Loop detector break response time	t_{LB}			10	ms	Z_L = 2kΩ (V_{OL} > 2.35)
CHCLK input frequency	F_{CLK}		256		kHz	
CHCLK input minimum pulse width	T_{CLK}		500		ns	

Recommended Operating Range

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply voltage	V_{CC}	+4.75	5.0	+5.25	V	
Negative supply voltage	V_{EE}	-4.75	-5.0	-5.25	V	
Battery supply voltage	V_{BAT}	-40.5	-48	-64	V	
Battery ground voltage	V_{BGND}	-0.1		+0.1	V	
Ambient temperature	T_{AMB}	0		+70	°C	

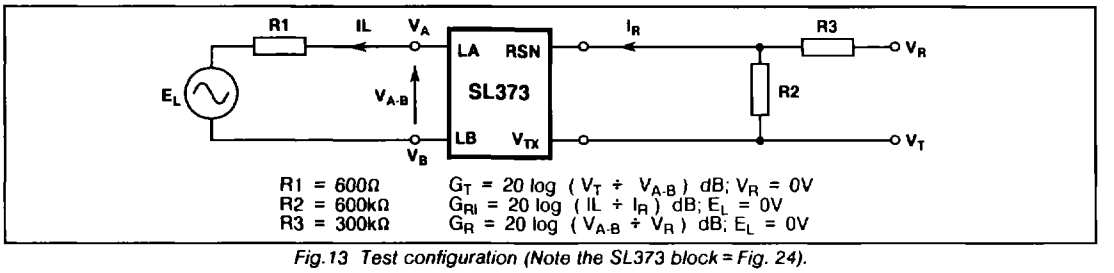


Fig.13 Test configuration (Note the SL373 block = Fig. 24).

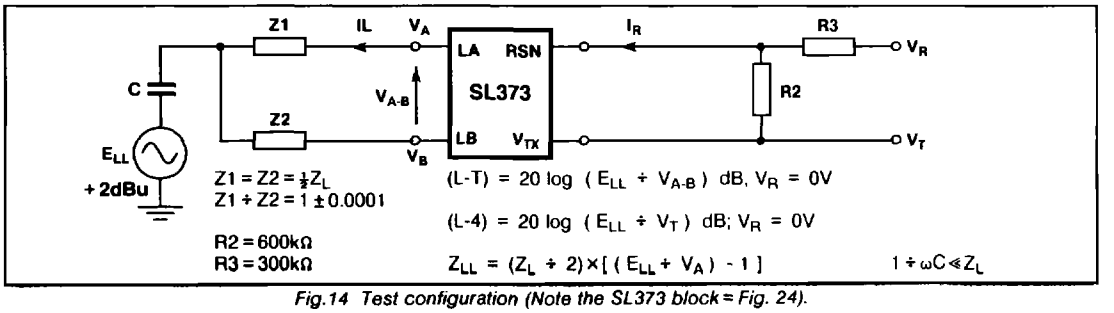


Fig.14 Test configuration (Note the SL373 block = Fig. 24).

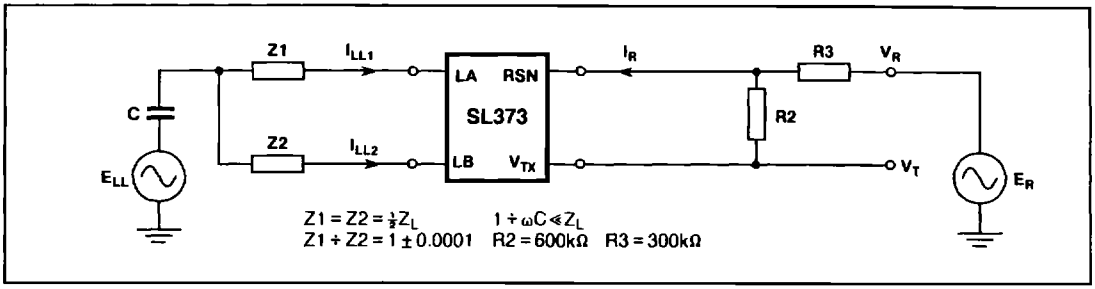


Fig.15 Test configuration (Note the SL373 block = Fig. 24).

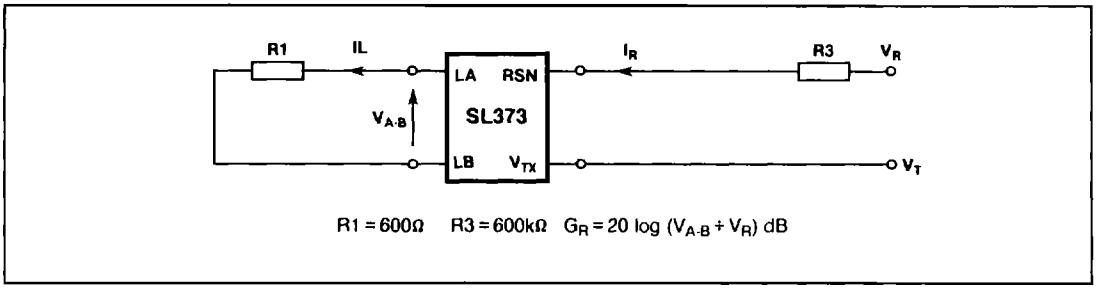


Fig.16 Test configuration (Note the SL373 block = Fig. 24).

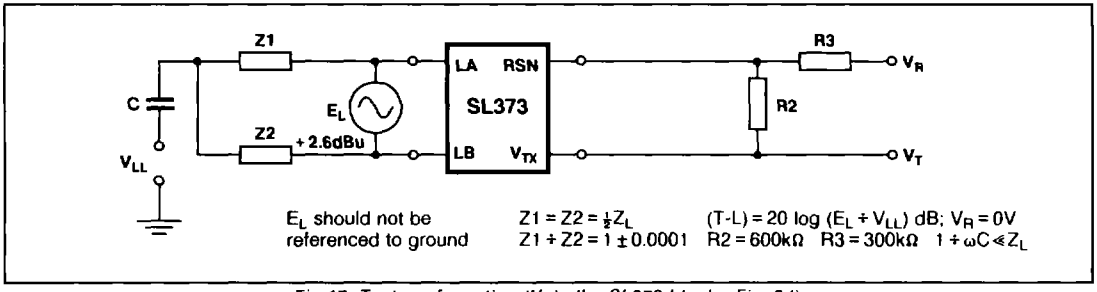


Fig.17 Test configuration (Note the SL373 block = Fig. 24).

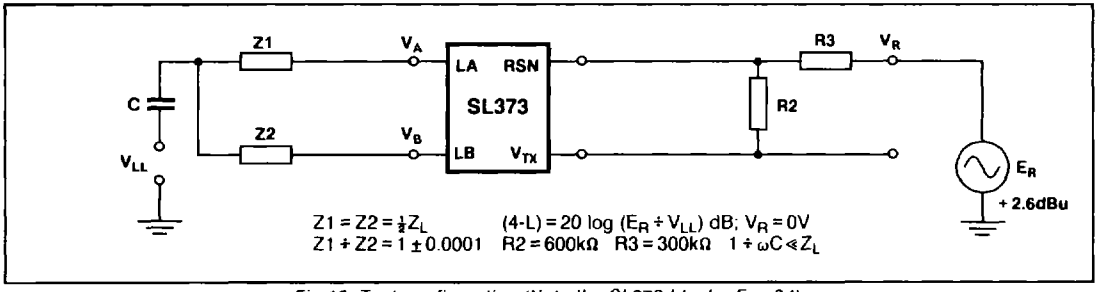
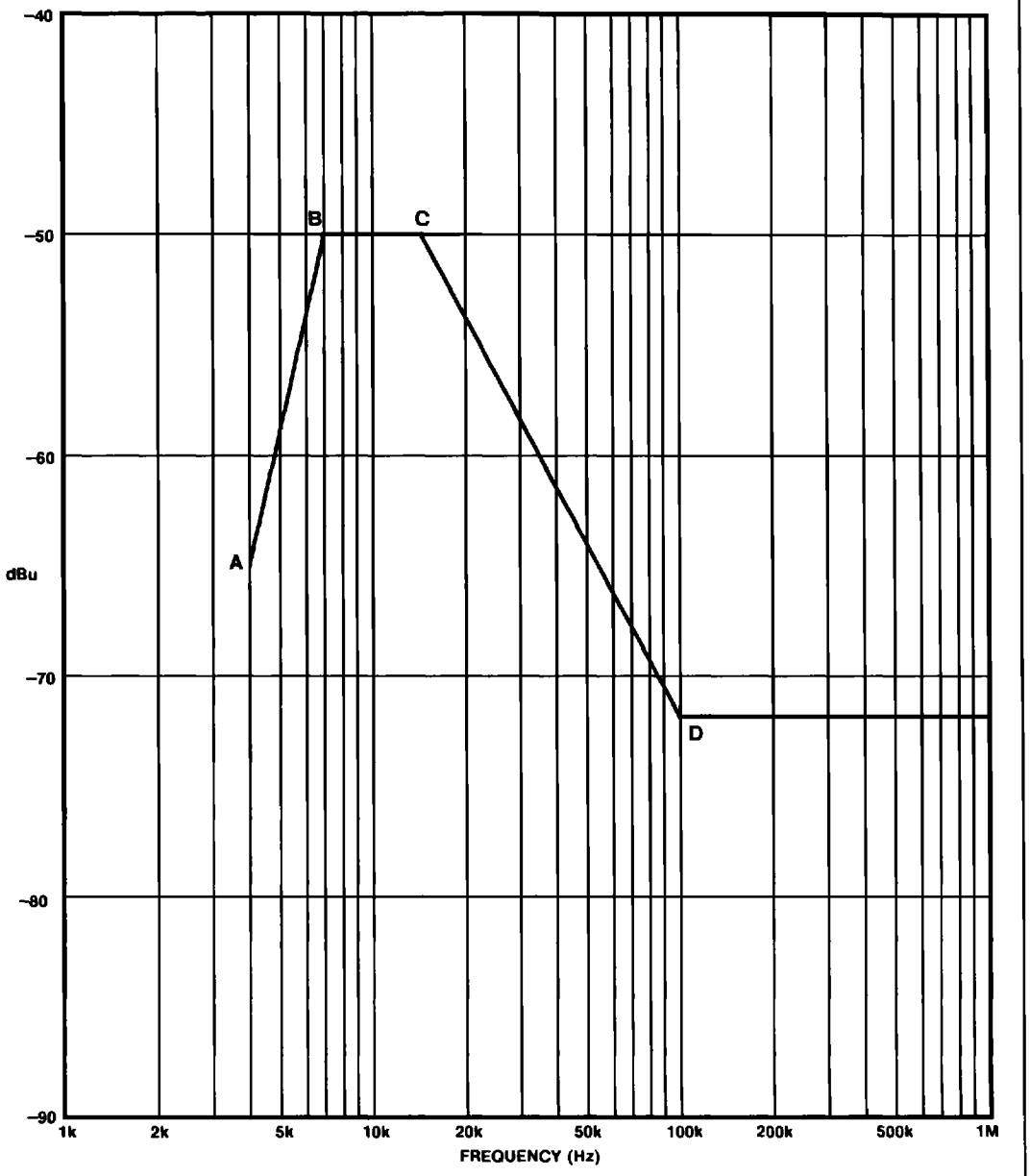


Fig.18 Test configuration (Note the SL373 block = Fig. 24).



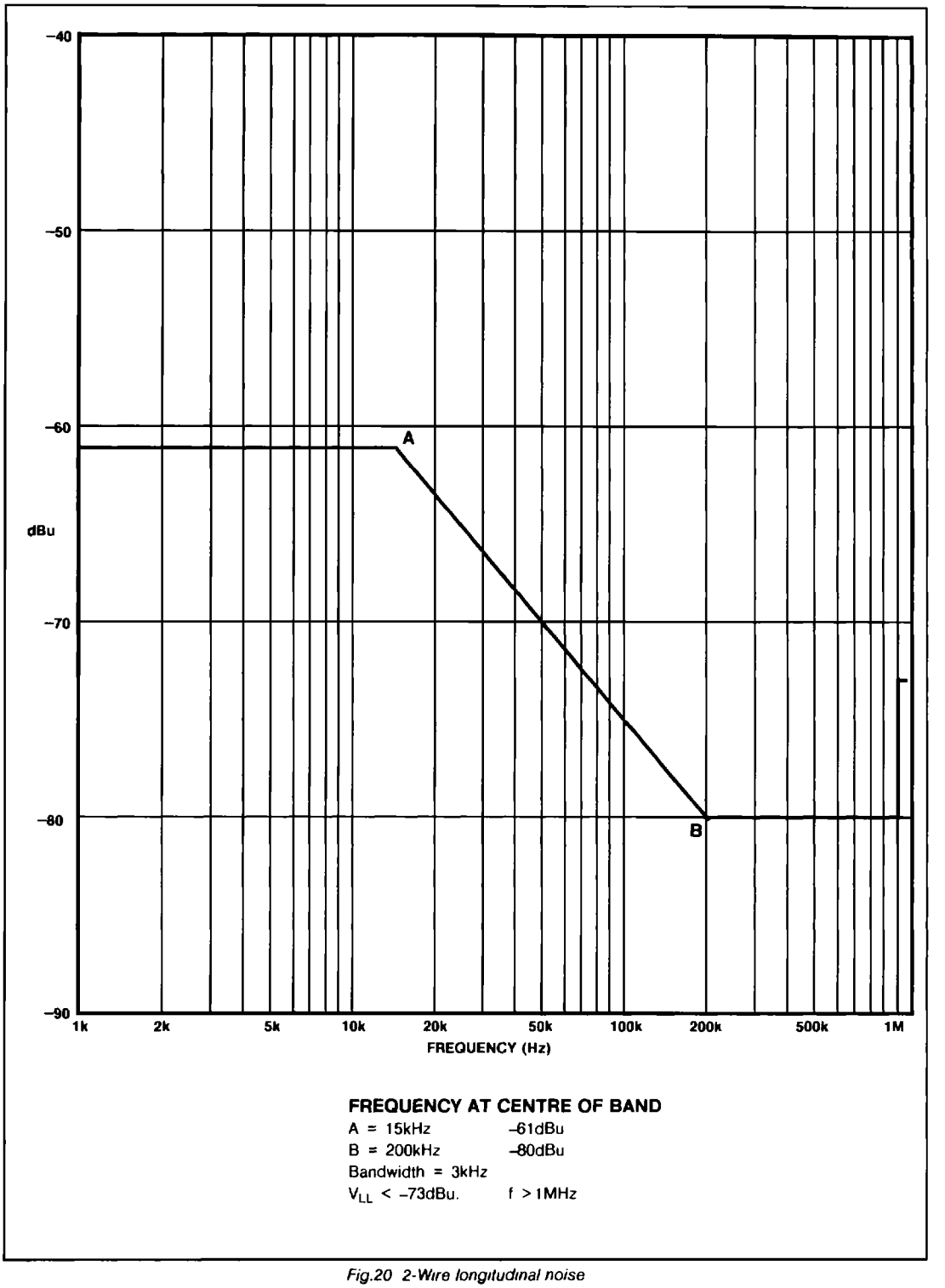
FREQUENCY AT CENTRE OF BAND

A = 4kHz	-65dBu	C = 15kHz	-50dBu
B = 7kHz	-50dBu	D = 100kHz	-73dBu

Bandwidth = 3kHz Minimum Centre Frequency = 1.6kHz

V_{A-B} < -73dBu. f > 1MHz

Fig.19 2-Wire differential noise



FREQUENCY AT CENTRE OF BAND

A = 15kHz –61dBu
B = 200kHz –80dBu
Bandwidth = 3kHz
V_{LL} < –73dBu. f > 1MHz

Fig.20 2-Wire longitudinal noise

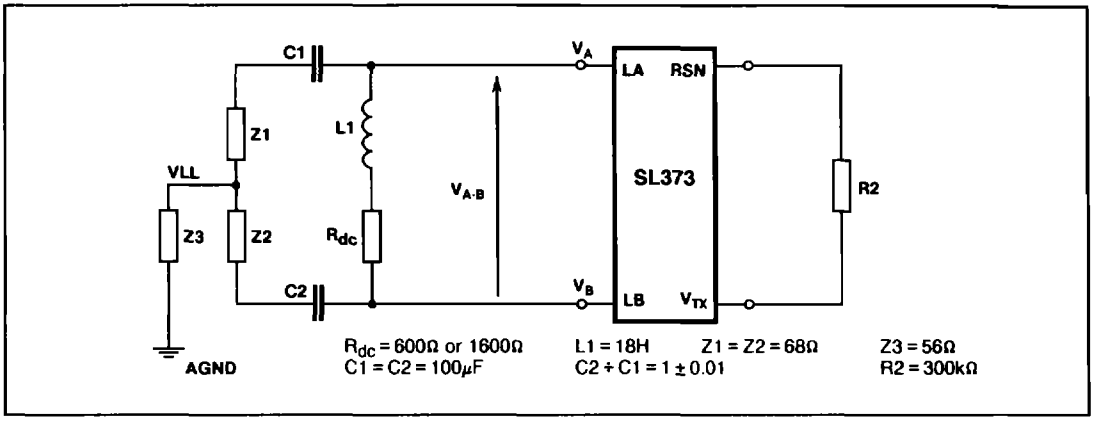


Fig.21 Test configuration (Note the SL373 block = Fig. 24)

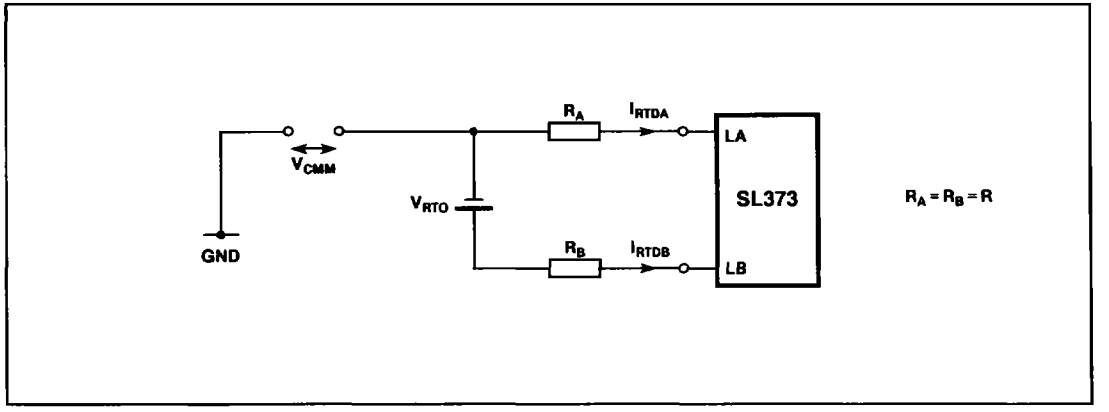


Fig.22 Test configuration (Note the SL373 block = Fig. 24)

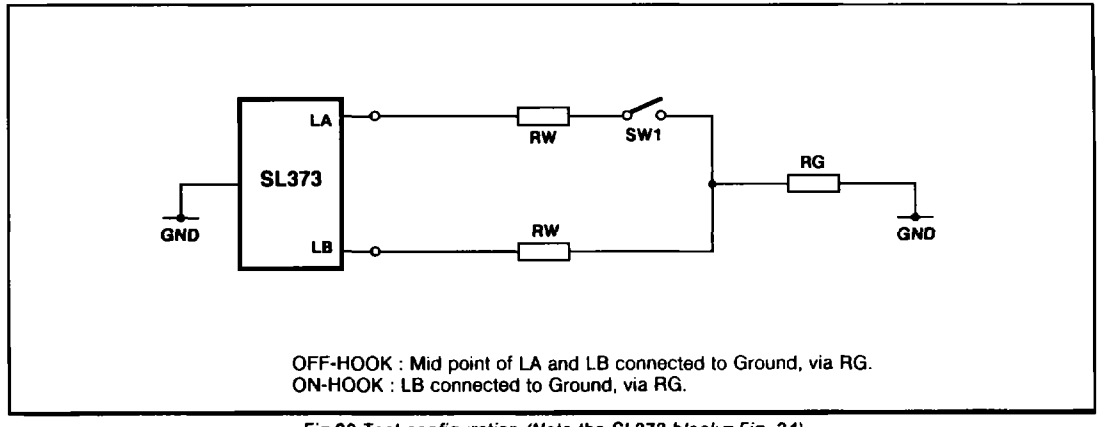
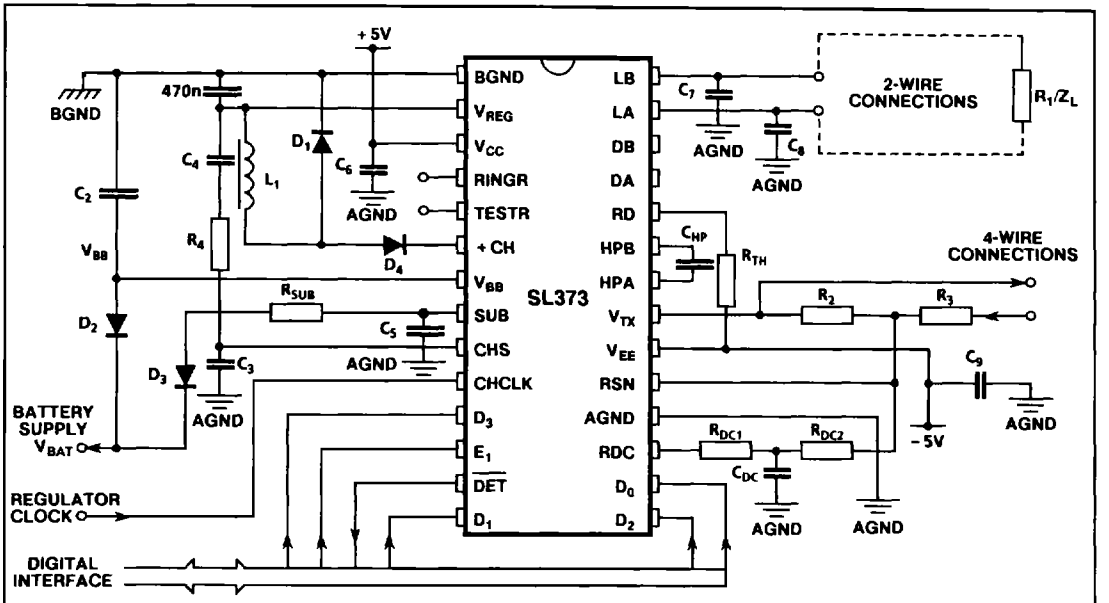


Fig.23 Test configuration (Note the SL373 block = Fig. 24)



C_1 = 470n	C_6 = 100n	C_{DC} = 82n	L_1 = 1mH	R_1 as Test Configuration
C_2 = 470n	C_7 = 10n	D_1 = 100V,100mA	R_{SUB} = 100Ω	R_2 as Test Configuration
C_3 = 560p	C_8 = 10n	D_2 = 100V,100mA	R_{TH} = 32kΩ (see Elec. Char.)	R_3 as Test Configuration
C_4 = 8.2n	C_9 = 100n	D_3 = 100V,100mA	R_{DC1} = R_{DC2} = 31.25kΩ(see Elec. Char.)	R_4 = 2.4kΩ
C_5 = 330n	C_{HP} = 330n	D_4 = 100V,100mA	Z_L = see Elec. Char.	

For all tests assume AGND = BGND

Fig.24 Test circuit for Figs. 13-18 and 21-23.

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Battery supply voltage	V_{BB}	- 70	+ 1.0	V
Continuous battery ground voltage	V_{BGNDC}	- 0.3	+ 0.3	V
Intermittent (10μs) battery ground voltage	V_{BGNDI}	- 4 0	+ 4.0	V
Positive supply voltage	V_{CC}	- 0.4	+ 7.0	V
Negative supply voltage	V_{EE}	- 7.0	+ 0.4	V
Subscriber line voltage on LA, LB or both, continuous	V_{LC}	- 70.0	+ 0.4	V
Differential DC line current	I_{LDC}		150	mA
Switched regulator voltage (off)	V_{CH}	V_{BB}	+ 1.0	V
Switched regulator current (on)	I_{CH}		150	mA
Relay drivers output voltage	V_{RLY}	V_{BAT}		V
Relay drivers output source current	I_{RLY}		30	mA
Ring-Trip input voltage (DA or DB)	V_{RT}	V_{BB}	0	V
Ring-Trip input current (non-repetitive 10 ms pulse)	I_{RT}	- 10.0	+ 10.0	mA
Digital input voltage	V_{ID}	- 0.4	V_{CC}	V
Digital input current (sink)	I_{ID}		5.0	mA
Digital output voltage	V_{OD}	- 0.3	V_{CC}	V
Digital output current (source)	I_{OD}		3	mA
Storage temperature	T_{ST}	- 55	+ 125	°C
Operating junction temperature †	T_{JOP}		150	°C
Package power dissipation (DG28)	P_{PDG28}		1 5	W

*** Exceeding these ratings may cause permanent damage.** Functional operation under these conditions is not implied.

† Circuit includes thermal protection such that T_{PROT} (MIN) = 150°C.