

Single Rail CODEC

Description

7508B (μ -law) and 7509B (A-law) are CMOS devices containing companding CODEC and PCM voice filters on a single chip.

An important feature is the operation with only a single + 5V power supply, which is useful for ISDN digital telephones, digital wireless equipment, etc.

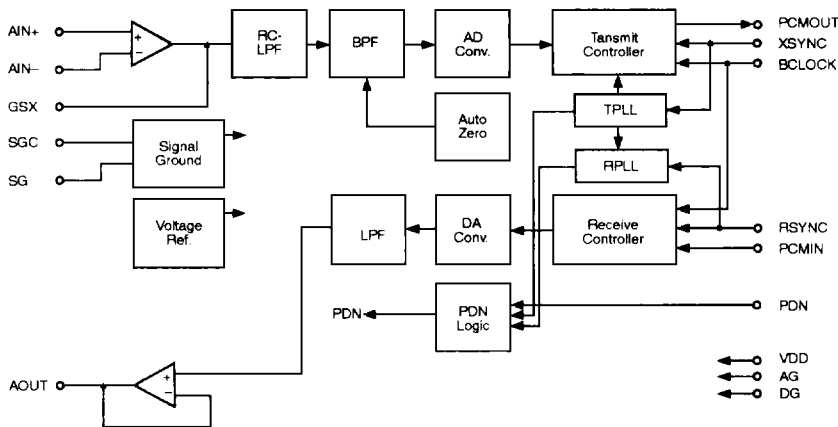
Features

- + 5V single power supply
- Low power dissipation
Operating mode : typ. 17.5 mW, max. 37 mW
Power down mode : typ. 1.5 mW, max. 3 mW
- Companding law
7508B : μ -law
7509B : A-law
- Transmit/receive synchronous mode only
- Serial data rate : 64/96/128/192/256/384/512/768/1024/1536/1544/2048 kbps
- On-chip full auto-zero and PLL
- On-chip analog pre-LPF
- Transmit gain adjustable
- On-chip precise voltage reference
- 16 pin plastic DIP
- 24 pin-V plastic SOP
- 28 pin plastic PLCC

Interface

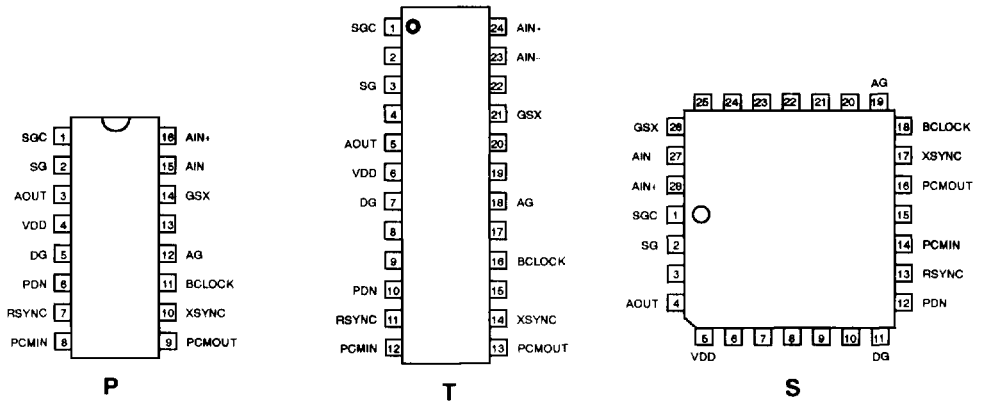
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Block Diagram



7508B/7509B

Pin Configuration



Pin Description

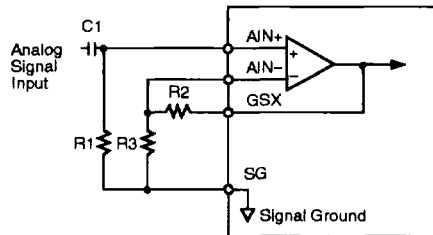
AIN+, AIN-, GSX

These three pins are used for the transmit gain adjustment. AIN+ is a Non-inverting Analog input pin which is connected to the non-inverting input of the transmit amplifier.

AIN- is a inverting Analog input pin which is connected to the inverting input of the transmit amplifier.

GSX is the transmit amplifier output in.

Gain adjustment should be referred to in the following figure.



$$\text{Gain} = 1 + \frac{R2}{R3} < 10$$

$$\begin{aligned} R2 + R3 &> 50 \text{ K}\Omega \\ R1 &> 50 \text{ K}\Omega \end{aligned}$$

AG

AG is the analog group (0V) pin.

VDD

VDD is the +5V power supply pin.

AOUT

AOUT is the analog signal output pin. The maximum voltage swing is 2.4Vpp and the AC ground is at the potential of SG (on-chip signal ground, VDD/2). Minimum load resistance is 20kΩ

PCMIN

PCM signal input pin. This signal is serial data and is converted to the analog signal under control of RSYNC and BCLOCK. The recommended PCM data rate is 64/96/128/192/256/384/512/768/1024/1536/1544/2048 kbps.

When the chip is in power down mode, the DC potential of AOUT is at on-chip signal ground (SG).

PCM serial data is shifted at the falling edge of BCLOCK. After the time when total 8 bits data are shifted, all 8 bits data are latched to the internal register. MSD (the first bit) is indicated at the rising edge of RSYNC.

BCLOCK

BCLOCK is the shift clock input pin. The clock frequency is same to the data transmission speed and is recommended to be 64/96/128/192/256/384/512/768/1024/1536/1544/2048 kHz.

When BCLOCK is continuously at digital "0" or "1" level, both transmit and receive sections are powered down.

RSYNC

Receive synchronizing signal input pin. This signal should be synchronous to BCLOCK and is used for taking in the required 8 bit data from the input serial PCM data stream. At the same time, this signal makes the whole receive operation timing to be synchronous.

XSYNC

Transmit synchronizing signal input pin. This signal should be synchronous to BCLOCK and is used for taking out the required 8 bits serial PCM data from PCMOUT. At the same time, this signal makes the whole transmit operation timing to be synchronous.

When XSYNC is continuously at digital "0" or "1" level, both transmit and receive sections are powered down.

Both RSYNC and XSYNC should be within 8 kHz \pm 50 ppm.

DG

DG is the digital ground (0V) pin. DG is separated from AG on the chip, but should be connected to AG on a printed circuit board.

PDN

Power-down control signal input pin. By putting PDN on digital "0" state, the whole transmit and receive sections enter to the power down mode.

PCMOUT

PCM signal output pin. This signal output being synchronized to the rising edge of BCLOCK with MSD first.

This pin shows the high output impedance except the 8 bit PCM data output duration, including the case of the power down mode.

Because of an open-drain output, wired-OR connections are easily performed.

The companding law and the coding pattern conform to CCITT recommendation.

In case of 7509B (A-law), the even bits are reversed except MSD.

	PCMIN / OUT	
	7508B	7509B
	MSD	MSD
+ Full scale	1000 0000	1010 1010
+ 0	1111 1111	1101 0101
- 0	0111 1111	0101 0101
- Full scale	0000 0000	0010 1010

SG

On-chip signal ground output pin. The potential is about a half of the supply voltage (\sim VDD/2) and its forcing/sinking capability is \pm 300 μ A.

SGC

The bypass capacitor for the signal ground should be put between SGC and AG.

A 0.1 μ F low inductance capacitor, such as a multilayer ceramic component, is recommended.

7508B/7509B

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Condition	Rating	Unit
V _{DD}	Supply Voltage	-	0 – 7	V
V _{AIN}	Analog Input Voltage	-	- 0.3 to V _{DD} + 0.3	V
V _{DIN}	Digital Input Voltage	-	- 0.3 to V _{DD} + 0.3	V
T _{OP}	Operating Temperature	-	0 to + 70	°C
T _{stg}	Storage Temperature	-	- 55 to + 150	°C

Recommended Operating Conditions

Symbol	Parameter		Condition	Min	Typ	Max	Unit
V _{DD}	Supply Voltage		-	+ 4.75	+ 5.0	+ 5.25	V
V _{AIN}	Analog Input Voltage		Transmit gain : 0dB	-	-	2.4	V _{PP}
V _{IH}	Input High Voltage		XSYNC,RSYNC,BCLOCK, PCMIN,PDN	+ 2.2	-	V _{DD}	V
V _{IL}	Input Low Voltage		XSYNC,RSYNC,BCLOCK, PCMIN,PDN	0	-	+ 0.6	V
F _C	Clock Frequency		BCLOCK	-	Note)	-	kHz
F _S	Sync. Pulse Frequency		XSYNC,RSYNC	-	8.0	-	kHz
D _C	Clock Duty Ratio		BCLOCK	40	50	60	%
T _{IR}	Digital	Rise Time	XSYNC,RSYNC,BCLOCK, PCMIN,PDN	-	-	50	ns
T _{IF}	Input	Fall Time	XSYNC,RSYNC,BCLOCK, PCMIN,PDN	-	-	50	ns
T _{XS}	Xmit Sync Timing		BCLOCK to XSYNC, Ref. Fig 2	100	-	-	ns
T _{SX}			XSYNC to BCLOCK, Ref. Fig 2	100	-	-	ns
T _{RS}	Receive Sync Timing		BCLOCK to RSYNC, Ref. Fig 2	100	-	-	ns
T _{SR}			RSYNC to BCLOCK, Ref. Fig 2	100	-	-	ns
T _{WS}	Sync Pulse Width		XSYNC,RSYNC	1 BCLK	-	100	s
T _{DS}	PCMIN Set-up Time		Ref. Fig 2	100	-	-	ns
T _{DH}	PCMIN Hold Time		Ref. Fig 2	100	-	-	ns
R _{AL}	Analog Output Load		AOUT	20	-	-	kΩ
			GSX	20	-	-	kΩ
C _{AL}			AOUT, GSX	-	-	100	pF
R _{DL}	Digital Output Load		Pull up Resistor	0.5	-	-	kΩ
C _{DL}				-	-	100	pF
V _{off}	Analog Input Allowable		Transmit gain : 0 dB	- 100	-	+ 100	mV
V _{off}	DC Offset		Transmit gain : + 20 dB	- 10	-	+ 10	mV

Note : 1. 64/96/128/192/256/384/512/768/1024/1536/1544/2048.

DC Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_a : 0 + 70^\circ\text{C}$)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD1}	Supply Current	Operating Mode	–	3.5	7.0	mA
I_{DD2}		Power Down Mode (PDN = 0)	–	0.3	0.5	mA
V_{IH}	Input High Voltage		2.2	–	V_{DD}	V
V_{IL}	Input Low Voltage		0.0	–	0.8	V
I_{IH}	Input Leakage Current	$V_I = V_{DD}$	–	–	2.0	μA
I_{IL}		$V_I = 0\text{ V}$	–	–	0.5	μA
V_{OL}	Output Low Voltage	1LSTTL, Pull-up ; 0.5 K Ω	0.0	0.2	0.4	V
I_O	Output Leakage Current	PCMOUT	–	–	10	μA
V_{off}	Analog Output Offset	AOUT	–100	–	100	mV
C_{IN}	Input Capacitance	All Pins	–	5	–	pF
R_{IN}	Input Resistance	AIN +, AIN –	10	–	–	M Ω

AC Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_a : 0 + 70^\circ\text{C}$)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
		Freq. (Hz)	Level (dBm0)				
Loss T1	Transmit Frequency Response	0 to 60	0	25	–	–	dB
Loss T2		300 to 3000	0	–0.15	–	0.20	dB
Loss T3		1020		Reference			
Loss T4		3300		–0.15	–	0.80	dB
Loss T5		3400		0	–	0.80	dB
Loss T6		3968.75		14	–	–	dB
Loss R1	Receive Frequency Response	0 to 3000		0	–0.15	–	0.20
Loss R2		1020	Reference				
Loss R3		3300	–0.15	–	0.80	dB	
Loss R4		3400	0	–	0.80	dB	
Loss R5		3968.75	14	–	–	dB	

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AC Characteristics (continued)

Symbol	Parameter	Condition			Min	Typ	Max	Unit
		Freq. (Hz)	Level (dBm0)					
SD T1	Transmit Signal to Distortion Ratio	1020	3	*1	35	-	-	dB
SD T2			0		35	-	-	dB
SD T3			-30		35	-	-	dB
SD T4			-40		28	-	-	dB
SD T5			-45		23	-	-	dB
SD R1	Receive Signal to Distortion Ratio	1020	3	*1	36	-	-	dB
SD R2			0		36	-	-	dB
SD R3			-30		36	-	-	dB
SD R4			-40		30	-	-	dB
SD R5			-45		25	-	-	dB
GT T1	Transmit Gain Tracking	1020	3		-0.2	-	0.2	dB
GT T2			-10		Reference			
GT T3			-40		-0.2	-	0.2	dB
GT T4			-50		-0.4	-	0.4	dB
GT T5			-55		-1.2	-	1.2	dB
GT R1	Receive Gain Tracking	1020	3		-0.2	-	0.2	dB
GT R2			-10		Reference			
GT R3			-40		-0.2	-	0.2	dB
GT R4			-50		-0.4	-	0.4	dB
GT R5			-55		-0.8	-	0.8	dB
ICN T	Idle Channel Noise			AIN=SG *1	-	-	-70/-69 *3	dBm0P
ICN R				*1 *2	-	-	-74	
AV T	Absolute Amplitude Level	1020	0	VDD : 5V±5%	0.5671	0.6007	0.6363	Vrms
AV R		1020	0	0 to 70 °C	0.5671	0.6007	0.6363	Vrms

*1 P message weighted

*2 7508B : PCMIN all "1"

7509B : PCMIN "11010101"

*3 7508B/7509B

AC Characteristics (continued)

Symbol	Parameter	Condition			Min	Typ	Max	Unit
		Freq. (Hz)	Level (dBm0)					
Td	Absolute Delay	1020	0	A to A, BCLOCK = 64kHz	-	-	0.60	ms
Tgd T1	Transmit Group Delay	500	0	* 4	-	0.19	0.75	ms
Tgd T2		600			-	0.11	0.35	ms
Tgd T3		1000			-	0.02	0.125	ms
Tgd T4		2600			-	0.05	0.125	ms
Tgd T5		2800			-	0.07	0.75	ms
Tgd R1	Receive Group Delay	500	0	* 4	-	0.00	0.75	ms
Tgd R2		600			-	0.00	0.35	ms
Tgd R3		1000			-	0.00	0.125	ms
Tgd R4		2600			-	0.09	0.125	ms
Tgd R5		2800			-	0.12	0.75	ms
CR T	Crosstalk Attenuation	300 to 3400	0	T to R	75	-	-	dB
CR R				R to T	70	-	-	dB
DIS	Discrimination Against Out-of-band Input Signal	4.6K to 72k	0	Measured ; 0 to 4000Hz	-	-	- 30	dB
S	Out-of-band Spurious "Noise" addition	300 to 3400	0	Measured ; 4.6 to 100kHz	-	-	- 30	dB
IMD	Intermodulation Distortion	fa, fb ; 300 to 3400	-4 to -21	Loop Around	-	-	- 41	dB
PSR T	Power Supply Noise Rejection Ratio	0 to 50K	50 mV pp		25	-	-	dB
PSR R								
Tsd	Digital Output Delay	CL=100 pF + 1 LSTTL Pull-up : 0.5 KΩ, Ref. Fig 2			50		200	ns
Txd1					50		200	ns
Txd2					50		200	ns
Txd3					50		200	ns

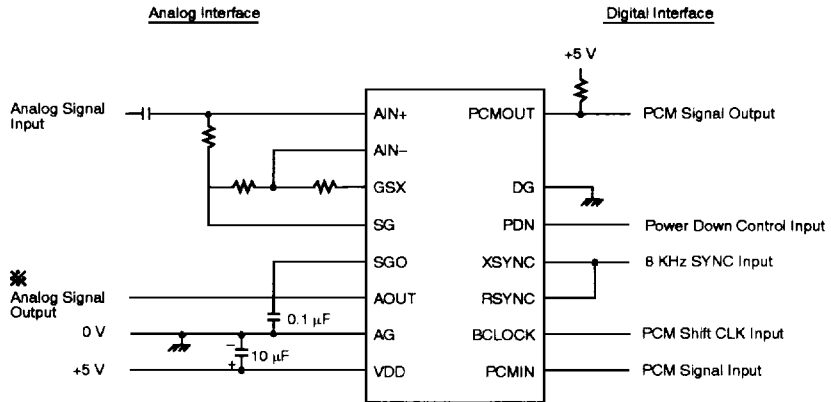
*4 The minimum value of the group delay distortion should be referred as 0 ms.

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7508B/7509B

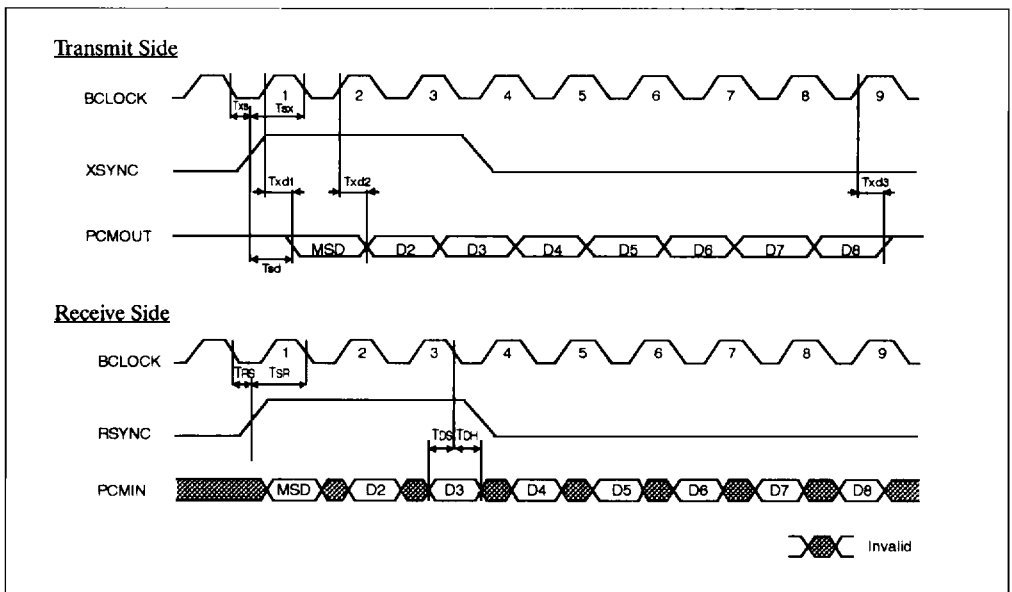
Application

Figure 1. Basic Circuit Configuration.

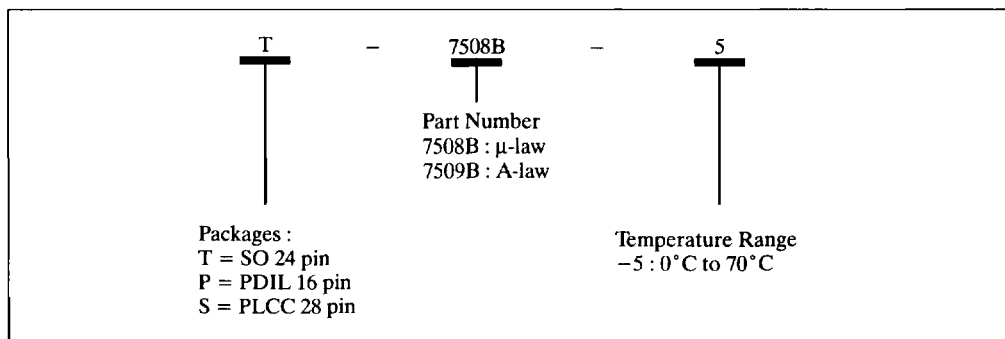


* The maximum voltage swing is 2.4 V_{pp} and AC ground is at around the potential of SG (on-chip signal ground, VDD/2).

Figure 2. Basic Timing Diagram.



Ordering Information



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