CY25C01/02/04/08/16

1 Kbit, 2 Kbit, 4 Kbit, 8 Kbit, and 16 Kbit (x8) SPI Serial EEPROM

Features

- Continuous voltage operation
  - V_{CC} = 1.8V to 5.5V
- Internally organized as 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K), or 2048 x 8 (16K)
- Serial peripheral interface compatible
- Supports SPI modes 0 (0,0) and 3 (1,1)
- Block write protection
  - Protect 1/4,1/2, or entire array
- Fast clock rate
  - 20 MHz clock rate (V_{CC} = 4.5V to 5.5V)
  - 10 MHz clock rate (V_{CC} = 1.8V to 5.5V)
- Write protect ($\overline{WP}$) pin and write disable instructions for both hardware and software data protection
- 32-byte page write mode
- Self timed write cycle (5 ms max)
- High reliability
  - Endurance: 1 million write cycles
  - Data retention: 100 years
- Industrial temperature range
- 8-Pin SOIC and 8-Pin TSSOP packages
- Pb-free and RoHS compliant

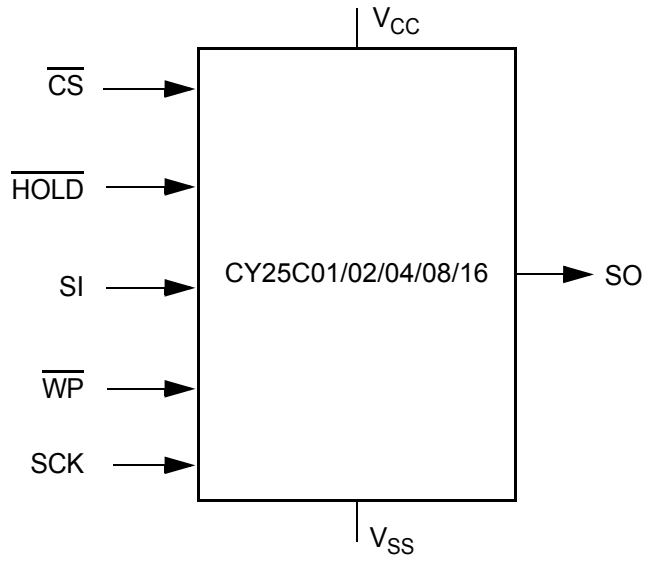
Functional Description

The CY25C01/02/04/08/16 provides 1024, 2048, 4096, 8192, and 16384 bits of serial Electrically Erasable and Programmable Read Only Memory (EEPROM) organized as 128, 256, 512, 1024, or 2048 words of eight bits each. The device is optimized for use in many industrial applications where low power and low voltage operations are essential. The CY25C01/02/04/08/16 is available in space saving 8-Pin SOIC, and 8-Pin TSSOP packages.

The CY25C01/02/04/08/16 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self timed and no separate erase cycle is required before write.

Block write protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided through the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin can be used to suspend any serial communication without resetting the serial sequence.

Logic Block Diagram



Pin Configuration

Figure 1. Pin Diagram - 8-Pin SOIC/TSSOP

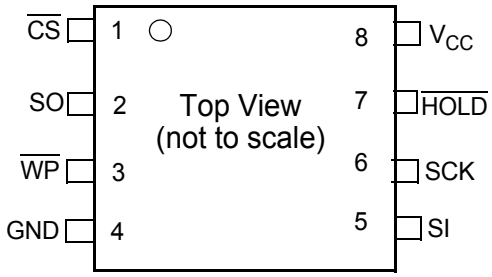


Table 1. Pin Definitions - 8 Pin SOIC/TSSOP

Pin Name	8-SOIC/PDIP/TSSOP Pin Number	I/O Type	Description
$\overline{CS}$	1	Input	Chip Select
SO	2	Output	Serial Data Output
$\overline{WP}$	3	Input	Write Protect
GND	4	Input	Ground
SI	5	Input	Serial Data Input
SCK	6	Input	Serial Data Clock
$\overline{HOLD}$	7	Input	Suspends Serial Input
V_{CC}	8	Input	Power Supply

Serial Interface Description

Master

The device that generates the serial clock.

Slave

The CY25C01/02/04/08/16 always operates as a slave because the Serial Clock pin (SCK) is always an input.

Transmitter or Receiver

The CY25C01/02/04/08/16 has separate pins designated for data transmission (SO) and reception (SI).

MSB

The Most Significant Bit (MSB) is the first bit transmitted and received.

Serial Op-Code

After the device is selected with $\overline{CS}$ going low, the first byte is received. This byte contains the op-code that defines the operations to be performed.

Invalid Op-Code

If an invalid op-code is received, no data is shifted to the CY25C01/02/04/08/16. The serial output pin (SO) remains in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This reinitializes the serial communication.

Chip Select

The CY25C01/02/04/08/16 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data is not accepted through the SI pin and the serial output pin (SO) remains in a high impedance state.

Hold

The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the CY25C01/02/04/08/16. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low when the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high when the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). The $\overline{HOLD}$ signal behaves as a level sensitive signal. This means, if the $\overline{HOLD}$ signal is asserted when SCK is high, its value is latched and when SCK becomes low, the latched value is considered to halt the transmission. Inputs to the SI pin are ignored when the SO pin is in the high impedance state.

Write Protect

The write protect pin ($\overline{WP}$) enables normal read or write operations when held high. When the $\overline{WP}$ pin is brought low, all write operations are inhibited. WP going low while $\overline{CS}$ is still low interrupts a write to the CY25C01/02/04/08/16. If the internal write cycle is already initiated, $\overline{WP}$ going low has no effect on the write operation.

SPI Modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the following modes:

- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (SCK) and output data is available from the falling edge of Serial Clock (SCK).

The difference between the two modes, shown in Figure 2 and Figure 3, is the clock polarity when the bus master is in standby mode and not transferring data:

- SCK remains at 0 for (CPOL=0, CPHA=0)
- SCK remains at 1 for (CPOL=1, CPHA=1)

Figure 2. SPI Mode 0

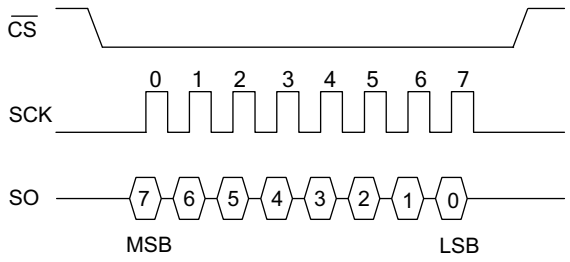
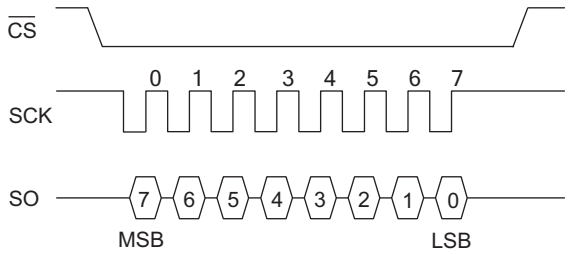


Figure 3. SPI Mode 3



Operating Features

Power Up

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{CS}$) must be allowed to follow the V_{CC} voltage. It must not be allowed to float, but must be connected to V_{CC} through a suitable pull up resistor. As a built in safety feature, Chip Select ($\overline{CS}$) is edge sensitive and level sensitive. After power up, the device is not selected until a falling edge is first detected on Chip Select ($\overline{CS}$). This ensures that the Chip Select ($\overline{CS}$) was high, before going low to start the first operation.

Device Internal Reset

To prevent inadvertent write operations during power up, a Power On Reset (POR) circuit is included. During power up (continuous rise up of V_{CC}), the device does not respond to any instruction until the V_{CC} reaches the POR threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage

During power down (continuous decay of V_{CC}), as soon as V_{CC} drops from the normal operating voltage, below the POR threshold voltage, the device stops responding to any instruction sent to it.

Power Down

During power down, the device must be deselected and in standby power mode (no internal write cycle in progress). Chip Select ($\overline{CS}$) must be allowed to follow the voltage applied on V_{CC}.

Active Power and Standby Power Modes

When Chip Select ($\overline{CS}$) is low, the device is selected in the active power mode. The device consumes I_{CC}, as specified in DC Electrical Characteristics on page 9. When Chip Select ($\overline{CS}$) is high, the device is deselected. If an erase or write cycle is currently not in progress, the device goes into the standby power mode, and the device consumption drops to I_{SB1}.

Functional Description

The CY25C01/02/04/08/16 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CY25C01/02/04/08/16 to interface directly with many of the popular microcontrollers.

The CY25C01/02/04/08/16 uses an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 2. All instructions, addresses, and data are transferred with the MSB, and it starts with a high to low ($\overline{CS}$) transition.

defined). When V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- Standby power mode
- Deselected (after power up, a falling edge is required on Chip Select (S) before any instructions are started)
- Not in the hold condition

Status register state:

- The Write Enable (WEN) bit is reset to 0
- ($\overline{RDY}$) is set to 1

The WPEN[1], BP1 and BP0 bits of the status register are unchanged from the previous power down (they are non volatile bits). Before selecting and issuing instructions to the memory, a valid and stable V_{CC} voltage must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and for a write instruction, until the completion of the internal write cycle (t_{WR}).

Table 2. Instruction Set

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data From Memory Array
WRITE	0000 X010	Write Data To Memory Array

Write Enable (WREN)

The device powers up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

Write Disable (WRDI)

To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the WP pin.

Read Status Register (RDSR)

The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device is determined by the RDSR instruction. Similarly, the block write protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Note
1. WPEN bit is applicable only for 8K and 16K devices.

Table 3. Status Register Format for CY25C01/02/04

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	RDY

Table 4. Status Register Format for CY25C08/16

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	RDY

Table 5. Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = '0' ($\overline{RDY}$) indicates the device is READY. Bit 0 = '1' indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= '0' indicates the device is not WRITE ENABLED. Bit 1 = '1' indicates the device is write enabled.
Bit 2 (BP0)	See Table 6.
Bit 3 (BP1)	See Table 6.
Bits 4–6 are '0's when device is not in an internal write cycle.	
Bit 7 (X / WPEN)	When the device is not in an internal write cycle, this bit is 0 in CY25C01/02/04 and WPEN (See Table 7 on page 5) in CY25C08/16
Bits 0–7 are '1's during an internal write cycle.	

Write Status Register (WRSR)

The WRSR instruction enables the user to select one of four levels of protection. The CY25C01/02/04/08/16 is divided into four array segments. One quarter, one half, or all of the memory segments can be protected. Any of the data within any selected segment is therefore read only. The block write protection levels and corresponding status register control bits are shown in Table 6.

The three bits BP0, BP1, and WPEN[1] are nonvolatile cells that have the same properties and functions as the regular memory cells (for example, WREN, t_{WC}, RDSR).

The WRSR instruction in CY25C08/16 also allows the user to enable or disable the write protect (WP) pin using the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is '1'. Hardware write protection is disabled when the $\overline{WP}$ pin is high or when the WPEN bit is '0' (See Table 7).

When the device is hardware write protected, writes to the status register, including the block protect bits and the WPEN[1] bit, and the block protected sections in the memory array are disabled. Writes are only allowed to sections of the memory that are not block protected.

Table 6. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected				
	BP1	BP0	CY25C01	CY25C02	CY25C04	CY25C08	CY25C16
0	0	0	None	None	None	None	None
1 (1/4)	0	1	60 - 7F	C0 - FF	180 - 1FF	0300 - 03FF	0600 - 07FF
2 (1/2)	1	0	40 - 7F	80 - FF	100 - 1FF	0200 - 03FF	0400 - 07FF
3 (All)	1	1	00 - 7F	00 - FF	000 - 1FF	0000 - 03FF	0000 - 07FF

Table 7. WPEN Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

Read Sequence (READ)

Reading the CY25C01/02/04/08/16 through the Serial Output (SO) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the read op-code (including A8) is transmitted through the SI line followed by the byte address to be read (A7–A0). When completed, any data on the SI line is ignored. The data (D7–D0) at the specified address is shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line must be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data continues to be shifted out. When the highest address is reached, the address counter rolls over to the lowest address allowing the entire memory to be read in one continuous read cycle.

Write Sequence (WRITE)[2]

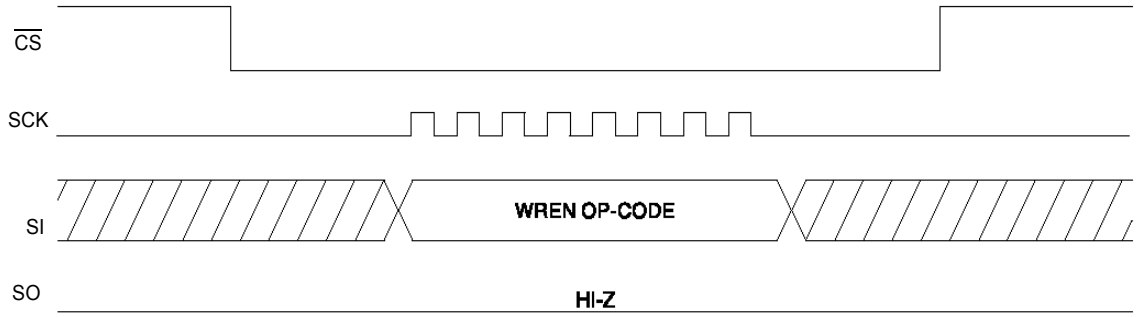
To program the CY25C01/02/04/08/16, two separate instructions must be executed. First, the device must be write enabled through the WREN instruction. Then a write (WRITE) instruction can be executed. Also, the address of the memory locations to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands are ignored except the RDSR instruction.

The sequence for a write instruction is as follows. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code is transmitted throuh the SI line followed by the byte address (A7–A0) and the data (D7–D0) to be programmed. Programming starts after the $\overline{CS}$ pin is brought high. The low to high transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The READY/$\overline{BUSY}$ status of the device is determined by initiating a read status register (RDSR) instruction. If Bit 0 = ‘1’, the write cycle is still in progress. If Bit 0 = ‘0’, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

The CY25C01/02/04/08/16 is capable of a 32-byte page write operation. After each byte of data is received, the five low order address bits are internally incremented by one; the high order bits of the address remain constant. If more than 16 bytes of data are transmitted, the address counter rolls over and the previously written data is overwritten. The CY25C01/02/04/08/16 is automatically returned to the write disable state at the completion of a write cycle. WEN bit is reset after every write instruction regardless of it belonging to a protected array.

Figure 4. Write Enable (WREN) Instruction Timing



Note
2. If the device is not write enabled (WREN), the device ignores the write instruction and return to the standby state, when $\overline{CS}$ is brought HIGH. A new $\overline{CS}$ falling edge is required to re initiate the serial communication.

Figure 5. Write Disable (WRDI) Instruction Timing

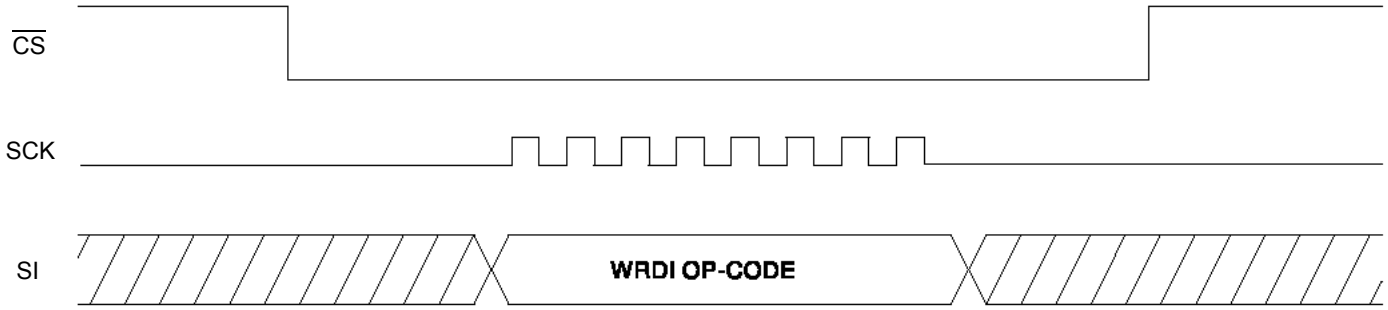


Figure 6. Read Status Register (RDSR) Instruction Timing

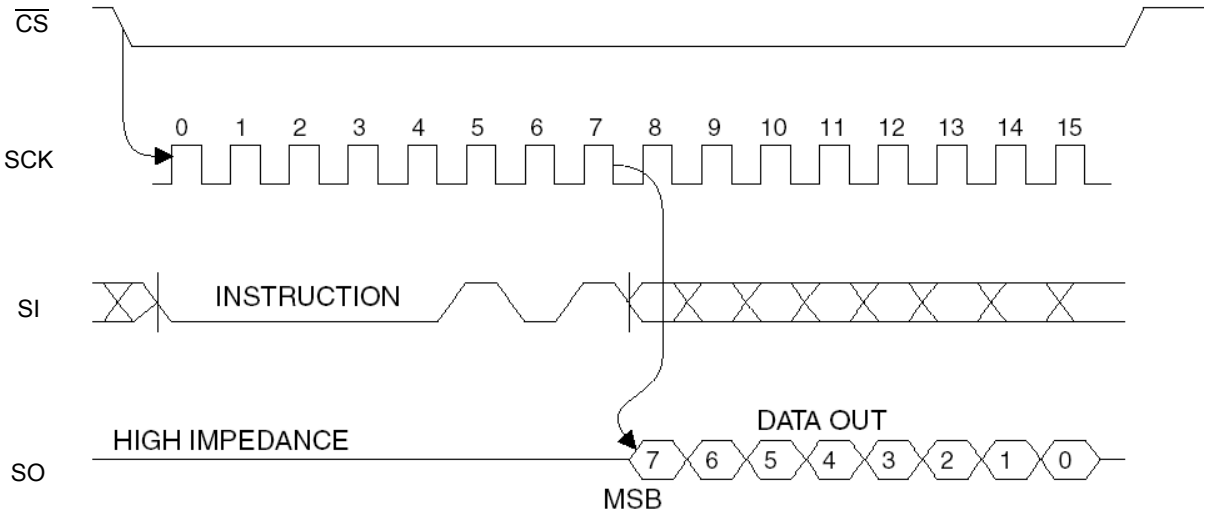


Figure 7. Write Status Register (WRSR) Instruction Timing

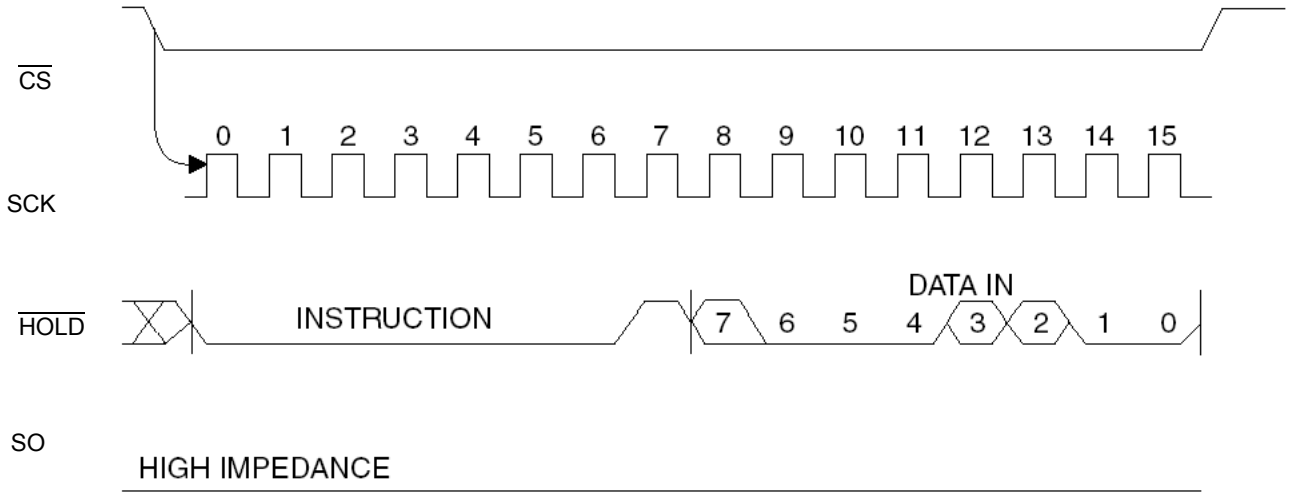


Figure 8. Read Instruction Timing

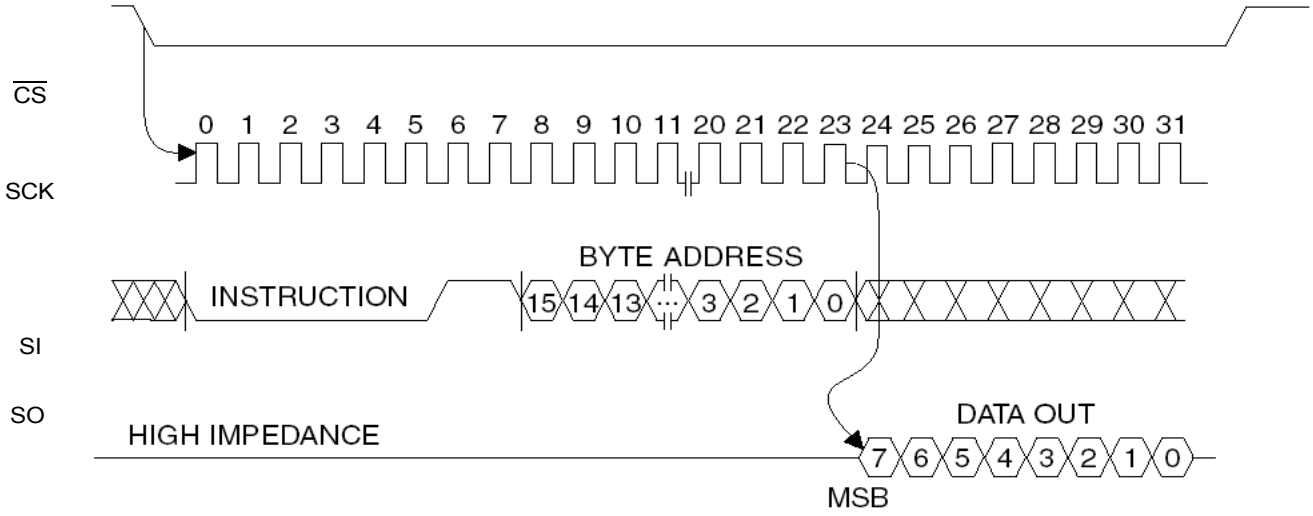
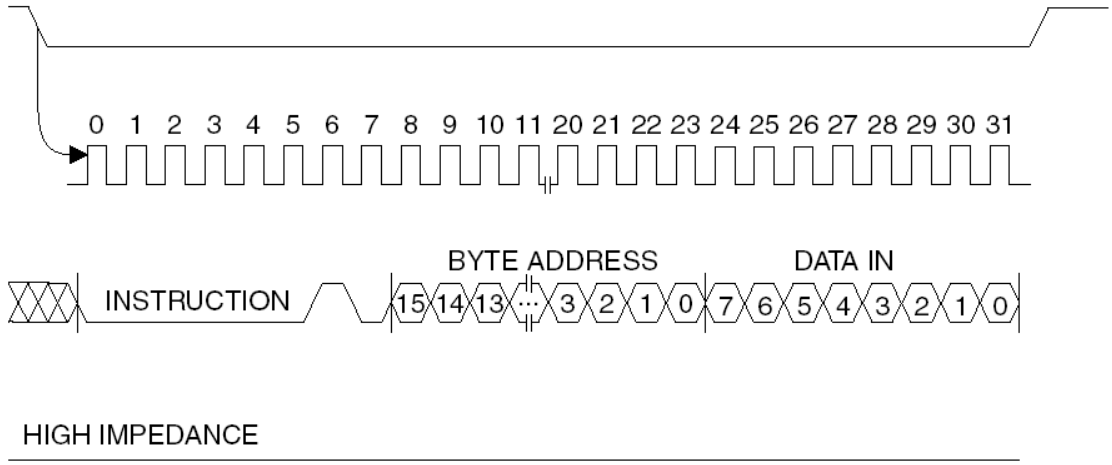


Figure 9. Write Instruction Timing



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65°C to +150°C

Ambient temperature with power applied ..... –40°C to +125°C

Supply voltage on V_{CC} relative to GND.....–0.6V to +6.0V

DC voltage applied to outputs in high-Z state..... –0.5V to V_{CC} + 1.0V

Input voltage..... –0.5V to V_{CC} + 0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... –1.0V to V_{CC} + 2.0V

Package power dissipation capability (T_A = 25°C) 1.0W

Surface mount lead soldering temperature (3 Seconds)..... +260°C for 10 seconds

Output short circuit current[3] ..... 50 mA

Static discharge voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	1.8V to 5.5V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 1.8V to 5.5V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		1.8	5.5	V
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}		1	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}		1.1	µA
I_{SB3}	Standby Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{CC}		1.2	µA
I_{CC1}	Supply Current (Read)	V_{CC} = 1.8V - 5.5V at 10 MHz		5	mA
		V_{CC} = 4.5V - 5.5V at 20 MHz		10	mA
I_{CC2}	Supply Current (Write)	V_{CC} = 5.5V		5	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		1	µA
I_{LO}	Output Leakage Current	V_{IN} = V_{CC} or V_{SS}		1	µA
V_{IL}	Input LOW Voltage	1.8V ≤ V_{CC} ≤ 2.7V	–0.6 [4]	0.3 V_{CC}	V
		2.7V ≤ V_{CC} ≤ 5.5V	–0.6 [4]	0.8	
V_{IH}	Input HIGH Voltage	1.8V ≤ V_{CC} ≤ 5.5V	0.7 V_{CC}	V_{CC} + 0.5 [4]	V
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA, 3.6 ≤ V_{CC} ≤ 5.5V		0.4	V
		I_{OL} = 0.15 mA, 1.8 ≤ V_{CC} ≤ 3.6V		0.2	
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA, 1.8 ≤ V_{CC} ≤ 3.6V	V_{CC} – 0.2		V
		I_{OH} = -1.6 mA, 3.6 ≤ V_{CC} ≤ 5.5V	V_{CC} – 0.8		

Note
3. Outputs shorted for only one second. Only one output shorted at a time.
4. This parameter is characterized but not tested.

Capacitance

In the following table, the capacitance parameters are listed. [5]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.5V	6	pF
C_{OUT}	Output Pin Capacitance		8	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[5]

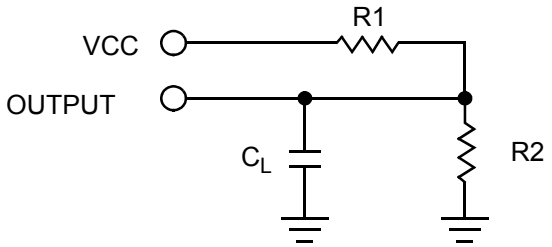
Parameter	Description	Test Conditions	8-SOIC	8-TSSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	120.83	119.31	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		90.31	82.77	°C/W

Reliability Characteristics

In the following table, the reliability characteristics parameters are listed.[5]

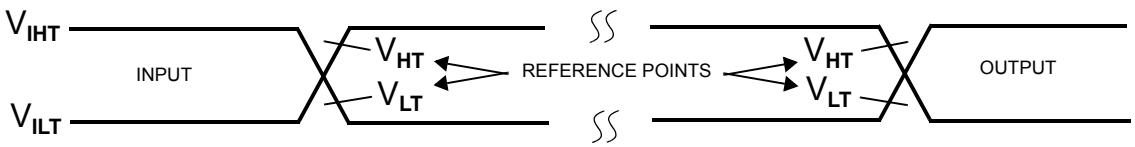
Parameter	Description	Test Method	Min	Unit
N_{END}	Endurance	JEDEC Standard A117	1 Million	Cycles
T_{DR}	Data Rentention	JEDEC Standard A103	100	Years
I_{LTH}	Latch Up	JEDEC Standard 78	100 + I_{CC}	mA

Figure 10. AC Test Loads and Waveforms



Parameters	Frequency	1.8V - 2.7V	2.7V - 5.5V	Unit
R1	20/10 MHz	1.8K	1.8K	Ω
R2	20/10 MHz	1.3K	1.3K	Ω
C_L	20 MHz	-	30	pF
	10 MHz	30		

Figure 11. AC Input/Output Reference Waveforms



AC test inputs are driven at V_{IHT} (0.9V_{CC}) for a logic “1” and V_{ILT} (0.1V_{CC}) for a logic “0”. Measurement reference points for inputs and outputs are V_{LT} (V_{CC}/2 - 0.1V) and V_{HT} (V_{CC}/2 + 0.1V). Input rise and fall times (10%–90%) are <20 ns

Note
5. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC Switching Characteristics

Cypress Parameter	Alt Parameter	Description	20 MHz (4.5V to 5.5V)		10 MHz (1.8V to 5.5V)		Unit
			Min	Max	Min	Max	
f_{SCK}	f_{SCK}	Clock Frequency, SCL		20		10	MHz
t_{CL}	t_{LOWH}	Clock Pulse Width Low	20		40		ns
t_{CH}	t_{WL}	Clock Pulse Width High	20		40		ns
t_{CE}	t_{CS}	$\overline{CS}$ High Time	30		50		ns
t_{CES}	t_{CSS}	$\overline{CS}$ Setup Time	25		50		ns
t_{CEH}	t_{CSH}	$\overline{CS}$ Hold Time	25		50		ns
t_{SD}	t_{SU}	Data In Setup Time	5		10		ns
t_{HD}	t_{H}	Data In Hold Time	5		10		ns
$t_{H.HLD}$	t_{HD}	$\overline{HOLD}$ Hold Time	5		10		ns
$t_{S.HLD}$	t_{CD}	$\overline{HOLD}$ Setup Time	5		10		ns
t_{CO}	t_{V}	Output Valid		20		40	ns
t_{HZ}	t_{HZ}	$\overline{HOLD}$ to Output High Z		40		80	ns
t_{LZ}	t_{LZ}	$\overline{HOLD}$ to Output Low Z		25		50	ns
t_{OH}	t_{HO}	Output Hold Time	0		0		ns
t_{HZCE}	t_{DIS}	Output Disable Time		40		80	ns
t_{WC}	t_{WC}	Write Cycle Time		5		5	ms
t_{r}	t_{r}	Rise Time		4.8		10	ns
t_{f}	t_{f}	Fall Time		4.8		10	ns

Figure 12. Synchronous Data Timing (Mode 0)

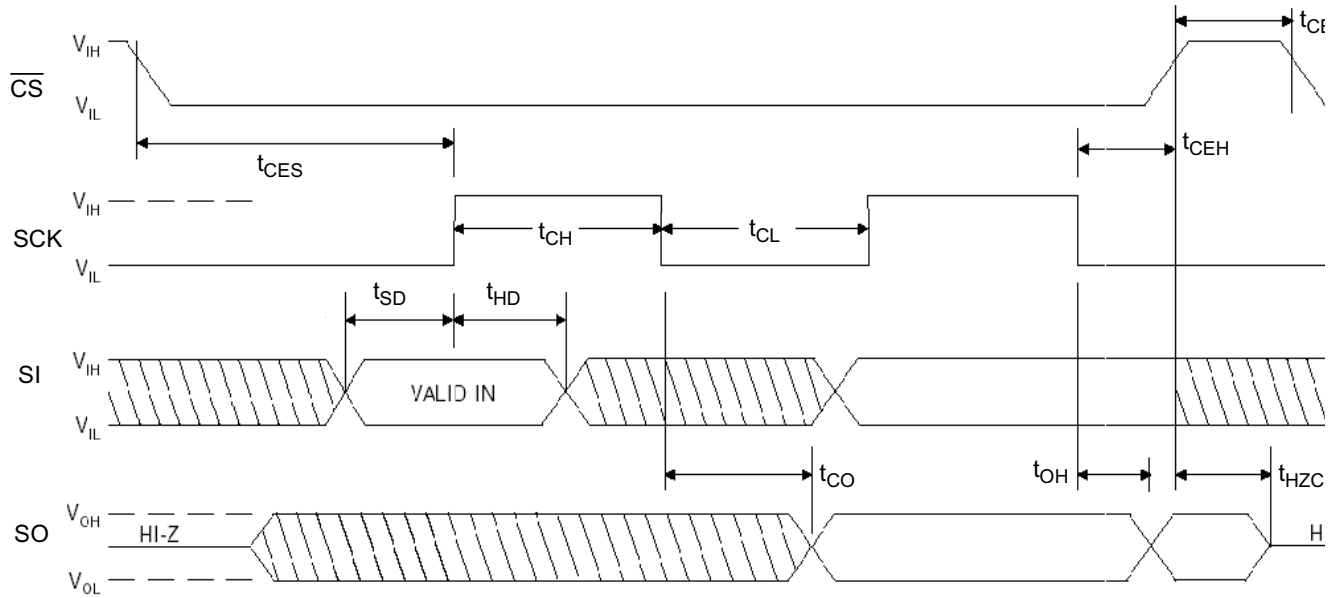
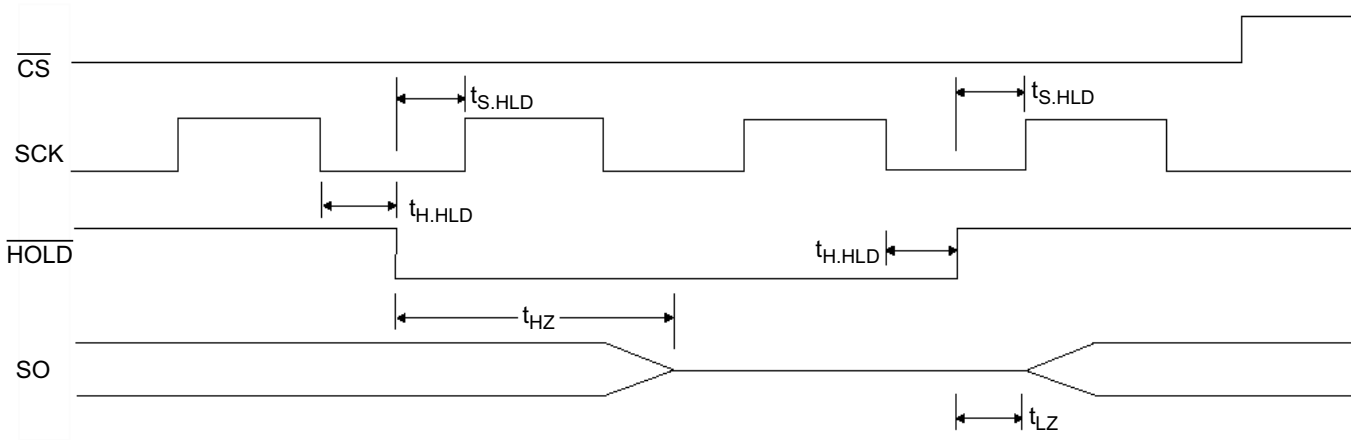
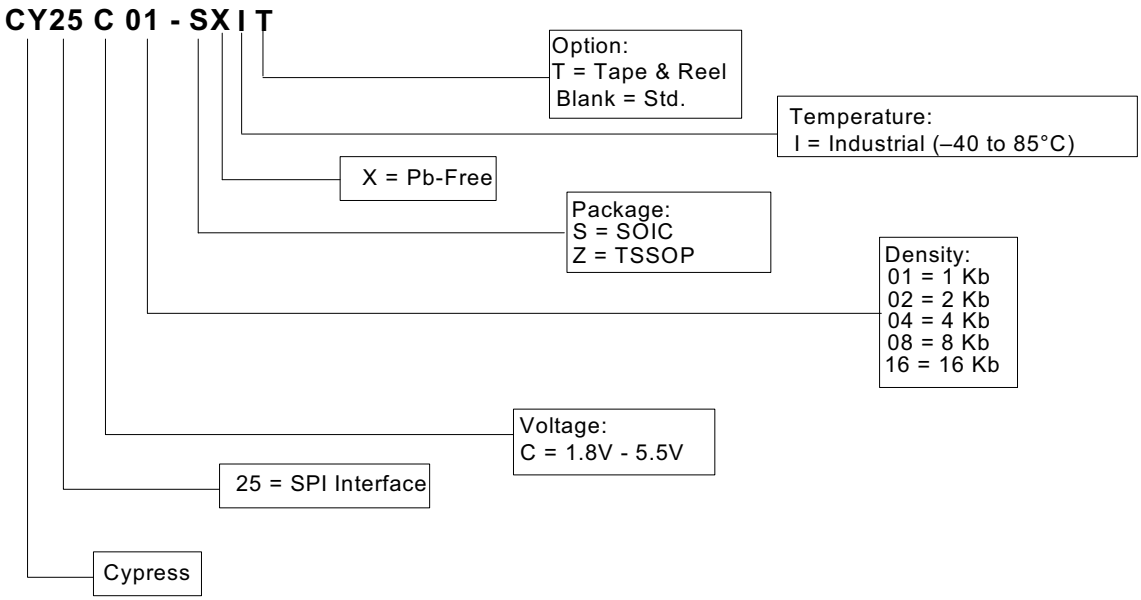


Figure 13. $\overline{\text{HOLD}}$ Timing



Part Numbering Nomenclature



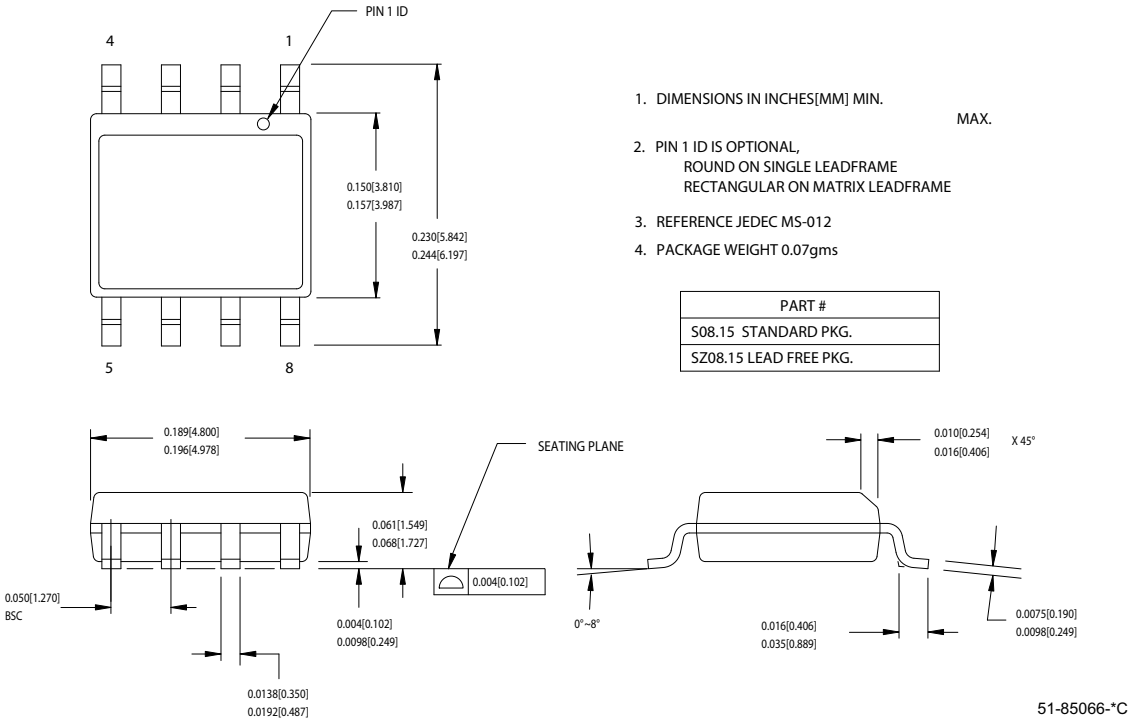
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
1 Kbit	CY25C01-SXI	51-85066	8-Pin SOIC	Industrial
	CY25C01-SXIT		8-Pin SOIC (Tape & Reel)	
	CY25C01-ZXI	51-85093	8-Pin TSSOP	
	CY25C01-ZXIT		8-Pin TSSOP (Tape & Reel)	
2 Kbit	CY25C02-SXI	51-85066	8-Pin SOIC	Industrial
	CY25C02-SXIT		8-Pin SOIC (Tape & Reel)	
	CY25C02-ZXI	51-85093	8-Pin TSSOP	
	CY25C02-ZXIT		8-Pin TSSOP (Tape & Reel)	
4 Kbit	CY25C04-SXI	51-85066	8-Pin SOIC	Industrial
	CY25C04-SXIT		8-Pin SOIC (Tape & Reel)	
	CY25C04-ZXI	51-85093	8-Pin TSSOP	
	CY25C04-ZXIT		8-Pin TSSOP (Tape & Reel)	
8 Kbit	CY25C08-SXI	51-85066	8-Pin SOIC	Industrial
	CY25C08-SXIT		8-Pin SOIC (Tape & Reel)	
	CY25C08-ZXI	51-85093	8-Pin TSSOP	
	CY25C08-ZXIT		8-Pin TSSOP (Tape & Reel)	
16 Kbit	CY25C16-SXI	51-85066	8-Pin SOIC	Industrial
	CY25C16-SXIT		8-Pin SOIC (Tape & Reel)	
	CY25C16-ZXI	51-85093	8-Pin TSSOP	
	CY25C16-ZXIT		8-Pin TSSOP (Tape & Reel)	

This table contains Preliminary information. Please contact your local Cypress sales representative for availability of these parts.

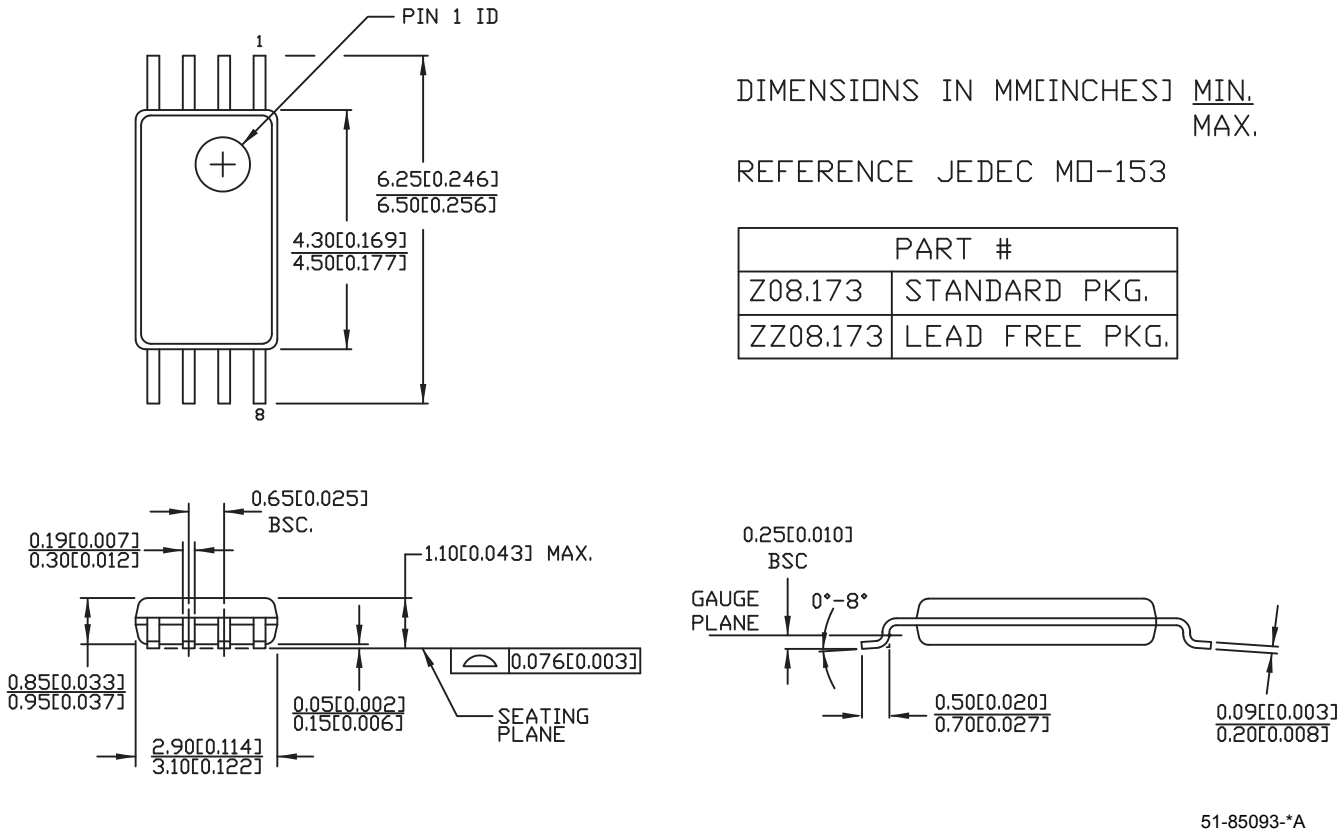
Package Diagrams

Figure 14. 8-Pin (150-Mil) SOIC, 51-85066



Package Diagrams (continued)

Figure 15. 8-Pin (4.4 mm) TSSOP, 51-85093



Document History Page

Document Title: CY25C01/02/04/08/16, 1 Kbit, 2 Kbit, 4 Kbit, 8 Kbit, and 16 Kbit (x8) SPI Serial EEPROM Document Number: 001-15633				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1069220	UHA	See ECN	New Data Sheet
*A	2522135	GVCH/ PYRS	06/27/08	32 byte Page Mode in Features Added Pb-Free and RoHS compliant information in “Features” Removed PDIP package Removed Automotive Temperature range Updated Status Register Bit Definition Table 3. Added description on write status Register(WRSR) Added WPEN Operation Table 5. Changed Supply voltage on V_{CC} relative to GND max value from 5.0V to 6.0V Corrected Typo of Vcc max value from 5.0V to 5.5V Table 10: Added Thermal Resistance values for 8-TSSOP package Table 12: Changed tr and tf values from 9.75 ns to 10 ns Added AC test load values for different parameters Updated Part Numbering Nomenclature and Ordering Information
*B	2611873	VKN/ PYRS	11/24/08	Changed Part # from CY25D01/02/04 to CY25C01/02/04 Added 8 Kbit and 16 Kbit parts and their related information Added footnote 1 related to WPEN Added 20 MHz clock rate specifications Updated part numbering nomenclature Updated ordering information table
*C	2656511	VKN/PYRS	02/09/09	Converted from preliminary to final Added figures 2 and 3 Included V_{IL} spec of 0.8V for the V_{CC} range between 2.7V to 5.5V Updated V_{IH} test conditions Added footnote #4 Updated V_{OL} and V_{OH} test conditions On page 10, specified V_{CC} range for AC test load conditions Changed C_L from 100pF to 30pF for 10MHz On page 10, corrected AC measurement reference points from V_{IT} and V_{OT} to V_{LT} and V_{HT} respectively Changed V_{LT} level from $0.3V_{CC}$ to $V_{CC}/2$ - 0.1V Changed V_{HT} level from $0.7V_{CC}$ to $V_{CC}/2$ + 0.1V

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