



# GLT5160L16

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16M (2-Bank x 524288-Word x 16-Bit) Synchronous DRAM

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## FEATURES

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- Single 3.3 V  $\pm 0.3$  V power supply
- Clock frequency 100 MHz / 125 MHz / 143 MHz / 166 MHz
- Fully synchronous operation referenced to clock rising edge
- Dual bank operation controlled by BA (Bank Address)
- CAS latency- 2 / 3 (programmable)
- Burst length- 1 / 2 / 4 / 8 & Full Page (programmable)
- Burst type- sequential / interleave (programmable)
- Industrial grade available
- Byte control by DQMU and DQML
- Column access - random
- Auto precharge / All bank precharge controlled by A[10]
- Auto refresh and Self refresh
- 4096 refresh cycles / 64 ms
- LVTTL Interface
- 400-mil, 50-Pin Thin Small Outline Package (TSOP II) with 0.8 mm lead pitch
- 60-Ball, 6.4mmx10.1mm VFPGA package with 0.65mm Ball pitch & 0.35mm Ball diameter.
- 48-Ball, 6mmx8mmx0.95mm VFPGA package with 0.75mm Ball pitch & 0.3mm ball diameter.

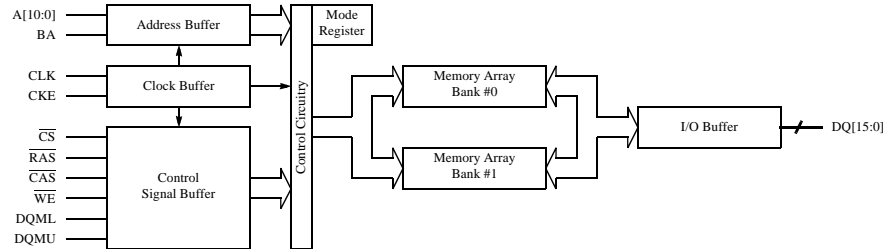
## GENERAL DESCRIPTION

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The GLT5160L16 is a 2-bank x 524288-word x 16-bit Synchronous DRAM, with LVTTL interface. All inputs and outputs are referenced to the rising edge of CLK. The GLT5160L16 achieves

very high speed data rate up to 166 MHz, and is suitable for main memory or graphic memory in computer systems.

## FUNCTIONAL BLOCK DIAGRAM



**Figure 1. 16M (2-Bank x 524288-Word x 16-Bit) Synchronous DRAM**

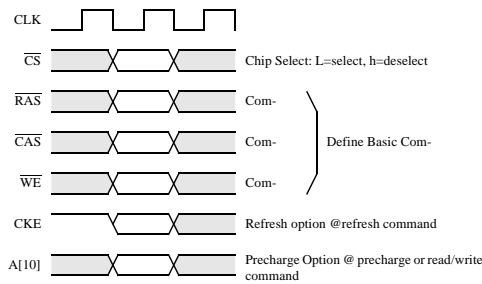
### Signal Description

Signal	Type	Description
CLK	Input	Master Clock: All other inputs are referenced to the rising edge of CLK.
CKE	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
$\overline{CS}$	Input	Chip Select: When $\overline{CS}$ is high, any command means No Operation.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Input	Combination of $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ defines basic commands.
A[10:0]	Input	A[10:0] specify the Row / Column Address in conjunction with BA. The Row Address is specified by A[10:0]. The Column Address is specified by A[7:0]. A[10] is also used to indicate precharge option. When A[10] is high at a read / write command, an auto precharge is performed. When A[10] is high at a precharge command, both banks are precharged.
BA	Input	Bank Address: BA is not simply A[11]. BA specifies the bank to which a command is applied. BA must be set with ACT, PRE, READ, WRITE commands.
DQ[15:0]	Input / Output	Data In and Data out are referenced to the rising edge of CLK.
DQML	Input	Lower Din[7:0] Mask / Lower Output[7:0] Disable: When DQML is high in burst write, lower Din[7:0] for the current cycle is masked. When DQML is high in burst read, lower Dout[7:0] is disabled at the next but one cycle.
DQMU	Input	Upper Din[15:8] Mask / Upper Output[15:8] Disable: When DQMU is high in burst write, upper Din[8-15] for the current cycle is masked. When DQMU is high in burst read, upper Dout[15:8] is disabled at the next but one cycle.
$V_{DD}$ , $V_{SS}$	Power Supply	Power Supply for the memory array and peripheral circuitry.
$V_{DDQ}$ , $V_{SSQ}$	Power Supply	$V_{DDQ}$ and $V_{SSQ}$ are supplied to the Output Buffers only.

## FUNCTIONAL DESCRIPTION

The GLT5160L16 provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh. Each command is defined by control signals of  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$  at CLK rising edge. In addition to 3 signals,  $\overline{\text{CS}}$ ,  $\overline{\text{CKE}}$  and A[10] are used as chip select, refresh option, and precharge option, respectively.

To know the detailed definition of commands, please see the command truth table.



### Activate (ACT) [ $\overline{\text{RAS}} = \text{L}$ , $\overline{\text{CAS}} = \overline{\text{WE}} = \text{H}$ ]

ACT command activates a row in an idle bank indicated by BA.

### Read (READ) [ $\overline{\text{RAS}} = \text{H}$ , $\overline{\text{CAS}} = \text{L}$ , $\overline{\text{WE}} = \text{H}$ ]

READ command starts burst read from the active bank indicated by BA. First output data appears after  $\overline{\text{CAS}}$  latency. When A[10] = H at this command, the bank is deactivated after the burst read (auto-precharge, READA).

### Write (WRITE) [ $\overline{\text{RAS}} = \text{H}$ , $\overline{\text{CAS}} = \overline{\text{WE}} = \text{L}$ ]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A[10] = H at this command, the bank is deactivated after the burst write (auto-precharge, WRITEA).

### Precharge (PRE) [ $\overline{\text{RAS}} = \text{L}$ , $\overline{\text{CAS}} = \text{H}$ , $\overline{\text{WE}} = \text{L}$ ]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A[10] = H at this command, both banks are deactivated (precharge all, PREA).

### Auto-Refresh (REFA) [ $\overline{\text{RAS}} = \overline{\text{CAS}} = \text{L}$ , $\overline{\text{WE}} = \overline{\text{CKE}} = \text{H}$ ]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically. Any other command should not be asserted until  $t_{RC}$  is met.

Command Truth Table <sup>[1]</sup>

Command	Mnemonic	CKE n-1	CKE n	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA	A[10]	A[9:0]
Deselect	DESEL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	L	X
Precharge All Banks	PREA	H	X	L	L	H	L	V	H	X
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	L	V
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	H	V
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X
Burst Terminate	TBST	H	X	L	H	H	L	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	X	L	V

1. H = High Level, L = Low Level, V = Valid, X = Don't Care, n = CLK cycle number

**Function Truth Table** <sup>[1][2]</sup>

Current State	CS	RAS	CAS	WE	Address <sup>[3]</sup>	Command	Action <sup>[4]</sup>
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL <sup>[5]</sup>
	L	H	L	X	BA, CA, A[10]	READ / WRITE	ILLEGAL <sup>[5]</sup>
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A[10]	PRE / PREA	NOP <sup>[6]</sup>
	L	L	L	H	X	REFA	Auto-Refresh <sup>[7]</sup>
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set <sup>[7]</sup>
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	NOP
	L	H	L	H	BA, CA, A[10]	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A[10]	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL <sup>[5]</sup>
	L	L	H	L	BA, A[10]	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	REFA	ILLEGAL
READ	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A[10]	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge <sup>[8]</sup>
	L	H	L	L	BA, CA, A[10]	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge <sup>[8]</sup>
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL <sup>[5]</sup>
	L	L	H	L	BA, A[10]	PRE / PREA	Terminate Burst, Precharge
WRITE	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A[10]	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge <sup>[8]</sup>
	L	H	L	L	BA, CA, A[10]	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge <sup>[8]</sup>
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL <sup>[5]</sup>
	L	L	H	L	BA, A[10]	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

**Function Truth Table <sup>[1][2]</sup> (Continued)**

Current State	CS	RAS	CAS	WE	Address <sup>[3]</sup>	Command	Action <sup>[4]</sup>
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	H	BA, CA, A[10]	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A[10]	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL <sup>[5]</sup>
	L	L	H	L	BA, A[10]	PRE / PREA	ILLEGAL <sup>[5]</sup>
	L	L	L	H	X	REFA	ILLEGAL
WRITE with AUTO PRECHARGE	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	H	BA, CA, A[10]	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A[10]	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL <sup>[5]</sup>
	L	L	H	L	BA, A[10]	PRE / PREA	ILLEGAL <sup>[5]</sup>
PRE -CHARGING	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESEL	NOP (Idle after t <sub>RP</sub> )
	L	H	H	H	X	NOP	NOP (Idle after t <sub>RP</sub> )
	L	H	H	L	X	TBST	ILLEGAL <sup>[5]</sup>
	L	H	L	X	BA, CA, A[10]	READ / WRITE	ILLEGAL <sup>[5]</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>[5]</sup>
	L	L	H	L	BA, A[10]	PRE / PREA	NOP <sup>[6]</sup> (Idle after t <sub>RP</sub> )
ROW ACTIVATING	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESEL	NOP (Row Active after t <sub>RCD</sub> )
	L	H	H	H	X	NOP	NOP (Row Active after t <sub>RCD</sub> )
	L	H	H	L	X	TBST	ILLEGAL <sup>[5]</sup>
	L	H	L	X	BA, CA, A[10]	READ / WRITE	ILLEGAL <sup>[5]</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>[5]</sup>
	L	L	H	L	BA, A[10]	PRE / PREA	ILLEGAL <sup>[5]</sup>
WRITE RECOVERING	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	ILLEGAL <sup>[5]</sup>
	L	H	L	X	BA, CA, A[10]	READ / WRITE	ILLEGAL <sup>[5]</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>[5]</sup>
	L	L	H	L	BA, A[10]	PRE / PREA	ILLEGAL <sup>[5]</sup>
WRITE RECOVERING	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

**Function Truth Table <sup>[1][2]</sup> (Continued)**

Current State	CS	RAS	CAS	WE	Address <sup>[3]</sup>	Command	Action <sup>[4]</sup>
REFRESHING	H	X	X	X	X	DESEL	NOP (Idle after t <sub>RC</sub> )
	L	H	H	H	X	NOP	NOP (Idle after t <sub>RC</sub> )
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	X	BA, CA, A[10]	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A[10]	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after t <sub>RSC</sub> )
	L	H	H	H	X	NOP	NOP (Idle after t <sub>RSC</sub> )
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	X	BA, CA, A[10]	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A[10]	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

1. H = High Level, L = Low Level, X = Don't Care.
2. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
3. BA = Bank Address, RA = Row Address, CA = Column Address, NOP = No Operation.
4. ILLEGAL = Device operation and/or data-integrity are not guaranteed.
5. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
6. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
7. ILLEGAL if any bank is not idle.
8. Must satisfy bus contention, bus turn around, write recovery requirements.

**Function Truth Table for CKE [1]**

Current State	CKE n-1	CKE n	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Add	Action
SELF-REFRESH [2]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after $t_{RC}$ )
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after $t_{RC}$ )
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
ALL BANKS IDLE [3]	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State = Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle [4]
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle [4]
	L	L	X	X	X	X	X	Maintain CLK Suspend

1. H = High Level, L= Low Level, X = Don't Care.
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
4. Must be legal command.

### Power On Sequence

Before starting normal operation, the following power on sequence is necessary to prevent damage or malfunction.

1. Apply power and start clock. Attempt to maintain CKE high, DQMU / DQML high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200  $\mu$ s.

3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after  $t_{RP}$ ), issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After this sequence, the SDRAM is idle state and ready for normal operation.

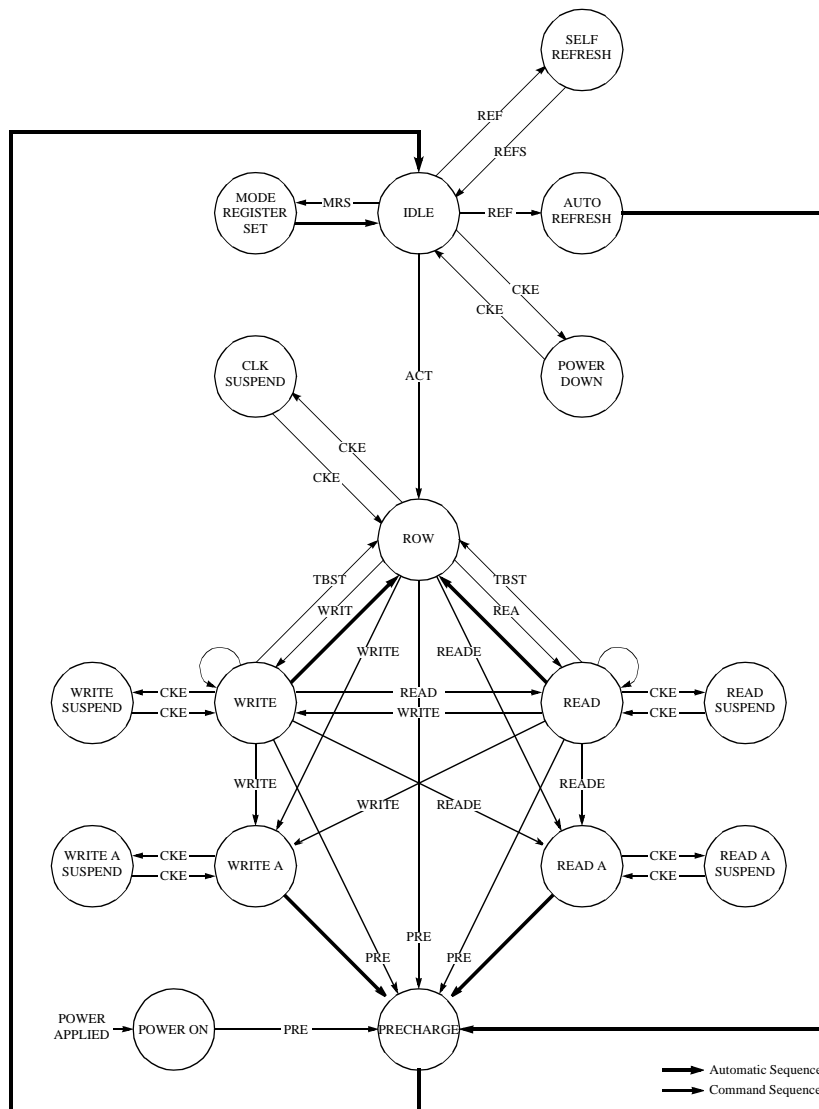
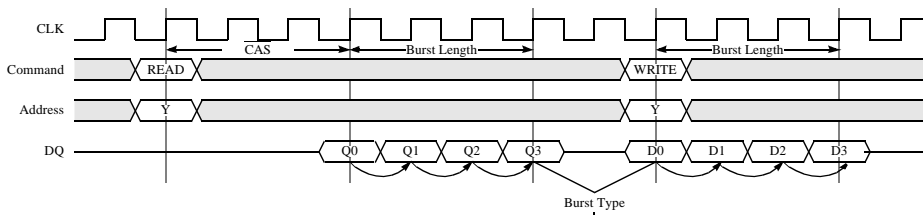
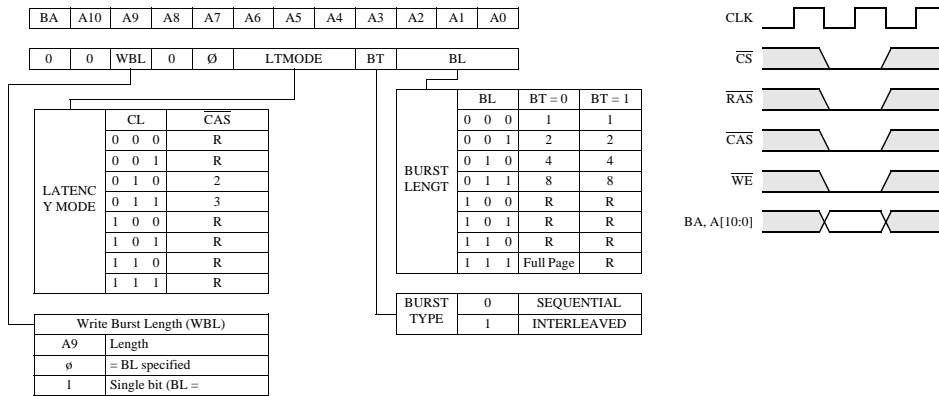


Figure 2. Simplified State Diagram

### Mode Register

Burst Length, Burst Type and CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in idle state. After  $t_{RSC}$  from a MRS command, the SDRAM is ready for new command.



Initial Address			B L	Column Addressing															
A2	A1	A0		Sequential							Interleaved								
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0	
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

## OPERATIONAL DESCRIPTION

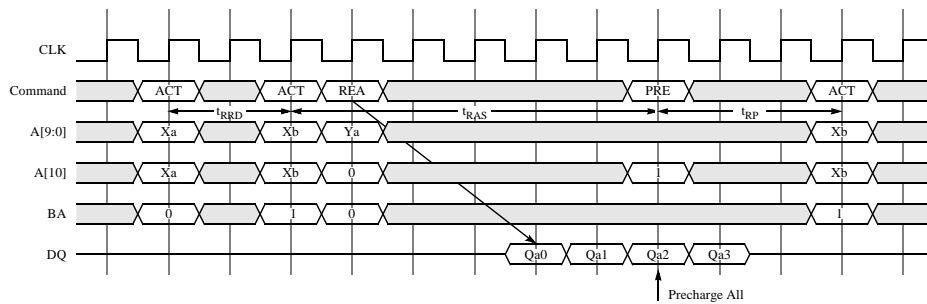
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### Bank Activate

The SDRAM has two independent banks. Each bank is activated by the ACT command with the bank address (BA). A row is indicated by the row address A[10:0]. The minimum activation interval between one bank and the other bank is  $t_{RRD}$ .

### Precharge

The PRE command deactivates the bank indicated by BA. When both banks are active, the precharge all command (PREA, PRE + A[10] = H) is available to deactivate them at the same time. After  $t_{RP}$  from the precharge, an ACT command can be issued.

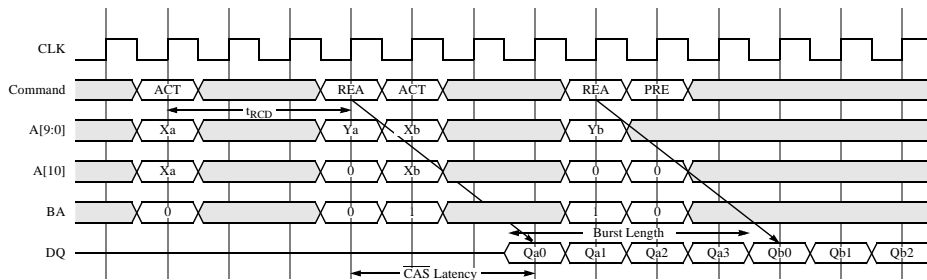


**Figure 3. Bank Activation and Precharge All (BL=4, CL=3)**

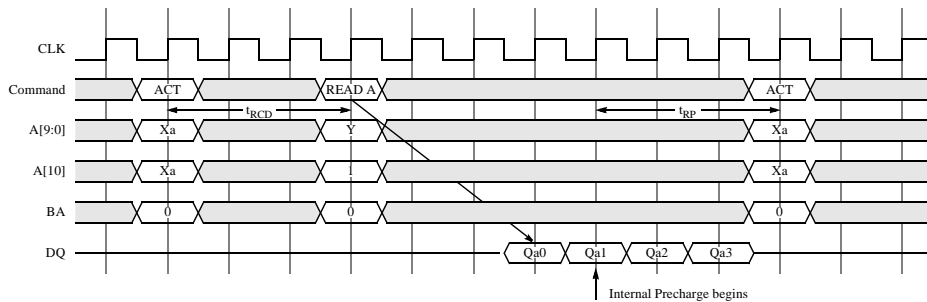
## Read

After  $t_{RCD}$  from the bank activation, a READ command can be issued. 1st output data is available after the CAS Latency from the READ, followed by (BL-1) consecutive data when the Burst Length is BL. The start address is specified by A[7:0], and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time

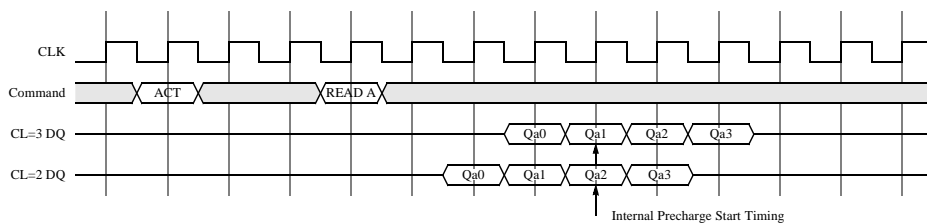
( $t_{RP}$ ) can be hidden behind continuous output data (in case of BL = 4) by interleaving the dual banks. When A[10] is high at a READ command, the auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge start timing depends on CAS Latency. The next ACT command can be issued after  $t_{RP}$  from the internal precharge timing.



**Figure 4. Dual Bank Interleaving READ (BL=4, CL=3)**



**Figure 5. READ with Auto-Precharge (BL=4, CL=3)**

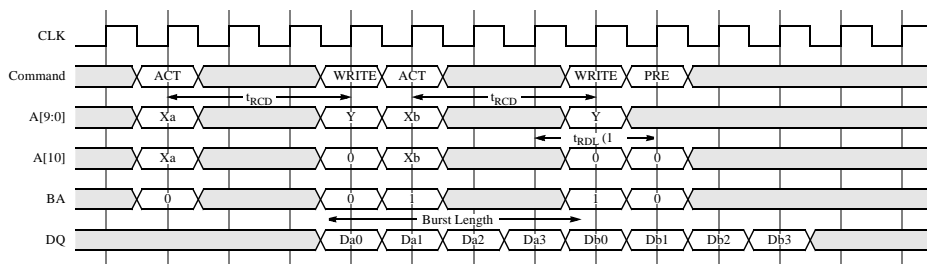


**Figure 6. READ Auto-Precharge Timing (BL=4)**

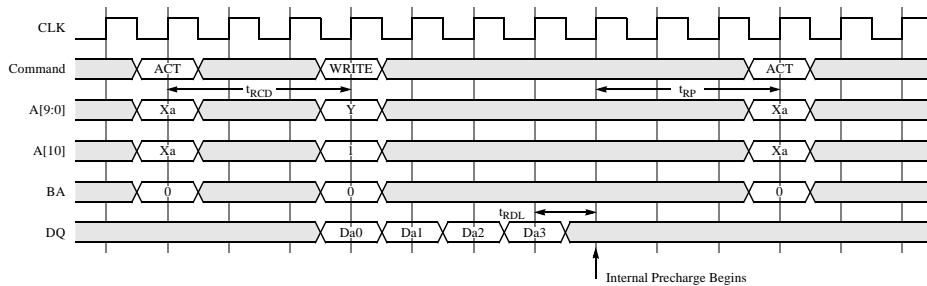
### Write

After  $t_{RCD}$  from the bank activation, a WRITE command can be issued. 1st input data is set at the same cycle as the WRITE. Following (BL-1) data are written into the RAM, when the Burst Length is BL. The start address is specified by A[7:0], and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time ( $t_{RP}$ ) can be hidden behind continuous input data (in case of BL = 4)

by interleaving the dual banks. From the last input data to the PRE command, the write recovery time ( $t_{RDL}$ ) is required. When A[10] is high at a WRITE command, the auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge begins at  $t_{WR}$  after the last input data cycle. The next ACT command can be issued after  $t_{RP}$  from the internal precharge timing.



**Figure 7. Dual Bank Interleaving WRITE (BL=4)**



**Figure 8. WRITE with Auto-Precharge (BL=4)**

## Burst Interruption

### [Read Interrupted by Read]

The burst read operation can be interrupted by a new read of the same or the other bank. GLT5160L16 allows random column access. READ to READ interval is 1 CLK minimum.

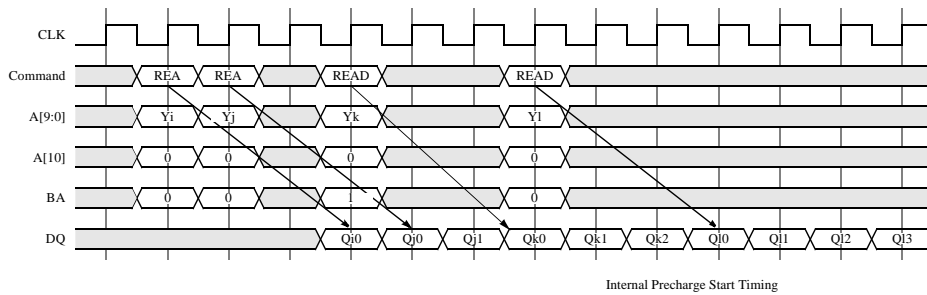


Figure 9. READ Interrupted by READ (BL=4, CL=3)

### [Read Interrupted by Write]

Burst read operation can be interrupted by write of the same or the other bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQMU / DQML to prevent the bus contention. The output is disabled automatically 2 cycles after WRITE assertion.

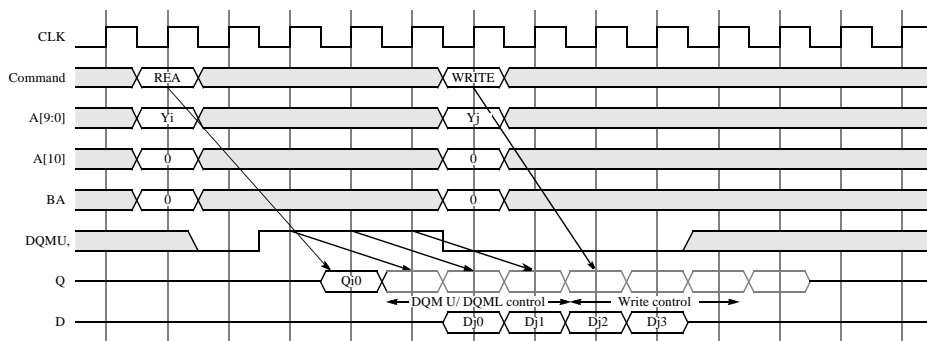
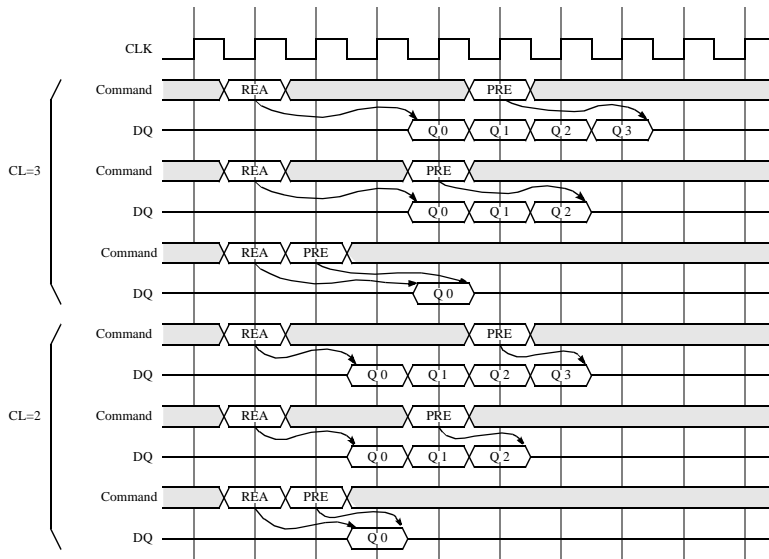


Figure 10. READ Interrupted by WRITE (BL=4, CL=3)

*[Read Interrupted by Precharge]*

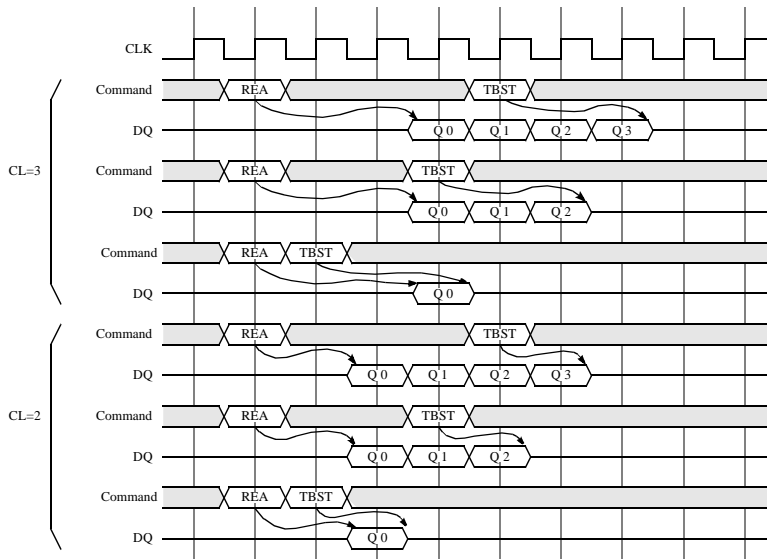
Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is minimum 1 CLK. A PRE command disables the data output, depending on the CAS Latency. The figure below shows examples, when the data-out is terminated.



**Figure 11. READ Interrupted by Precharge (BL=4)**

**[Read Interrupted by Burst Terminate]**

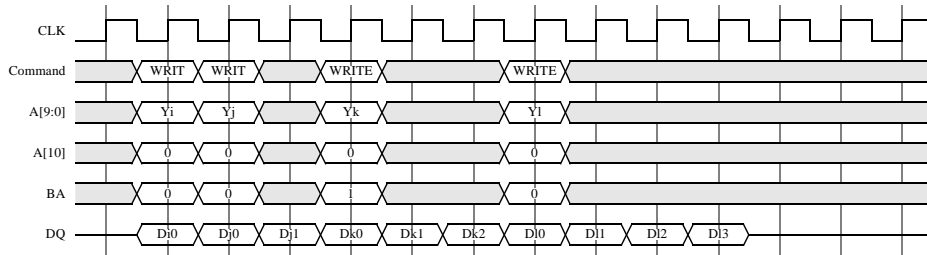
Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. READ to TBST interval is minimum 1 CLK. The figure below shows examples, when the data-out is terminated.



**Figure 12. READ Interrupted by Burst Terminate (BL=4)**

**[Write Interrupted by Write]**

Burst write operation can be interrupted by new write of the same or the other bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

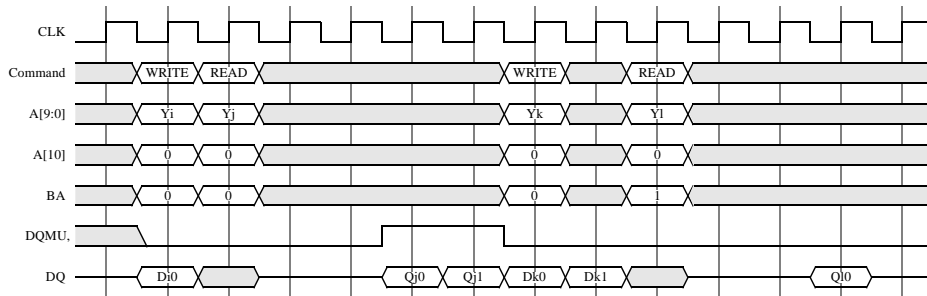


**Figure 13. WRITE Interrupted by WRITE (BL=4)**

**[Write Interrupted by Read]**

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ

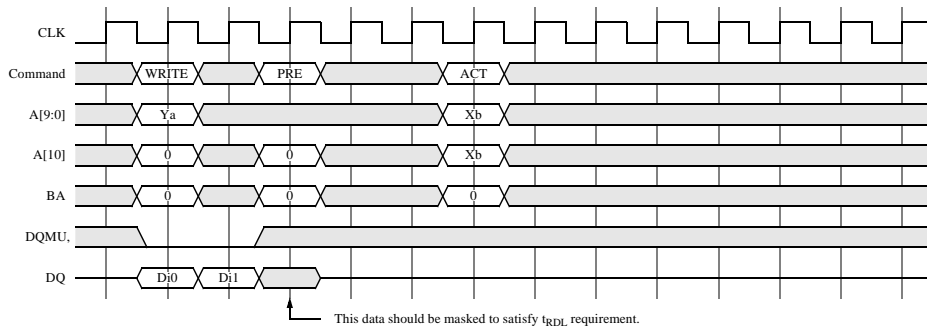
interval is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care". Using the DQMU / DQML to prevent the bus contention is optional.



**Figure 14. WRITE interrupted by READ (BL=4, CL=3)**

**[Write Interrupted by Precharge]**

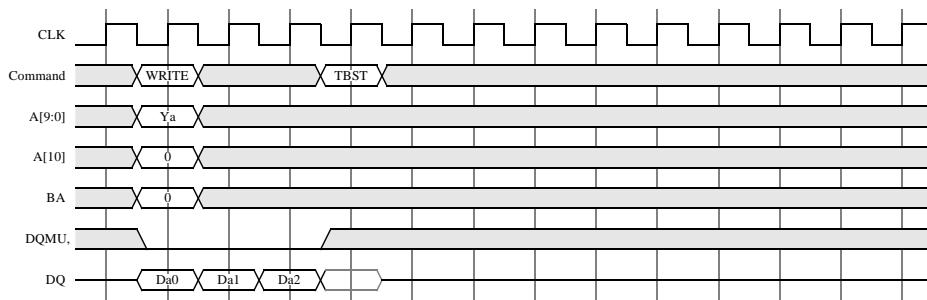
Burst write operation can be interrupted by precharge of the same bank. Random column access is allowed. Because the write recovery time ( $t_{RD_L}$ ) is required between the last input data and the next PRE, 3rd data should be masked with DQMU / DQML shown as below.



**Figure 15. WRITE Interrupted by Precharge (BL=4)**

**[Write Interrupted by Burst Terminate]**

Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. The figure below shows the case 3 words of data are written. Random column access is allowed. WRITE to TBST interval is minimum 1 CLK.



**Figure 16. WRITE Interrupted by Burst Terminate (BL=4)**

### Auto Refresh

Single cycle of auto-refresh is initiated with a REFA ( $\overline{CS} = \overline{RAS} = \overline{CAS} = L$ ,  $\overline{WE} = \text{CKE} = H$ ) command. The refresh address is generated internally. 4096 REFA cycles within 64 ms refresh 16 Mbit

memory cells. The auto-refresh is performed on each bank alternately (ping-pong refresh). Before performing an auto-refresh, both banks must be in the idle state. Additional commands must not be supplied to the device before  $t_{RC}$  from the REFA command.

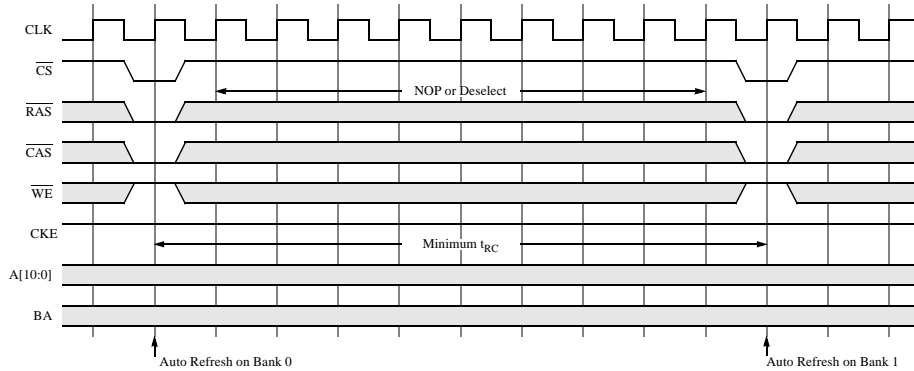


Figure 17. Auto Refresh

### Self Refresh

Self-refresh mode is entered by issuing a REFS command ( $\overline{CS} = \overline{RAS} = \overline{CAS} = L$ ,  $\overline{WE} = H$ ,  $\text{CKE} = L$ ). Once the self-refresh is initiated, it is maintained as long as  $\text{CKE}$  is kept low. During the self-refresh mode,  $\text{CKE}$  is asynchronous and the only enabled input (but asynchronous), all other inputs including  $\text{CLK}$  are disabled and ignored, and power consumption due to synchronous inputs is

saved. To exit the self-refresh, supplying stable  $\text{CLK}$  inputs, asserting  $\text{DESEL}$  or  $\text{NOP}$  command and then asserting  $\text{CKE}$  ( $\text{REFSX}$ ). After  $t_{RC}$  from  $\text{REFSX}$  both banks are in the idle state and a new command can be issued after  $t_{RC}$ , but  $\text{DESEL}$  or  $\text{NOP}$  commands must be asserted till then.

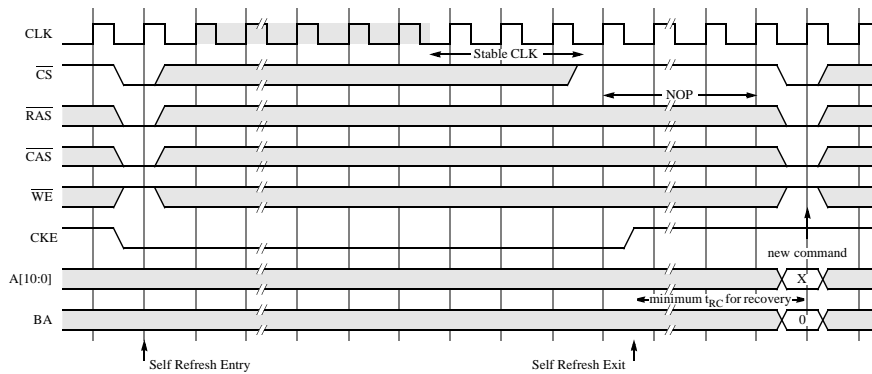
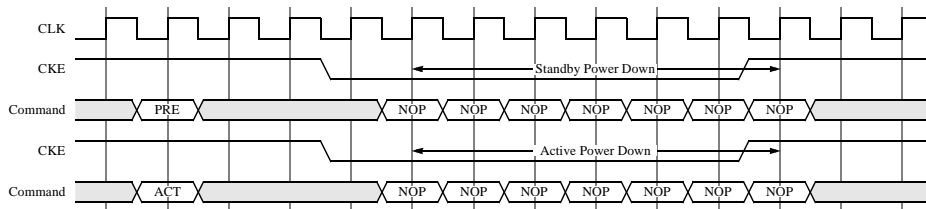
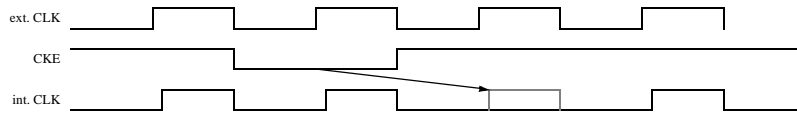


Figure 18. Self-Refresh

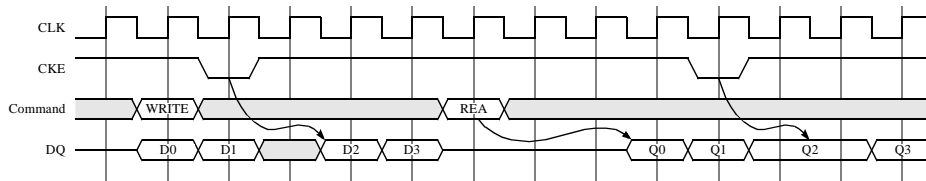
### CLK Suspend

CKE controls the internal CLK at the following cycle. Figure 19 and Figure 20 show how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power

down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle, but a command at the following cycle is ignored.



**Figure 19. Power Down by CKE**

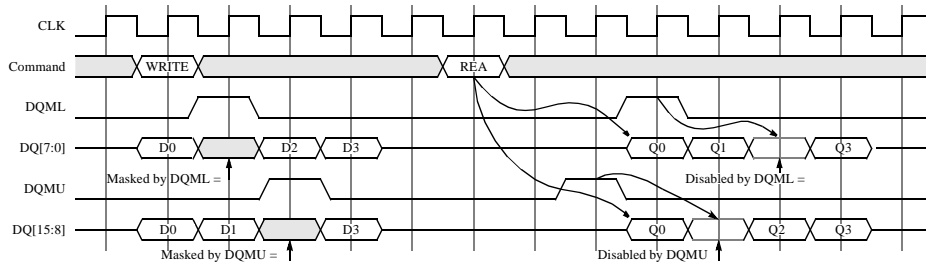


**Figure 20. DQ Suspend by CKE**

### DQMU / DQML Control

DQMU / DQML is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQMU / DQML masks upper / lower input data word by word. DQMU / DQML masks upper / lower input data word by word. DQMU /

DQML to write mask latency is 0. During reads, DQMU / DQML forces upper / lower output to Hi-Z word by word. DQMU / DQML to output Hi-Z latency is 2.



**Figure 21. DQMU / DQML Function**

## ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings <sup>[1]</sup>

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>DD</sub>	Supply Voltage	with respect to V <sub>SS</sub>	-1.0 to 4.6	V
V <sub>DDQ</sub>	Supply Voltage for Output	with respect to V <sub>SSQ</sub>	-1.0 to 4.6	V
V <sub>I</sub>	Input Voltage	with respect to V <sub>SS</sub>	-1.0 to 4.6	V
V <sub>O</sub>	Output Voltage	with respect to V <sub>SSQ</sub>	-1.0 to 4.6	V
I <sub>O</sub>	Output Current		50	mA
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> = 25 °C	1000	mW
T <sub>OPR</sub>	Operating Temperature	consumer	0 to 70	°C
		Industrial	-40 to 85	°C
T <sub>STG</sub>	Storage Temperature		-65 to 150	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended Operating Conditions (T<sub>A</sub> = 0 to +70°C, unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply Voltage	3.0	3.3	3.6	V
V <sub>DDQ</sub>	Supply Voltage for Output	3.0	3.3	3.6	V
V <sub>IH</sub> <sup>[1]</sup>	High-Level Input Voltage all inputs	2.0		V <sub>DDQ</sub> +0.3	V
V <sub>IL</sub> <sup>[2]</sup>	Low-Level Input Voltage all inputs	-0.3		0.8	V

- V<sub>IH</sub> (max) = 5.6 V for pulse width less than 3 ns.
- V<sub>IL</sub> (min) = -2.0 V for pulse width less than 3 ns.

### DC Characteristics (T<sub>A</sub> = 0 to +70°C, V<sub>DD</sub> = V<sub>DDQ</sub> = 3.3 ±0.3V, V<sub>SS</sub> = V<sub>SSQ</sub> = 0 V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -2 mA	2.4		V
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 2 mA		0.4	V
I <sub>OZ</sub>	Off-state Output Current	Q floating V <sub>O</sub> = 0 to V <sub>DDQ</sub>	-10	10	μA
I <sub>I</sub>	Input Current	V <sub>IH</sub> = 0 to V <sub>DDQ</sub> + 0.3 V	-10	10	μA

### Capacitance (T<sub>A</sub> = 0 to +70°C, V<sub>DD</sub> = V<sub>DDQ</sub> = 3.3 ±0.3 V, V<sub>SS</sub> = V<sub>SSQ</sub> = 0 V, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Unit
C <sub>I(A)</sub>	Input Capacitance, address pin	V <sub>I</sub> = V <sub>SS</sub> f = 1 MHz V <sub>I</sub> = 25 mVrms	2.5	5	pF
C <sub>I(C)</sub>	Input Capacitance, control pin		2.5	5	pF
C <sub>I(K)</sub>	Input Capacitance, CLK pin		2.5	5	pF
C <sub>I/O</sub>	Input Capacitance, I/O pin		4	7	pF

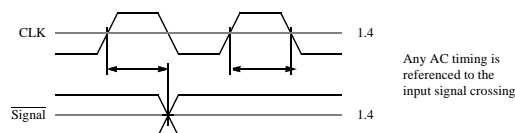
**Average Supply Current from V<sub>DD</sub>**
**(T<sub>A</sub> = 0 to +70°C, V<sub>DD</sub> = V<sub>DDQ</sub> = 3.3 ±0.3 V, V<sub>SS</sub> = V<sub>SSQ</sub> = 0 V, unless otherwise noted)**

Symbol	Parameter	Test Conditions	Rating (Max)				Unit
			-6	-7	-8	-10	
I <sub>CC1S</sub>	Operating Current, Single Bank	t <sub>RC</sub> = min, t <sub>CLK</sub> = min, BL = 1, CL = 3	120	110	100	90	mA
I <sub>CC1D</sub>	Operating Current, Dual Bank	t <sub>RC</sub> = min, t <sub>CLK</sub> = min, BL = 1, CL = 3	170	150	140	120	mA
I <sub>CC2H</sub>	Standby Current, CKE = H	both banks idle, t <sub>CLK</sub> = min, CKE = H	20	20	20	20	mA
I <sub>CC2L</sub>	Standby Current, CKE = L	both banks idle, t <sub>CLK</sub> = min, CKE = L	2	2	2	2	mA
I <sub>CC3H</sub>	Active Standby Current, CKE = H	both banks active, t <sub>CLK</sub> = min, CKE = H	35	35	35	35	mA
I <sub>CC3L</sub>	Active Standby Current, CKE = L	both banks active, t <sub>CLK</sub> = min, CKE = L	4	4	4	4	mA
I <sub>CC4</sub>	Burst Current	t <sub>CLK</sub> = min, BL = 4, CL = 3, both banks active	180	170	160	140	mA
I <sub>CC5</sub>	Auto-Refresh Current	t <sub>RC</sub> = min, t <sub>CLK</sub> = min	110	100	90	80	mA
I <sub>CC6</sub>	Self-Refresh Current	CKE < 0.2 V	1	1	1	1	mA
		Low Power	500	500	500	500	µA

**AC Characteristics (T<sub>A</sub> = 0 to +70°C, V<sub>DD</sub> = V<sub>DDQ</sub> = 3.3 ±0.3 V, V<sub>SS</sub> = V<sub>SSQ</sub> = 0 V, unless otherwise noted) [1]**

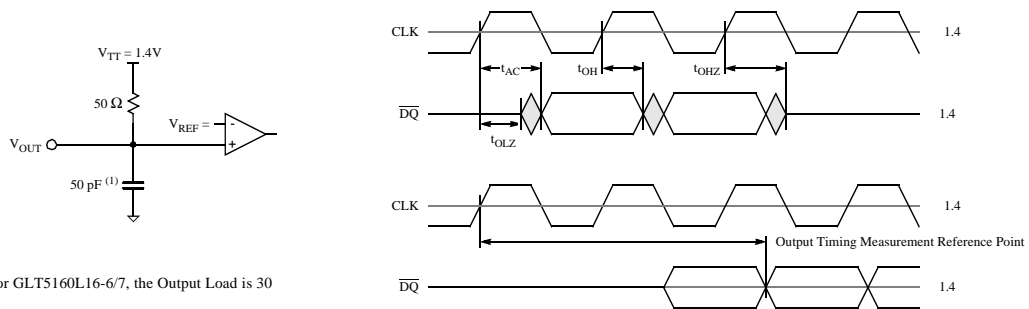
Symbol	Parameter	-6		-7		-8		-10		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>CLK</sub>	CLK Cycle Time	CL=2	-		9		10		13	ns
		CL=3	6		7		8		10	ns
t <sub>CH</sub>	CLK High Pulse Width	2.5		3		3		3.5		ns
t <sub>CL</sub>	CLK Low Pulse Width	2.5		3		3		3.5		ns
t <sub>T</sub>	Transition Time of CLK	1	10	1	10	1	10	1	10	ns
t <sub>IS</sub>	Input Setup Time (all inputs)	2		2.5		2.5		2.5		ns
t <sub>IH</sub>	Input Hold Time (all inputs)	1		1		1		1		ns
t <sub>RC</sub>	Row Cycle Time	60		63		72		90		ns
t <sub>RCD</sub>	Row to Column Delay	18		21		24		30		ns
t <sub>RAS</sub>	Row Active Time	42	100k	42	100k	48	100k	60	100k	ns
t <sub>RP</sub>	Row Precharge Time	18		21		24		30		ns
t <sub>CCD</sub>	Column Address to Column Address Delay	1		1		1		1		CLK
t <sub>RRD</sub>	Act to Act Delay Time	2		2		2		2		CLK
t <sub>RSC</sub>	Mode Register Set Cycle Time	1		1		1		1		CLK
t <sub>RDL</sub>	Last Data-In to Row Precharge Delay	1		1		1		1		CLK
t <sub>REF</sub>	Refresh Interval Time		65.6		65.6		65.6		65.6	ms

1. Input Pulse Levels: 0.4 V to 2.4 V with t<sub>r</sub>/t<sub>f</sub> = +1/+1 ns. Input Timing Measurement Level: 1.4 V.



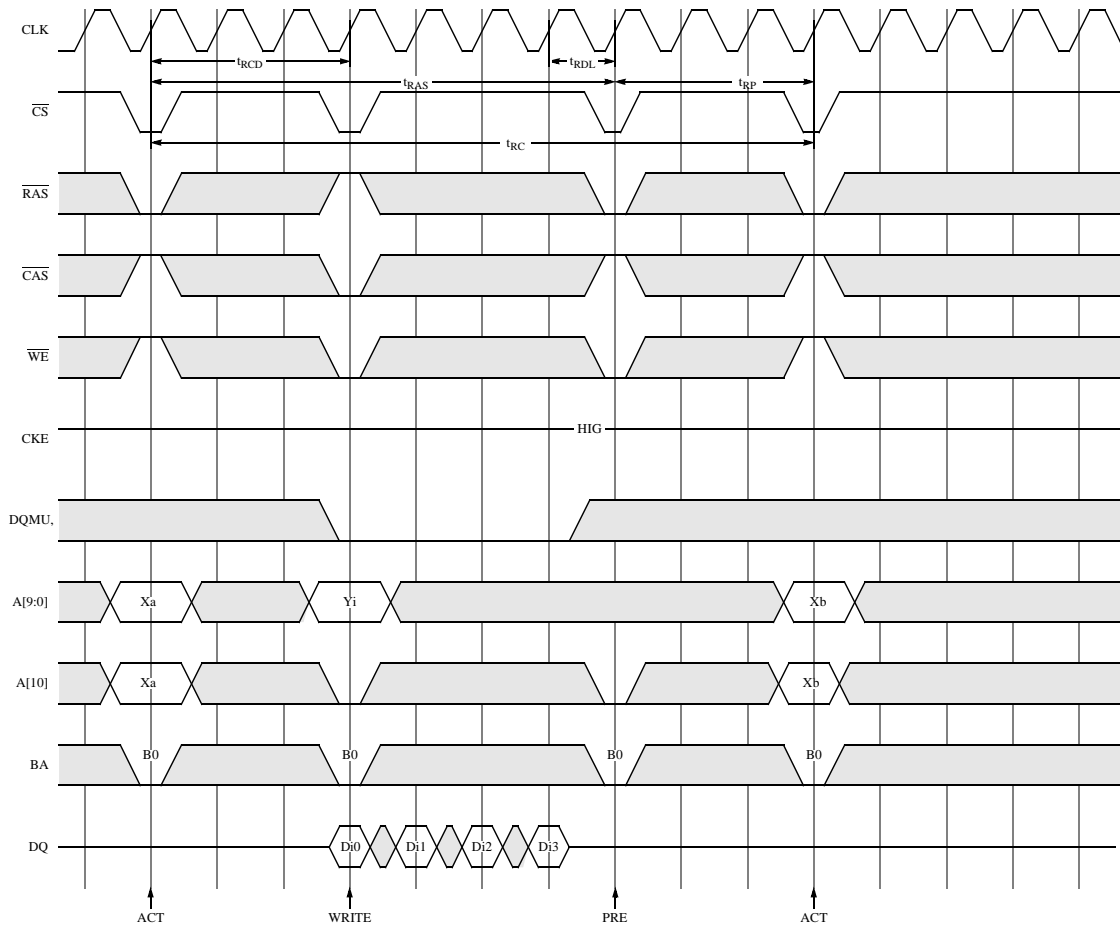
**Switching Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{DD} = V_{DDQ} = 3.3 \pm 0.3$  V,  $V_{SS} = V_{SSQ} = 0$  V unless otherwise noted)

Symbol	Parameter	-6		-7		-8		-10		Unit	
		Min	Max	Min	Max	Min	Max	Min	Max		
$t_{AC}$	Access Time from	CL=2		-		7		9		10	ns
		CL=3		5.5		6		6		7	ns
$t_{OH}$	Output Hold Time from CLK	2.5		2.5		3		3		ns	
$t_{OLZ}$	Delay Time, Output Low Impedance from CLK	1		1		1		1		ns	
$t_{OHZ}$	Delay Time, Output High Impedance from CLK	CL=2		-		7		7		9	ns
		CL=3		5.5		6		6		7	ns

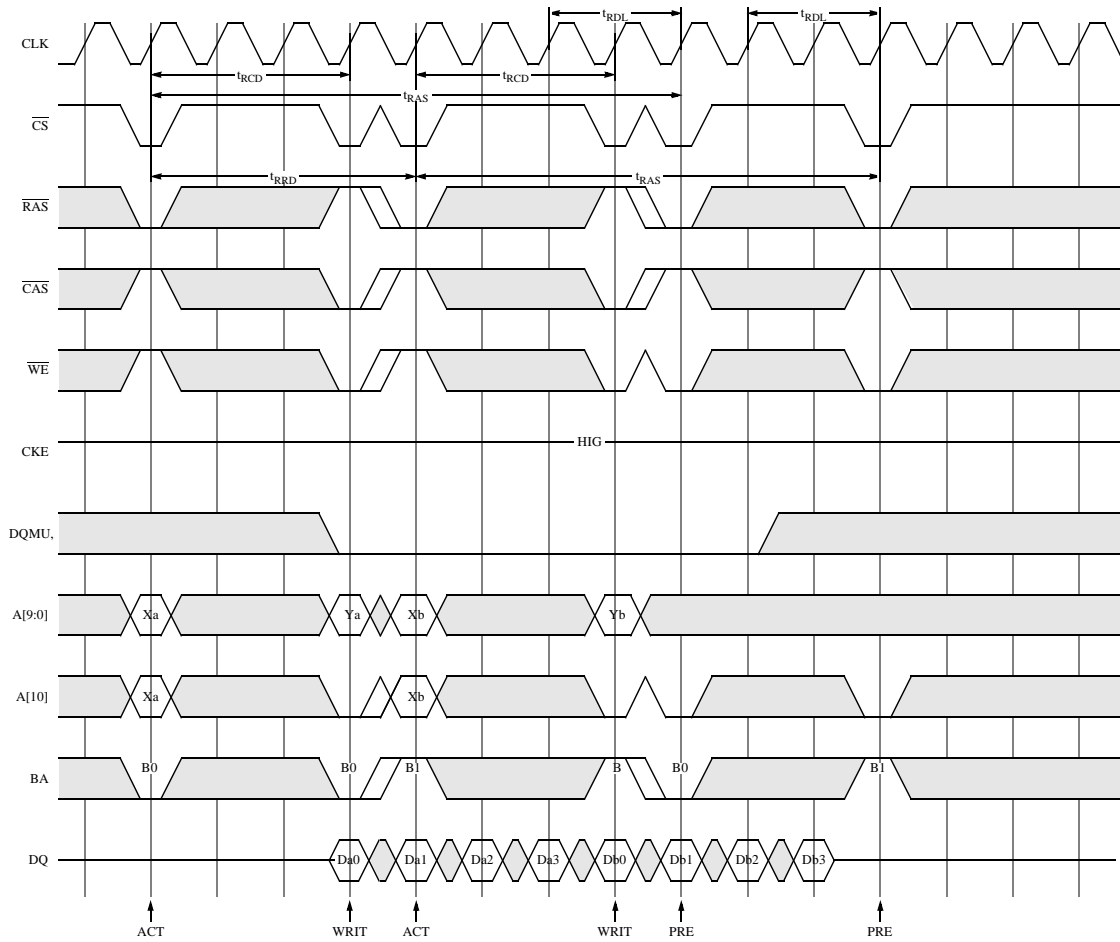


1. For GLT5160L16-6/7, the Output Load is 30

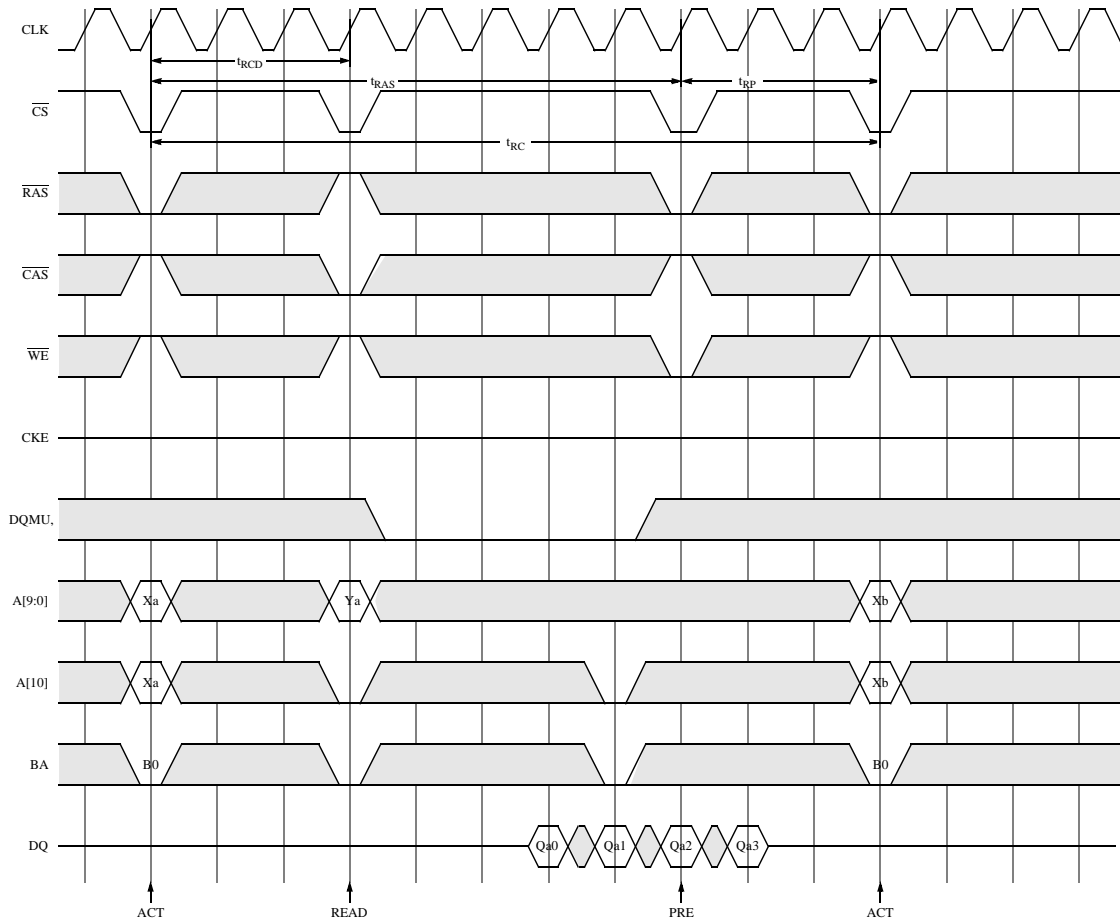
**Figure 22. Output Load Condition**



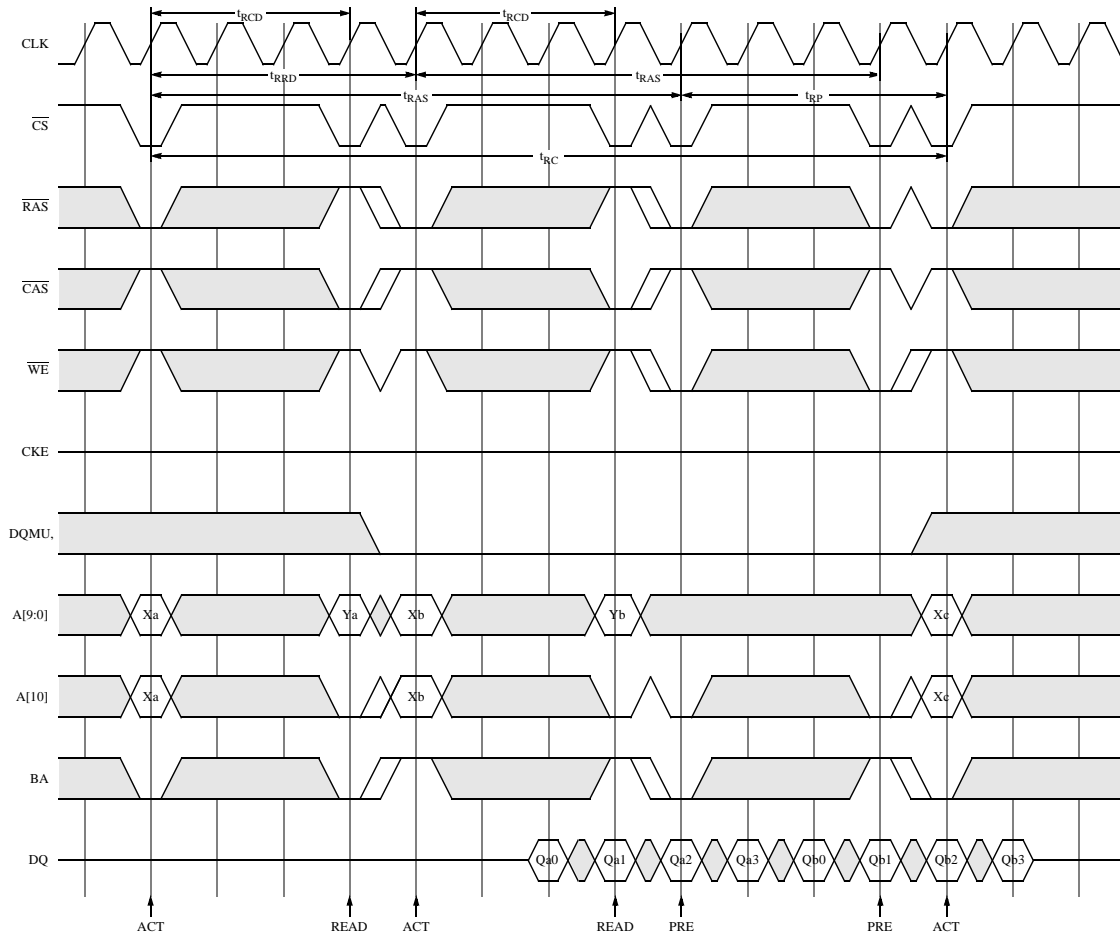
**Figure 23. WRITE Cycle (single bank) BL=4**



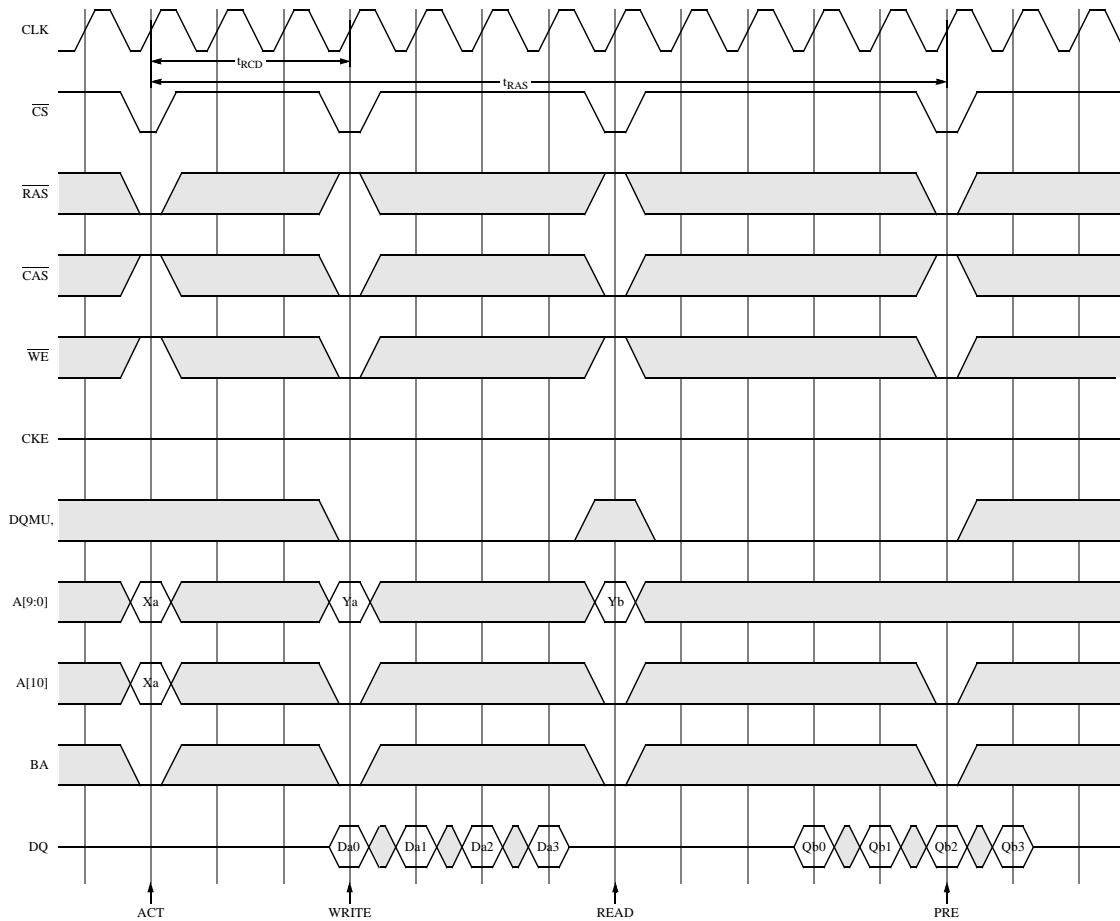
**Figure 24. WRITE Cycle (Dual Bank) BL=4**



**Figure 25. READ Cycle (Single Bank) BL=4, CL=3**

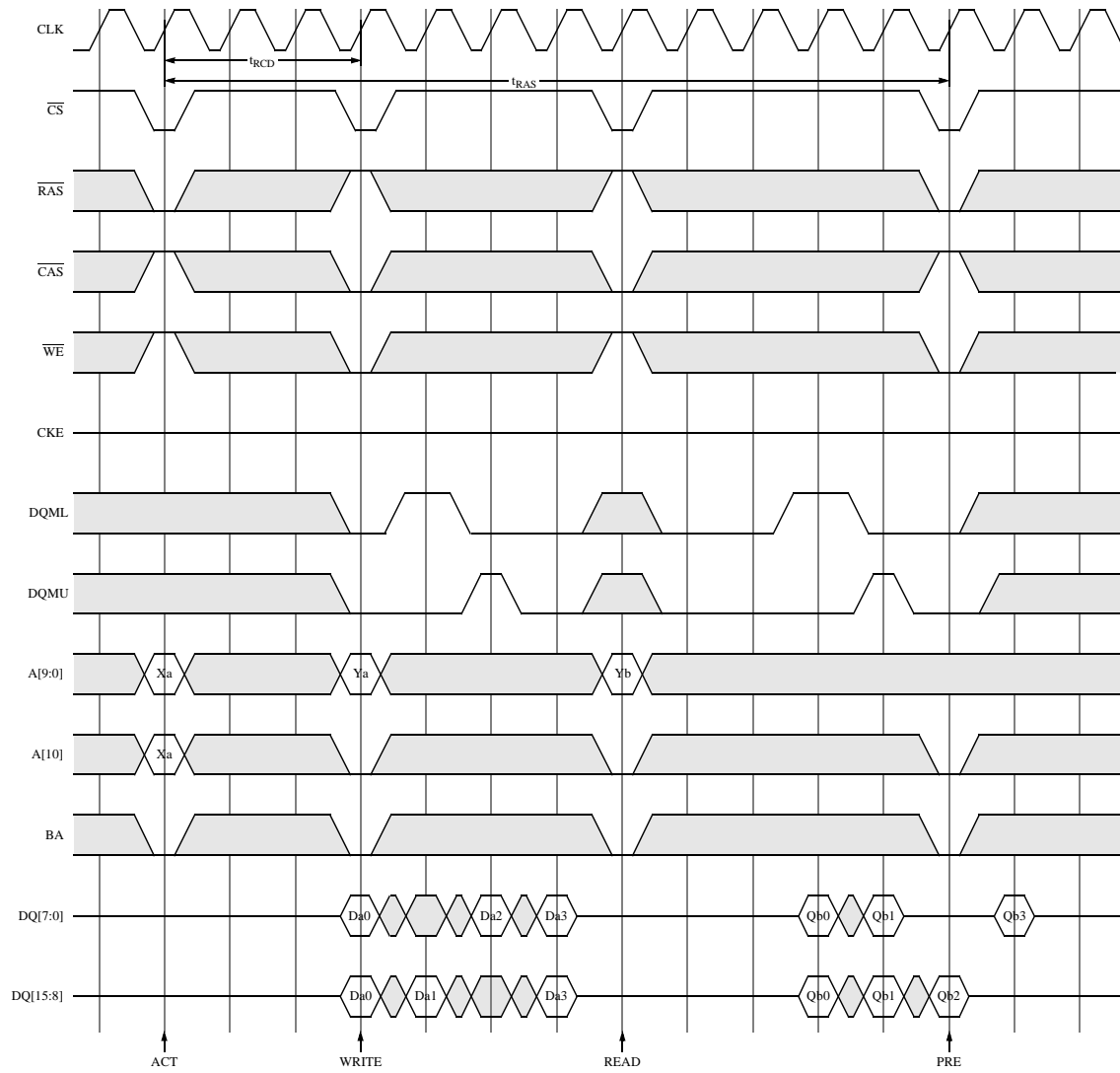


**Figure 26. READ Cycle (Dual Bank) BL=4, CL=3**

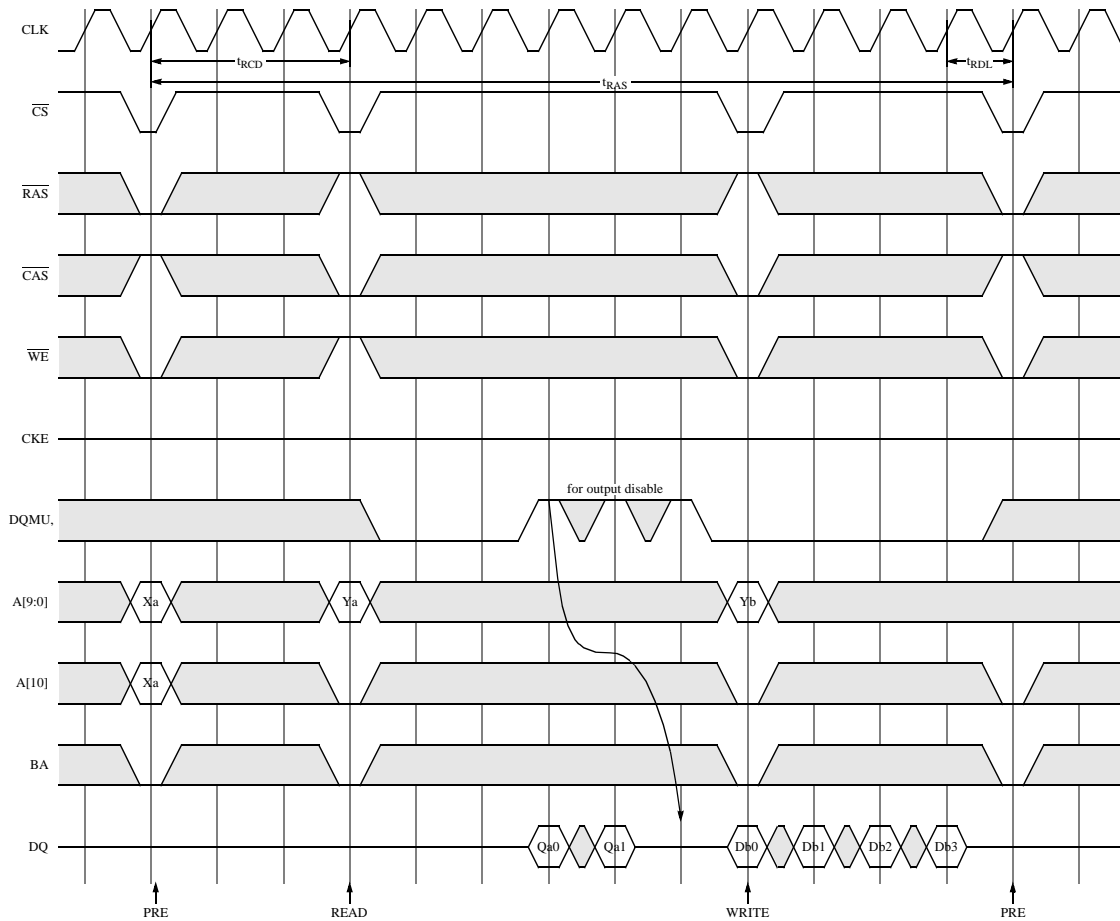


**Figure 27. WRITE to READ (Single Bank) BL=4, CL=3**



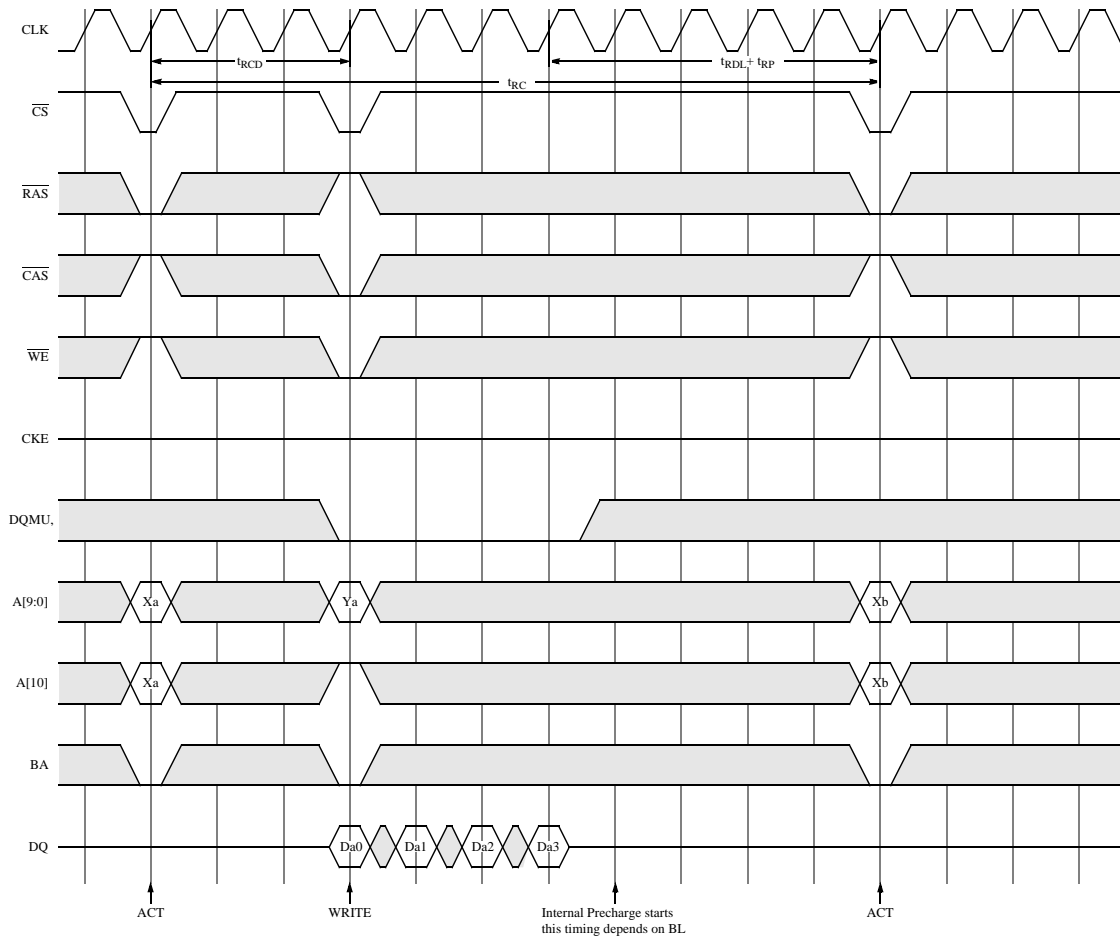


**Figure 29. DQM Byte Control for WRITE to READ (Single Bank) BL=4, CL=3**

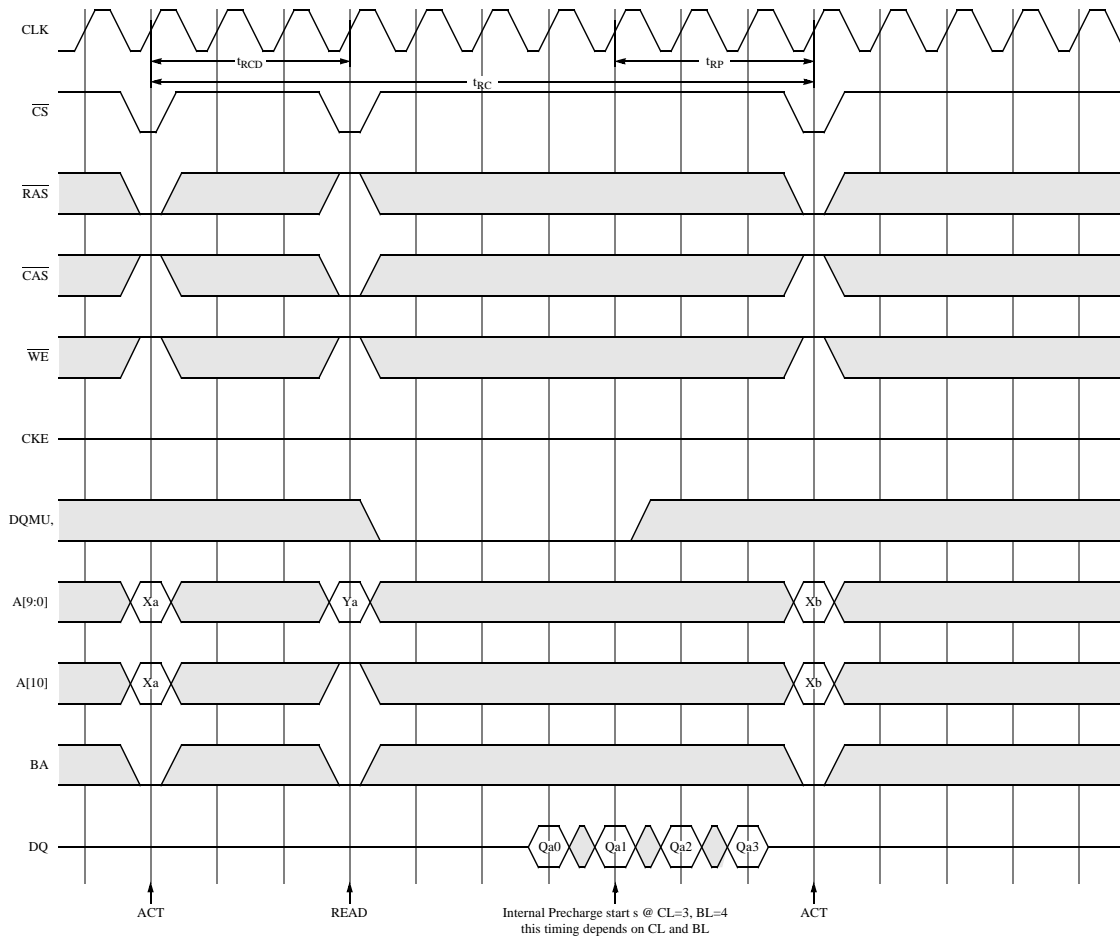


**Figure 30. READ to WRITE (Single Bank) BL=4, CL=3**

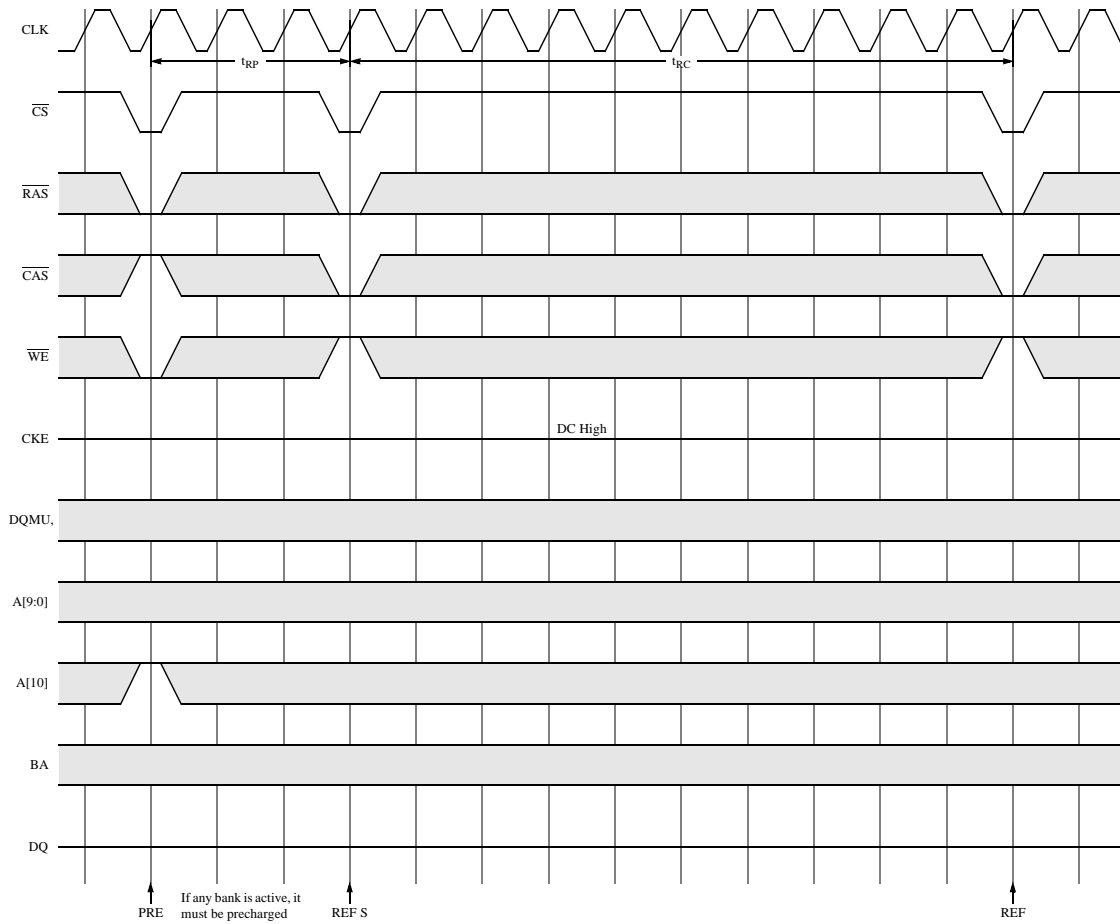




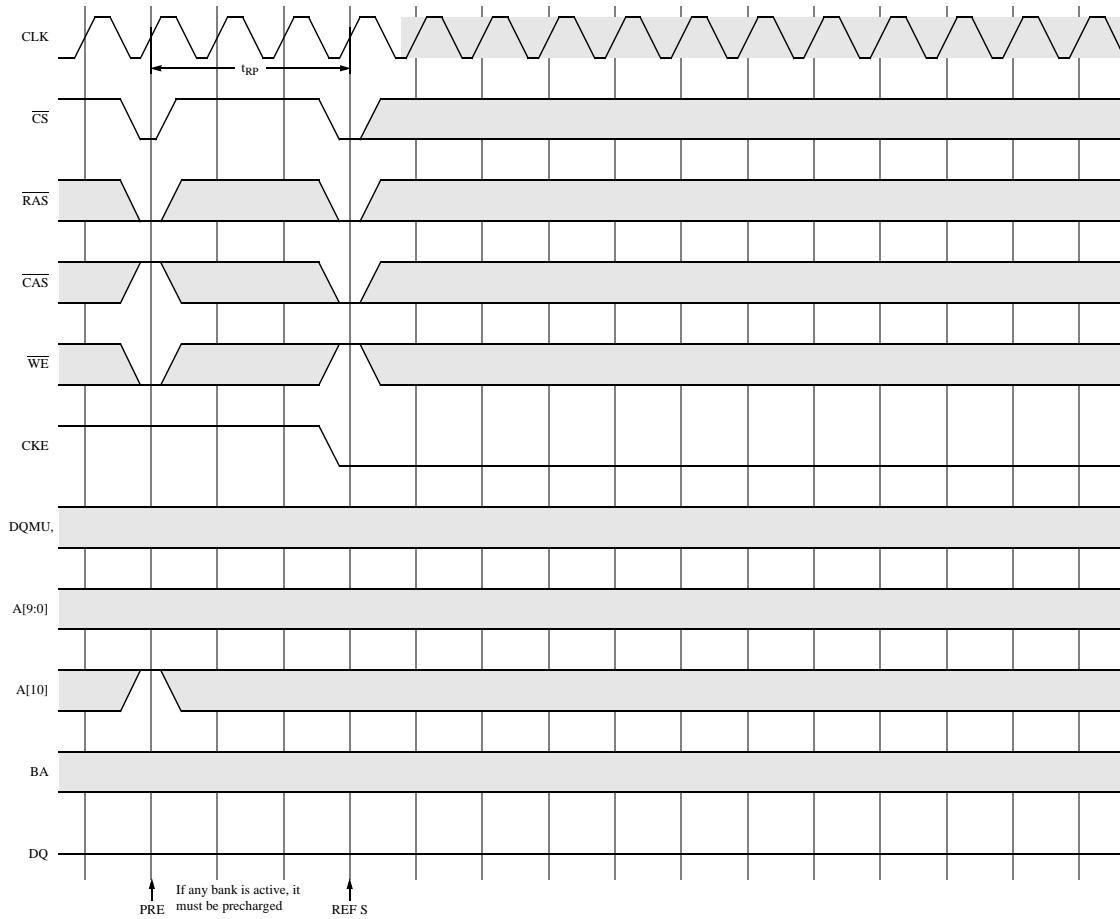
**Figure 32. Write with Auto-Precharge BL=4**



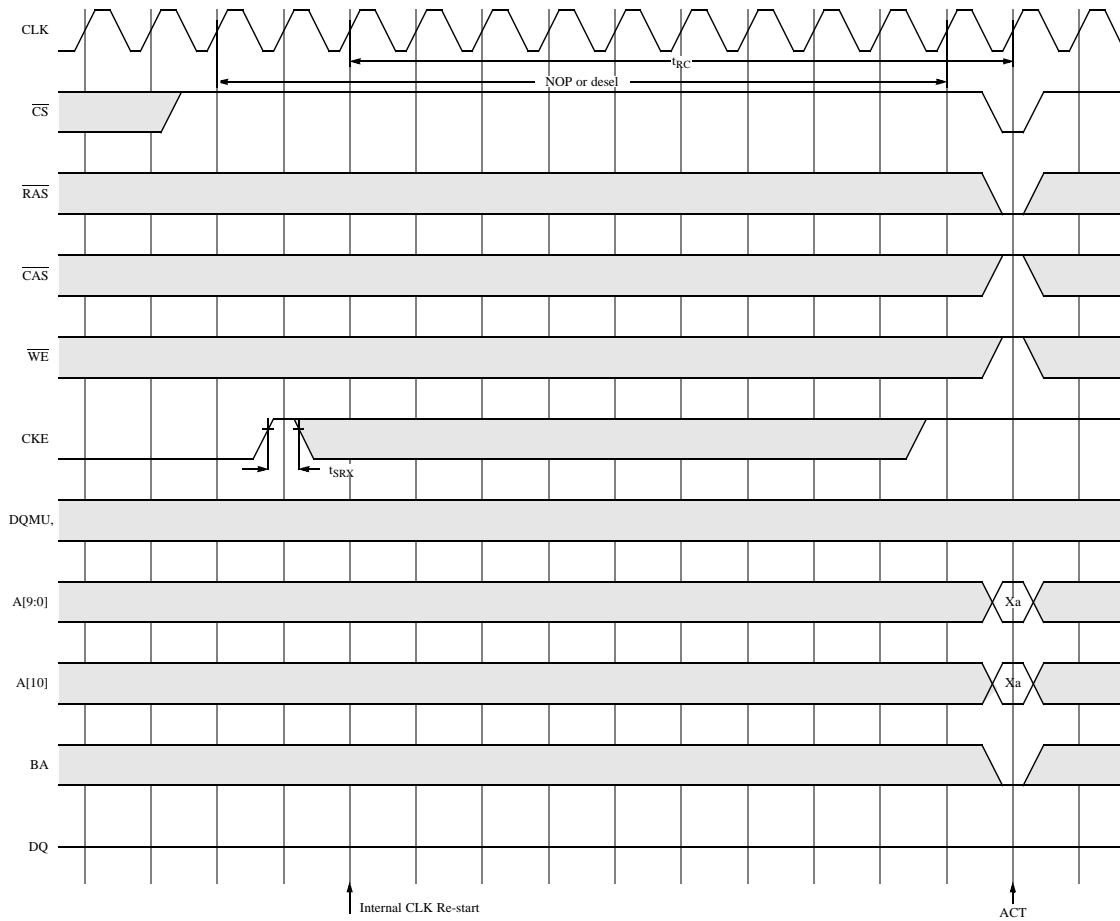
**Figure 33. Read with Auto-Precharge BL=4, CL=3**



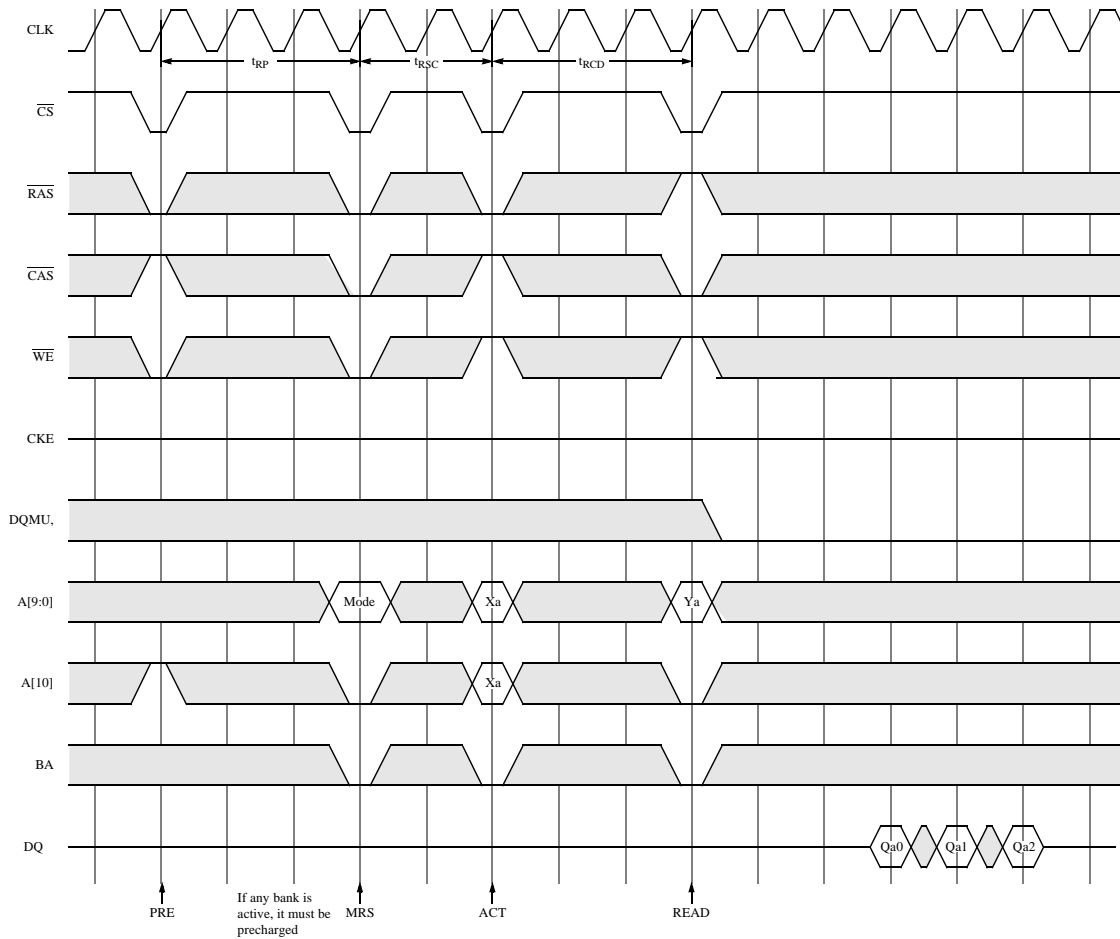
**Figure 34. Auto-Refresh**



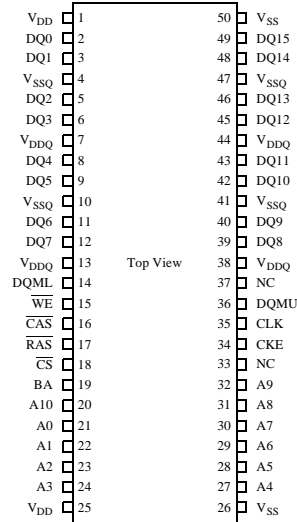
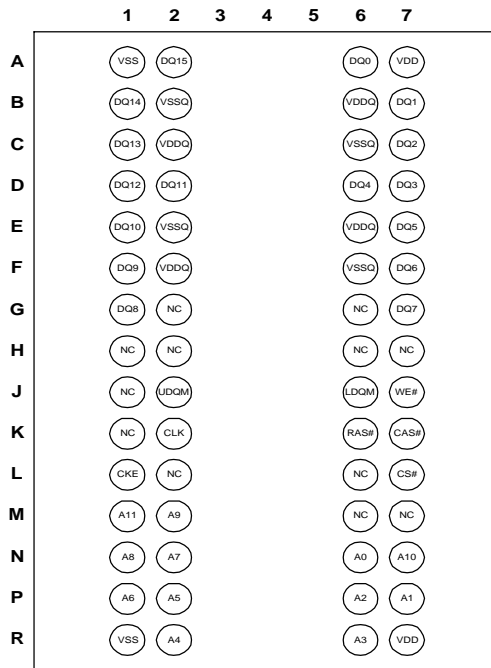
**Figure 35. Self-Refresh Entry**

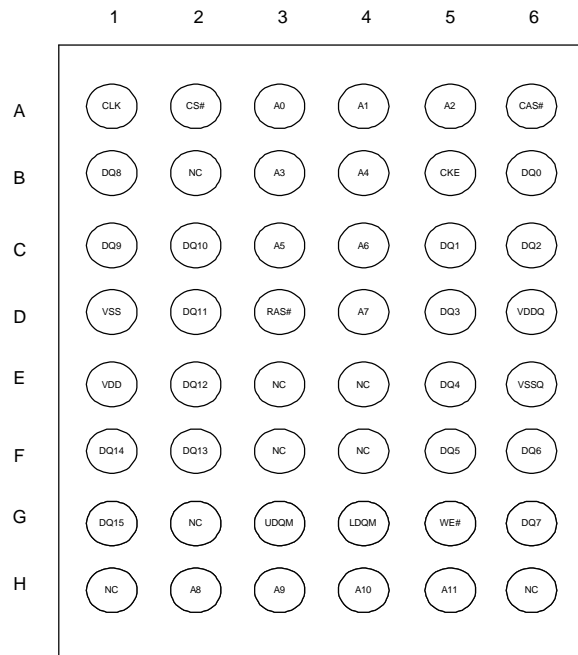


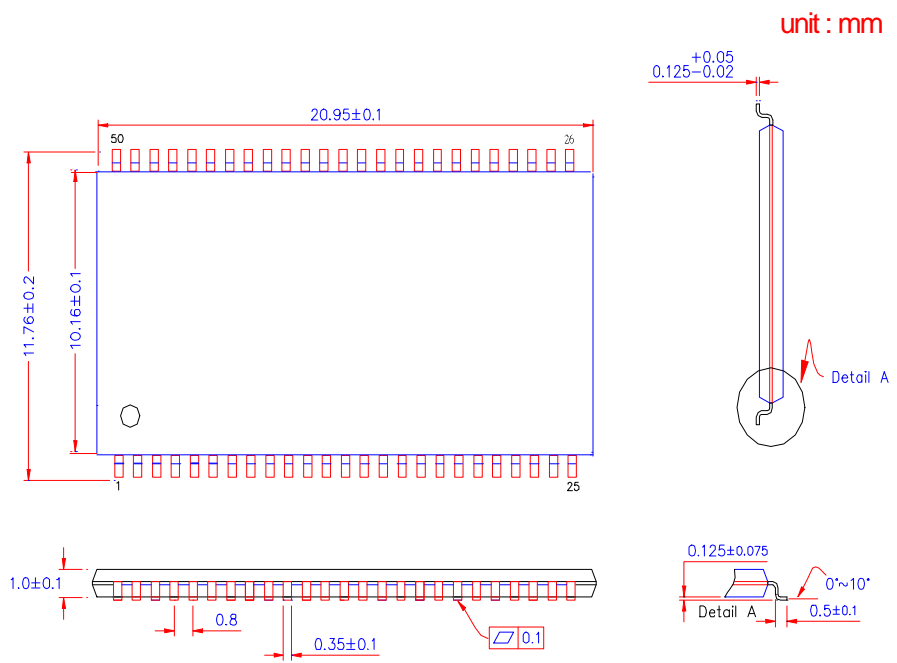
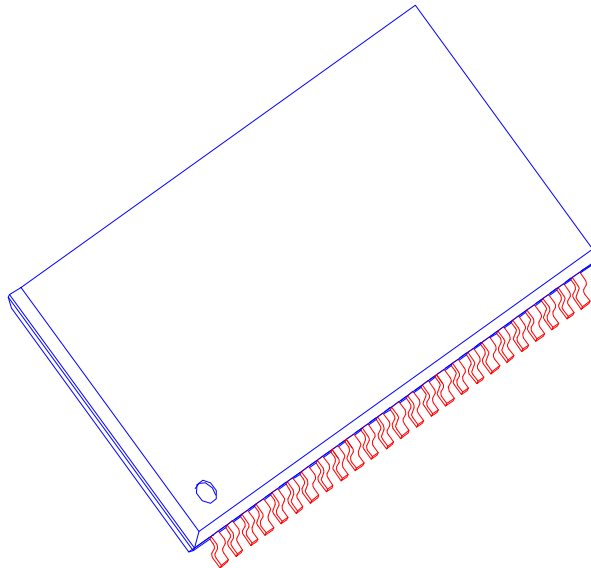
**Figure 36. Self-Refresh Exit**

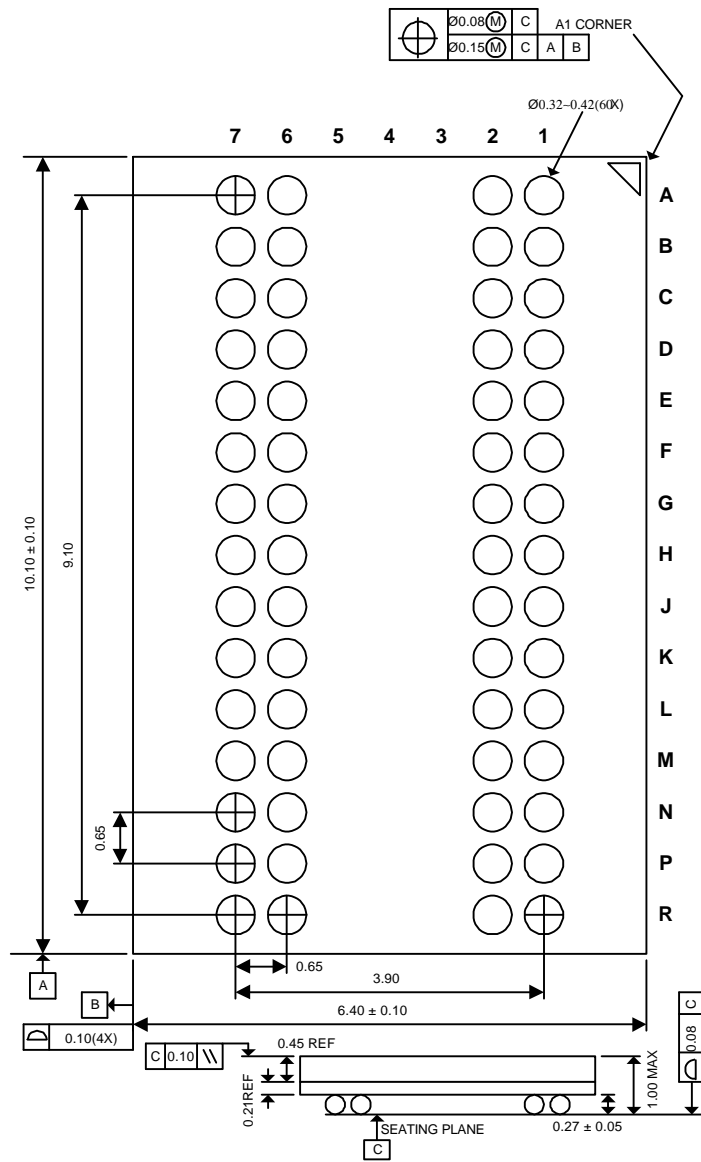


**Figure 37. Mode Register Set BL=4, CL=3**

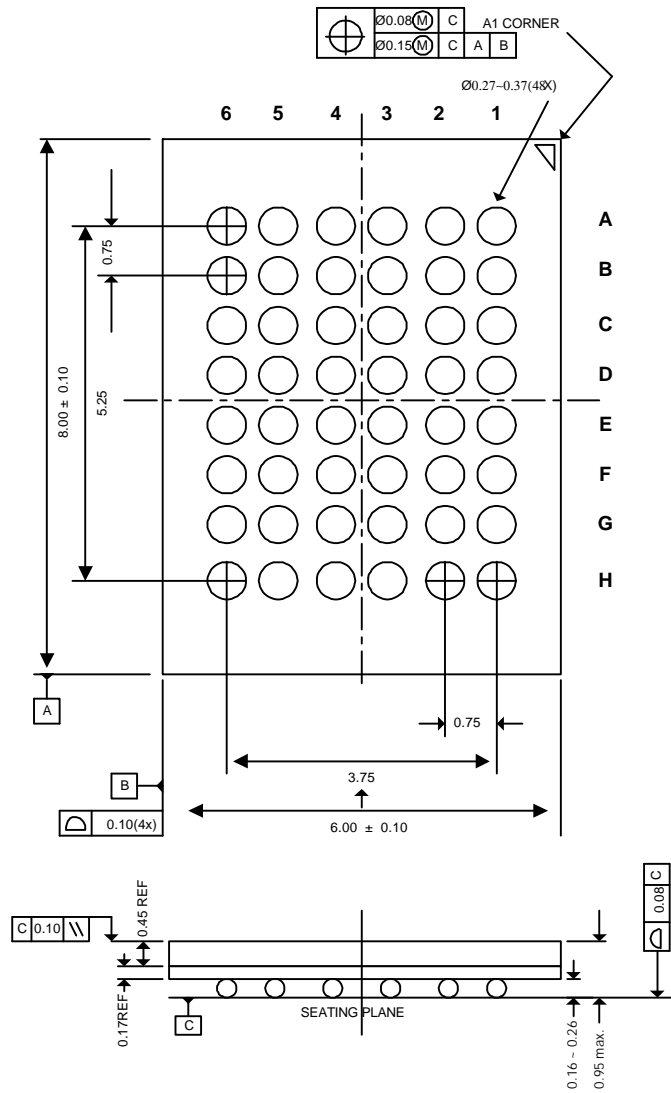
**PACKAGING INFORMATION**

**Figure 38. 50-Pin 400 mil TSOP II Pin Assignment**

**Figure 38-1. 60-Ball VFBGA Ball**

**PACKAGING INFORMATION**

**Figure 38-2. 48-Ball VFBGA Ball**





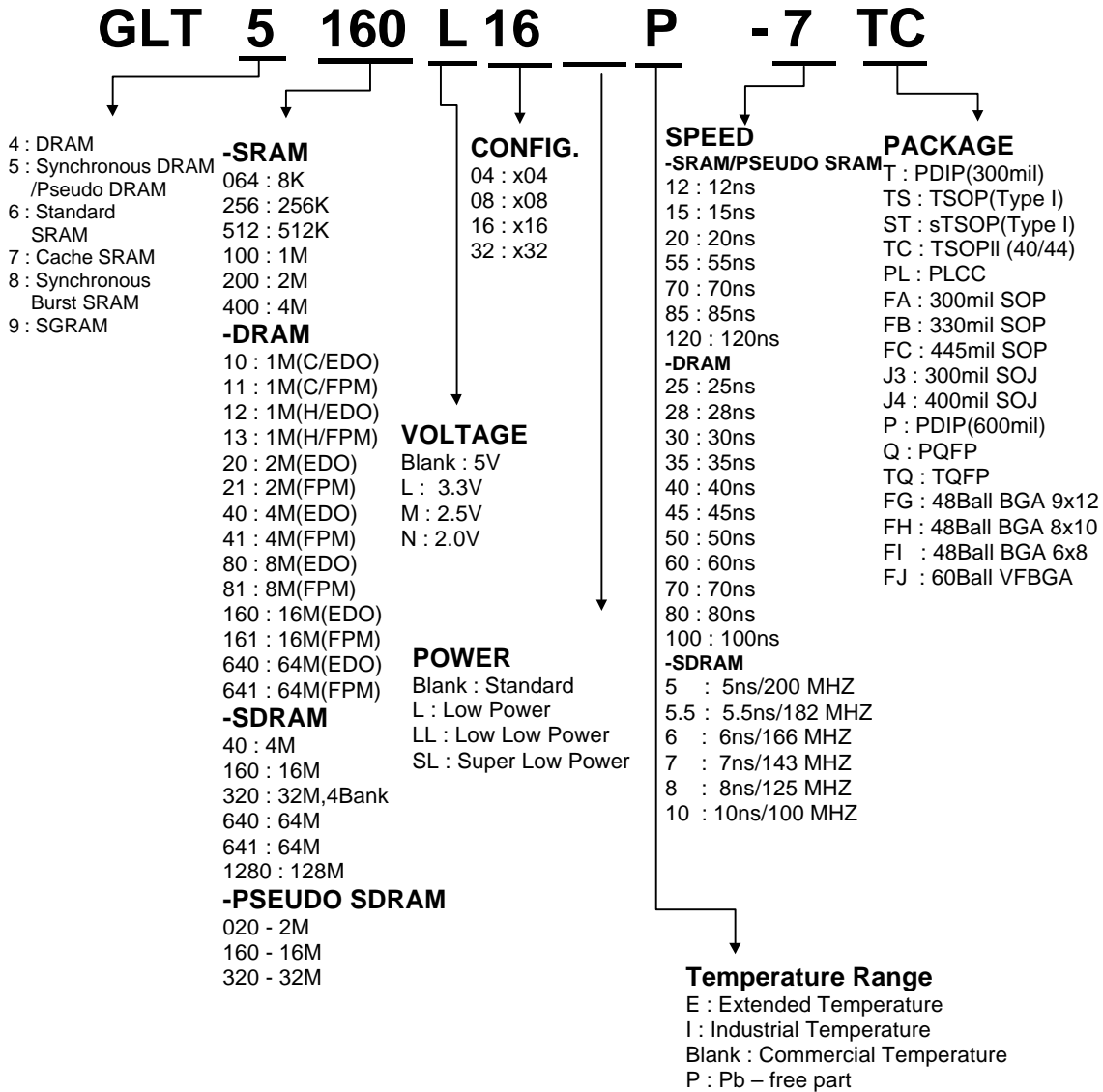
**60-Ball VFBGA ( BOTTOM VIEW )**



**48-Ball VFBGA ( BOTTOM VIEW )**

**ORDERING INFO**
**GLT5160L16**

Part Number	Mode	Cycle Time	Max Frequency	Interface	Package
GLT5160L16-10TC	Synchronous	10	100 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16-8TC	Synchronous	8	125 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16-7TC	Synchronous	7	143 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16-6TC	Synchronous	6	166 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16-10FJ	Synchronous	10	100 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16-8FJ	Synchronous	8	125 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16-7FJ	Synchronous	7	143 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16-6FJ	Synchronous	6	166 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16-10FI	Synchronous	10	100 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16-8FI	Synchronous	8	125 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16-7FI	Synchronous	7	143 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16-6FI	Synchronous	6	166 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16I-10TC	Synchronous	10	100 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16I-8TC	Synchronous	8	125 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16I-7TC	Synchronous	7	143 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16I-6TC	Synchronous	6	166 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16I-10FJ	Synchronous	10	100 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16I-8FJ	Synchronous	8	125 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16I-7FJ	Synchronous	7	143 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16I-6FJ	Synchronous	6	166 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16I-10FI	Synchronous	10	100 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16I-8FI	Synchronous	8	125 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16I-7FI	Synchronous	7	143 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16I-6FI	Synchronous	6	166 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16P-10TC	Synchronous	10	100 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16P-8TC	Synchronous	8	125 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16P-7TC	Synchronous	7	143 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16P-6TC	Synchronous	6	166 MHz	LVTTTL	50-Pin 400 mil Plastic TSOP II
GLT5160L16P-10FJ	Synchronous	10	100 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16P-8FJ	Synchronous	8	125 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16P-7FJ	Synchronous	7	143 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16P-6FJ	Synchronous	6	166 MHz	LVTTTL	60-Ball VFBGA
GLT5160L16P-10FI	Synchronous	10	100 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16P-8FI	Synchronous	8	125 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16P-7FI	Synchronous	7	143 MHz	LVTTTL	48-Ball VFBGA
GLT5160L16P-6FI	Synchronous	6	166 MHz	LVTTTL	48-Ball VFBGA

**ORDERING INFO**
**Parts Numbers (Top Mark) Definition :**




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