Inphi
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13751DE
13 Gbps Differential Encoder
Data Sheet

Applications

- High-speed (up to 13 Gbps) optical duobinary systems
- High-speed (up to 13 Gbps) optical differential phase shift keying systems (DPSK)
- High-speed (up to 13 GHz) digital logic
- Broadband test and measurement equipment

Features

- Supports data rates up to 13 Gbps
- Fast rise and fall times typically < 15 ps
- Low power consumption: 380 mW
- 305° input phase margin (at 12.5 Gbps)
- Supports single-ended and differential operation
- Output signal swing 1200 mVpp differential
- Single +3.3 V power supply
- Available in LGA package or die
- Evaluation board available

Description

The 13751DE differential encoder performs modulo two addition of the input data bit with the previous output bit. The part operates up to 13 Gbps and retimes the input data before performing the encoding operation, thereby providing a large input phase margin.

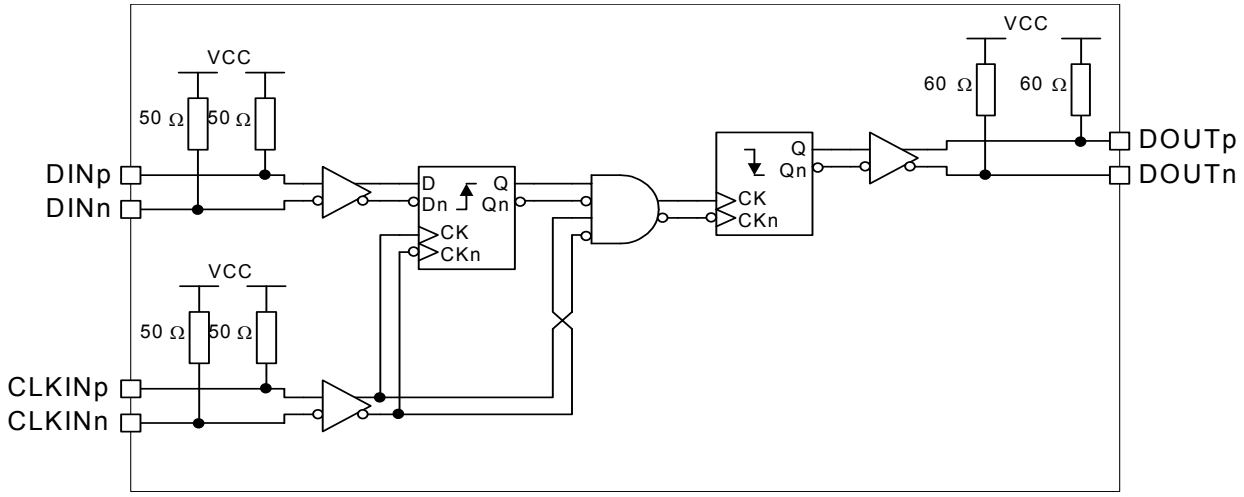
The encoder is nominally positive-edge triggered; however, by reversing the positive and negative clock connections, a negative-edge triggered application can be accommodated.

All differential data and differential clock inputs are DC coupled and terminated on-chip with 50 Ω resistors to V_{CC}. For direct-coupled applications, the differential data outputs should be terminated off chip with 50 Ω resistors to V_{CC} (+3.3 V). For applications requiring termination to DC levels other than V_{CC} (i.e. ground referenced systems), external AC coupling to a good RF ground is required. See the application note for various termination examples.

The 13751DE operates from a single 3.3 V power supply and dissipates only 380 mW.

It is available in a land grid array (LGA) ceramic package or in die form. The packaged part is also available on an evaluation board with SMA connectors.

Block Diagram



Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply Level	V_{CC}		-0.5	3.6	V
Input Signals (Data & Clock)			V_{CC} - 2	V_{CC} + 1	V
Output Signals			V_{CC} - 2	V_{CC} + 1	V
Junction Temperature – Die	T_J		–5	+175	°C
Case Temperature – Package paddle	T_C		–15	+125	°C
Shipping/Storage Temperature	T_{STORE}		–40	+125	°C
Humidity	RH		0	100	%
ESD Protection (Human Body Model)	ESD	Clock and Data inputs	500	---	V
		Data outputs	250	---	V
		Power Supply	750	---	V

Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Level	V_{CC}	± 5% Tolerance	3.135	3.300	3.465	V
On-Chip Power Dissipation	P_D		---	380	500	mW
Power Supply Current	I_{CC}		---	110	144	mA
Operating Temperature (Junction) – Die	T_J		+15	---	+125	°C
Operating Temperature (Case) – Package	T_C		–5	---	+85	°C
Thermal Resistance – junction to paddle	R_{JC} (θ_{JC})	Bottom of paddle	---	60	---	°C/W

Electrical Specifications

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions.						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Maximum Data Rate		10^{-12} BER (NRZ format)	13	---	---	Gbps
Maximum Clock Frequency	f_{MAX}		13	---	---	GHz
Minimum Clock Slew Rate	S_{MIN}	At CLKINp/CLKINn crossing	---	---	1	V/ns
Input High Level (Data & Clock)	V_{IH}	V_{CC} referenced	–0.5	---	0.5	V
Input Low Level (Data & Clock)	V_{IL}	V_{CC} referenced	–1.0	---	0	V
Input Amplitude (Data & Clock)	VIN_{pp}, $VCLK_{pp}$	Differential peak-to-peak	300	---	2000	mVpp
		Single ended peak-to-peak	300	---	1000	mVpp
Input Return Loss (Data) [1]	RL_{IN}	< 13 GHz; Input common mode < V_{CC}	10	---	---	dB
		< 13 GHz; Input common mode < V_{CC} + 0.5 V	6			dB
Input Return Loss (Clock) [1]	RL_{IN}	< 13 GHz	10			dB
Clock Phase Margin	CPM	At 12.5 Gbps	270	305	---	deg
Data Output Amplitude[2]	$VOUT_{pp}$	Differential peak-to-peak	900	1200	1400	mVpp
Output High Level	V_{OH}	DC coupled, V_{CC} referenced	V_{CC} -50	V_{CC} -4	V_{CC}	mV
Output Common Mode	V_{OCM}	DC coupled, V_{CC} referenced	---	V_{CC}-300	---	mV
Output Rise/Fall Time	t_r/t_f	20–80%	---	15	20	ps
Output Return Loss[3]	RL_{OUT}	< 13 GHz	10	---	---	dB
Deterministic Jitter[4, 5]	J_D	Peak-to-peak	---	2	4	ps
Random Jitter[4, 5]	J_R	RMS	---	0.2	0.4	ps
Clock-to-Data Output Delay[4, 6]	t_Q	Die Packaged	40 90	50 110	60 130	ps ps
Set-up Time[6, 7]	t_{set}	Measured at package pins	10	6		ps
Hold Time[6, 7]	t_{hold}	Measured at package pins	10	6		ps

Notes:

[1] Inputs are designed to be a broadband match to 50 Ω impedance and are terminated with a 50 Ω resistor to V_{CC}.

[2] Outputs are CML and referenced to VCC. Values given are based on DC measurements.

[3] Outputs are designed to be a broadband match to 50 Ω impedance and are terminated with a 60 Ω resistor to V_{CC}.

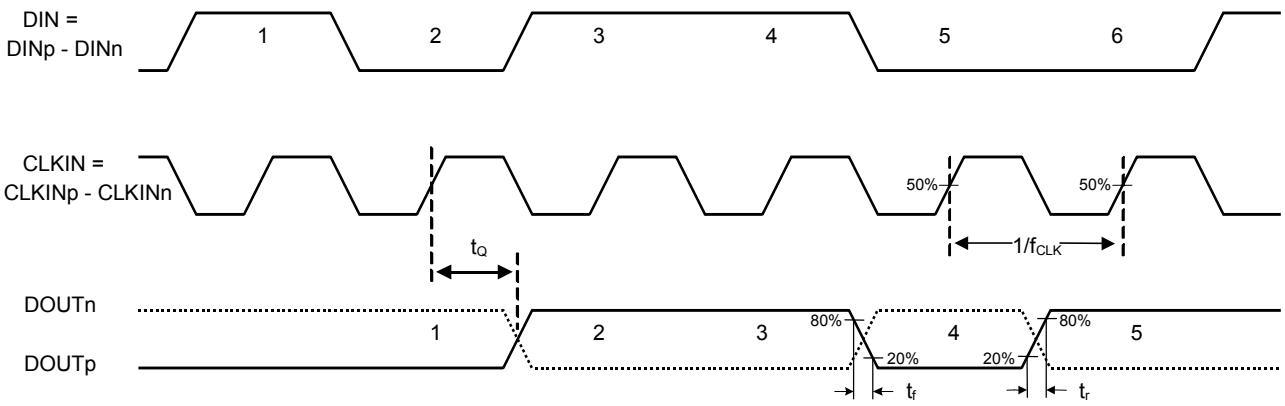
[4] Valid when clock-to-data phase is near center of CPM window.

[5] It should be noted that because the random and deterministic jitter of Inphi's high-speed logic parts are "in the noise" of the measurement techniques used, these specifications are conservative. The deterministic jitter (J_D) specified is the peak-to-peak total jitter measured using a 2^{31}-1 PRBS data pattern. The random jitter (J_R) is the RMS jitter measured on a 1010... pattern. The jitter of the source and measurement equipment was not removed from the measured data.

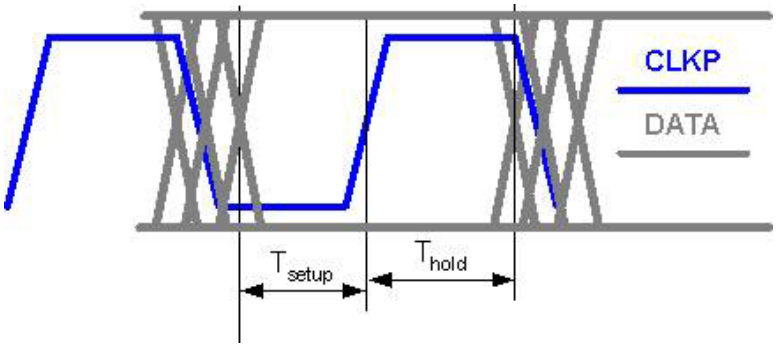
[6] Values based on design simulations.

[7] The setup and hold time specifications were determined from phase margin measurements and the assumption, supported by simulation, that Set-up and Hold times are equal to within a picosecond. See timing diagram on page 4 for definition.

Timing Diagram



Set-up and Hold Time Definition



Truth Table

DIN_{k-1}	$DOUT_{k-1}$	$DOUT_k$
0	0	0
0	1	1
1	0	1
1	1	0

$DOUT_k = DOUT_{k-1} \oplus DIN_{k-1}$

This equation corresponds to the well-known differential encoder equation $DOUT_k = DOUT_{k-1} \oplus DIN_k$, modified to include a one bit period delay in input data for retiming.

Notes:

DIN = DINp – DINn
DOUT = DOUTp – DOUTn

Typical DC Operating Characteristics

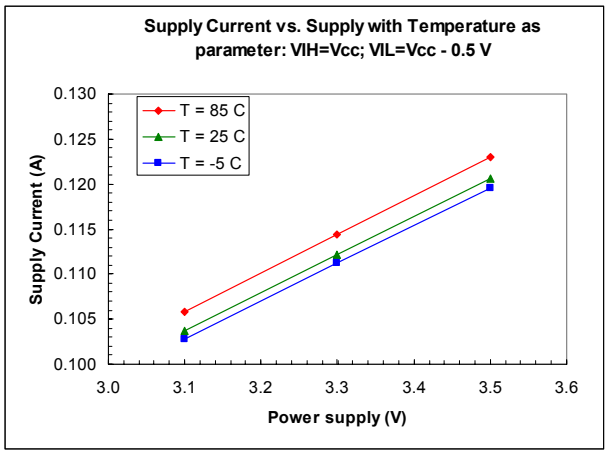


Figure 1. Supply current versus power supply with temperature as parameter

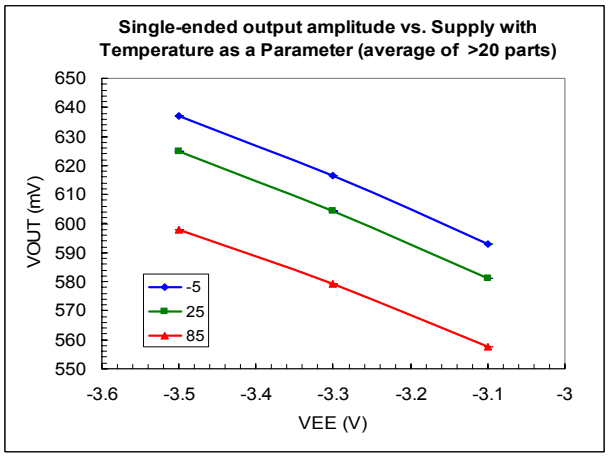


Figure 2. Single-ended peak-to-peak output vs. power supply with temperature as parameter*

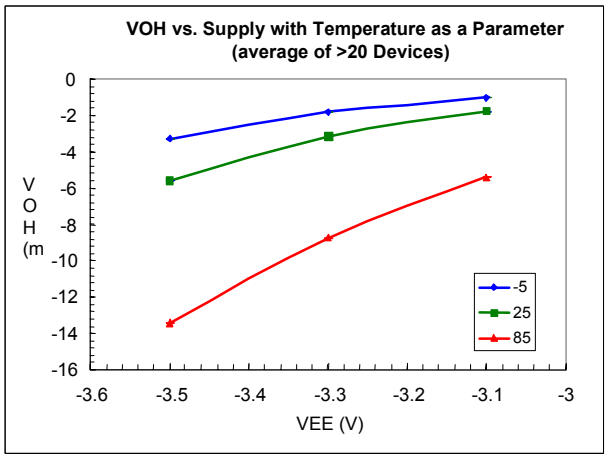


Figure 3. V_{OH} versus power supply with temperature as parameter*

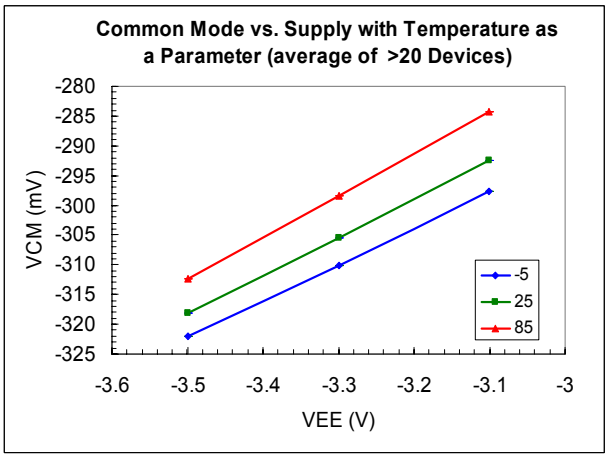


Figure 4. Output common mode vs. power supply with temperature as parameter*

* From measurements of the 13750DE. The 13750 DE is identical to the 13751DE, but operates from a negative 3.3 V power supply.

Time Domain Operating Characteristics

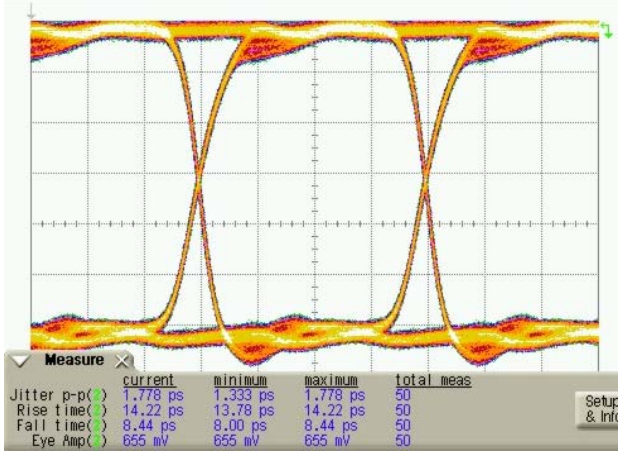


Figure 5. Output eye diagram at 12.5 Gbps; Horizontal scale is 20 ps per division. T = 25°C; Vcc = 3.3 V

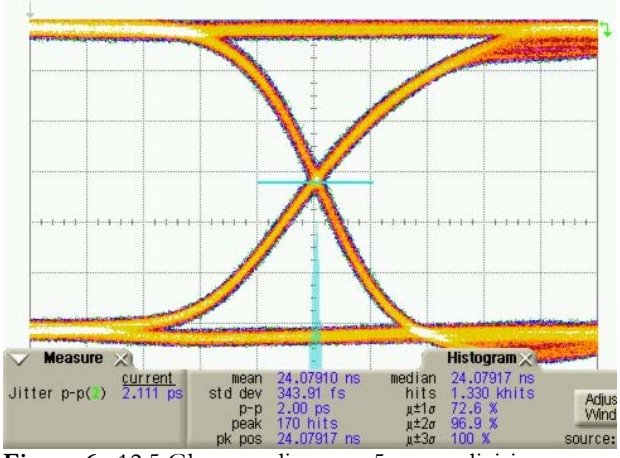


Figure 6. 12.5 Gbps eye diagram; 5 ps per division.; Histogram used to measure peak-to-peak jitter.

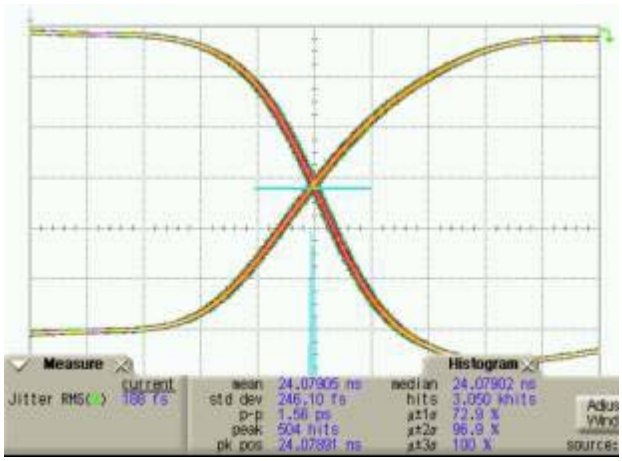


Figure 7. Histogram of output zero-crossing for 1010 output; T = 25° C and Vcc = 3.3 V

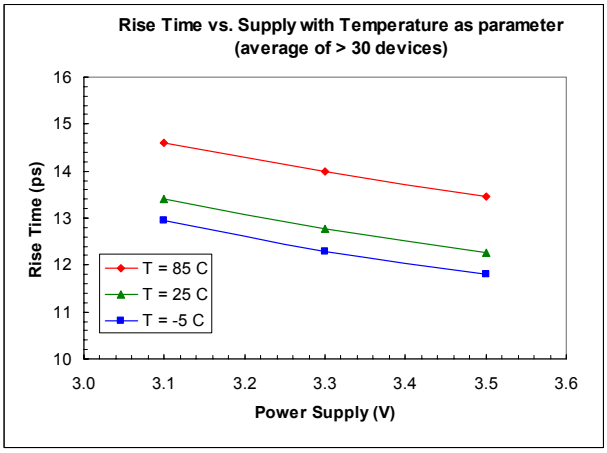


Figure 8. Rise time vs. power supply with temperature as parameter

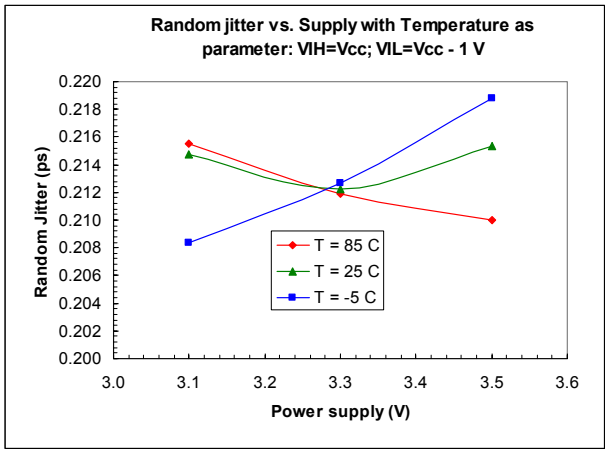


Figure 9. Random jitter vs. power supply with temperature as parameter

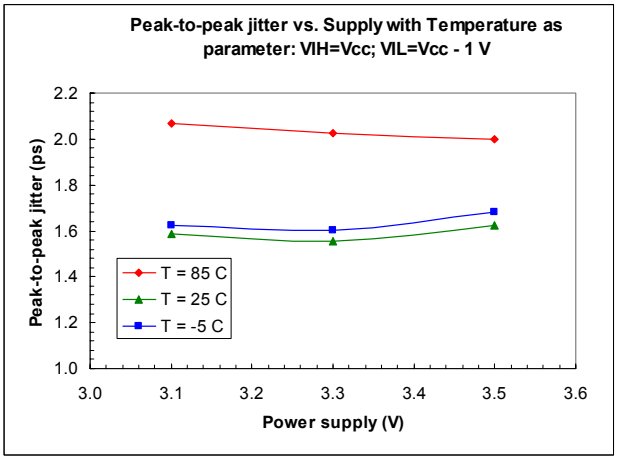


Figure 10. Peak-to-peak jitter vs. power supply with temperature as parameter

Typical Return Losses

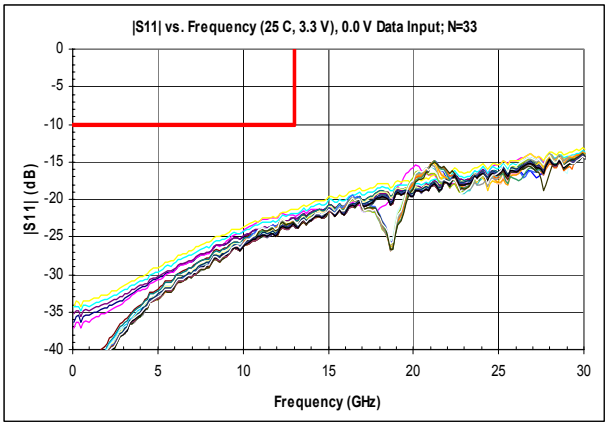


Figure 11. |S11| versus frequency of 33 parts; Die level data

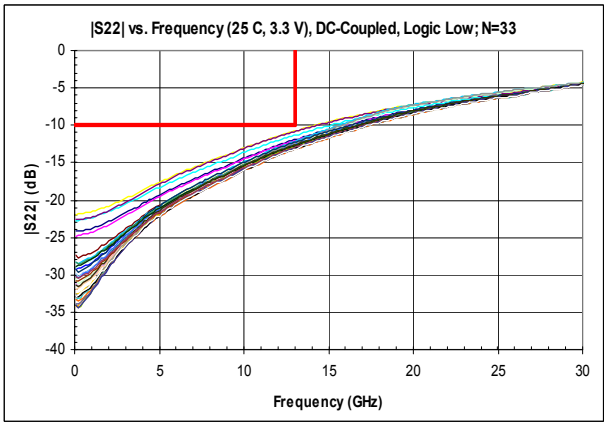


Figure 12. |S22| versus frequency with output in low state (worst case) of 33 parts; Die level data

Clock to Data Phase Margin

The clock to data phase margin is defined in degrees with 360° being a full period of the clock at 12.5 Gbps. It is measured by gradually adjusting the phase of the clock input relative to the data input and looking at the error rate of the differential encoder with a bit error rate tester. As indicated in figure 13, the 13751DE's phase margin is large: typically 305°.

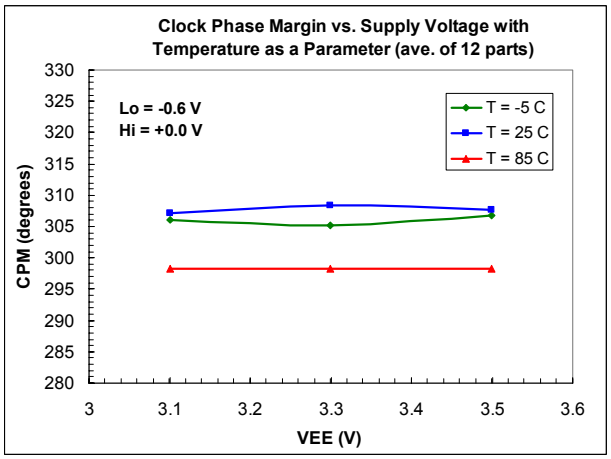
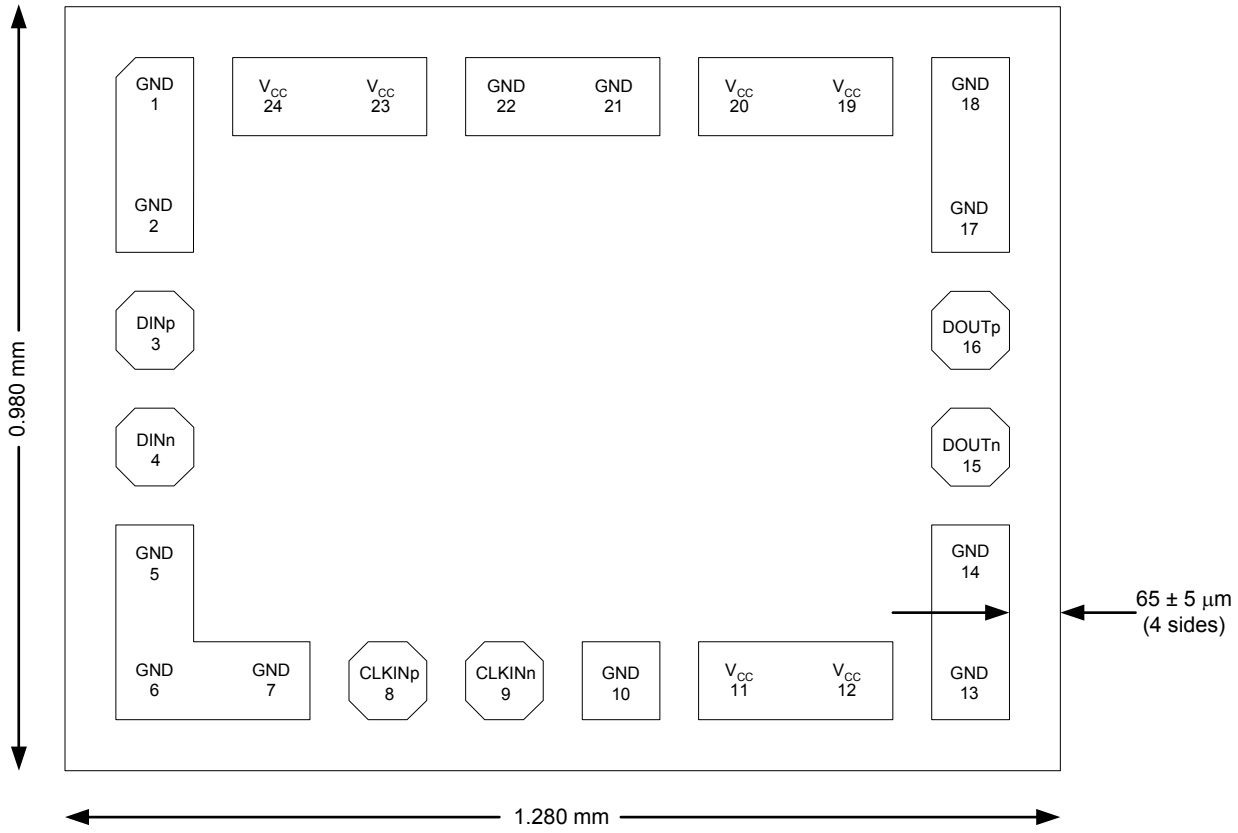


Figure 13. Clock phase margin vs. operating conditions at 12.5 Gbps

Set-up and Hold Times

Direct measurement of the set-up and hold times is difficult because it involves accurately measuring the electrical delay of the clock and input from signal generators to the package pins and knowledge of the phase between the two signals at their respective generators. Since simulations indicate that the set-up and hold times are equal to within a picosecond, they can be determined from the phase margin. Since the phase margin is typically 305°, the typical set-up and hold times are one half of 55°/360° times 80 ps, or 6 ps.

Die Pad Layout



Notes:
[1]100 µm pads on 150 µm pitch
[2]150 ± 10 µm die thickness
[3]The bonding pad locations specified are merged into larger metal pads on the die

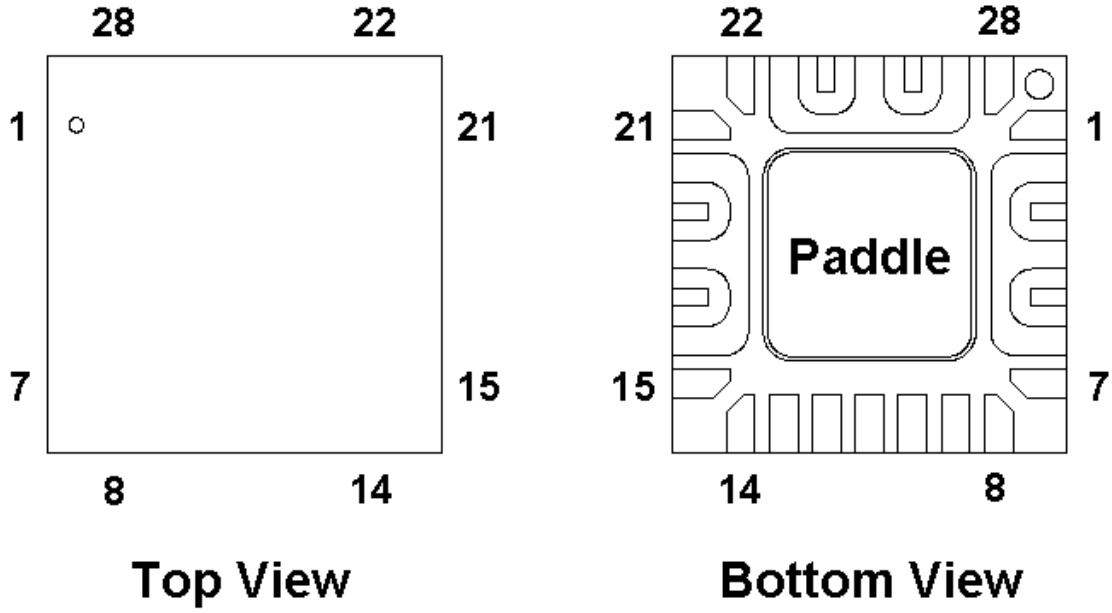
Name	Pad	Description	Function
DINp	3	Non-inverting Data Input	Input
DINn	4	Inverting Data Input	Input
CLKINp	8	Non-inverting Clock Input	Input
CLKINn	9	Inverting Clock Input	Input
DOUTp	16	Non-inverting Data Output	Output
DOUTn	15	Inverting Data Output	Output
GND	1, 2, 5, 6, 7, 10, 13, 14, 17, 18, 21, 22	Ground	Supply
V_{CC}	11, 12, 19, 20, 23, 24	Power Supply: Connect to +3.3 V DC	Supply

Die Pad Locations

For dimensioning purposes, reference origin (0,0) is the lower left corner of the lower left pad.

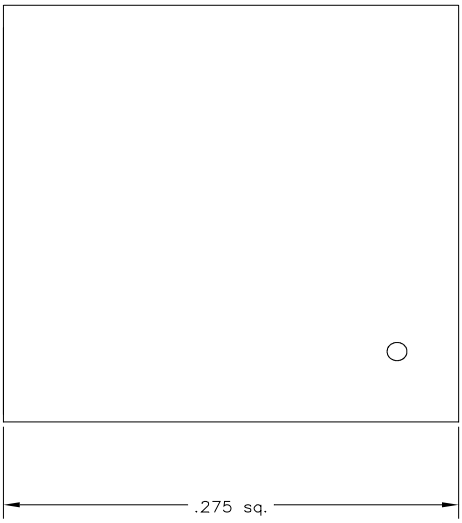
Pad #	Signal	Pad Lower Left Corner	
		X	Y
1	GND	0	750
2	GND	0	600
3	DINp	0	450
4	DINn	0	300
5	GND	0	150
6	GND	0	0
7	GND	150	0
8	CLKINp	300	0
9	CLKINn	450	0
10	GND	600	0
11	V_{CC}	750	0
12	V_{CC}	900	0
13	GND	1050	0
14	GND	1050	150
15	DOUTn	1050	300
16	DOUTp	1050	450
17	GND	1050	600
18	GND	1050	750
19	V_{CC}	900	750
20	V_{CC}	750	750
21	GND	600	750
22	GND	450	750
23	V_{CC}	300	750
24	V_{CC}	150	750

LGA Pin Assignment



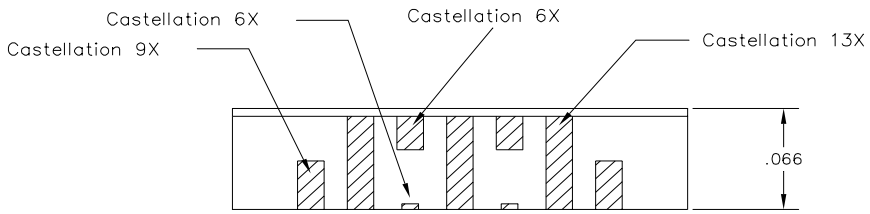
Name	Pin	Description	Function
DINp	5	Non-inverting Data Input	Input
DINn	3	Inverting Data Input	Input
CLKINp	26	Non-inverting Clock Input	Input
CLKINn	24	Inverting Clock Input	Input
DOUTp	17	Non-inverting Data Output	Output
DOUTn	19	Inverting Data Output	Output
GND	2, 4, 6, 9, 12, 13, 16, 18, 20, 21, 23, 25, 27, Paddle	Ground	Supply
V_{CC}	10, 11, 22	Power Supply: Connect to +3.3 V DC	Supply
NC	1, 7, 8, 14, 15, 28	Not Connected	NC

LGA Package Outline Drawing

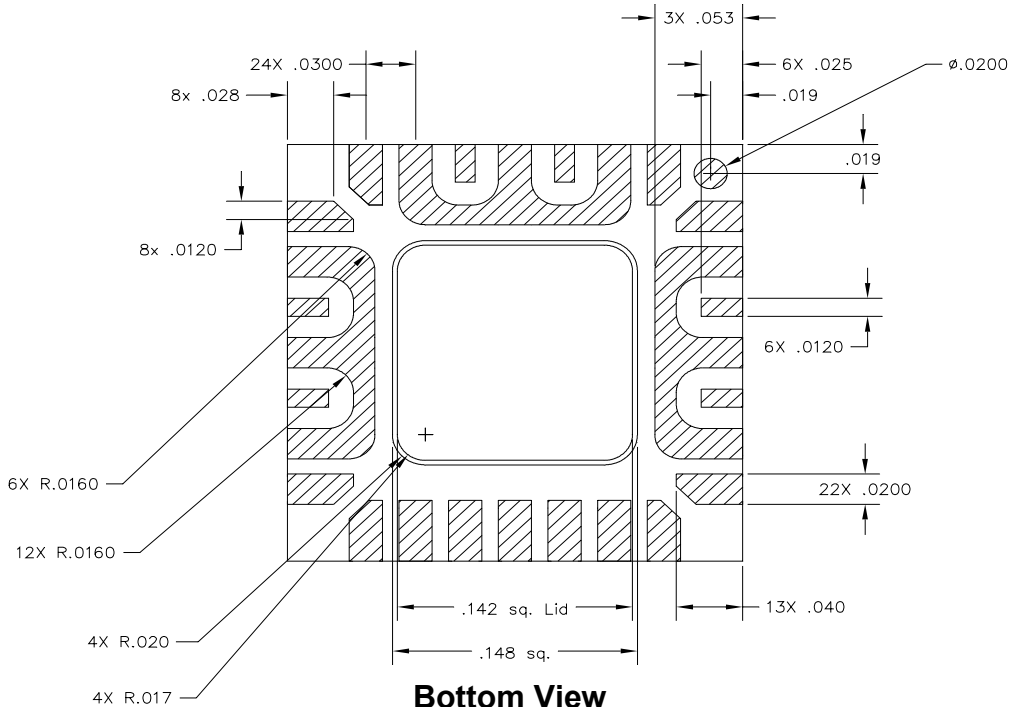


UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± 1/64
DECIMALS XX ±.01, .XXX ±.002, .XXXX ±0.0005
ANGLES ± 0°30'

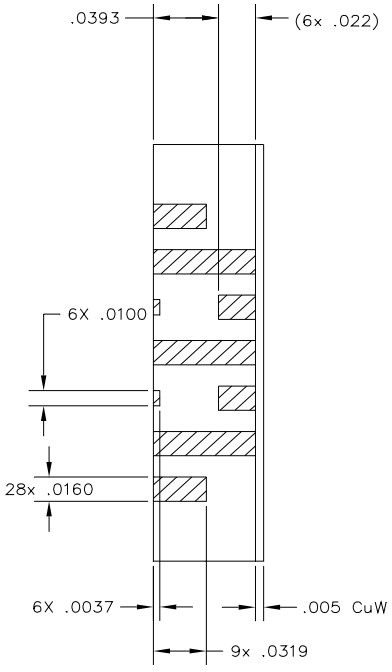
Top View



Side View



Bottom View



Order Information

Part No.	Description
13751DE-S02D	13 Gbps Differential Encoder (+3.3 V Supply) – Die
13751DE-S02L	13 Gbps Differential Encoder (+3.3 V Supply) in LGA Package
13751DE-S02LEVB	13 Gbps Differential Encoder (+3.3 V Supply) in LGA Package on an Evaluation Board with SMA Connectors

Contact Information

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Qualification Notification

The 13751DE-S02 is fully qualified. Please contact Inphi for the qualification report.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Version Updates

From Version 3.0 to 3.1 (11/11/2005)

1. Various typographical errors were corrected throughout the document.
2. Absolute Maximum table: deleted the "typical" column and added the disclaimer statements.
3. Changes to Operating Conditions table:
    a. Added Power Supply Current: max. spec. = 144 mA; typical = 110 mA.
    b. Deleted note 1.
4. Changes to Electrical Specifications table:
    a. Input Amplitude (Data & Clock) Differential peak-to-peak spec. from 1400 to 2000 mVpp.
    b. Input Return Loss: changed Input Common Mode condition to be referenced from Vcc.
    c. Data Output Amplitude: max from – to 1400 mVpp. Also added "Values based on DC measurements" to note 1.
    d. Output High Voltage: added V_{CC} to min. and typical specs.
    e. Output Common Mode: added V_{OCM} as symbol.
    f. Output Rise/Fall Time: changed max. spec. from 25 to 20 ps; typical from – to 15 ps.
    g. Deterministic Jitter: added max. spec. of 4 ps; and note 4.
    h. Random Jitter: added max. spec. of 0.4 ps; changed typical from 0.5 to 0.2 ps; and note 4.
5. Die Pad Layout section: separated all differential pin pairs (i.e. DINp & DINn) onto separate lines.
6. LGA Pinout section: separated all differential pin pairs (i.e. DINp & DINn) onto separate lines.
7. Limited Qualification Notification section: changed to say that 13751DE-S02 is fully qualified.

From Version 3.1 to 3.2 (6/22/2006)

1. Absolute Maximum table (page 2):
    a. Changed Input Signals' maximum level from V_{CC} +0.6 to V_{CC} +1 V.
    b. Changed Output Signals' minimum level from V_{CC} –1.5 to V_{CC} -2 V.
    c. Added ESD specs..
2. Added Thermal Resistance to Operating Conditions table (page 2).
3. Electrical Specifications table (page 3):
    a. Added notes 1, 3, & 6.
    b. Changed note numbers on parameter descriptions.
1. LGA Package Outline Drawing (page 11): replaced the old drawing with a new drawing. The package height was incorrect (corrected from 60 mils to 66 mils).
4. Qualification Notification section (page 12):
    a. Added statement on radiation tolerance.

From Version 3.2 to 3.3 (dated 2007-06-22)

1. Removed radiation tolerance statement from Qualification Notification section (page 12).