

DRAM

64K x 16 DRAM

LOW POWER
EXTENDED REFRESH

WIDE DRAM

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle (MT4C1664 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1665 L only)
- Reduced CMOS STANDBY CURRENT
- Low power, 1mW standby; 225mW active, typical
- Extended refresh: 256 cycles over 32ms (125µs cycles)

OPTIONS

- Timing
 - 70ns access
 - 80ns access
 - 100ns access
- Write Enable
 - Byte or Word
 - Word only
- Mask Enable
 - Not available
 - Always available
- Packages
 - Plastic SOJ (400mil)
 - Plastic TSOP (400mil)
 - Plastic ZIP (475mil)

MARKING

- 7	MT4C1664 L
- 8	MT4C1665 L
-10	
	MT4C1664 L
	MT4C1665 L

NOTE: Available in die form Please consult factory for die data sheets.

- Part Number Example: MT4C1664DJ-7 L

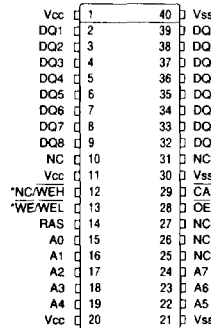
GENERAL DESCRIPTION

The MT4C1664/5 L are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1664 L has both BYTE and WORD WRITE access cycles while the MT4C1665 L has only WORD WRITE access cycles.

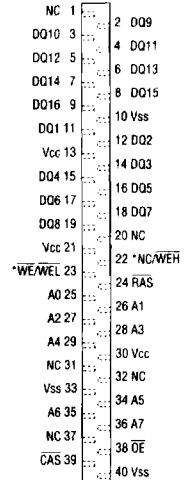
The MT4C1664 L functions in a similar manner to the MT4C1665 L except that replacing \overline{WE} with \overline{WEL} and \overline{WEH} allows for BYTE WRITE access cycles. \overline{WEL} and \overline{WEH} function in an identical manner to \overline{WE} : either \overline{WEL}

PIN ASSIGNMENT (Top View)

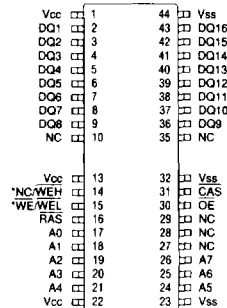
40-Pin SOJ (Q-6)



40-Pin Zip (O-4)



40-Pin TSOP (R-5)



*MT4C1665 L/MT4C1664 L

or \overline{WEH} will generate an internal \overline{WE} through an AND gate (inverted NOR gate).

The MT4C1664 L " \overline{WE} " function and timing are determined by the first BYTE WRITE (\overline{WEL} or \overline{WEH}) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: \overline{WEL} transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or \overline{WEH} transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

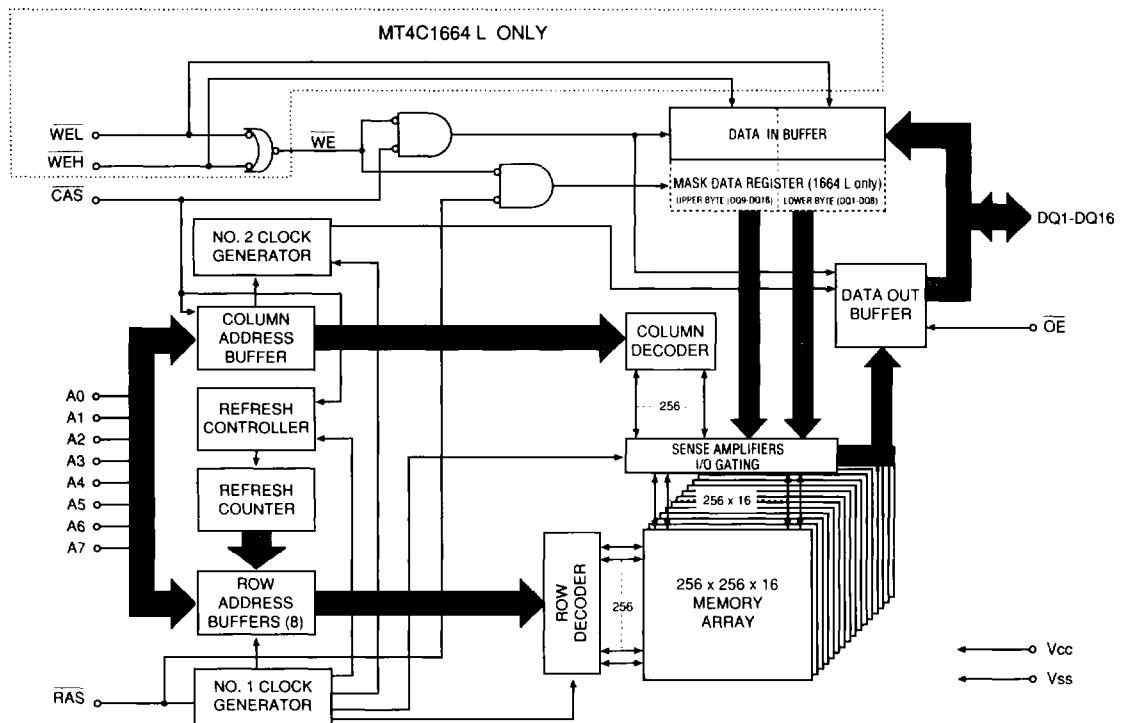
The MT4C1665 L has NONPERSISTENT MASKED WRITE capability.

The extended refresh of the MT4C1664/5 L provides a factor-of-eight reduction of refresh intervals required, as compared to a standard 64K x 16 DRAM (MT4C1664/5).

The MT4C1664/5 L offers lower operating power as well as reduced refresh and standby currents. The MT4C1664/5 L are the same devices as the MT4C1664/5, but with low power capabilities.

WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	RAS	Input	ROW Address Strobe: RAS is used to clock-in the 8 row address bits and strobe the WEL, WEH and DQ inputs for the MASKED WRITE function.
29	39	31	CAS	Input	Column Address Strobe: CAS is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	OE	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WEL and WEH must be HIGH before OE will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	WE/WEL*	Input	WRITE Enable Lower Byte: WEL on MT4C1664 L is WE control for the DQ1 through DQ8 inputs. WE on MT4C1665 L controls DQ1 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/WEH*	Input	Write Enable Upper Byte: WEH on MT4C1664 L is WE control for the DQ9 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1665 L as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one 16-bit word out of the 64K available words.
2-9, 32-39	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITES can be performed by using WEL or WEH to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	10, 27-29, 35	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1665 L/MT4C1664 L

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. \overline{RAS} is used to latch the first 8 bits and \overline{CAS} the latter 8 bits.

READ or WRITE cycles on the MT4C1665 L are selected with the \overline{WE} input while either \overline{WEL} or \overline{WEH} perform the " \overline{WE} " on the MT4C1664 L. The MT4C1664 L " \overline{WE} " function is determined by the first BYTE WRITE (\overline{WEL} or \overline{WEH}) to transition LOW and the last one to transition back HIGH.

A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Taking \overline{WE} LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after \overline{CAS} goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by \overline{OE} , \overline{WEL} and \overline{WEH} (MT4C1664 L) or \overline{WE} (MT4C1665 L).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} , or HIDDEN refresh) so that all 256 combinations of \overline{RAS} addresses (A0-A7) are executed at least every 32ms, regardless of sequence. The \overline{CAS} -BEFORE- \overline{RAS} refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. \overline{RAS} or \overline{CAS} time refers to the time at which \overline{RAS} or \overline{CAS} transition from HIGH to LOW).

BYTE WRITE DESCRIPTION (MT4C1664 L ONLY)

The BYTE WRITE mode is determined by the use of \overline{WEL} and \overline{WEH} . Enabling \overline{WEL} will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling \overline{WEH} will select an upper BYTE WRITE (DQ9-DQ16). Enabling both \overline{WEL} and \overline{WEH} selects a WORD WRITE cycle.

The MT4C1664 L may be viewed as two 64K x 8 DRAMs which have common input controls, with the exception of the \overline{WE} input. Figure 1 illustrates the MT4C1664 L BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1665 L ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and \overline{WE} is LOW at \overline{RAS} time. The MT4C1665 L is only word selectable when \overline{WE} is LOW at \overline{RAS} time (the MT4C1664 L does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at \overline{RAS} time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At \overline{CAS} time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1665 L MASKED WRITE operation (Note: \overline{RAS} or \overline{CAS} time refers to the time at which \overline{RAS} or \overline{CAS} transition from HIGH to LOW).

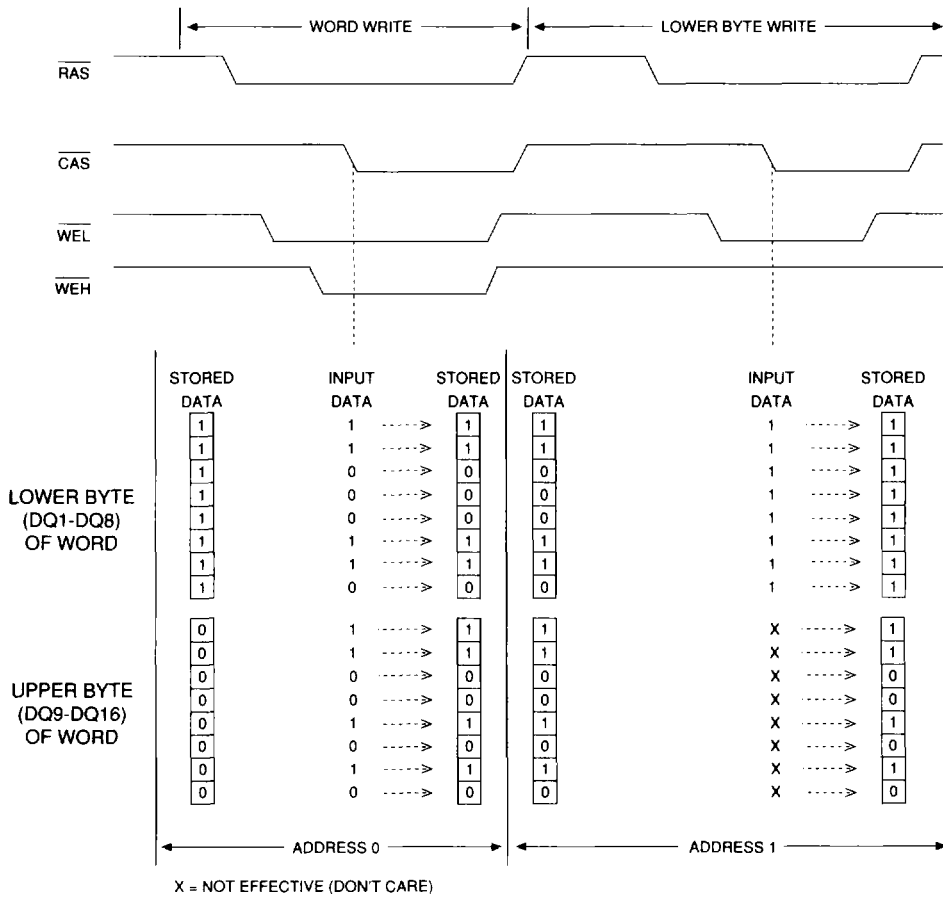


Figure 1
MT4C1664 L WORD AND BYTE WRITE EXAMPLE

WIDE DRAM

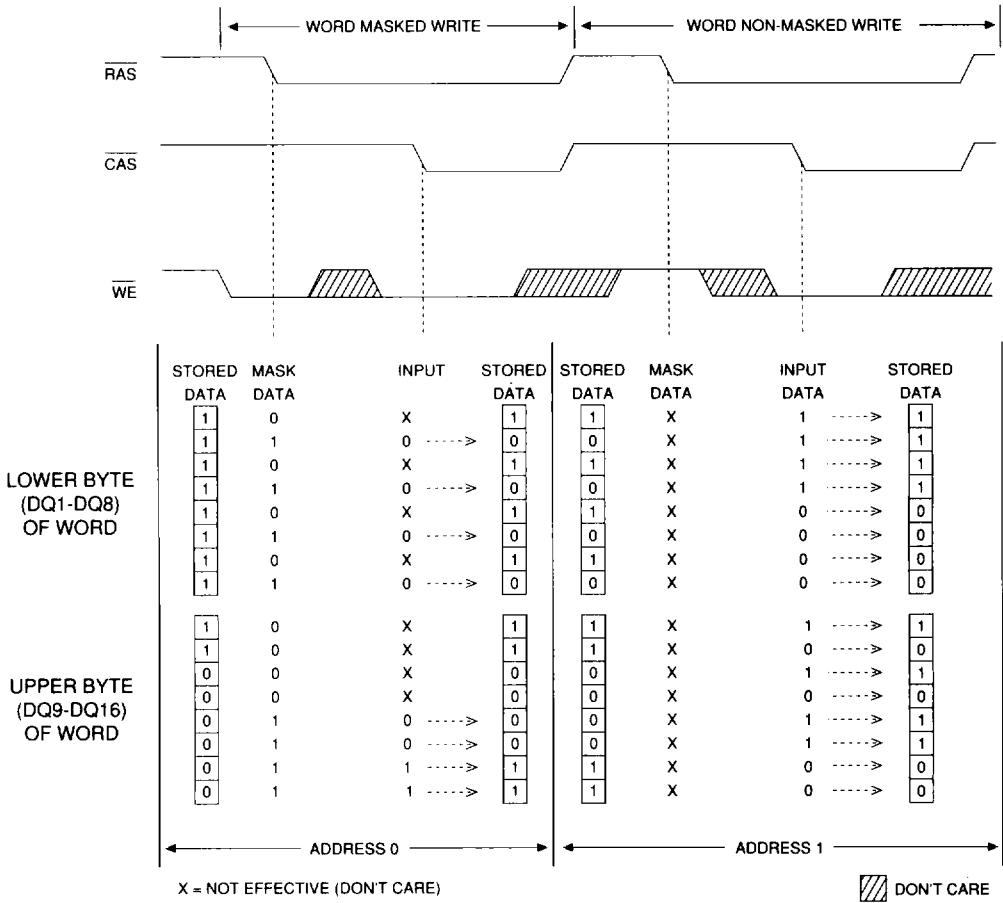


Figure 2
MT4C1665 L MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1664 L

FUNCTION	RAS	CAS	WEL	WEH	OE	ADDRESSES		DQs	NOTES	
						'R	'C			
Standby	H	H→X	X	X	X	X	X	High-Z		
READ	L	L	H	H	L	ROW	COL	Data Out		
WRITE: WORD (EARLY-WRITE)	L	L	L	L	X	ROW	COL	Data In		
WRITE: LOWER BYTE (EARLY)	L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z		
WRITE: UPPER BYTE (EARLY)	L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In		
READ-WRITE	L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH	L	H	X	X	X	ROW	n/a	High-Z		
CAS-BEFORE-RAS REFRESH	H→L	L	X	X	X	X	X	High-Z		
BATTERY BACKUP REFRESH	H→L	L	X	X	X	X	X	High-Z		

WIDE DRAM

NOTE: 1. These cycles may also be BYTE WRITE cycles (either \overline{WEL} or \overline{WEH} active).
2. EARLY-WRITE only.

TRUTH TABLE: MT4C1665 L

WIDE DRAM

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DQs	NOTES
						'r	'c		
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out	
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss -1V to +7V
 Operating Temperature, T_A (Ambient) 0°C to +70°C
 Storage Temperature (Plastic) -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V _{IH}	2.4	V _{CC} +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V _{IN} ≤ V _{CC} (All other pins not under test = 0V)	I _I	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	I _{OZ}	-10	10	μA	
OUTPUT LEVELS					
Output High Voltage (I _{OUT} = -2.5mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 2.1mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-7	-8	-10		
STANDBY CURRENT: (TTL) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I _{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	I _{CC2}	300	300	300	μA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (\overline{RAS} , \overline{CAS} , Address Cycling; $I_{RC} = I_{RC} (MIN)$)	I _{CC3}	120	110	100	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS} = V_{IL}$; \overline{CAS} , Address Cycling; $I_{PC} = I_{PC} (MIN)$; I_{CP} , $I_{ASC} = 10ns$)	I _{CC4}	80	70	60	mA	3, 4, 32
REFRESH CURRENT: \overline{RAS} -ONLY Average power supply current (\overline{RAS} Cycling, $\overline{CAS} = V_{IH}$; $I_{RC} = I_{RC} (MIN)$)	I _{CC5}	120	110	100	mA	3, 32
REFRESH CURRENT: \overline{CAS} -BEFORE- \overline{RAS} Average power supply current (\overline{RAS} , \overline{CAS} , Address Cycling; $I_{RC} = I_{RC} (MIN)$)	I _{CC6}	120	110	100	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current with $\overline{CAS} = 0.2V$ or CBR; $\overline{RAS} =$ minimum I_{RAS} to 1μs; A0-A7, \overline{WE} , \overline{OE} and DQs = V _{CC} - 0.2V or 0.2V (DQs may float); $I_{RC} = 125\mu s$	I _{CC7}	400	400	400	μA	3, 31

WIDE DRAM

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, (WEL, WEH)/ WE, OE	C _{I2}		7	pF	2
Input/Output Capacitance: DQ	C _{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS	PARAMETER	SYM	-7		-8		-10		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	'RC		130		145		170		ns	
READ-WRITE cycle time	'RWC		175		185		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	'PC		45		50		60		ns	
FAST-PAGE-MODE READ-WRITE cycle time	'PRWC		95		100		120		ns	
Access time from RAS	'RAC			70		80		100	ns	14
Access time from CAS	'CAC			25		25		30	ns	15
Output Enable time	'OE			25		25		30	ns	
Access time from column address	'AA			40		45		50	ns	
Access time from CAS precharge	'CPA			45		50		55	ns	
RAS pulse width	'RAS	70	100,000	80	100,000	100	100,000		ns	
RAS pulse width (FAST PAGE MODE)	'RASP	70	100,000	80	100,000	100	100,000		ns	
RAS hold time	'RSH	20		20		25			ns	
RAS precharge time	'RP	45		45		60			ns	
CAS pulse width	'CAS	25	100,000	25	100,000	30	100,000		ns	
CAS hold time	'CSH	70		80		100			ns	
CAS precharge time	'CPN	10		10		15			ns	16
CAS precharge time (FAST PAGE MODE)	'CP	10		10		10			ns	
RAS to CAS delay time	'RCD	20	45	20	50	25	60		ns	17
CAS to RAS precharge time	'CRP	5		5		5			ns	
Row address setup time	'ASR	0		0		0			ns	
Row address hold time	'RAH	10		10		10			ns	
RAS to column address delay time	'RAD	15	35	15	40	15	50		ns	18
Column address setup time	'ASC	0		0		0			ns	
Column address hold time	'CAH	15		15		15			ns	
Column address hold time (referenced to RAS)	'AR	55		60		70			ns	
Column address to RAS lead time	'RAL	35		40		50			ns	
Read command setup time	'RCS	0		0		0			ns	26
Read command hold time (referenced to CAS)	'RCH	0		0		0			ns	19, 26
Read command hold time (referenced to RAS)	'RRH	0		0		0			ns	19
CAS to output in Low-Z	'CLZ	0		0		0			ns	

WIDE DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Output buffer turn-off delay	t _{OFF}	0	20	0	20	0	20	ns	20, 30
Output disable time	t _{OD}		15		15		20	ns	30
Write command setup time	t _{WCS}	0		0		0		ns	21, 26
Write command hold time	t _{WCH}	15		15		15		ns	26
Write command hold time (referenced to RAS)	t _{WCR}	50		55		65		ns	26
Write command pulse width	t _{WP}	15		15		15		ns	26
Write command to RAS lead time	t _{RWL}	20		20		20		ns	26
Write command to CAS lead time	t _{CWL}	20		20		20		ns	26
Data-in setup time	t _{DS}	0		0		0		ns	22
Data-in hold time	t _{DH}	15		15		20		ns	22
Data-in hold time (referenced to RAS)	t _{DHR}	50		55		65		ns	
RAS to WE delay time	t _{RWD}	90		100		125		ns	21
Column address to WE delay time	t _{AWD}	65		70		80		ns	21
CAS to WE delay time	t _{CWD}	50		55		70		ns	21
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	t _{REF}		32		32		32	ms	28
RAS to CAS precharge time	t _{RPC}	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	t _{CSR}	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	t _{CHR}	15		15		15		ns	5
MASKED WRITE command to RAS setup time	t _{WRS}	0		0		0		ns	26, 27
MASKED WRITE command to RAS hold time	t _{WRH}	15		15		15		ns	26, 27
Mask data to RAS setup time	t _{MS}	0		0		0		ns	26
Mask data to RAS hold time	t _{MH}	15		15		15		ns	26
OE hold time from WE during READ-MODIFY-WRITE cycle	t _{OEH}	10		10		20		ns	29
OE setup prior to RAS during HIDDEN REFRESH cycle	t _{ORD}	0		0		0		ns	

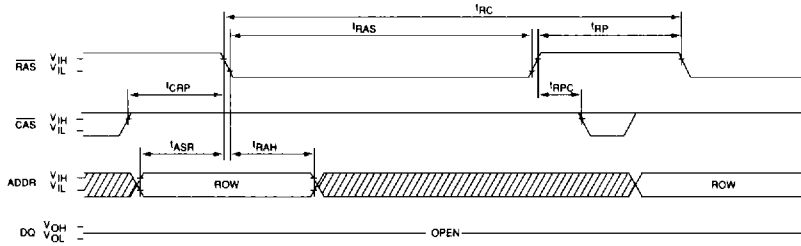
WIDE DRAM

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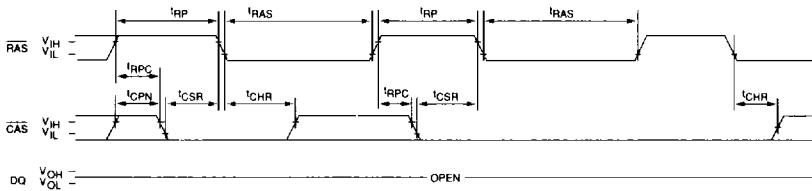
1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$, $f = 1\text{ MHz}$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) is assured.
7. An initial pause of $100\mu\text{s}$ is required after power-up followed by any eight $\overline{\text{RAS}}$ cycles before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-up should be repeated any time the $\overline{\text{REF}}$ refresh requirement is exceeded.
8. AC characteristics assume $t_T = 5\text{ns}$.
9. V_{IH} (MIN) and V_{II} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{II} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{II} (or between V_{II} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}} = V_{IH}$, data output is high impedance.
12. If $\overline{\text{CAS}} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gates and 50pF .
14. Assumes that $t_{\text{RCD}} < t_{\text{RCD}}(\text{MAX})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX})$.
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for t_{CPN} .
17. Operation within the $t_{\text{RCD}}(\text{MAX})$ limit ensures that $t_{\text{RAC}}(\text{MAX})$ can be met. $t_{\text{RCD}}(\text{MAX})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{MAX})$ limit, then access time is controlled exclusively by t_{CAC} .
18. Operation within the $t_{\text{RAD}}(\text{MAX})$ limit ensures that $t_{\text{RCD}}(\text{MAX})$ can be met. $t_{\text{RAD}}(\text{MAX})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{MAX})$ limit, then access time is controlled exclusively by t_{AA} .
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. $t_{\text{OFF}}(\text{MAX})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
21. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{MIN})$, the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{MIN})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{MIN})$ and $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{MIN})$, the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE-WRITE ($\overline{\text{OE}}$ controlled) cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}} = \text{LOW}$ and $\overline{\text{OE}} = \text{HIGH}$.
25. All other inputs at $V_{CC} - 0.2\text{V}$.
26. WRITE command is defined as either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ or both going LOW on the MT4C1664 L. WRITE command is defined as $\overline{\text{WE}}$ going LOW on the MT4C1665 L.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. The refresh period may be extended to 8ms without causing problems.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken back LOW after t_{OEH} is met. If $\overline{\text{CAS}}$ goes HIGH prior to $\overline{\text{OE}}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once t_{OD} or t_{OFF} occur. If $\overline{\text{CAS}}$ goes HIGH first, $\overline{\text{OE}}$ becomes a "don't care." If $\overline{\text{OE}}$ goes HIGH and $\overline{\text{CAS}}$ stays LOW, $\overline{\text{OE}}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{\text{OE}}$ is taken back LOW (while $\overline{\text{CAS}}$ remains LOW).
31. BBU current does not significantly change when t_{RAS} is reduced from its maximum specification during BBU cycle.
32. Column address changed once while $\overline{\text{RAS}} = V_{IL}$ and $\overline{\text{CAS}} = V_{IH}$

WIDE DRAM

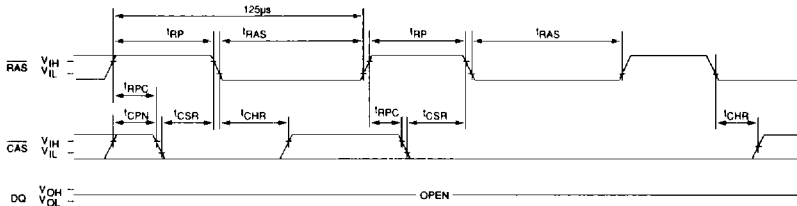
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A7, \overline{OE} ; \overline{WEL} , \overline{WEH} or \overline{WE} = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A7 \overline{WEL} , \overline{WEH} or \overline{WE} , and \overline{OE} = DON'T CARE)

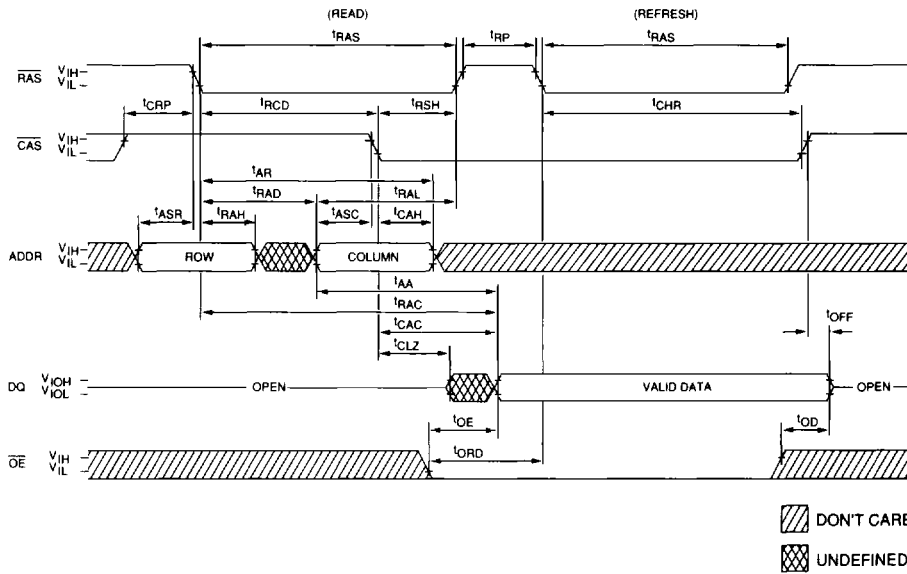


BATTERY BACKUP REFRESH CYCLE
(A0-A7 \overline{WEL} , \overline{WEH} or \overline{WE} , and \overline{OE} = DON'T CARE)



▨ DON'T CARE
▩ UNDEFINED

HIDDEN REFRESH CYCLE ²⁴
(\overline{WEL} , \overline{WEH} or \overline{WE} = HIGH; \overline{OE} = LOW)



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