HD153035F
56-Mbps Read Channel

HITACHI

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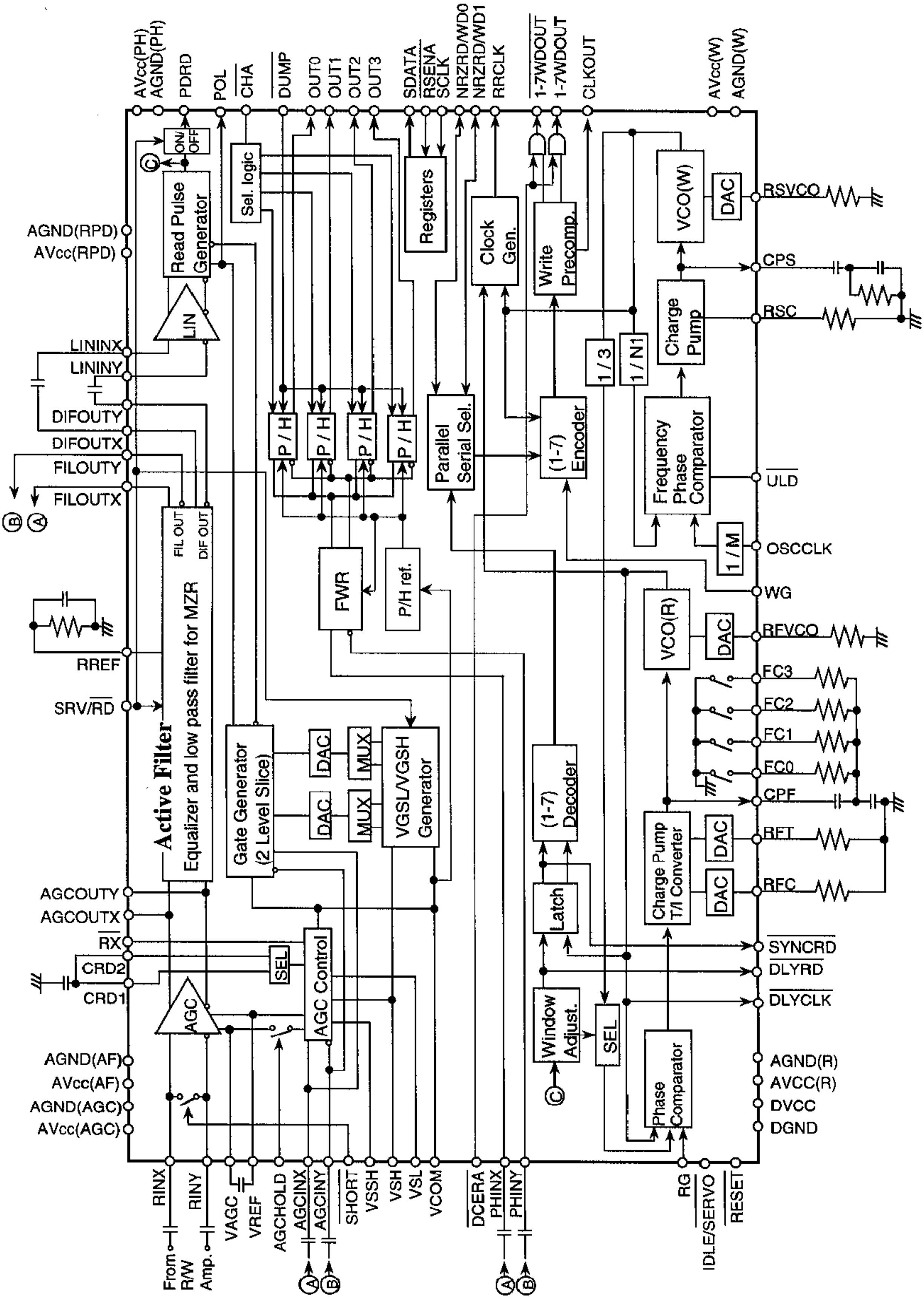
Description

The HD153035F is a 56 Mbps 1-7 ENDEC data separator with built-in read pulse detector, active filter, frequency synthesizer and synchronizer, developed for use in magnetic disk drives. In read mode the HD153035 F decodes the read wave form output from the read/write amplifier into an NRZ signal. In write mode it encodes the NRZ signal output from the controller into a 1-7 RLL code.

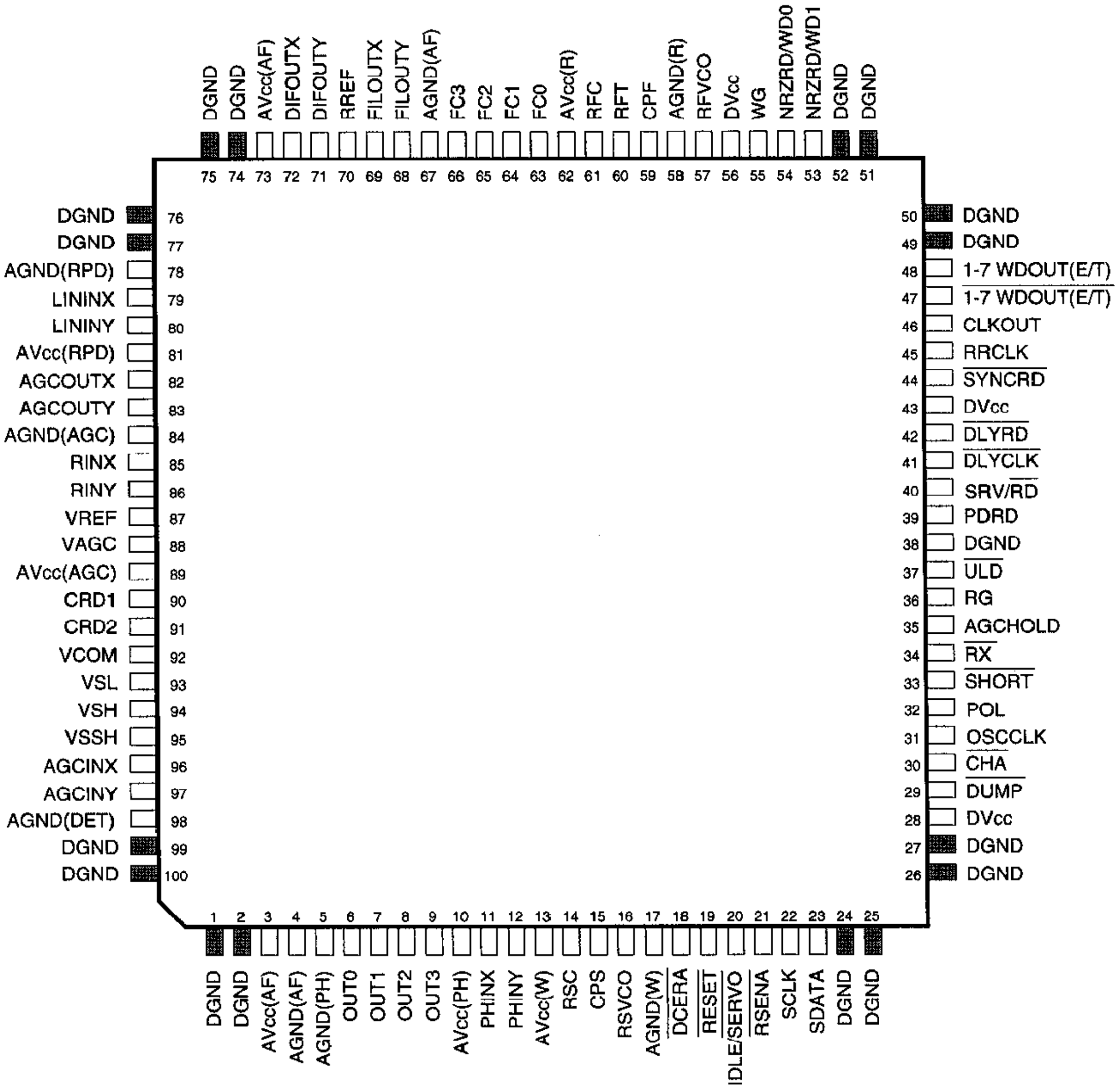
Features

- Maximum NRZ data transfer rate : 56Mbps.
- Data transfer clock frequency : 1.5 data transfer rate (84MHz maximum).
- Settings are micro-computer programmable.
- On-chip frequency synthesizer generates encode clock for writing (f_{MAX}/f_{MIN}=3.98).
- Programmable window centering adjustment and window monitoring functions.
- User-selectable single zone recording or multiple zone recording options. The following are programmable for multiple zone recording : VCO center frequency (192 settings), loop Filter constant (2 settings), charge pump current levels (8 settings), T/I converter output current (8 settings), active filter cutoff frequency for servo and data modes (128 settings).
- Dual-mode phase detector compares both phase and frequency to ensure a wide capture range.
- Separate active filter 7-bit programmable cut-off frequencies.
- Two sets of 4-bit High and Low slice levels for reliable pulse detection .
- 1-7WDOUT outputs are selectable differential pseudo-ECL or TTL pair for high speed transfer without timing error.
- High-speed acquisition can be accomplished with highly stable reproduction by switching between normal-gain and high-gain modes, and by switching loop filter constants.
- VCO oscillation timing capacitor is built in for better noise immunity.
- PLL characteristic frequency and damping rate are defined without 2T-8T (1-7RLL) signal cycle.
- Built-in AGC amplifier for stable reproduction despite varying media and head characteristics.
- Gate generator eliminates incorrect read pulse problems that occur with time-domain filtering with appropriate slice-level setting.
- Head resolution can be increased without incorrect read pulse worries.
- AGC amplifier gain can be set to zero during writing.
- Built-in write phase compensation function with programmable delay time.
- Early or Late write pre-compensation amounts can be programmed independently.
- Built-in active filter with 7-bit programmable cut-off frequency.
- High speed data transfer inputs and outputs are done via complementary TTL output pairs.
- Hi-BiCMOS process achieves high speed with low power dissipation .
- Idle mode and power down functions.
- QFP-100 pin package suitable for compact surface mounting (resin size : 14mm x 14mm)
- Required only a single 5V supply.

2. Block diagram



3. Pin arrangement



(Top view)

4. Pin Functions

Pin Name	Pin No.	Type	Function
RINX RINY	85 86	Differential input	Differential input lines for the signal read from the recording medium.
AGCOUTX AGCOUTY	82 83	Differential output	Differential output lines for monitor from the AGC amplifier. The outputs are open-emitter type and would need ext. 1~10K pulldowns.
CRD1	90	External component required	In reading the normal data, the charge /discharge current output line for the AGC output amplitude detector. Connected to pin 91 (CRD2).
CRD2	91	External component required	External capacitor is needed for AGC output amplitude detector. Connected to pin 90 (CRD1).
VCOM	92	External component required	Reference voltage output line for the AGC output amplitude detector and the Gate generator.
VSL	93	External component required	Voltage input line for setting the low slice level of AGC output amplitude detector. Corresponds to the discharge current threshold. Normally this level is set 67% of the VSH level.
VSH	94	External component required	Voltage input line for setting the high slice level of the AGC output amplitude detector. Corresponds to the charge current threshold
VSSH	95	External component required	Voltage input line for setting the fast attack(high gain) high slice voltage of the AGC output amplitude detector. Normally this level is set to 160% of the VSH level.
VREF	87	Monitor line	Monitor line for the AGC amplifier reference voltage.
VAGC	88	Monitor line	Monitor line for the AGC amplifier gain setting voltage.
FILOUTX FILOUTY	69 68	Differential output	Differential output line from Active Filter. Connect to AGCINX,Y and PHINX,Y through bypass capacitors.
DIFOUTX DIFOUTY	72 71	Differential output	Differential output line from Active Filter. Connect to LININX,Y through bypass capacitors.
AGCINX AGCINY	96 97	Differential input	Differential input lines to the AGC output amplitude detector. Connect to FILOUTX/Y outputs of the AF with bypass capacitors.
RREF	70	External component required	Connect to a resistor and a capacitor to set the reference current for the Active Filter's DAC.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
$\overline{\text{SHORT}}$	33	In (TTL)	When this terminal is 'L', RINX and RINY are shorted together.
$\overline{\text{RX}}$	34	In (TTL)	TTL-level input that switches the AGC loop on or off. When RX signal turn Low to High, AGC gain starts from maximum gain. $\overline{\text{RX}}$ input — AGC loop High — AGC loop closed. Low — AGC loop open.
AGCHOLD	35	In (TTL)	TTL-Level input that locks the AGC amplifier gain. When AGCHOLD goes High the gain is locked at its immediately preceding value.
SRV/$\overline{\text{RD}}$	40	In(TTL)	"H":Servo Mode,"L":Read Mode. In the servo mode ,"CFCB" register set the A/F's cutoff frequency and VGSLB register set the gate slice low level. In the read mode ,"CFCA" register set the A/F's cutoff frequency and VGSLA register set the gate lowslice level.
PHINX PHINY	11 12	In	Differential inputs for the servo Peak/Hold circuit.
OUT0~ OUT3	6,7, 8,9	External component required	Connect to external capacitors for servo peak/hold.
$\overline{\text{CHA}}$	30	In (TTL)	Input pin of the control signal of Peak/hold circuit(TTL level) Position signal is sampled by $\overline{\text{CHA}}$="L"
$\overline{\text{DUMP}}$	29	In (TTL)	Input pin of the discharge control signal of Peak/Hold circuit. TTL level, $\overline{\text{DUMP}}$="L" is for discharge.
LININX LININY	79 80	Differential input	Differential input lines for the zero-crossing comparator. Normally connect to DIFOUTX/Y of the active filter with bypass capacitors.
PDRD	39	Out(TTL)	Output line for the data read from disk as reshaped into digital data by the read pulse detector. When SRV/$\overline{\text{RD}}$(pin40) goes high, PDRD outputs read data pulse. When SRV/$\overline{\text{RD}}$ goes low, PDRD is disable.
POL	32	Out(TTL)	Output pin of the polarity signal for read signal from disk drive.
RFVCO	57	External component required	Connect to a resistor to set the center frequency of the VCO in the decode clock generator's VFO.
RFC	61	External component required	Connect a resistor to set the charge pump output current for the decode clock generator's VFO. The charge pump current level is set by GAC[5:3] and CPO[4:0] registers.

Pin Functions (cont)

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Type</th><th>Function</th></tr>
<tr><td>RFT</td><td>60</td><td>External component required</td><td>Connect a resistor to set the T/I converter's sampling feedback gain to 1(nominal). The T/I converter's output current is determined by this resistor, and registers VFC[4:0] & GAC[2:0] & TIO[4:0].</td></tr>
<tr><td>CPF</td><td>59</td><td>External component required</td><td>Current output to the external loop filter.</td></tr>
<tr><td>FC0
FC1
FC2
FC3</td><td>63
64
65
66</td><td>External component required</td><td>Connect to a loop filter resistor to set the attenuation ζ of the PLL. Each line is grounded through an MOS switch is selected by PLL gain mode and bit 6 of register GAC.
<table>
<tr><th></th><th></th><th colspan="4">Pin</th></tr>
<tr><th>Bit 6 of register GAC</th><th>PLL gain mode</th><th>FC0</th><th>FC1</th><th>FC2</th><th>FC3</th></tr>
<tr><td rowspan="2">" 0 "</td><td>High</td><td>ON</td><td>ON</td><td>OFF</td><td>OFF</td></tr>
<tr><td>Normal</td><td>ON</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
<tr><td rowspan="2">" 1 "</td><td>High</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td></tr>
<tr><td>Normal</td><td>OFF</td><td>OFF</td><td>ON</td><td>OFF</td></tr>
</table></td></tr>
<tr><td>RG
(Read gate)</td><td>36</td><td>In(TTL)</td><td>High level at the input selects read mode. This signal switches the clock for counters and internal circuits, and begins phase synchronization of the decode clock generator's VFO with the 1-7 decode data.</td></tr>
<tr><td>$\overline{\text{DLYCLK}}$</td><td>41</td><td>Out(TTL)</td><td>Monitor pin(TTL level) for Window adjustment. This pin allows the VCO clock signal output by the PLL circuit to be monitored. Contact Hitachi,Ltd. for special instructions if use of this function is required.</td></tr>
<tr><td>$\overline{\text{DLYRD}}$</td><td>42</td><td>Out(TTL)</td><td>Monitor pin(TTL level) for Window adjustment. This pin allows the read data signal output from the window adjustment circuit to be monitored. Contact Hitachi,Ltd. for special instructions if use of this function is required.</td></tr>
<tr><td>$\overline{\text{SYNCRD}}$</td><td>44</td><td>Out(TTL)</td><td>Monitor pin(TTL level) for Window adjustment. This pin outputs the read data outputs the read data input to the PLL block latched by the VCO clock. Contact Hitachi,Ltd. for the special instructions if use of this function is required.</td></tr>
<tr><td>RSVCO</td><td>16</td><td>External component required</td><td>Connect a resistor to set the center frequency of the VCO in the encode clock generator's frequency synthesizer.</td></tr>
<tr><td>CPS</td><td>15</td><td>External component required</td><td>Current output to an external loop filter.</td></tr>
</table>

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
RSC	14	External component required	Connect a resistor to set the charge pump output current for the encode clock generator's frequency synthesizer.
OSCCLK (Oscillator clock)	31	In(TTL)	Clock synthesizer's reference clock input. The frequency synthesizer generates encode clock frequencies from the input on this line. Data writing is synchronized with the encode clock. When not reading data, the decode clock generator's VFO is also synchronized with frequency 1.5 times the data transfer rate.
$\overline{\text{ULD}}$ (Unlock detect)	37	Out(TTL)	Error output from the encode clock generator's frequency synthesizer. ULD goes low to indicate that the PLL in the encode clock generator's frequency synthesizer has lost lock. The disk controller should immediately halt the write operation. Data must be written again from the beginning.
WG	55	In(TTL)	Write gate signal input. Set this pin high during writing.
NRZRD/WD1	53	In/Out (TTL)	I/O pin of NRZ signal. This pin is effective only in the case of parallel transferring. NRZ Data select bit 7 of register($h8) controls parallel/serial. (When this bit is " H" , NRZ mode is parallel)
NRZRD/WD0	54	In/Out (TTL)	I/O pin of NRZ signal. In the serial transfer mode, only this pin is effective. NRZ Data select bit 7 of register($h8) controls parallel/ serial. (When this bit is " L" , NRZ mode is serial)
RRCLK	45	Out(TTL)	Read reference clock output(TTL level). At read time,this pin provides a clock which is synchronized with the converted NRZRD signal. This controller should read NRZRD by this clock. Other than read mode, reference clock is provided to disk controller.
1-7WDOUT $\overline{\text{1-7WDOUT}}$ (Write Data outputs)	48 47	Out (TTL/ECL)	1-7 RLL Write Data Differential Output. Pseudo ECL/TTL are available by bit 6 of register"$hD". When this bit is "H", these outputs are TTL. When this bit is "L", these outputs are ECL.These pin provide the 1-7WDOUT write data that goes to the Read/Write amplifier after the write pre-compensation. When WG goes high, 1-7WDOUT pin are output mode.
CLKOUT	46	Out(TTL)	This clock is for the external write pre-compensation in the Write mode. This clock(TTL level) is synchronized with 1-7WD.
$\overline{\text{DCERA}}$	18	In(TTL)	Input pin for the DC erase. When this pin is "L", 1-7WDOUT (pin#48) is "L" and $\overline{\text{1-7WDOUT}}$ (pin#47) is "H".
$\overline{\text{RESET}}$	19	In(TTL)	Low input initializes internal circuits. Drive this line low at power-up. Low input also locks the two built-in VCOs to their center frequencies. Keep this line high during normal operation.
$\overline{\text{RSENA}}$	21	In(TTL)	This active low input selects the device and enables the serial port.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
SCLK	22	In(TTL)	This is the serial clock sent in by the hard disk controller or other ASIC device. When the serial port is not enabled, this clock line should be driven low. For either read or write transfer, a 16 clock burst is required for proper operation. Data is latched in during write or sent out during read at the rising edge of the SCLK.
SDATA	23	In/Out (TTL)	Data is transmitted in 16-bit packet MSB first. The first 2 bits determine the read or write mode, the next bit is "Don't Care", the next 4 bits are for the register address, followed by 1 "Don't Care" bit, then the last 8 bits are for the Write or Read Data.
IDLE/$\overline{\text{SERVO}}$	20	In(TTL)	The input is used in combination with the two Mode bits in the PCN register to reduce power consumption in the Idle mode. When PCN= 00, device is in the R/W normal mode, all circuits are ON. When PCN = 11, device is in the Sleep mode, all circuits are OFF except the I/O and logic. When PCN = 10, then depending on the logic level of the IDLE/$\overline{\text{SERVO}}$ pin; if it is High, then chip is in the Idle mode and all circuits are OFF except for the I/O, logic, and the bias CKT's; if it is Low, then the device is in the Servo mode and the I/O, logic, bias CKT's, AGC, active filter, Read Pulse Detector, and Peak/Hold will be ON with only the RD PLL and the WR PLL being OFF.
DVcc	28, 43, 56	Power	Digital Vcc power supply.
DGND	1, 2, 24,25,26, 27, 38, 49, 50, 51, 52, 74, 75, 76, 77, 99,100	Ground	Digital ground.
AVcc(AGC)	89	Power	Analog Vcc power supply for AGC.
AGND(AGC)	84	Ground	Analog ground for AGC.
AGND(DET)	98	Ground	Analog ground for AGC control circuit
AVcc(AF)	3, 73	Power	Analog Vcc power supplies for active filter.
AGND(AF)	4, 67	Ground	Analog ground for active filter.
AVcc(RPD)	81	Power	Analog Vcc power supply for read pulse detector.
AGND(RPD)	78	Ground	Analog ground for read pulse detector.
AVcc(PH)	10	Power	Analog Vcc power supply for peak hold.
AGND(PH)	5	Ground	Analog ground for peak hold.
AVcc(R)	62	Power	Analog Vcc power supply for synchronizer.
AGND(R)	58	Ground	Analog ground for synchronizer.
AVcc(W)	13	Power	Analog Vcc power supply for synthesizer.
AGND(W)	17	Ground	Analog ground for synthesizer.

5. Registers

The HD153035F has 16 addressable 8-bits registers that control the center frequency of the decode clock generator's VFO and the frequency of the encode clock generator's frequency synthesizer, control the synthesizer's gain, control the read data pulse width and its polarity, control the synchronizer's gain and offset, adjust the decode window, apply the early/late write precompensation, control the prescaling value, adjust the active filter's cut-off frequency, and controls various functions.

Address register value MSB LSB	Name	Abbreviation
0 0 0 0	VCO center frequency control register	VFC register
0 0 0 1	RD-PLL Gain control register Synchronizer loop filter gain control bit. Synthesizer operating mode control bit	GAC register RFCA bit SPSYNT bit
0 0 1 0	RD-PLL Charge Pump Offset control register Write pre-compensation delay control register (L)	CPO register WPL register
0 0 1 1	RD-PLL T/I offset control register Write precompensation delay control register (S)	TIO register WPS register
0 1 0 0	Window adjustment register (0.67ns typ. /step) Window fine adjustment register(0.25ns typ. /step)	WAJ register WFA register
0 1 0 1	AGC Mode control bit (FAST / SLOW) Read data (PDRD) polarity control register Read data (PDRD) pulse width control register WR-PLL Gain control register	AGS bit RDSEL register PW register SGC register
0 1 1 0	Prescaler of WR-PLL control register	PSC register
0 1 1 1	AF cut-off frequency control register (for Read)	CFCA register
1 0 0 0	NRZ Data 1bit - serial / 2-bit parallel select bit AF cut-off frequency control register (for Servo)	NRZM bit CFCB register
1 0 0 1	Unlock detect gain control register (for WR-PLL) Boost level control register	ULD register BLC register
1 0 1 0	Boost enable bit at servo mode High pass filter cut-off frequency control register (for Read)	SRVBE bit HPCA register
1 0 1 1	High pass filter cut-off frequency control register (for Servo)	HPCB register
1 1 0 0	Gate generator's High-slice level control register (for Read) Gate generator's Low-slice level control register (for Read)	VGSHA register VGSLA register
1 1 0 1	1-7 WDOUT output type control bit (ECL / TTL) Write pre-compensation delay control register (E) Write pre-compensation delay control register (N)	WDM bit WPE register WPN register
1 1 1 0	AGCOUT enable control bit Power management control register Gate generator's Low-slice level control register (forServo)	AOE bit PCN register VGSLB register
1 1 1 1	Test Mode control register	MDC register

6. Register Descriptions

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Register Functions
0 0 0 0	▨ VFC7	VFC6	VFC5	VFC4	VFC3	VFC2	VFC1	VFC0	VFC: controls the center frequency of the WR-PLL & RD-PLL.
0 0 0 1	SPSYNT	RFCA	▨ GAC5	GAC4	GAC3	▨ GAC2	GAC1	GAC0	GAC: controls the RD-PLL's T/I and Charge Pump gain. RFCA: selects the resistor sets of the RD-PLL's loop filter SPSYNT: controls the WR-PLL's operating mode
0 0 1 0	WPL2	WPL1	WPL0	▨ CPO4	CPO3	CPO2	CPO1	CPO0	CPO: controls the Off-Set of the RD-PLL's Charge Pump circuit. WPLL: sets the write precompensation delays. (L)
0 0 1 1	WPS2	WPS1	WPS0	▨ TIO4	TIO3	TIO2	TIO1	TIO0	TIO: controls the Off-Set of the RD-PLL's T/I converter. WPLS: sets the write precompensation delays. (S)
0 1 0 0	WFA2	WFA1	WFA0	▨ WAJ4	WAJ3	WAJ2	WAJ1	WAJ0	WFA: fine adjusts data window. WAJ: adjusts data window.
0 1 0 1	AGCSEL	RDSEL1	RDSEL0	PW1	PW0	▨ SGC2	SGC1	SGC0	AGCSEL: sets AGC mode Fast or Slow. RDSEL: controls PDRD pulse polarity PW: controls PDRD pulse width. SGC: sets the WR-PLL gain.
0 1 1 0	0	PSC6	PSC5	PSC4	PSC3	▨ PSC2	PSC1	PSC0	PSC: sets the WR-PLL prescaler's counter value.
0 1 1 1	0	▨ CFCA6	▨ CFCA5	▨ CFCA4	▨ CFCA3	▨ CFCA2	▨ CFCA1	▨ CFCA0	CFCA: controls Read Mode Active Filter's Cut-Off frequency.
1 0 0 0	NRZM	CFCB6	CFCB5	CFCB4	CFCB3	CFCB2	CFCB1	CFCB0	NRZM: selects 1bit or 2bits NRZ data transfer. CFCB: controls Servo Mode Active Filter's Cut-Off frequency.
1 0 0 1	TSTBF	ULD1	ULD0	BLC4	BLC3	BLC2	BLC1	BLC0	ULD: sets unlock detect period. BLC: controls AF's Boost level.
1 0 1 0	SRVBE	0	0	HPCA4	HPCA3	HPCA2	HPCA1	HPCA0	SRVBE: controls filter boost on / off (at servo mode) HPCA: controls high-pass filter cut-off frequency(for Read)
1 0 1 1	TSTPD	0	0	HPCB4	HPCB3	HPCB2	HPCB1	HPCB0	HPCB: controls high-pass filter cut-off frequency(for Servo)
1 1 0 0	VGSHA3	VGSHA2	VGSHA1	VGSHA0	VGSLA3	VGSLA2	VGSLA1	VGSLA0	VGSHA: sets high-slice level of the gate generator(for Read) VGSLA: sets low-slice level of the gate generator(for read)
1 1 0 1	0	WDM	WPN2	WPN1	WPN0	WPE2	WPE1	WPE0	WDM: selects output type of 1-7 WDOUT (TTL / pseudo ECL) WPE / WPN: sets the write precompensation delays. (E/N)
1 1 1 0	AOE	0	PCN1	PCN0	VGSLB3	VGSLB2	VGSLB1	VGSLB0	AOE: AGCOUTX/Y outputs enable control PCN: power saving control register for the analog modules. VGSLB: sets low-slice level of the gate generator(for Servo)
1 1 1 1	TEST	0	MDC5	MDC4	MDC3	MDC2	MDC1	MDC0	MDC: TEST mode control register.

▨ : these bits are set to "1" during reset time.

Register Descriptions (cont)

VCO Center Frequency Control register (VFC)

Address $h0 (at write = "C0" hex, at read = "80" hex),

VFC Register

MSB							LSB
▨ D7	D6	D5	D4	D3	D2	D1	D0

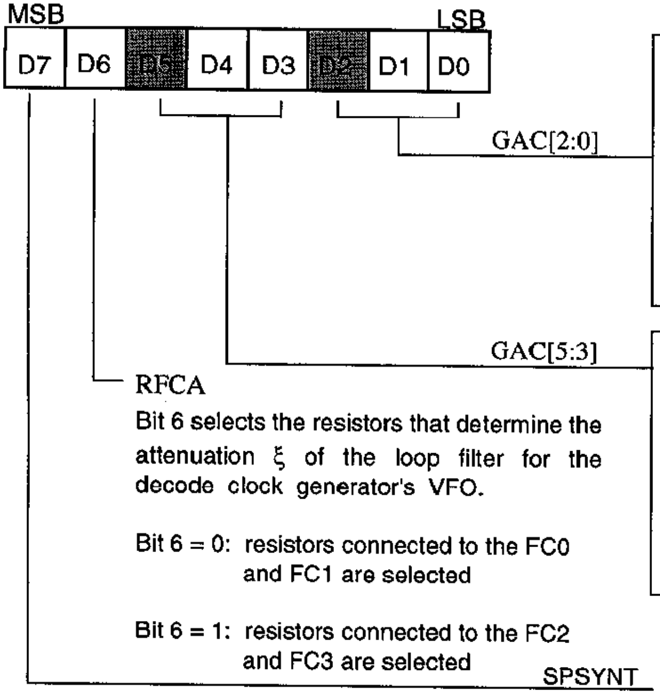
VFC register is 8 bits long.
This register is used in multiple-zone recording to set the center frequency of the decode clock generator's VCO, the T/I converter's reference current, and the oscillation frequency of the encode clock generator's frequency synthesizer. Bit D7 is cleared when reset pin is asserted.

Resistors connected to the RFVCO and RSVCO lines set these values for the minimum data transfer rate. The VFC register raises these values in step of 1.56%, permitting 192 settings up to a maximum transfer rate 3.98 times of the minimum rate.

0 1 0 0 0 0 0 0	Minimum transfer rate (reference rate)
.	
.	
.	
1 1 1 1 1 1 1 1	Maximum transfer rate (3.98 times speed)

Gain Control Register (GAC) = RFCA, GAC[5:0] for Read PLL synchronizer

Address $h1 (at write = "C2" hex, at read = "82" hex)



Bits 2 to 0: Select the output current of the T/I converter to vary the gain. Eight gain settings are possible.

0 0 0	Minimum gain (L=0)
.	
.	
.	
1 1 1	Maximum gain (L=7)

Bits 5 to 3: Select the output current of the Charge pump to vary the gain. Eight gain settings are possible.

0 0 0	Minimum gain (P=1)
.	
.	
.	
1 1 1	Maximum gain (P=8)

RFCA
Bit 6 selects the resistors that determine the attenuation ξ of the loop filter for the decode clock generator's VFO.

Bit 6 = 0: resistors connected to the FC0 and FC1 are selected

Bit 6 = 1: resistors connected to the FC2 and FC3 are selected

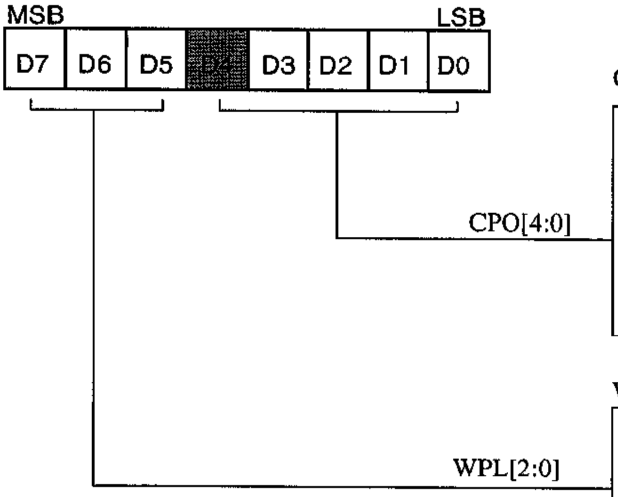
SPSYNT: Synthesizer operating mode control bit

0 : 56Mbps mode
1 : 50Mbps mode

Register Descriptions (cont)

Charge Pump Offset Control Register (CPO), Write pre-compensation delay control Register (WPLL)

Address $h2 (at write = "C4" hex, at read = "84" hex)



CPO register

Cancel the offset current of the charge pump.

0 0000	(-) offset < - 32% >	
•		
1 0000	zero offset	(2% steps)
•		
1 1111	(+) offset < + 30% >	

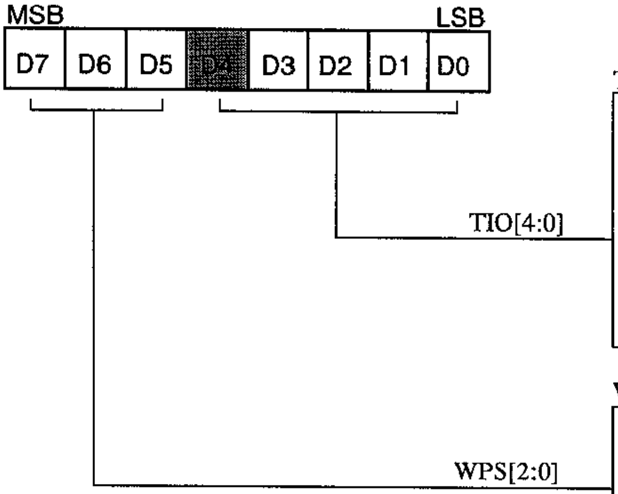
WPL register

sets the write precompensation delay for the L part of WP-table.

0 0 0 : Early
•
• (0.55ns/step typical)
•
1 1 1 : Late

T/I Offset Control Register (TIO) , Write pre-compensation delay control Register (WPLS)

Address $h3 (at write = "C6" hex, at read = "86" hex)



TIO register

Cancel the offset current of the T/I converter.

0 0000	(-) offset < - 40% >
•	
1 0000	zero offset (2.5% steps)
•	
1 1111	(+) offset < + 37.5% >

WPS register

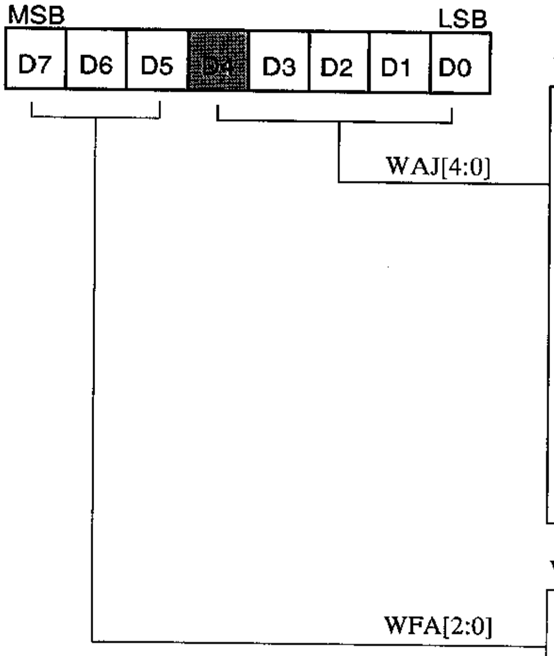
sets the write precompensation delay for the S part of WP-table.

0 0 0 : Early
•
• (0.55ns/step typical)
•
1 1 1 : Late

Register Descriptions (cont)

Window Fine Adjust Register WFA[2:0] and Window Adjust Register WAJ[4:0]

Address $h4 (at write = "C8" hex, at read = "88" hex)



WAJ register

This register adjusts the setting of the window. Window centering can be adjusted to 32 positions by an on-chip delay line. Bit D4 will always be cleared during reset. The microcontroller can center the window automatically with firmware by changing these values.

0 0000
.
. (-) negative delay adjustment
0 1111
1 0000 Center (0.67ns/step typical)
1 0001
. (+) positive delay adjustment
.
1 1111

WFA register

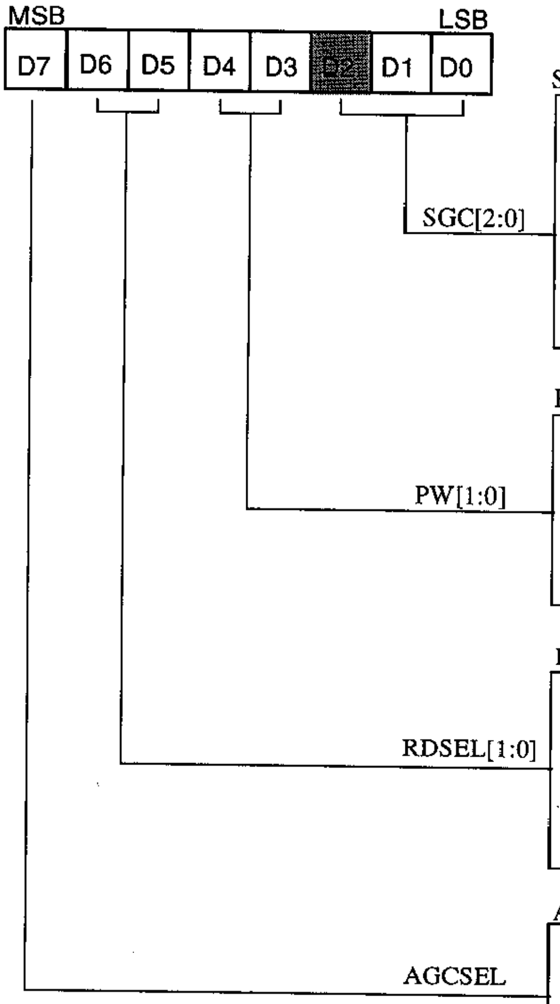
This register adjusts eight setting of the window fine adjust circuit. The register setting adds fine delay to the Window adjustment circuit.

0 1 0	- 2 delay	(- 0.50 ns typical)
0 0 1	- 1 delay	(- 0.25 ns typical)
0 0 0	Center	(0ns)
1 0 1	+ 1 delay	(+ 0.25 ns typical)
1 1 0	+ 2 delay	(+ 0.50 ns typical)

Register Descriptions (cont)

RD-PLL Gain Control Register (SGC), Read data Pulse Width Control Register (PW), Read data Polarity Control Register (RPC) and AGC Mode Selects bit (AGS)

Address $h5 (at write = "CA" hex, at read = "8A" hex)



SGC register

Select the output current of the RD-PLL's Charge pump. Eight settings are possible in relation to the reference current set by resistor RSC to determine the minimum transfer rate.

0 0 0 Nc=0 Reference current times 1.0

•

•

1 1 1 Nc=7 Reference current times 1.875

PW register

Set the pulse width of PDRD signal output line. Four settings are possible with 2.4ns per step.

0 0	Minimum pulse width
0 1	(2.4ns/step typical)
1 0	
1 1	Maximum pulse width

RDSEL register

RDSEL0 selects PDRD signal polarity

0	Signal value '1' = 'H"
1	Signal value '1' = 'L"

RDSEL1 composite POLARITY signal

0	Signal value '1' = composite
1	Signal value '1' = non-composite

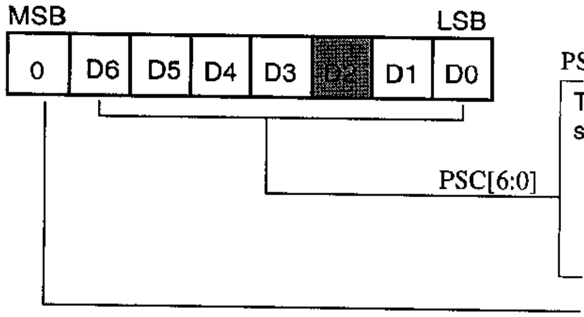
AGCSEL bit

This bit selects discharge current to the AGC capacitor.

0	Ich/Idisch = 5 to 1
1	Ich/Idisch = 5 to 0.1

Prescaler of the Synthesizer Control Register (PSC) [M value]

Address $h6 (at write = "CC" hex, at read = "8C" hex)



PSC Register

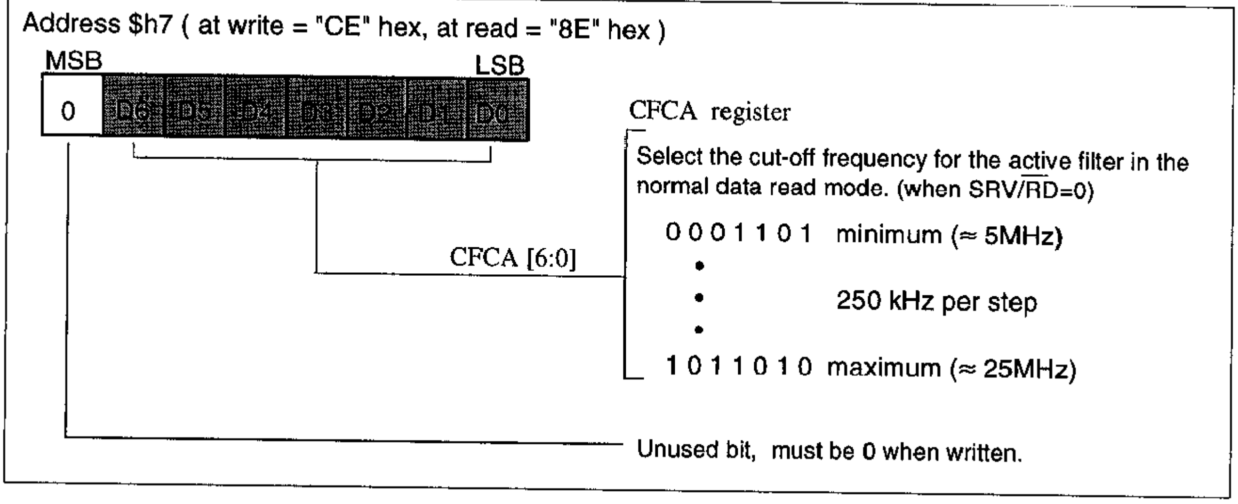
This register controls the prescale counter's value of the synthesizer. The OSCCLK signal is divided by 2 to 127.

0 0 0 0 0 1 0	divided by 2
.	
.	
1 1 1 1 1 1 1	divided by 127

Unused bit, must be 0 when written.

Register Descriptions (cont)

Read Mode AF Cut-Off Frequency Register (CFCA)



Address $h7 (at write = "CE" hex, at read = "8E" hex)

CFCA register

Select the cut-off frequency for the active filter in the normal data read mode. (when SRV/$\overline{\text{RD}}$=0)

0 0 0 1 1 0 1 minimum (≈ 5MHz)

•

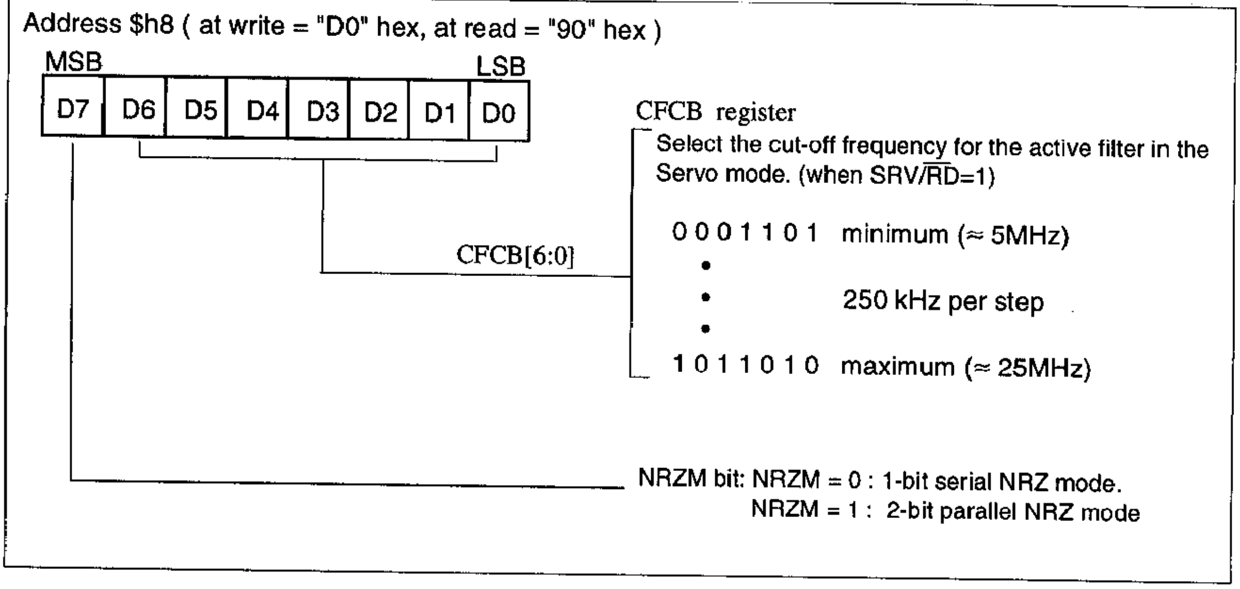
• 250 kHz per step

•

1 0 1 1 0 1 0 maximum (≈ 25MHz)

Unused bit, must be 0 when written.

NRZ Data mode select bit (NRZM), Servo Mode AF Cut-Off Frequency Register (CFCB)



Address $h8 (at write = "D0" hex, at read = "90" hex)

CFCB register

Select the cut-off frequency for the active filter in the Servo mode. (when SRV/$\overline{\text{RD}}$=1)

0 0 0 1 1 0 1 minimum (≈ 5MHz)

•

• 250 kHz per step

•

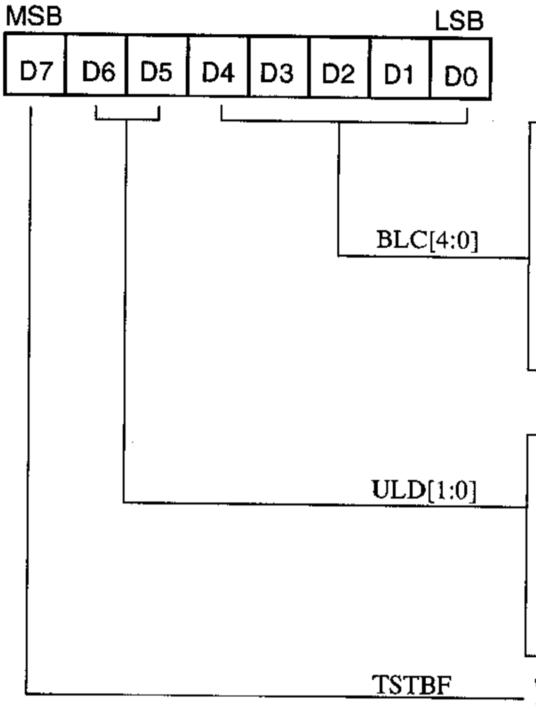
1 0 1 1 0 1 0 maximum (≈ 25MHz)

NRZM bit: NRZM = 0 : 1-bit serial NRZ mode.
NRZM = 1 : 2-bit parallel NRZ mode

Register Descriptions (cont)

Unlock Detect Register (ULD) and Boost Level Control Register (BLC)

Address $h9 (at write = "D2" hex, at read = "92" hex)



BLC register

This register sets the boost amplifier's gain of the active filter for the equalization.

0 0000 Minimum gain

•

•

1 1111 Maximum gain

ULD register

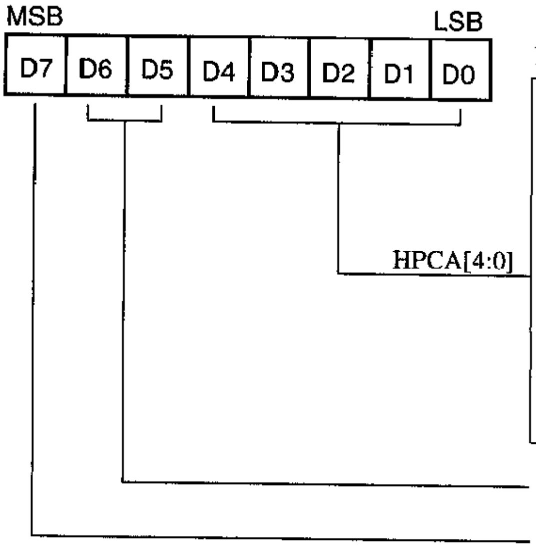
Select the unlocked detect gain for the RD-PLL synthesizer to activate the ULD~ output when unlock condition occurs.

0 0 : 2 OSCCLK
0 1 : 4 OSCCLK
1 0 : 6 OSCCLK
1 1 : 8 OSCCLK

When this bit sets "1" , $\overline{\text{SYNCRD}}$(pin 44), $\overline{\text{DLYRD}}$(pin 42), DLYCLK(pin 41) are output mode. Normaly this bit sets "0".

High-Pass Filter Cutoff Frequency Control Register (HPCA)

Address $hA (at write = "D4" hex, at read = "94" hex)



HPCA Register

This register controls the cutoff frequency of the high-pass filter in the active filter circuit during normal data read mode. (when SRV/$\overline{\text{RD}}$=0)The register changes it by 6.25% step.

0 1111 Maximum cutoff frequency (+ 193.75%)

•

•

•

0 0001

0 0000 Center cutoff frequency

1 0111 (100% depend on CFC)

•

•

1 0000 Minimum cutoff frequency (50%)

Unused bit, must be 0 when written.

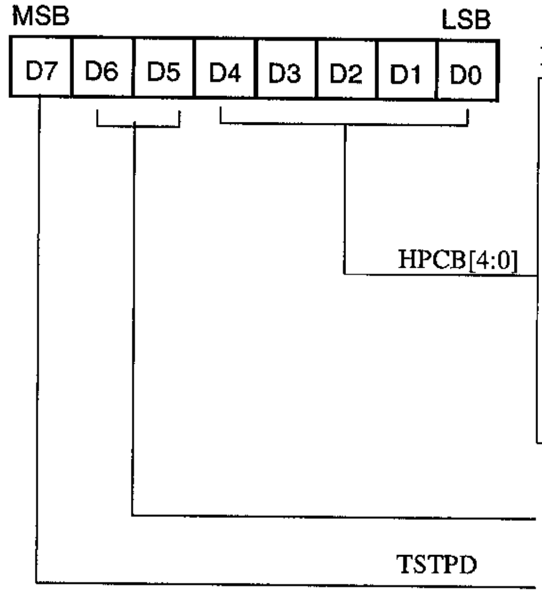
This bit controls filter boost function on and off at servo mode.

" 1" : No boost at servo mode
" 0" : Boost at servo mode
(boost level : the same level at read mode)

Register Descriptions (cont)

High-Pass Filter Cutoff Frequency Control Register (HPCB)

Address $hB (at write = "D6" hex, at read = "96" hex)



HPCB Register

This register controls the cutoff frequency of the high-pass filter in the active filter circuit during servo mode. (when SRV/$\overline{\text{RD}}$=1)The register changes it by 6.25% step.

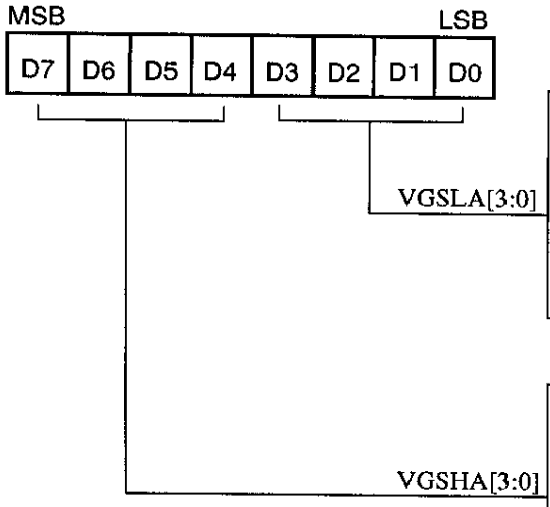
0 1111 Maximum cutoff frequency (+ 193.75%)
•
•
0 0001
0 0000 Center cutoff frequency
1 0111 (100% depend on CFC)
•
•
1 0000 Minimum cutoff frequency (50%)

Unused bit, must be 0 when written.

When this bit sets "1", PDRD output is enable.

High-Slice Level Register (VGSHA), Low-Slice Level Register (VGSLA)

Address $hC (at write = "D8" hex, at read = "98" hex)



VGSLA Register

These are input to the internal DAC using VCOM as reference source to generate the Low-Slice level for the Pulse detection circuit in the read mode. (when SRV/$\overline{\text{RD}}$= "L")

0 0 0 0 Minimum high-slice level (0% of V_{peak})
.
.
1 1 1 1 Maximum high-slice level (100% of V_{peak})

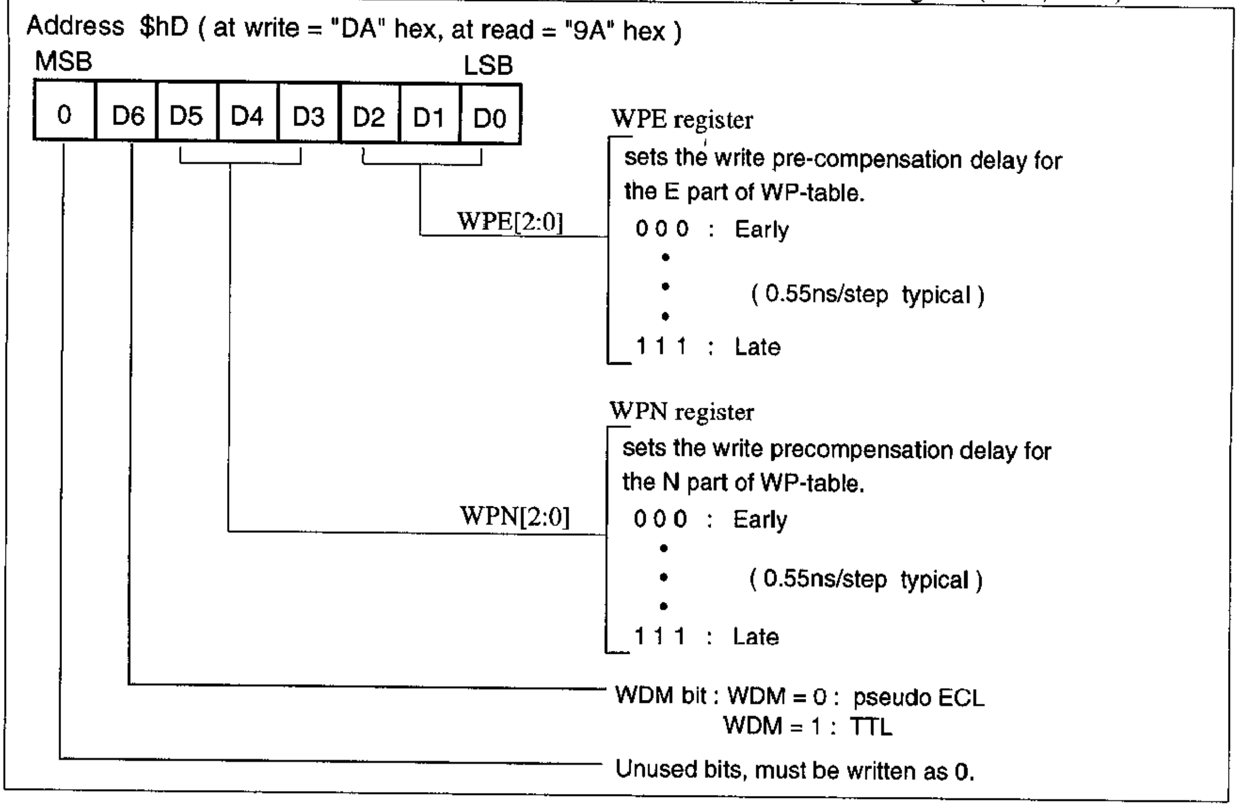
VGSHA Register

These are input to the internal DAC using VCOM as reference source to generate the programmable High-Slice level for the Pulse detection circuit used in the read and servo mode.

0 0 0 0 Minimum high-slice level (0% of V_{peak})
.
.
1 1 1 1 Maximum high-slice level (100% of V_{peak})

Register Descriptions (cont)

1-7WDOUT output type select bit (WDM), Write pre-compensation delay control register (WPE, WPN)



WPE register

sets the write pre-compensation delay for the E part of WP-table.

0 0 0 : Early
•
• (0.55ns/step typical)
•
1 1 1 : Late

WPN register

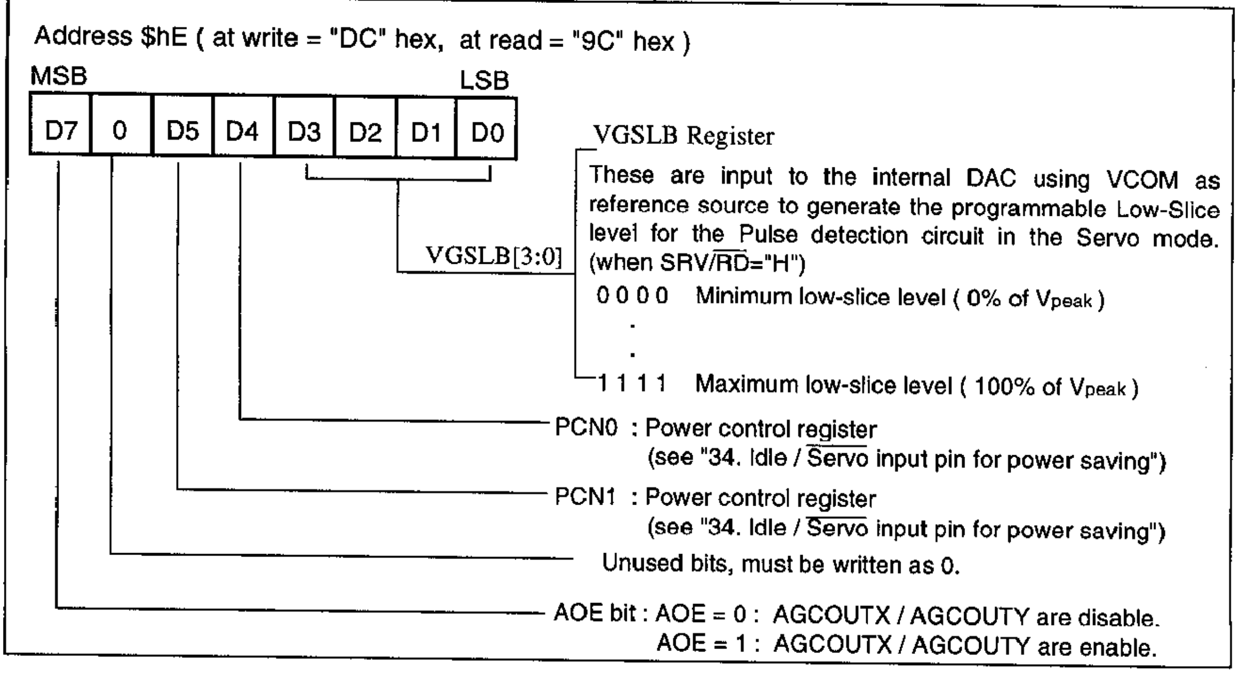
sets the write precompensation delay for the N part of WP-table.

0 0 0 : Early
•
• (0.55ns/step typical)
•
1 1 1 : Late

WDM bit : WDM = 0 : pseudo ECL
WDM = 1 : TTL

Unused bits, must be written as 0.

AGCOUTX/Y enable control bit (AOE), Power Control Register (PCN)



VGSLB Register

These are input to the internal DAC using VCOM as reference source to generate the programmable Low-Slice level for the Pulse detection circuit in the Servo mode. (when SRV/$\overline{\text{RD}}$="H")

0 0 0 0 Minimum low-slice level (0% of V_{peak})
.
.
1 1 1 1 Maximum low-slice level (100% of V_{peak})

PCN0 : Power control register
(see "34. Idle / $\overline{\text{Servo}}$ input pin for power saving")

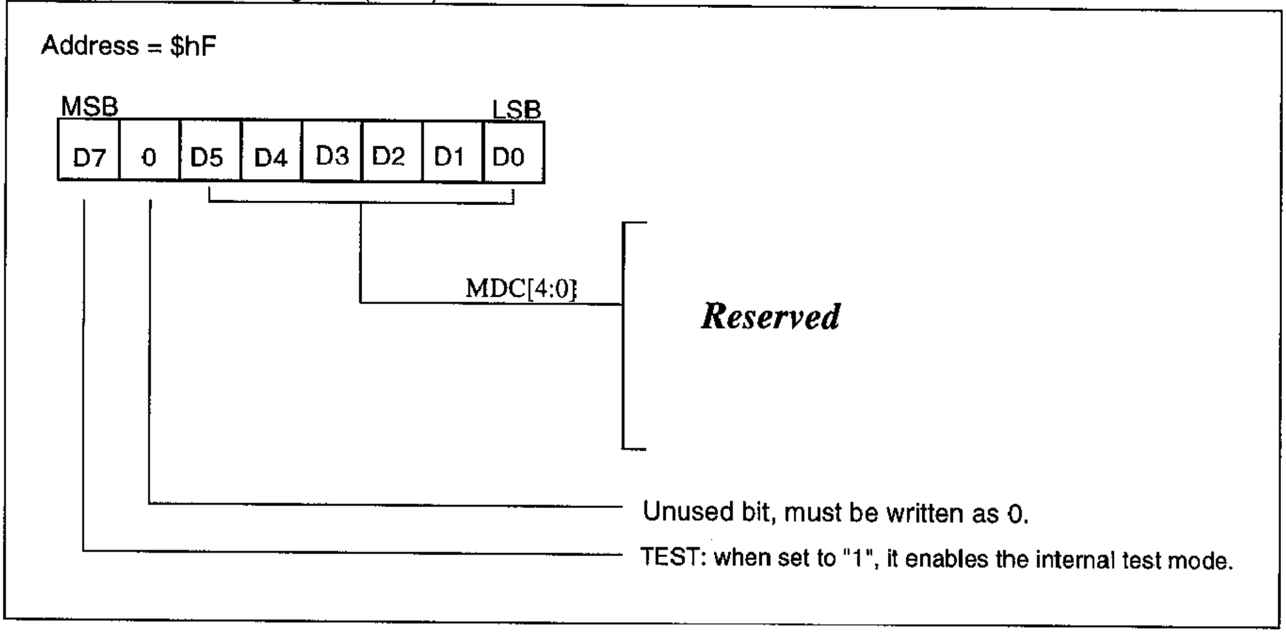
PCN1 : Power control register
(see "34. Idle / $\overline{\text{Servo}}$ input pin for power saving")

Unused bits, must be written as 0.

AOE bit : AOE = 0 : AGCOUTX / AGCOUTY are disable.
AOE = 1 : AGCOUTX / AGCOUTY are enable.

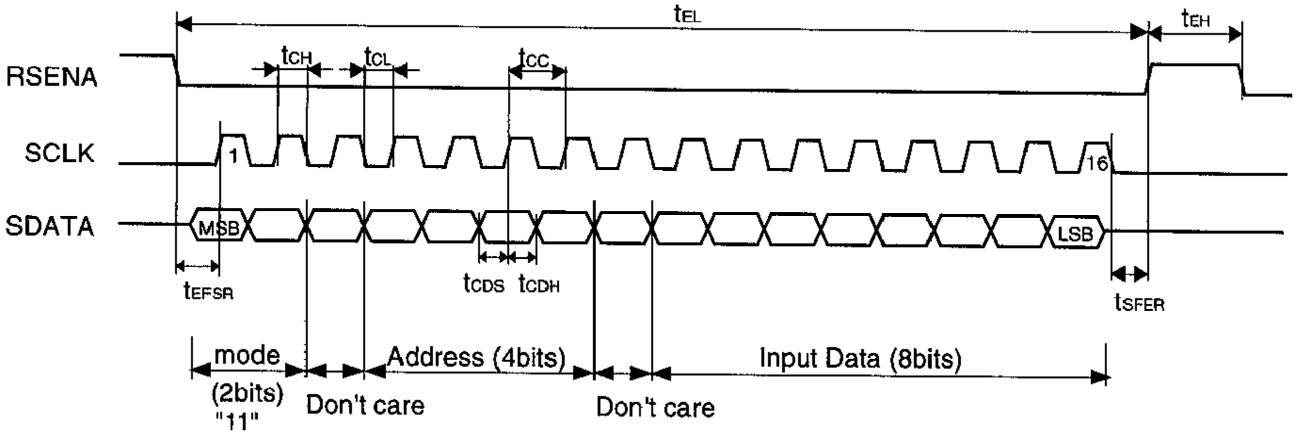
Register Descriptions (cont)

Test Mode Control Register (MDC)



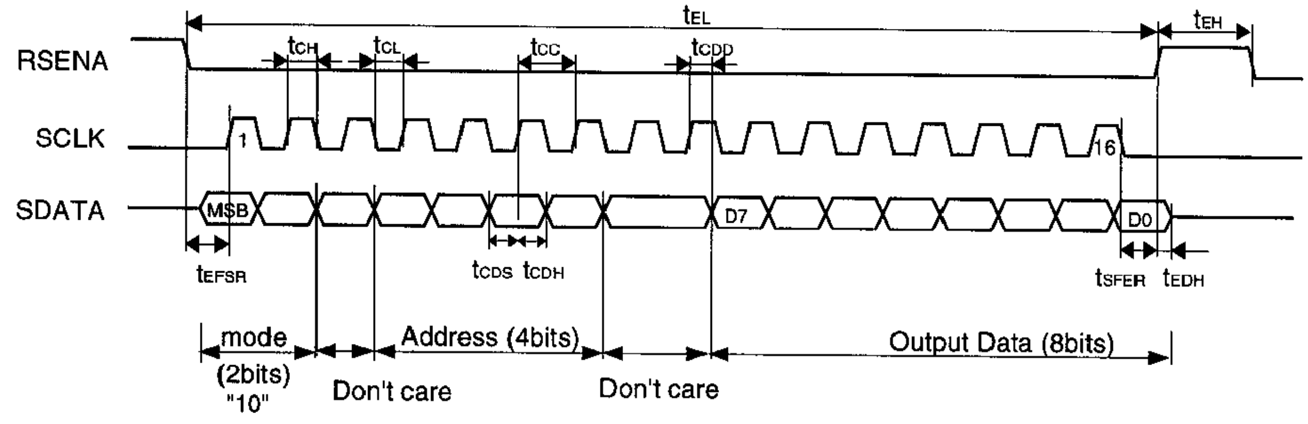
7. Read/Write timing of the control registers

< Write >



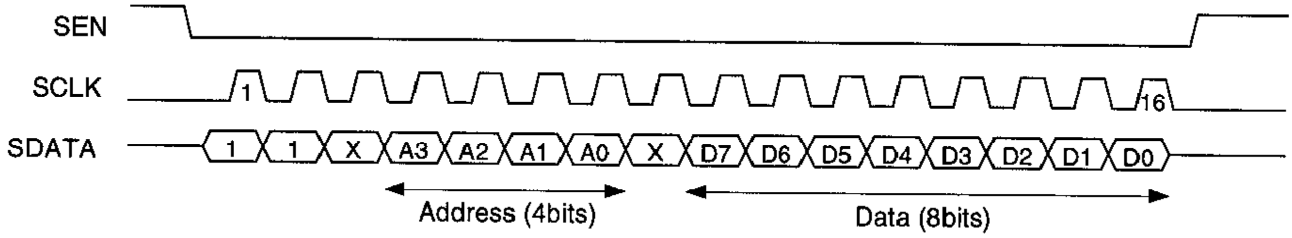
Read/Write timing of the control registers (cont)

< Read >

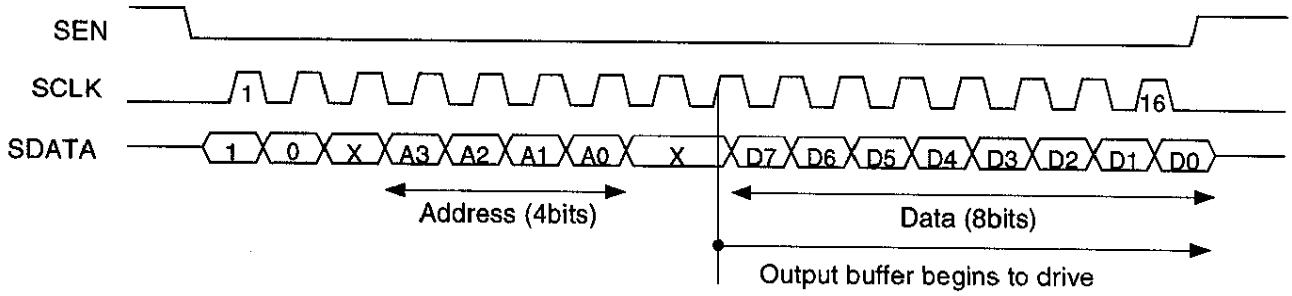


8. Write and read registers

Write to register

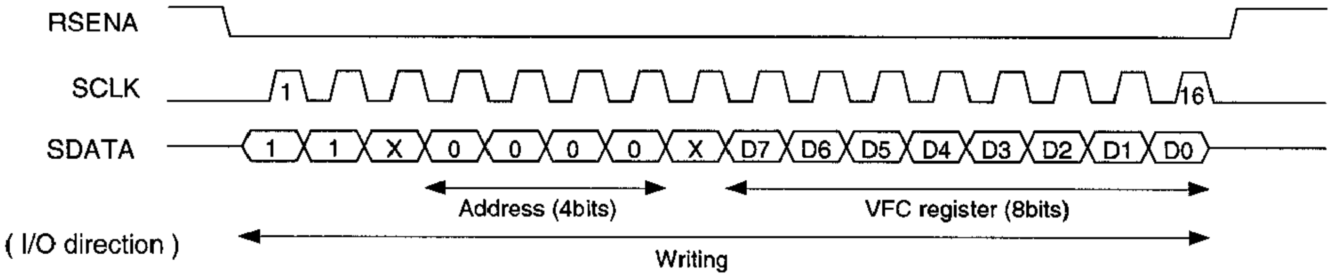


Read from register

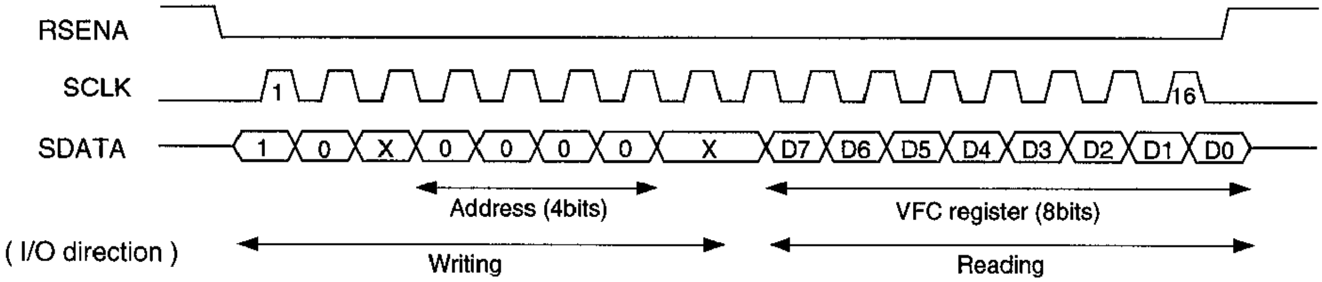


Write and read registers (cont)

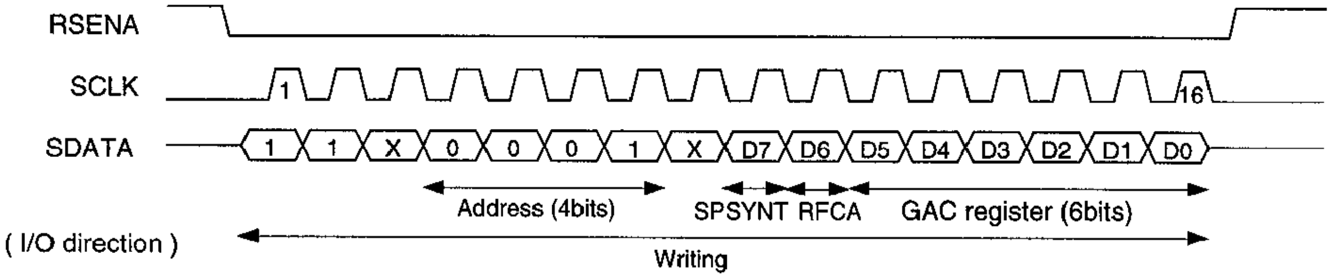
Write to VFC register



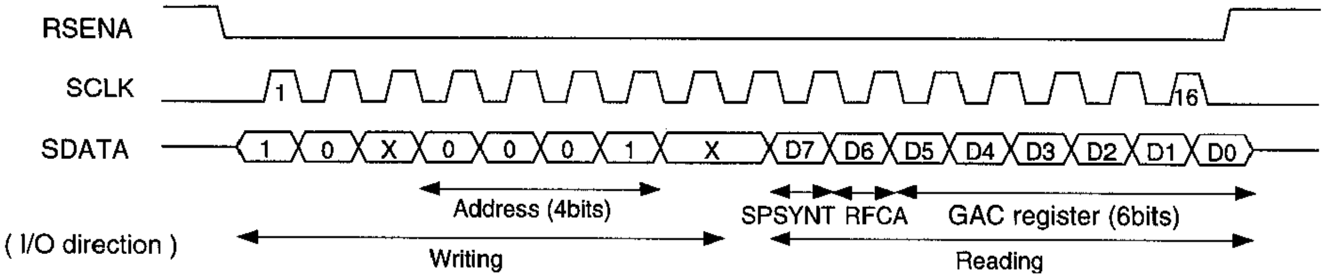
Read from VFC register



Write to GAC register

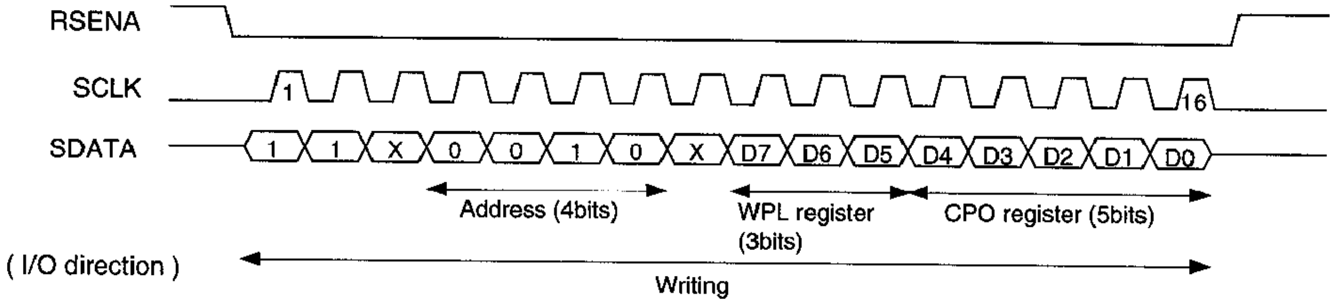


Read from GAC register

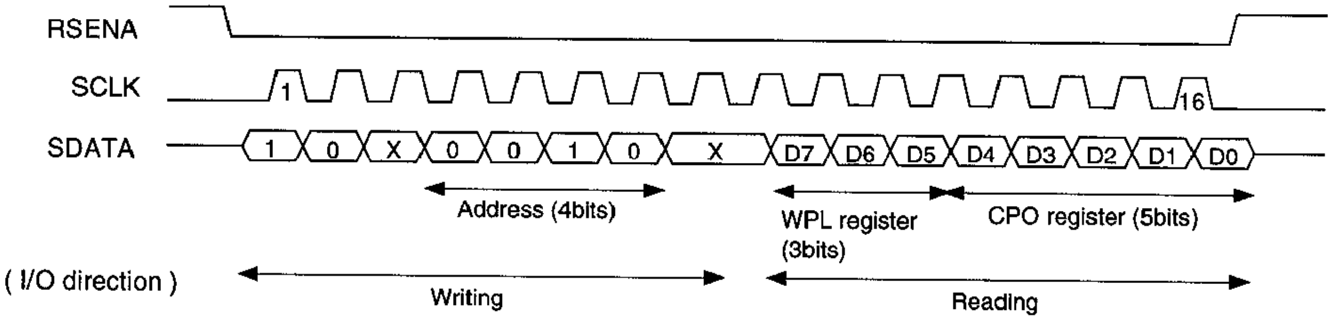


Write and read registers (cont)

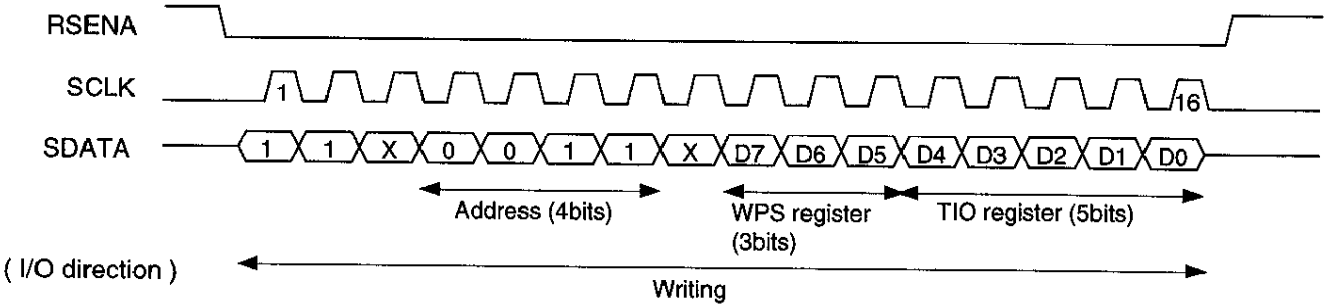
Write to WPLL & CPO register



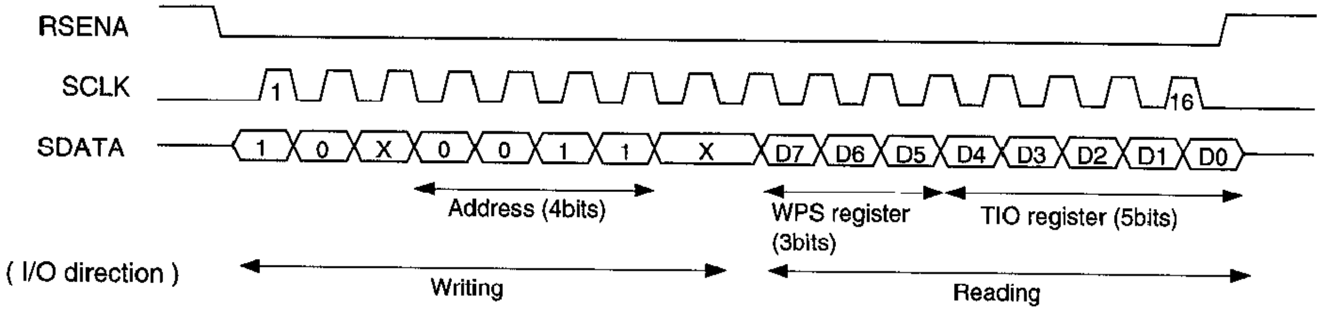
Read from WPLL &CPO register



Write to WPLS & TIO register

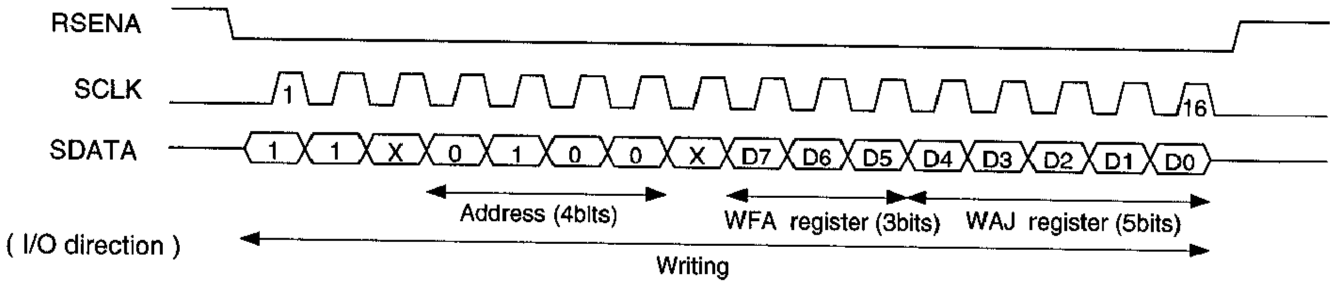


Read fromWPLS & TIO register

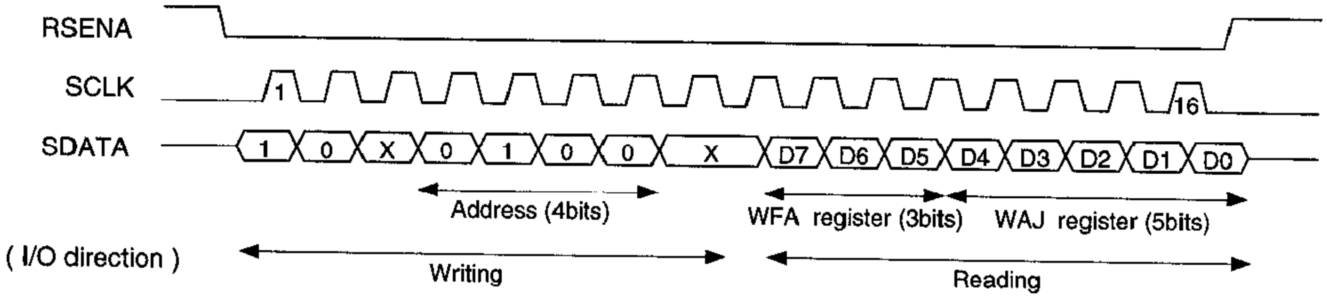


Write and read registers (cont)

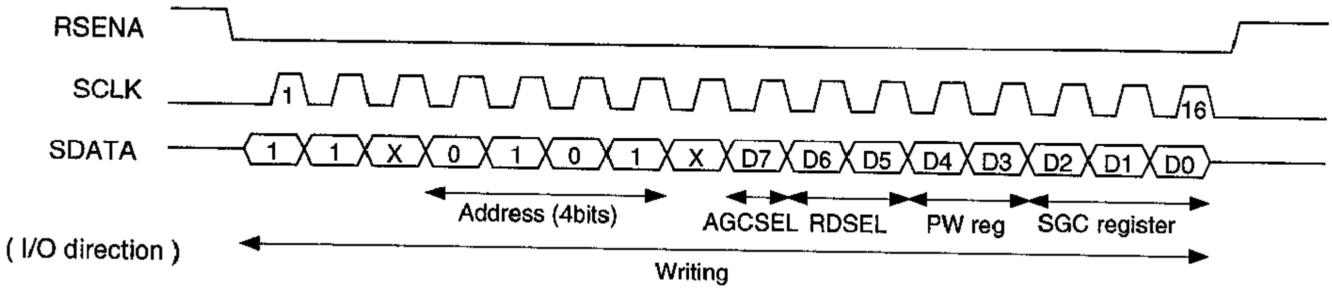
Write to WFA & WAJ register



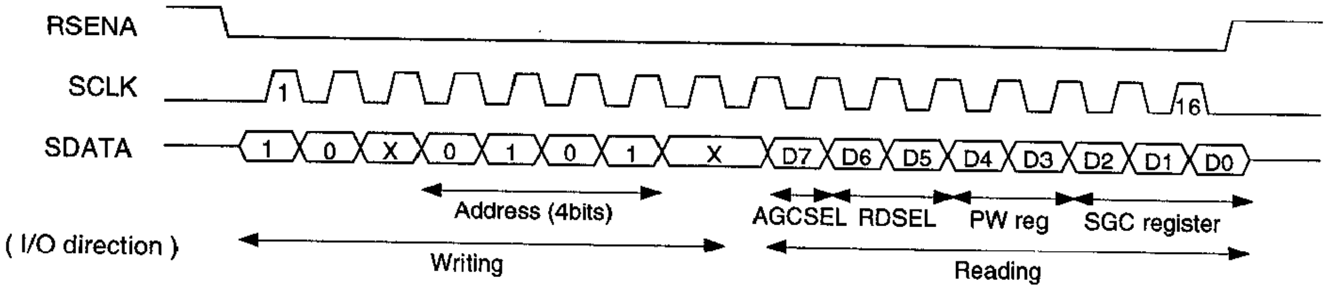
Read from WFA & WAJ register



Write to AGCSEL bit, RDSEL, PW & SGC register

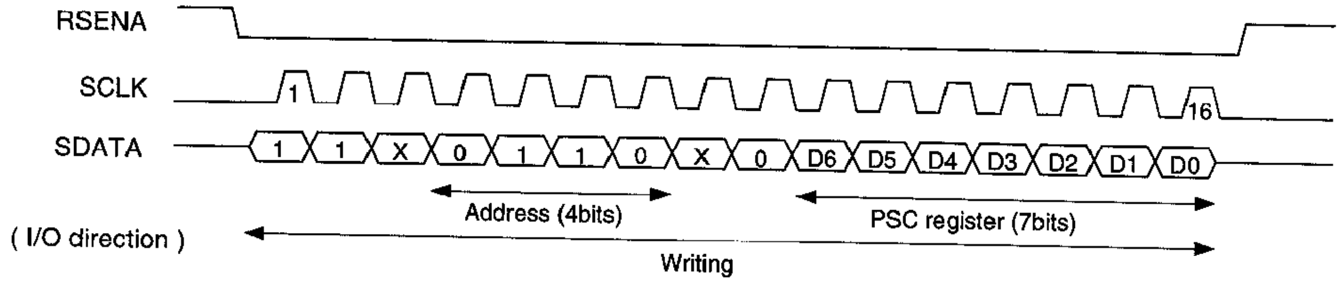


Read from AGS bit, RDS, PW & SGC register

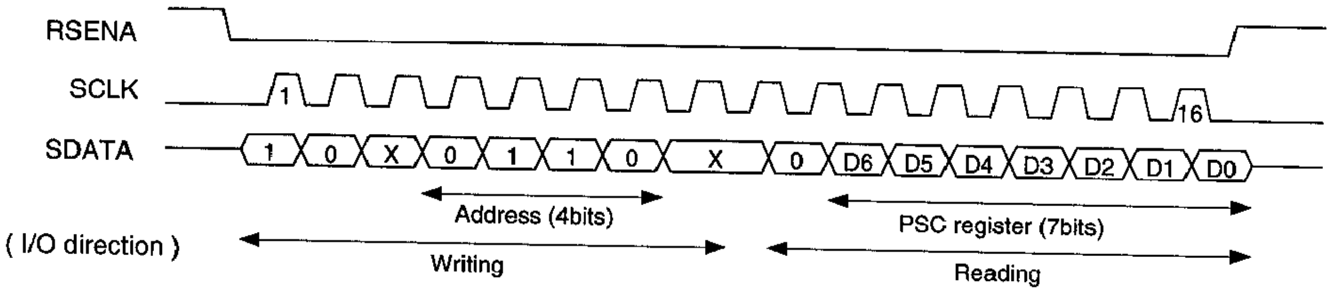


Write and read registers (cont)

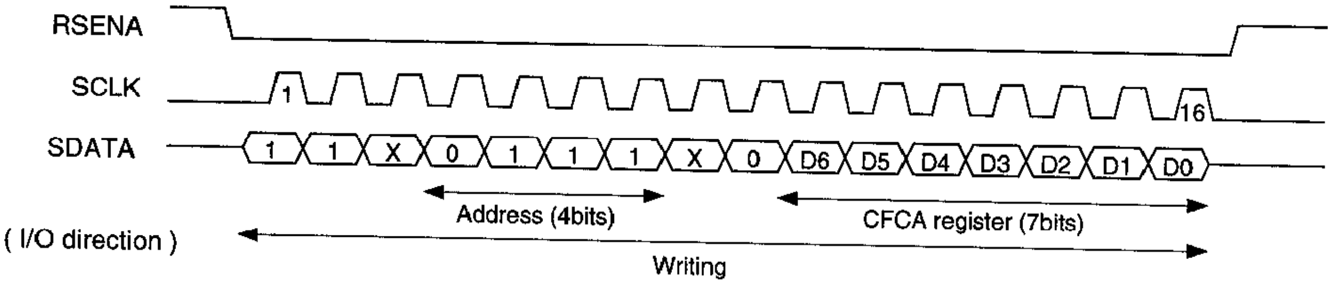
Write to PSC register



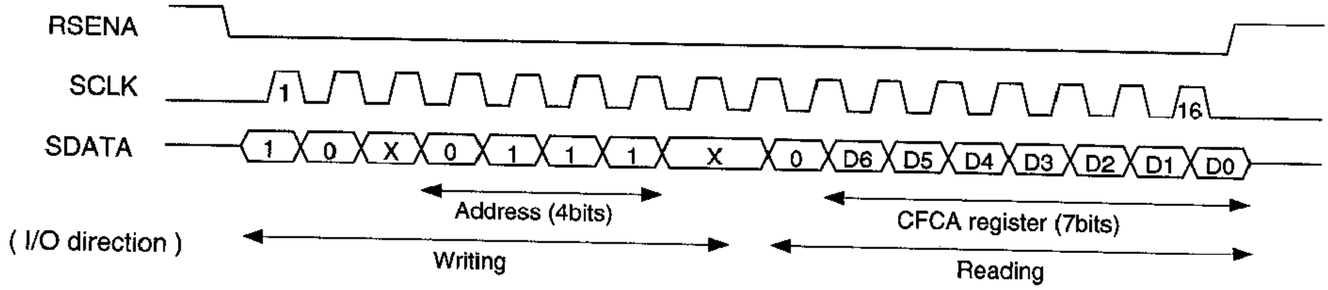
Read fromPSC register



Write to CFCA register

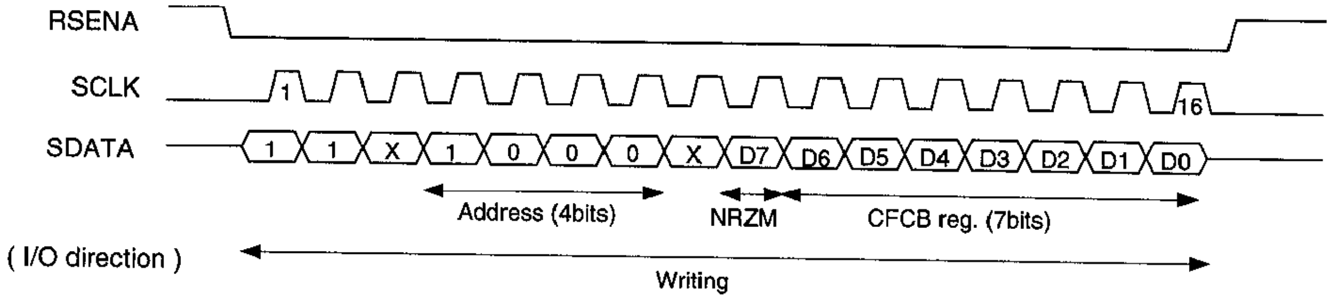


Read from CFC register

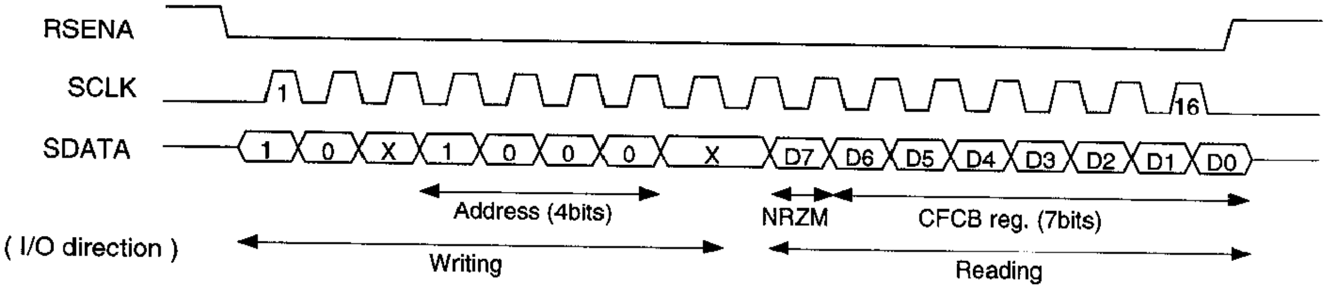


Write and read registers (cont)

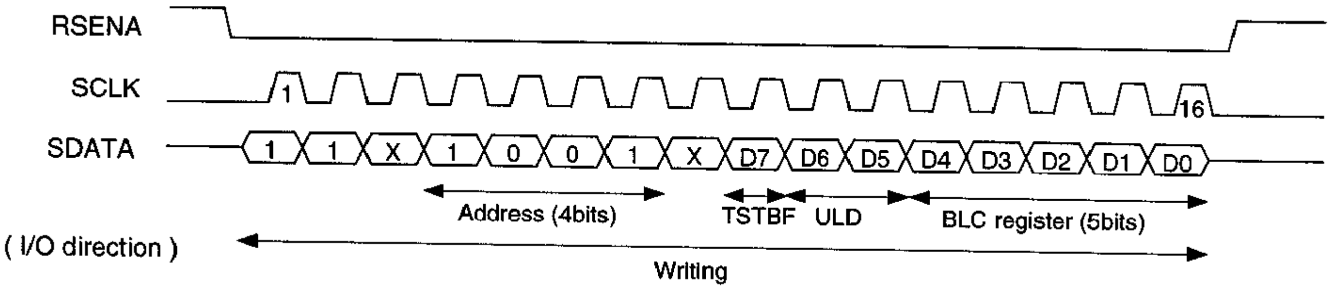
Write to NRZM bit & CFCB register



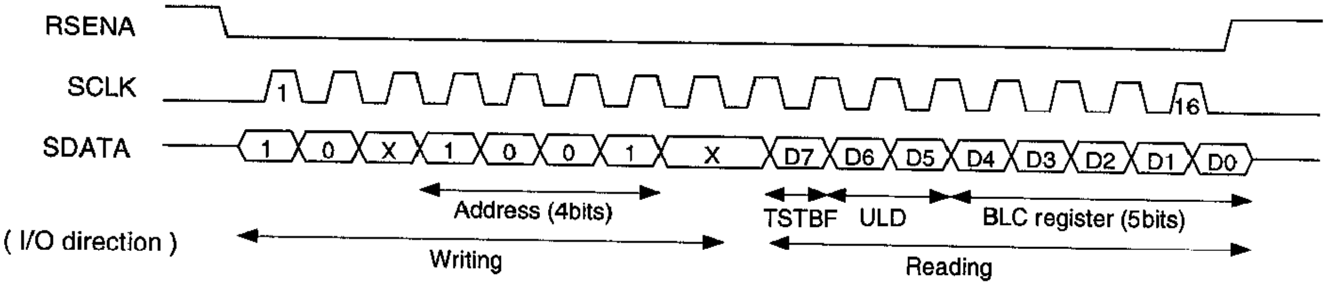
Read from NRZM bit & CFCB register



Write to ULD & BLC register

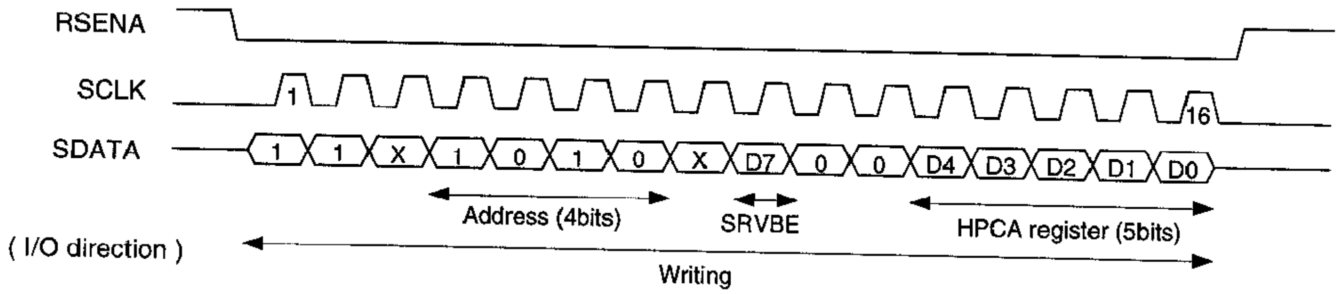


Read from ULD & BLC register

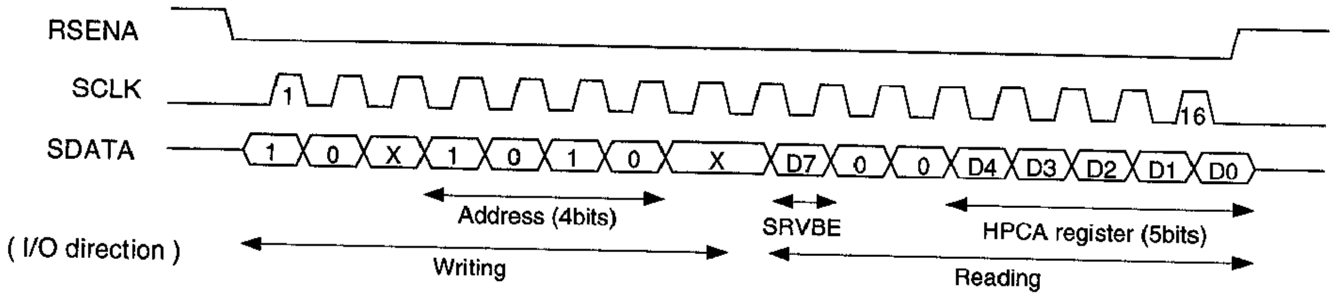


Write and read registers (cont)

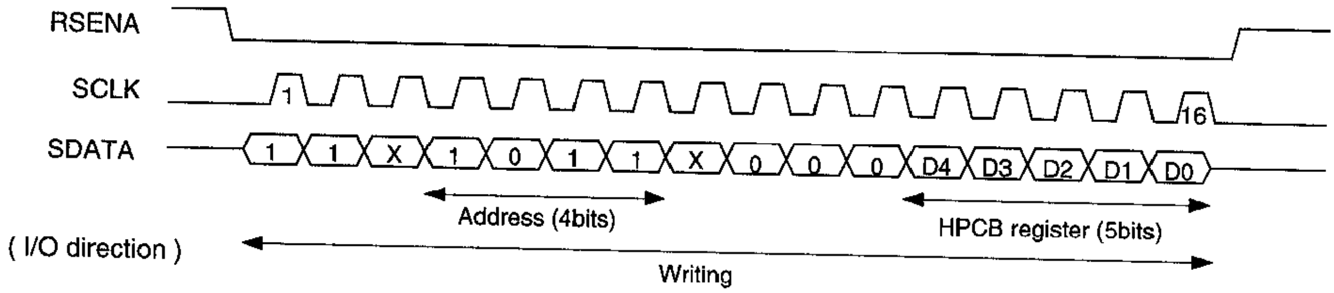
Write to HPCA register



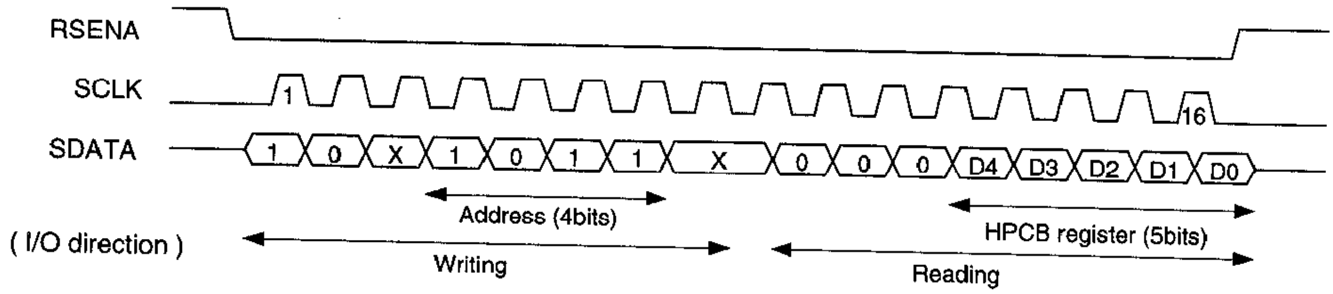
Read from HPCA register



Write to HPCB register

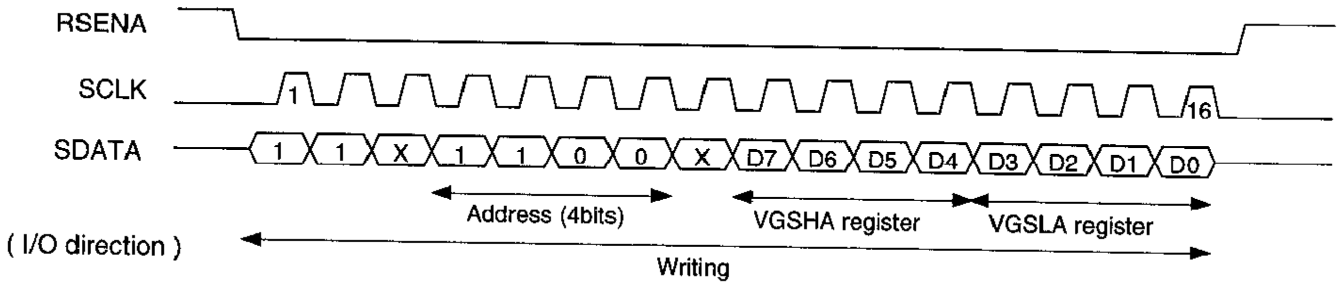


Read from HPCB register

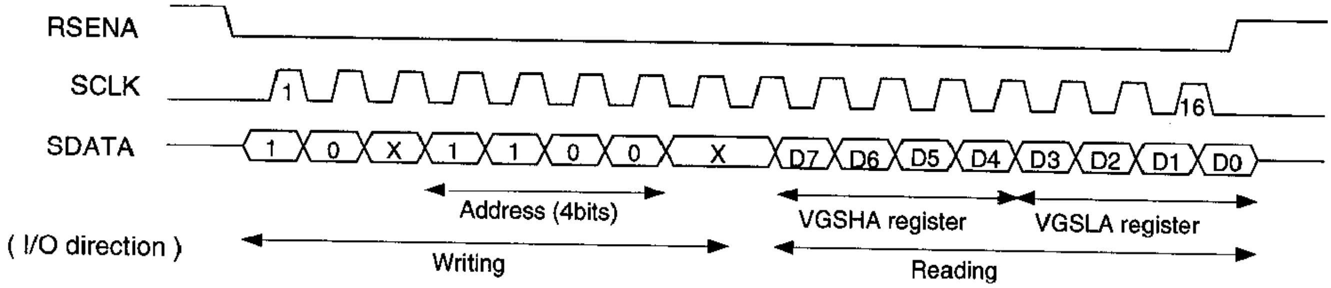


Write and read registers (cont)

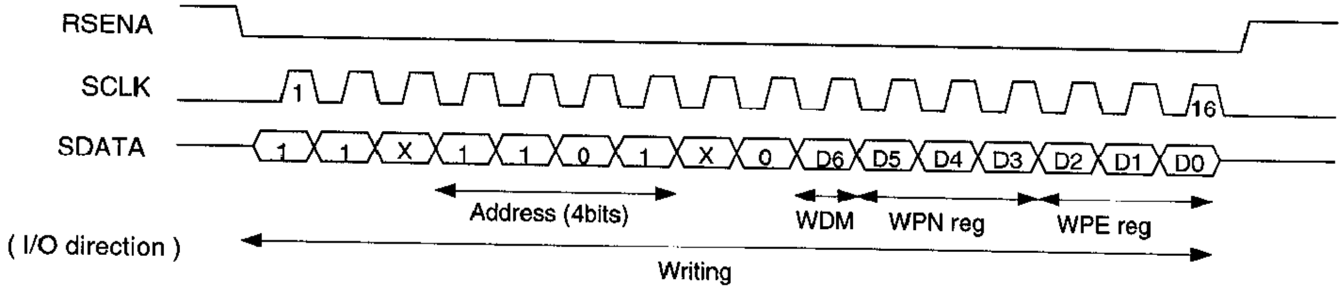
Write to VGSHA & VGSLA register



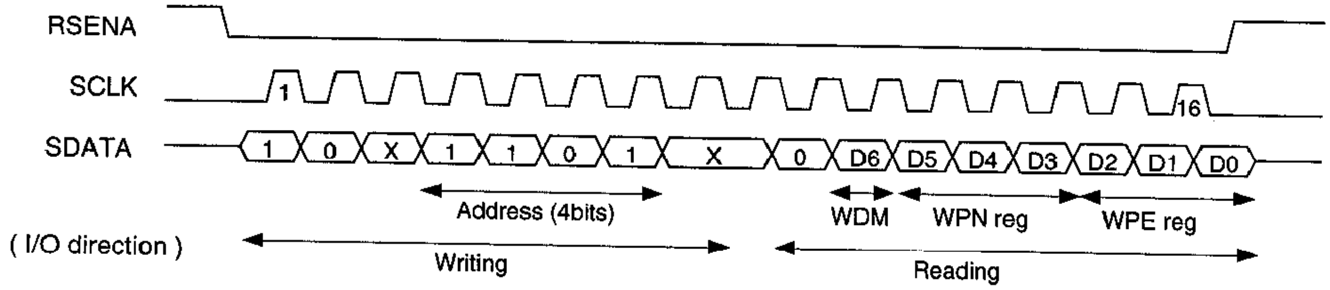
Read from VGSHA & VGSLA register



Write to WDM bit, WPN & WPE register

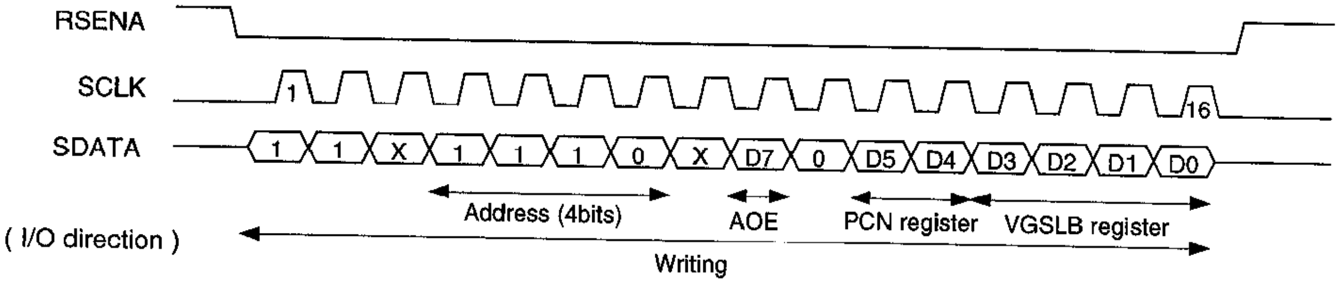


Read from WDM bit, WPN & WPE register

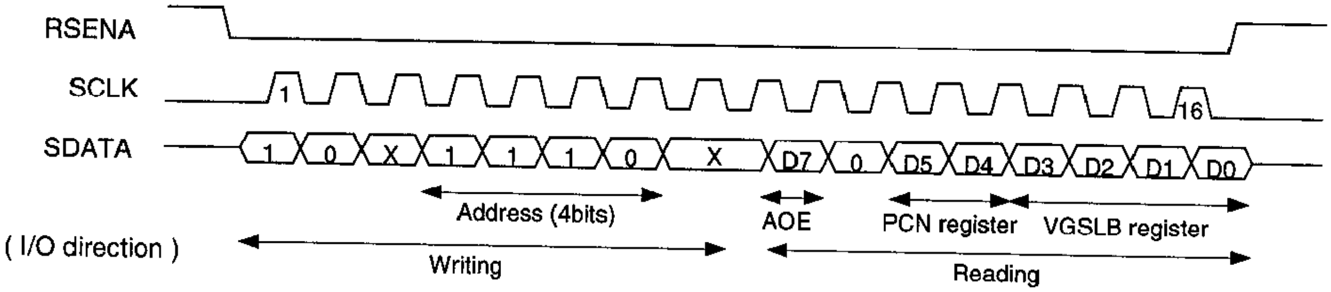


Write and read registers (cont)

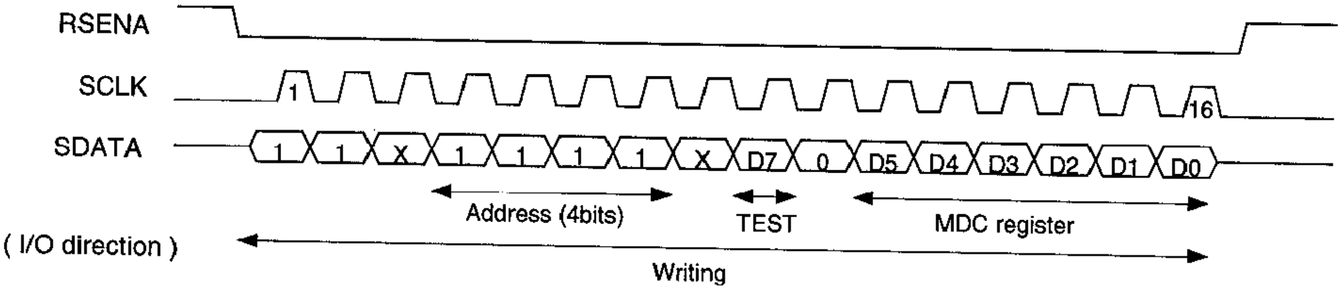
Write to AOE bit, VGSLB & PCN register



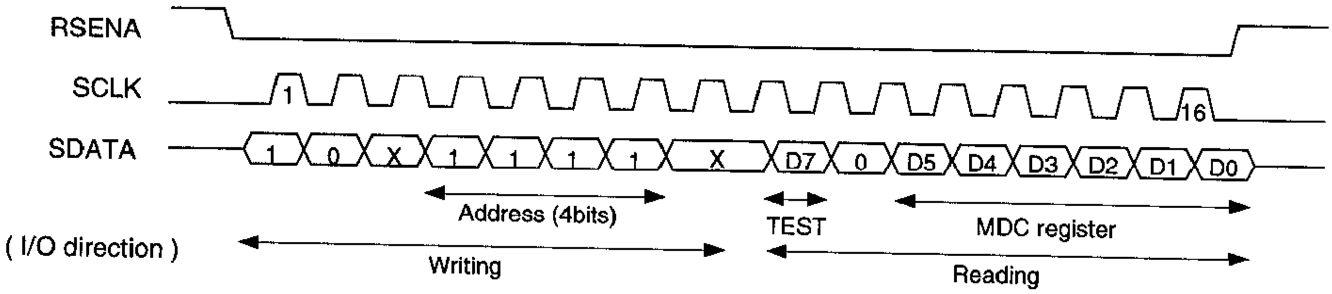
Read from AOE bit, VGSLB & PCN register



Write to MDC register



Read from MDC register



9. AGC(Automatic Gain Control) amplifier circuit

The AGC amplifier is a three-stage differential amplifier. The first stage has variable gain and the second and third stages have fixed gain. The AGC block consists of the first and second gain stages. The output of the active filter (FILOUT and DIFOUT) stage is the third gain stage of the AGC block.

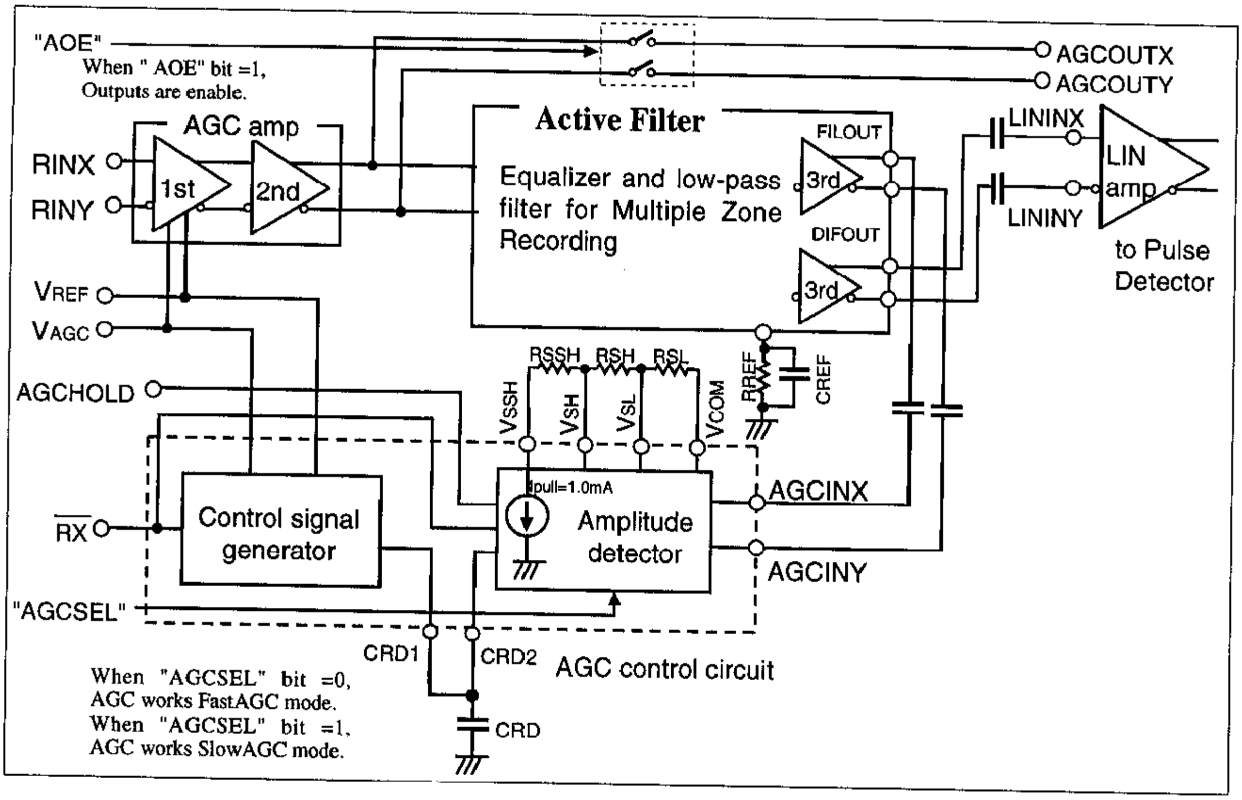


Fig. 9.1 Read Pulse Detector Block Diagram

The first-stage gain can be controlled in the range from - ∞ to approximately 17 dB by an amplitude control signal (VAGC) from the AGC control circuit. The first-stage gain is given by the following formula.

$$A_V = K_I \cdot \left(\frac{1}{1 + \exp\left(qV_C/_{kT} \right)} \right)$$

$K_I = 7.1$

$V_C = V_{AGC} - V_{REF}$

q: unit electrical charge

k: Bolzmann constant

T: absolute temperature

The second-stage amplifier has fixed gains of 6dB. The third-stage amplifier within the Active filter has fixed gains of 20dB (at the outputs of FILOUT). The AGC full gain is 142V/V (= 43 dB).

When bit 7 of register address "1110" (AOE bit) is set to "1", AGCOUTX and AGCOUTY pins can be used to monitor the output of the AGC amplifier. These pins are open emitter type. When monitor them, please terminate to ground by 1K~10KΩ resistor.

When bit 7 of register address "0101" (AGCSEL bit) is set to "0", AGC works FastAGC mode. When AGCSEL bit is set to "1", AGC works SlowAGC mode. The discharge current of AGC chargepump circuit is 200μA at FastAGC mode. It is 20μA at Slow AGCmode. The Charge current is 1mA at any mode.

The AGC amplifier gain control system is shown in figure 9.1. The AGC amplifier output is amplified by the post-amplifier and buffer amplifier, then passed through a low-pass filter. The low-pass filter output is connected to the differentiating amplifier, and is also feedback to the AGC control circuit. Here it is compared with reference voltages (V_{SH} and V_{SL}) that are set externally, then the external capacitor (C_{RD}) is charged or discharged. The charging/discharging of the external capacitor varies the control signal V_{AGC} which directly affects the gain of the AGC amplifier. The final amplitude V_P (of the AGCINX and AGCINY waveforms) in this control system can be calculated from the following equations, assuming sine waveforms:

$$T_1 \times I_{ch} = T_2 \times I_{dis} \qquad (9.1)$$

$$T_1 = \left(1 - \frac{2}{\pi}\sin^{-1}\frac{V_{COM} - V_{SH}}{V_P}\right) \times T \qquad (9.2)$$

$$T_2 = \left(1 - \frac{2}{\pi}\sin^{-1}\frac{V_{COM} - V_{SL}}{V_P}\right) \times T \qquad (9.3)$$

From equations (9.1), (9.2), and (9.3):

$$\sin^{-1}\frac{V_{COM} - V_{SH}}{V_P} - \frac{I_{dis}}{I_{ch}}\sin^{-1}\frac{V_{COM} - V_{SL}}{V_P} = \frac{\pi}{2}\left(1 - \frac{I_{dis}}{I_{ch}}\right) \qquad (9.4)$$

The final amplitude of the AGC amplifier loop is determined mainly by V_{SH} bias level. If appropriate values are set for V_{SL}, Ich and Idis, then from the preceding equations the final differential peak voltage V_{PDF} is:

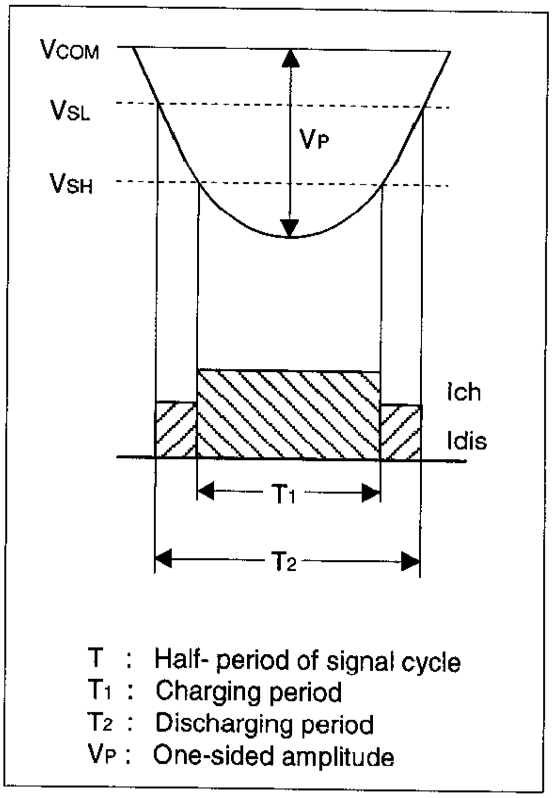
$$V_{PDF} = 4\,(V_{COM} - V_{SH}) \times m \qquad (9.5)$$

where m = 1.02 to 1.04

$$V_{COM} = Vcc - 1.0V$$

The preceding V_{PDF} is determined by the signal waveform, the output dynamic range of the amplifiers, and other factors. An appropriate value is V_{PDF} = 1.7V ± 0.1V. Accordingly, (V_{COM} - V_{SH}) should be around 0.41V. V_{SL} should normally be about:

$$V_{COM} - V_{SL} = 0.67\,(V_{COM} - V_{SH}) \qquad (9.6)$$



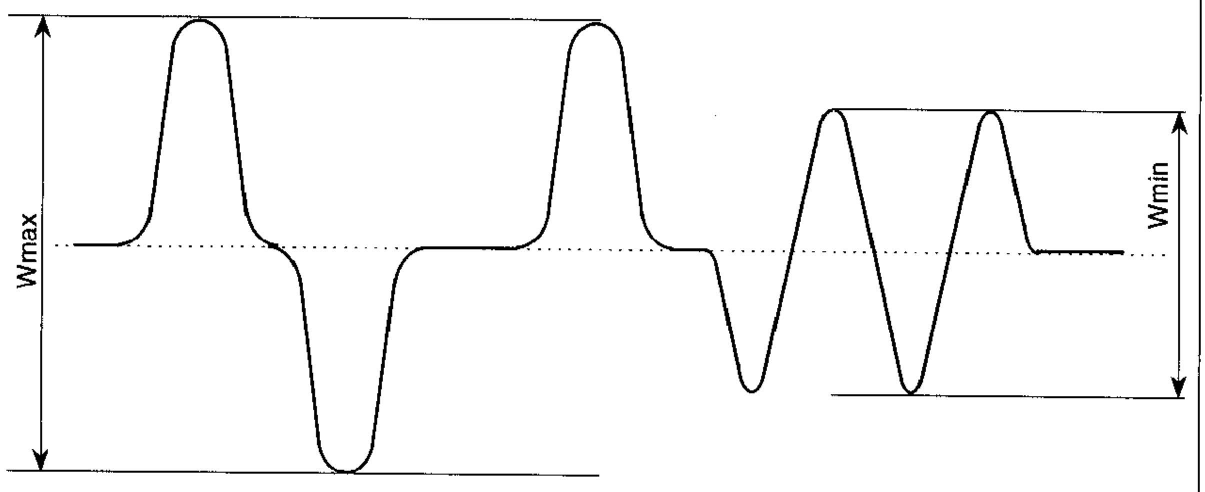
T : Half- period of signal cycle
T_1 : Charging period
T_2 : Discharging period
V_P : One-sided amplitude

Fig 9.2 Charge / Discharge timing

The value must be determined from the resolution specifications, however. The procedure is to determine V_{SH} and V_P from equation (9.4), then set Ich = 1.0mA and Idis = 0.2mA to determine VSL. Attenuation of signal amplitudes internal to the disk drive with respect to signal amplitudes external to the disk drive must be considered. For example, from equation (9.5), (V_{COM} - V_{SH}) = 0.41V and m = 1.03 gives V_{PDF} = 1.69 V, and from equation (9.4), (V_{COM} - V_{SL}) = 0.10 V, but if the input amplitude is instantaneously attenuated from its previous value to a new value that is not larger than (V_{COM} - V_{SL}), the amplitude recovery time might be excessively long. Next, it is necessary to consider the relationship of the recovery time to the charge-discharge capacitor C_{RD}. The C_{RD} capacitance should be close to the following value:

$$C_{RD} = \frac{300000}{\text{Transfer rate (Mbps)}}\ \text{(pF)} \qquad (9.7)$$

10. Setting for V_{SL}, V_{SH}, V_{SSH} level



RES = Wmax / Wmin (Resolution)

Fig. 10.1 Example of input signal for HD153035F

(1) V_{SH} level :

V_{FILOUT} = Peak to peak output signal amplitude of between FILOUTX and FILOUTY

$(V_{COM} - V_{SH}) = V_{FILOUT} \div m \div 4$,

Where V_{FILOUT}=2.0V, m=1.03
$V_{COM} - V_{SH} = 0.413$ V

Where Internal pull down current Ipull = 1.0mA
Hence, RSH + RSL = 413 Ω

(2) V_{SL} level :

$(V_{COM} - V_{SL}) = (V_{COM} - V_{SH}) \div RES \div 1.1$

Where RES=1.6,
$V_{COM} - V_{SL} = 0.235$ V

Therefore, RSL = 235 Ω, RSH= 178 Ω

(3) V_{SSH} level :

$(V_{COM} - V_{SSH}) = (V_{COM} - V_{SH}) \times RES \times 1.1$
$V_{COM} - V_{SSH} = 0.727$ V

Hence, RSSH + RSH + RSSL = 727 Ω
RSSH = 314 Ω

∴ RSL = 240 Ω

RSH = 180 Ω

RSSH = 300 Ω

11. Programable Active Filter

Active Filter consists of equalizer and electronic filter. Electronic filter is 7-pole, Bessel-type, low-pass filter and can be used in multiple zone recording (MZR) design. Cut-off frequency of filter is set by writing to register CFC. Writing to the HPC register will set the high-pass cut-off frequncy of the differential amplifier. The equalizer is double differentiation pulse sliming equalization. The Boost level is set by writing to register BLC.

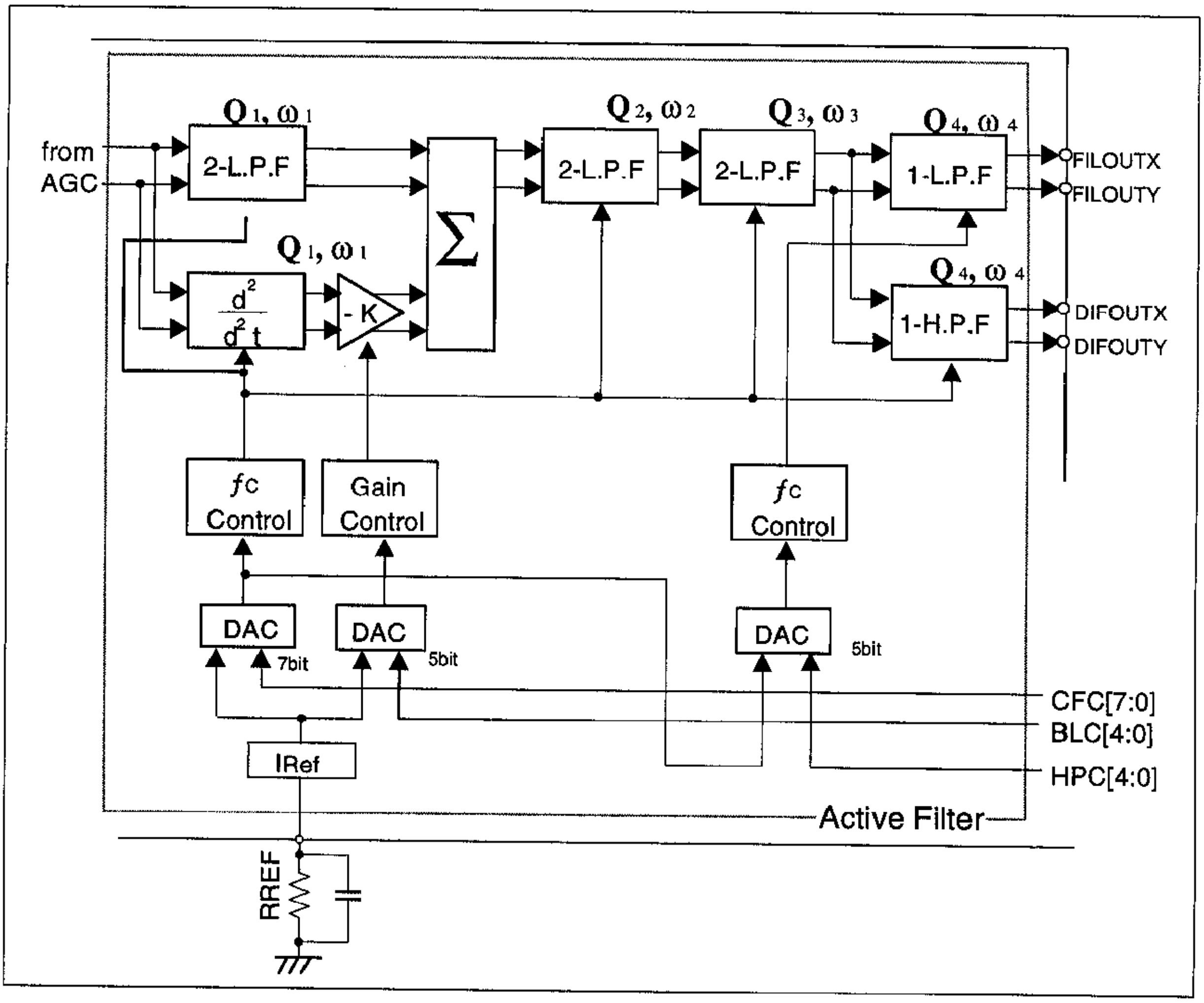
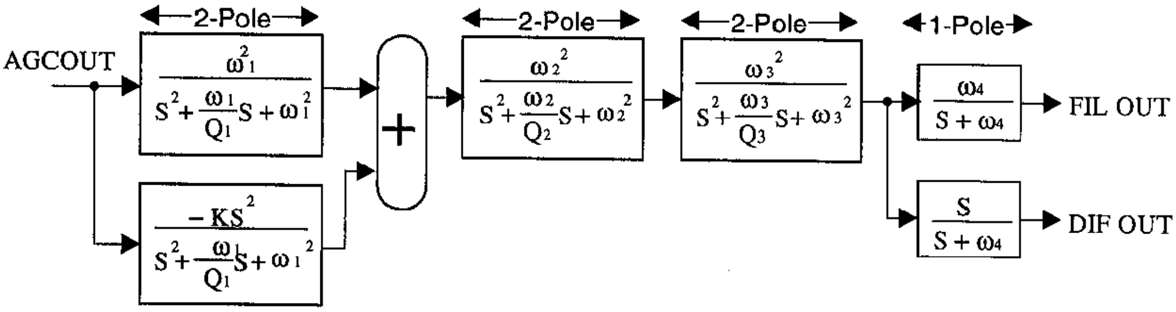


Fig. 11.1 Active Filter Block Diagram

Transfer function



Normalized Constant of 7-pole Bessel filter

Parameter	Normalized constant (ω_c = 1)
ω_1^2	2.94930
ω_1 / Q_1	3.22597
ω_2^2	3.32507
ω_2 / Q_2	2.75939
ω_3^2	4.20534
ω_3 / Q_3	1.82031
ω_4	1.68536

11.1 CFC and HFC register application

CFC register controls low pass cutoff frequency of the Active filter for FILOUTX/Y. HFC register controls high pass cutoff frequency of the Active filter for DIFOUTX/Y. When SRV/$\overline{\text{RD}}$ pin is low, the cutoff frequency is decided by CFCA and HPCA register values. When SRV/$\overline{\text{RD}}$ pin is high, the cutoff frequency is decided by CFCB and HPCB register value. When HPC register value is "0 0000", DIFOUTX/Y output is shifted 90° (defferential outputs) from FILOUTX/Y. Normally, HPC register is set "0 0000".

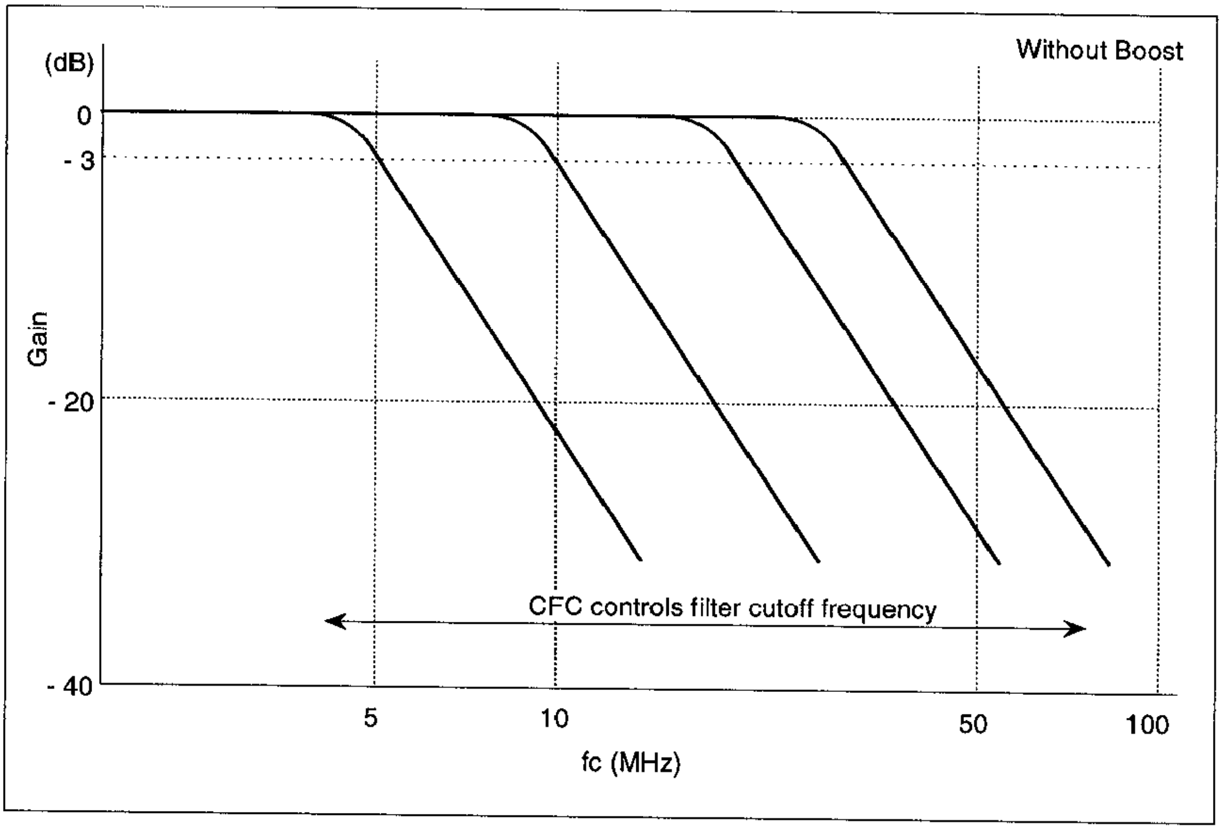


Fig. 11.2 Output bandwidth of FILOUTX and FILOUTY

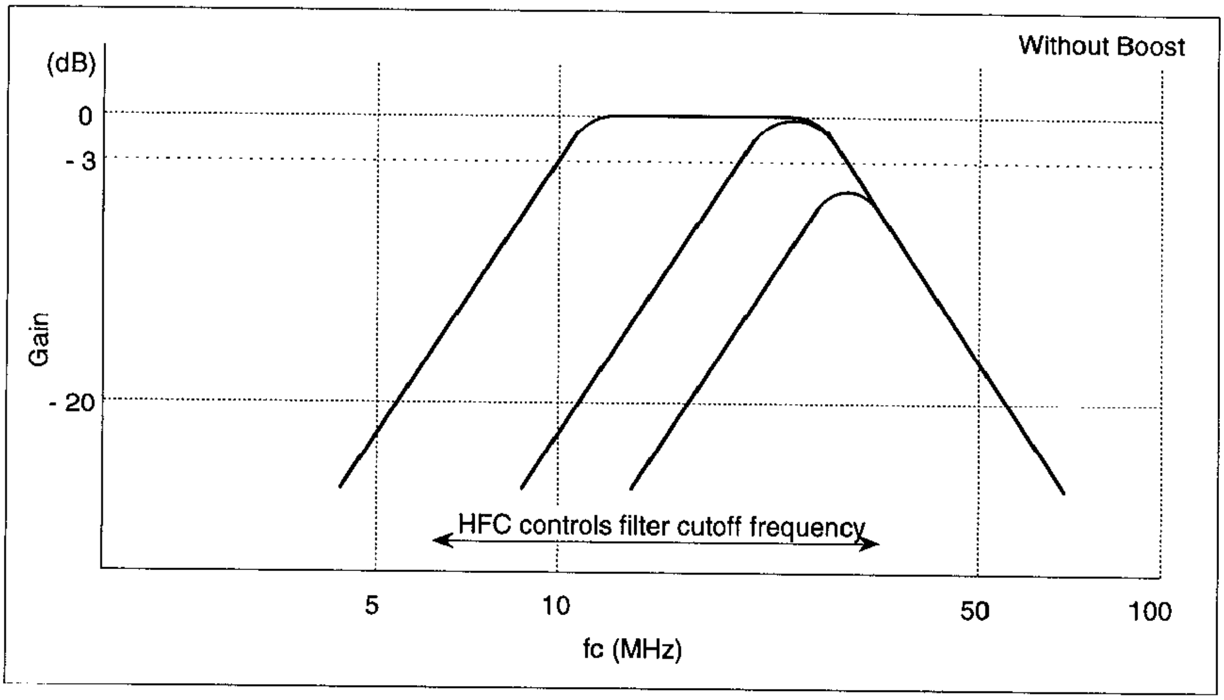


Fig. 11.3 Output bandwidth of DIFOUTX and DIFOUTY

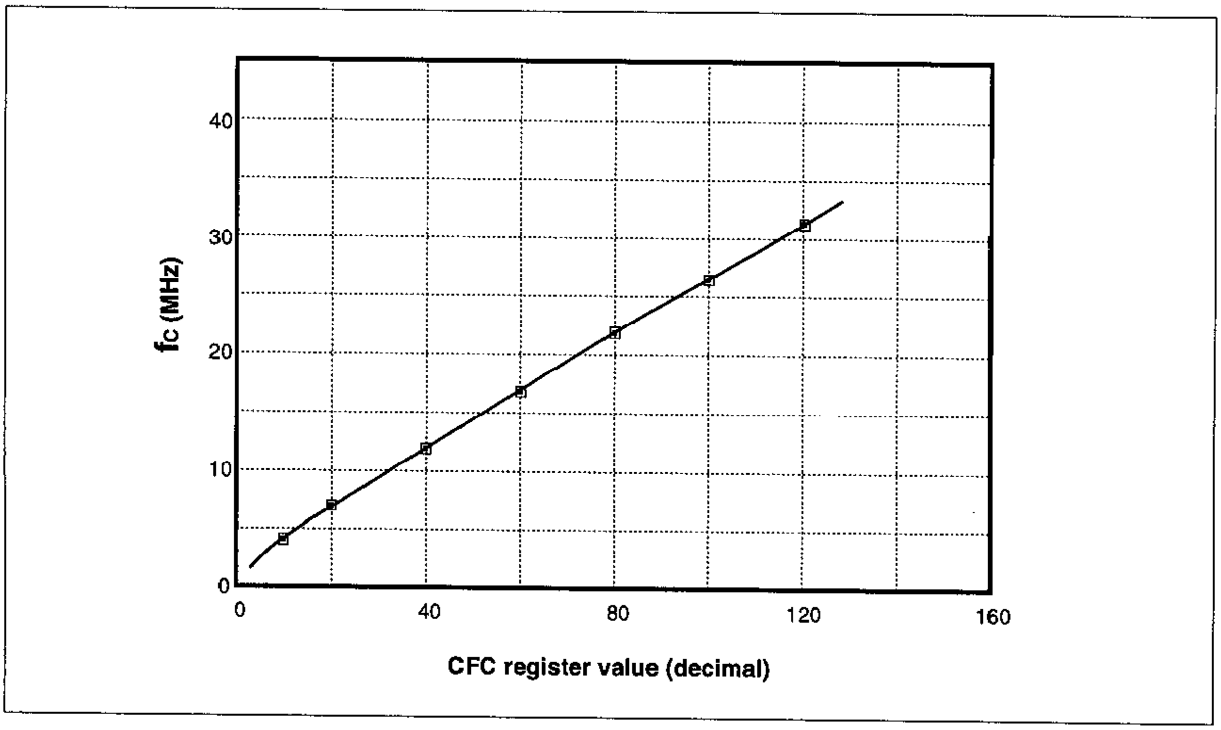


Fig 11. 4 fc vs CFC register

11.2 BLC register application

BLC register controls the Active filter Boost level. When sets BLC value except "0", filter boost is active, gets slimming pulse wave and low pass filter's cutoff frequecy will be shifted to higher frequency.

High boost level can get slimmed pulse easily, but it is caused distortion and noise. Boost level should be optimized for each zone.

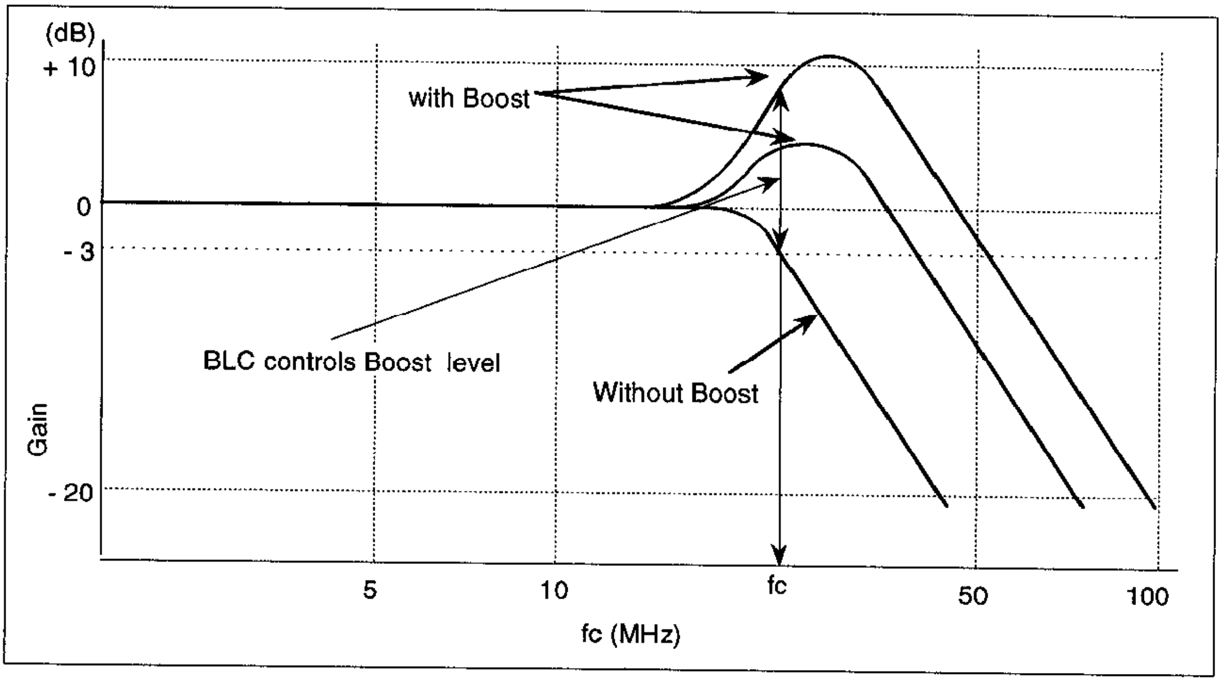


Fig. 11.5 Output bandwidth of FILOUTX and FILOUTY (with Boost)

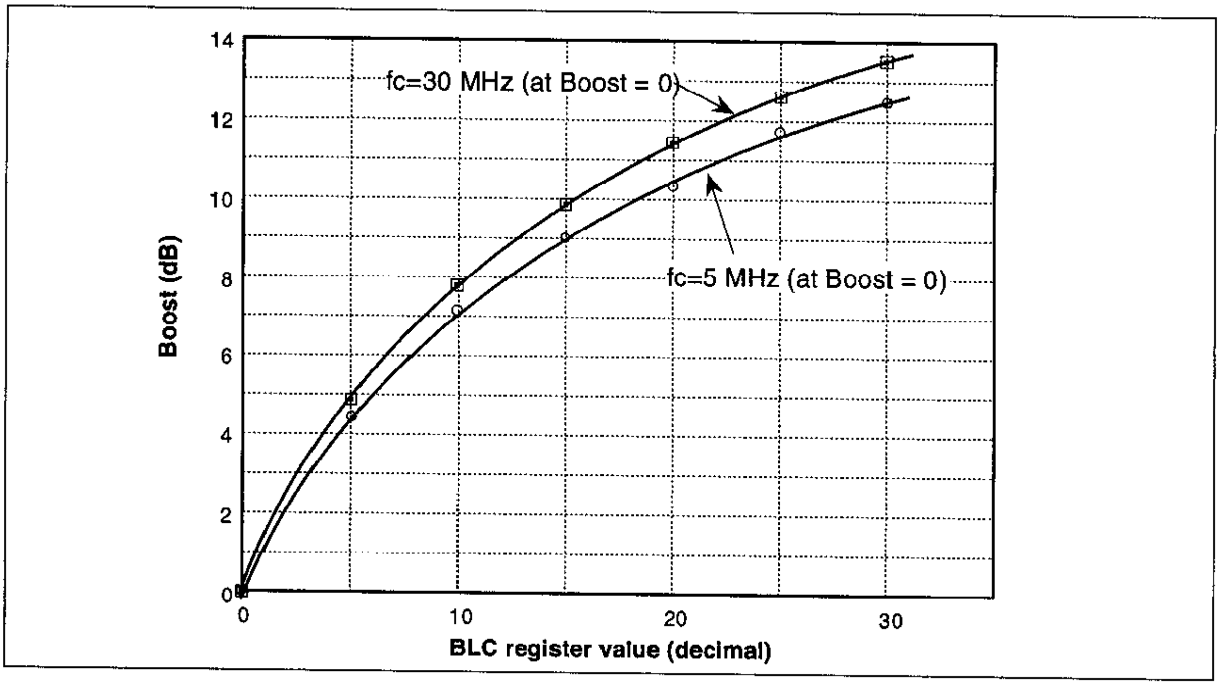
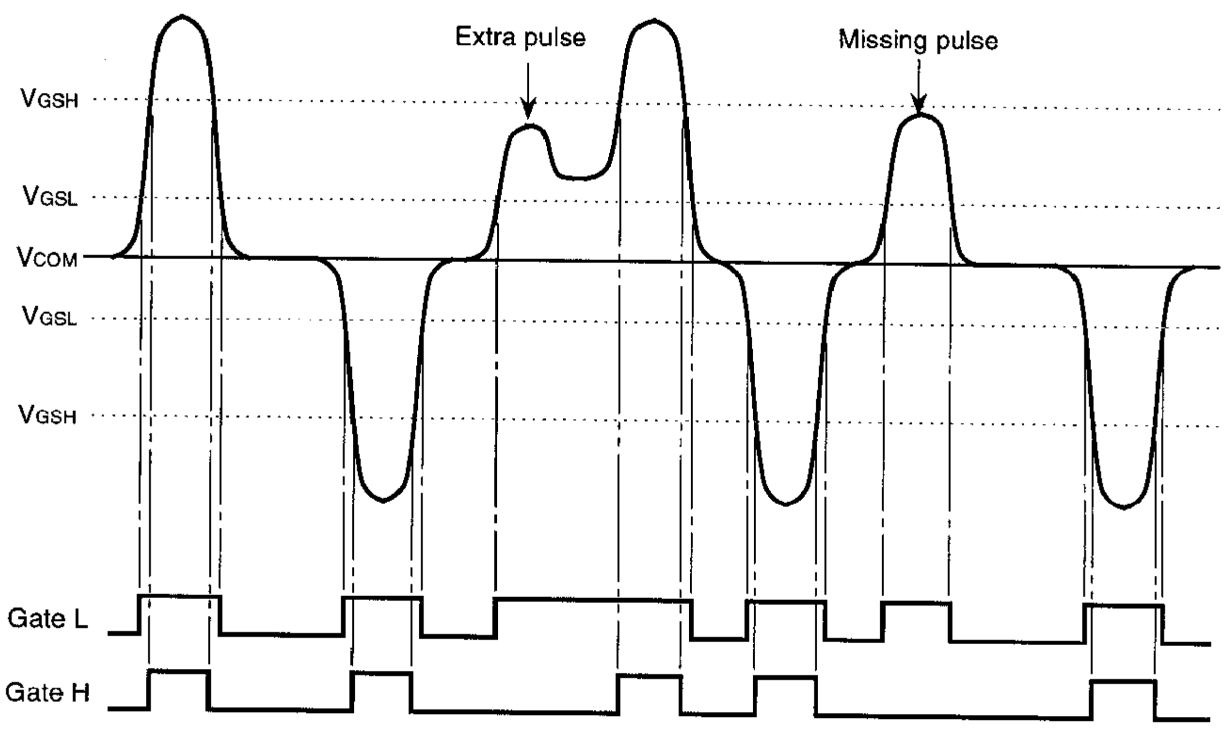


Fig. 11. 6 Boost vs BLC register at fc=30MHz

12. Gate Generator Circuit

A gate signal is used to gate the read signal near its peak value to remove incorrect read pulse. This gating signal is created by the gate generator circuit. The principle is to ensure that the read pulse crosses two programmable slice levels before being gated out as PDRD signal. For normal read mode, shifter and logic are used to qualify pulses that crosses only the low slice level or multiple peaks that would require polarity checking. The two slice levels VGSL and VGSH are set by writing to the VGSH and VGSL 4-bit registers. The High slice level is programmed to covered 0% to 100% of the VSH level and the Low slice level would covered 0% to 100% of the VSH. In servo mode, if one pulse is missing because it is not meeting the Low slice level, the next qualifying pulse will be dis-qualified as well.

Principal of Double-Slice-Level Gate Generation Circuit.

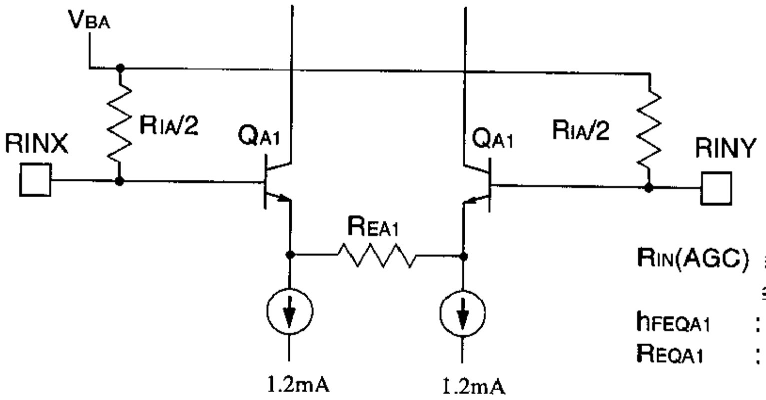


Read L	0	1	0	0	1	0	1	0	1	0	1	0	1	0	0	1	0
Read H	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0
Judge	↓	↓	↓	↓	↓	↓	↓ AND ↓	↓	↓	↓	↓	↓	↓ Polarity ↓	↓	↓	↓	↓
Correct data	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0

13. Input/Output impedance of the Read Pulse Detector's amplifiers

■ AGC amplifier

Input impedance



$R_{IA}/2$	1.5kΩ
R_{EA1}	167Ω
R_{EAQ1}	21.4Ω
h_{FEQA1}	80

$R_{IN}(AGC) \fallingdotseq R_{IA}/2 \ // \ h_{FEQA1} \times (R_{EA1}/2 + R_{EQA1})$

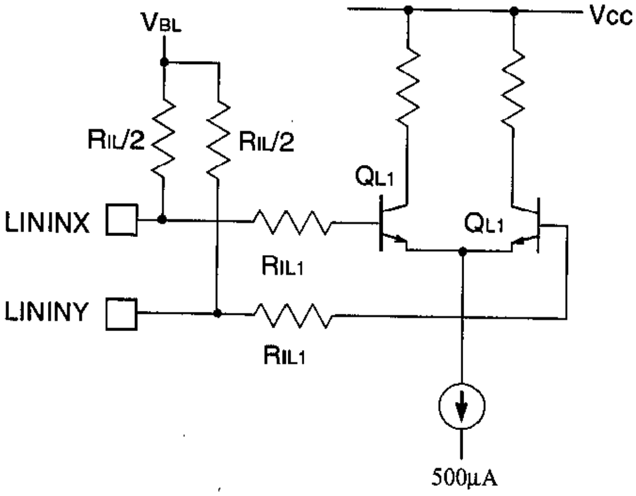
$\fallingdotseq 1.27\ k\Omega$

h_{FEQA1} : h_{FE} of Q_{A1}

R_{EQA1} : Emitter resistance of Q_{A1}

■ LIN amplifier

Input impedance



$R_{IL}/2$	4.5kΩ
R_{IL1}	100Ω
R_{EQL1}	103Ω
h_{FEQL1}	80

$R_{IN}(LIN) \fallingdotseq R_{IL}/2 \ // (R_{IL1} + h_{FEQL1} \times R_{EQL1})$

$\fallingdotseq 2.92k\Omega$

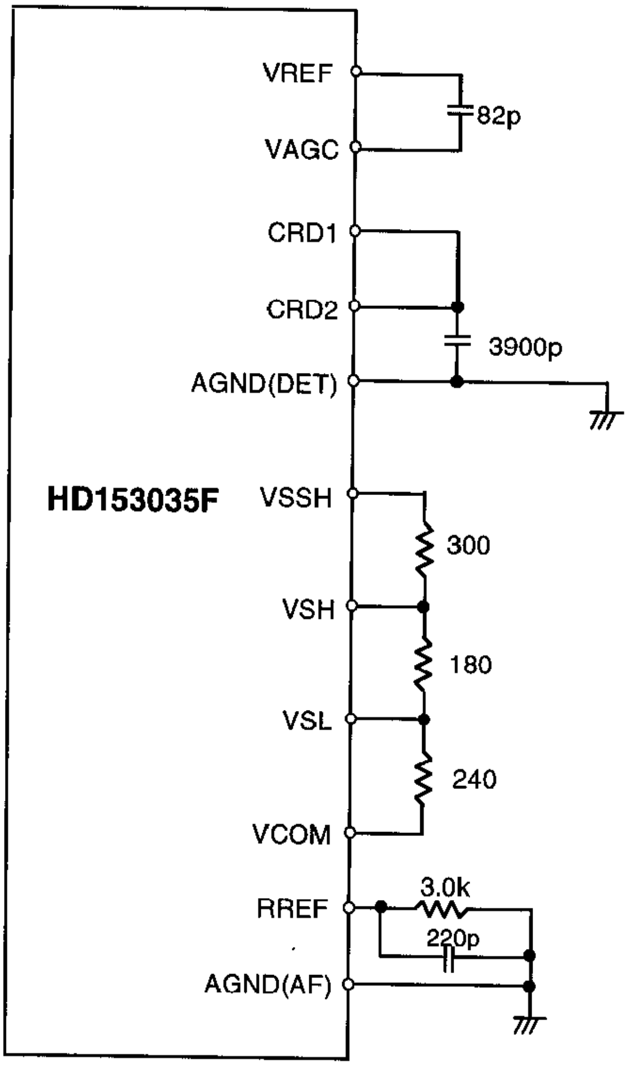
h_{FEQL1} : h_{FE} of Q_{L1}

R_{EQL1} : Emitter resistance of Q_{L1}

14. Example of External Components Connected to the RPD

These values are tentative.

NRZ transfer rate at 56 Mbps



Unit R: Ω
C : F

15. P/H circuit for Servo

The P/H circuits consists of a full-wave rectifier, sample and hold, followed by a gain stage that drives external capacitors through switches. Four outputs are made available to enable detection for four channel servo. When, the $\overline{\text{DUMP}}$ signal goes low, all output capacitors are discharged. Then, the $\overline{\text{CHA}}$ signal is activated producing a succession of four negative pulses. During each negative going pulse, one of the four external capacitors is shorted to the output of the gain stage for holding the peak of the servo burst signal into the capacitor.

Hitachi use OUT0 and OUT1 pin to monitor the internal signals in test mode. So, if you don't use P/H circuit, the P/H Vcc pin(#10) should be connected to the power supply line.

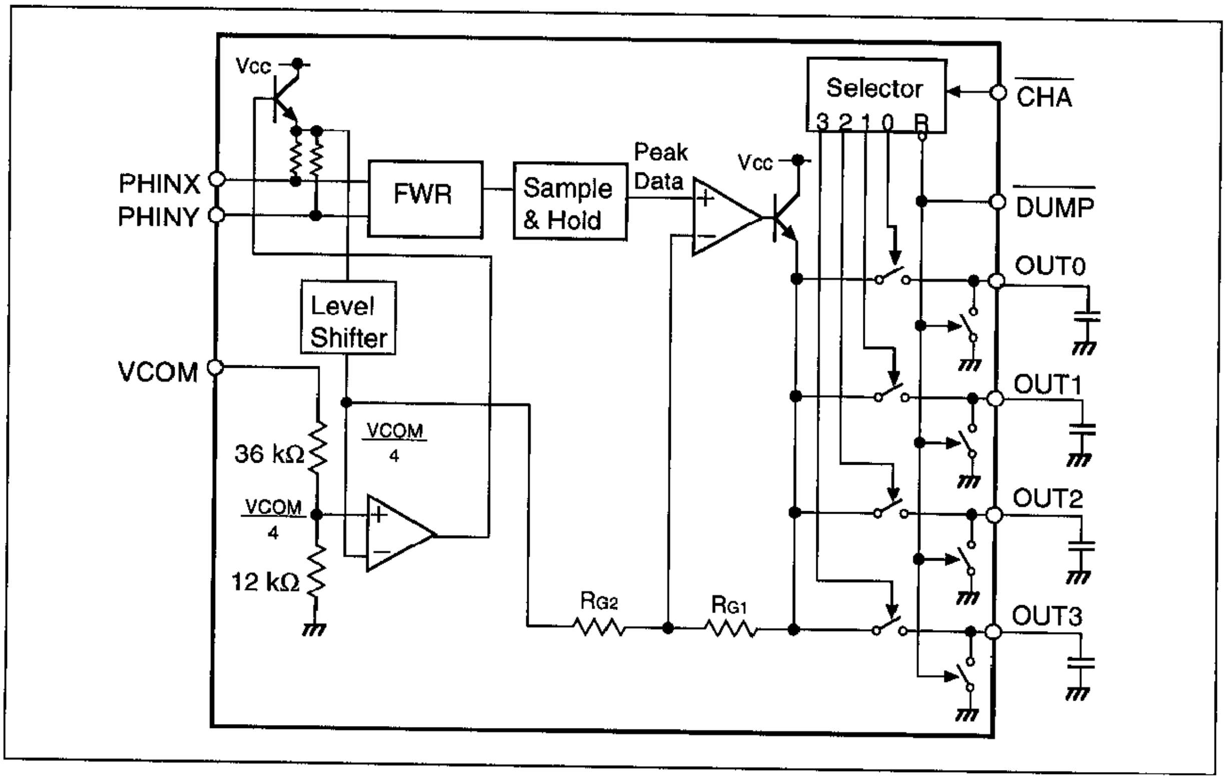
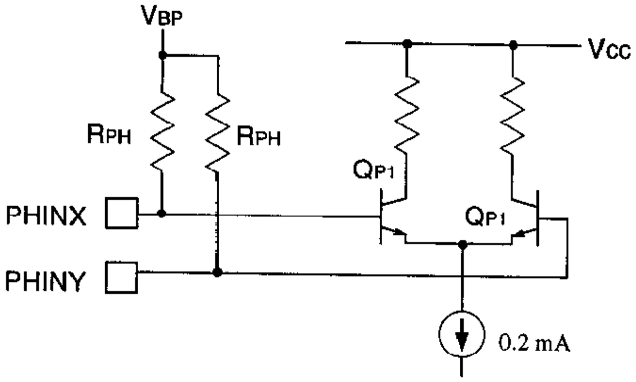


Fig. 15.1 P/H circuit Block Diagram

■ Input impedance of P/H circuit



R_{PH}	6 kΩ
R_{EQP1}	258 Ω
h_{FEQL1}	80

$R_{IN}(LIN) \cong R_{PH} // (h_{FEQL1} \times R_{EQP1})$

$\cong 4.87\ k\Omega$

h_{FEQP1} : h_{FE} of Q_{P1}

R_{EQP1} : Emitter resistance of Q_{P1}

16. Servo application example

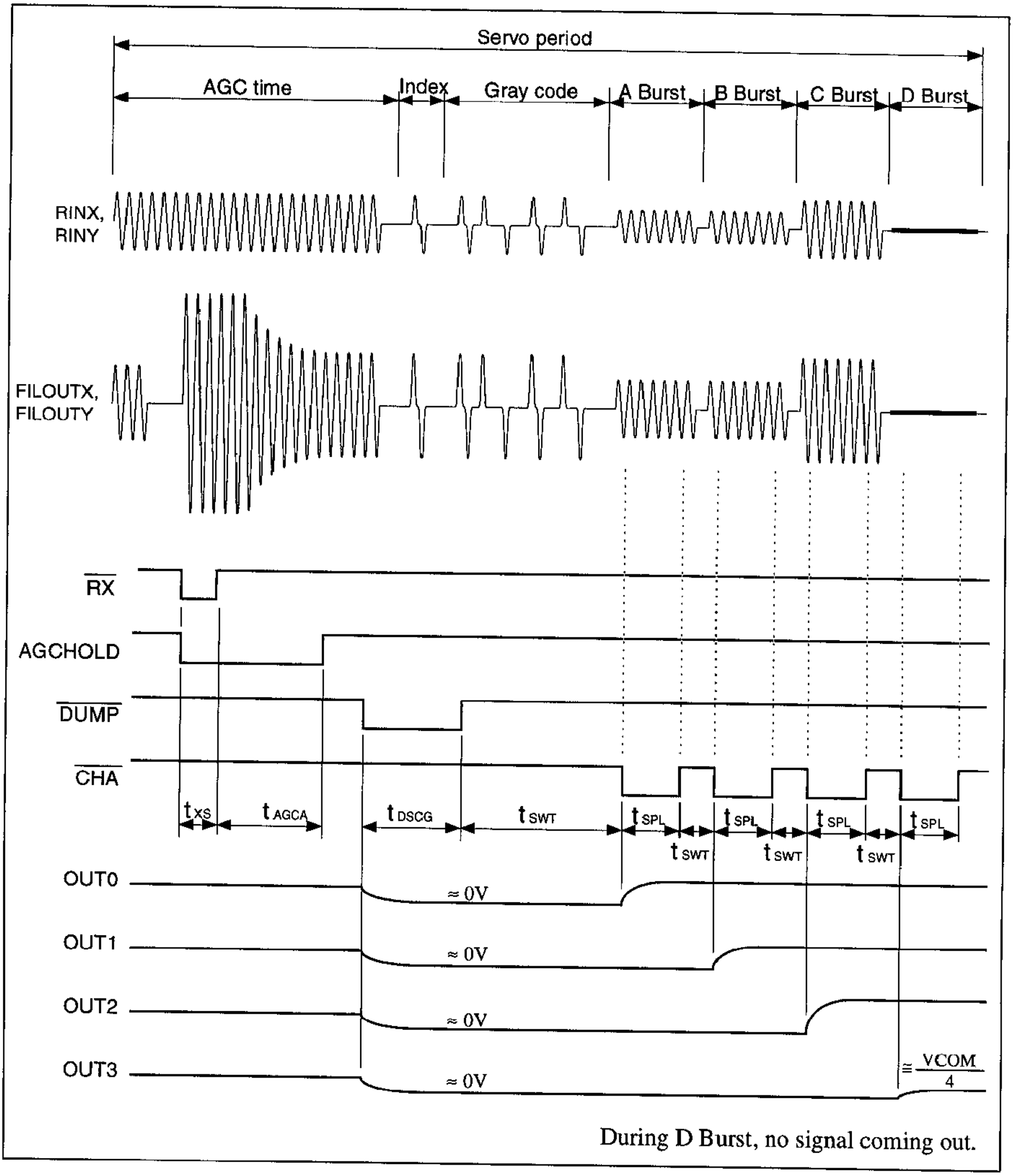
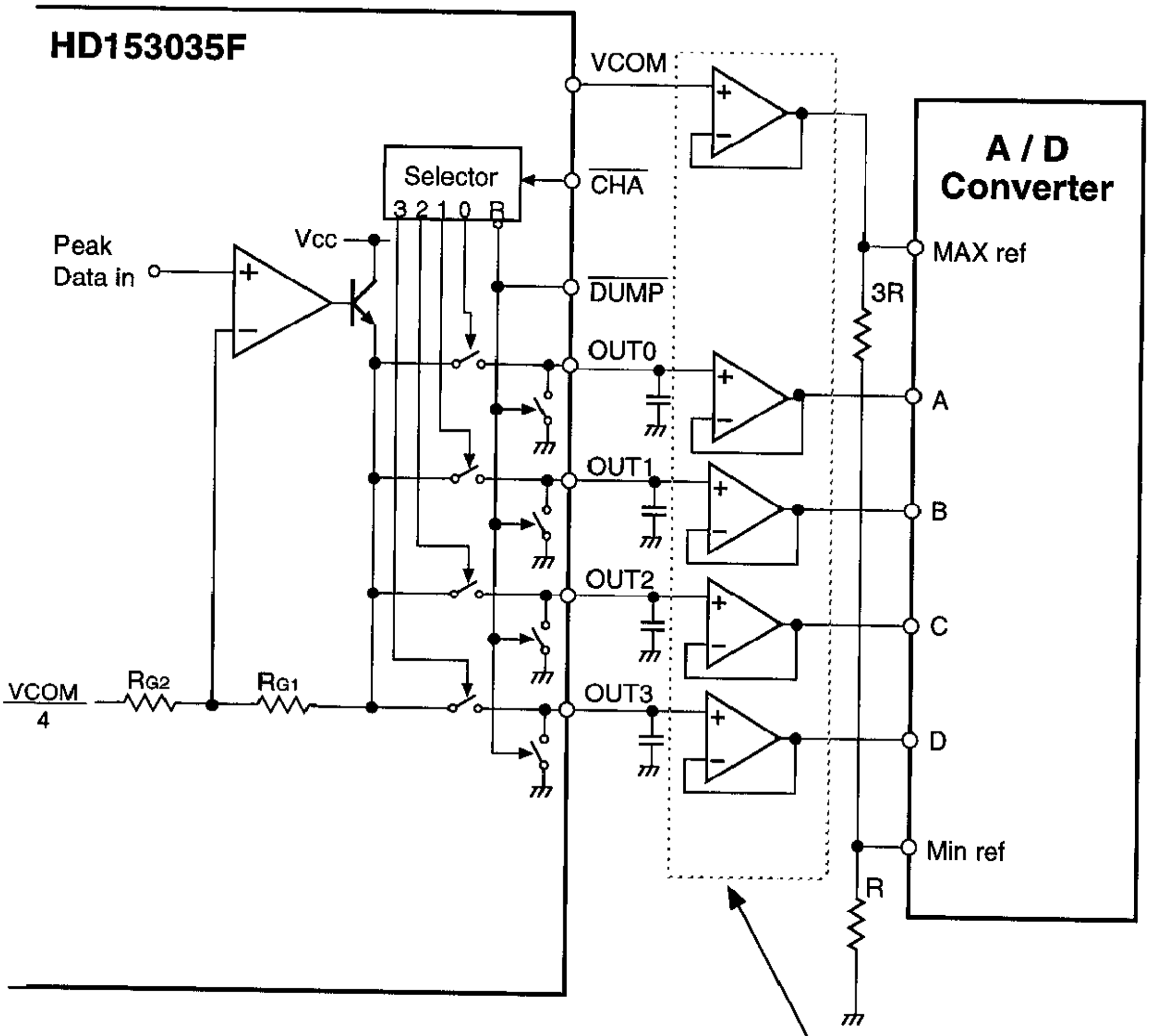


Fig. 16.1 Timing Diagram of the servo function

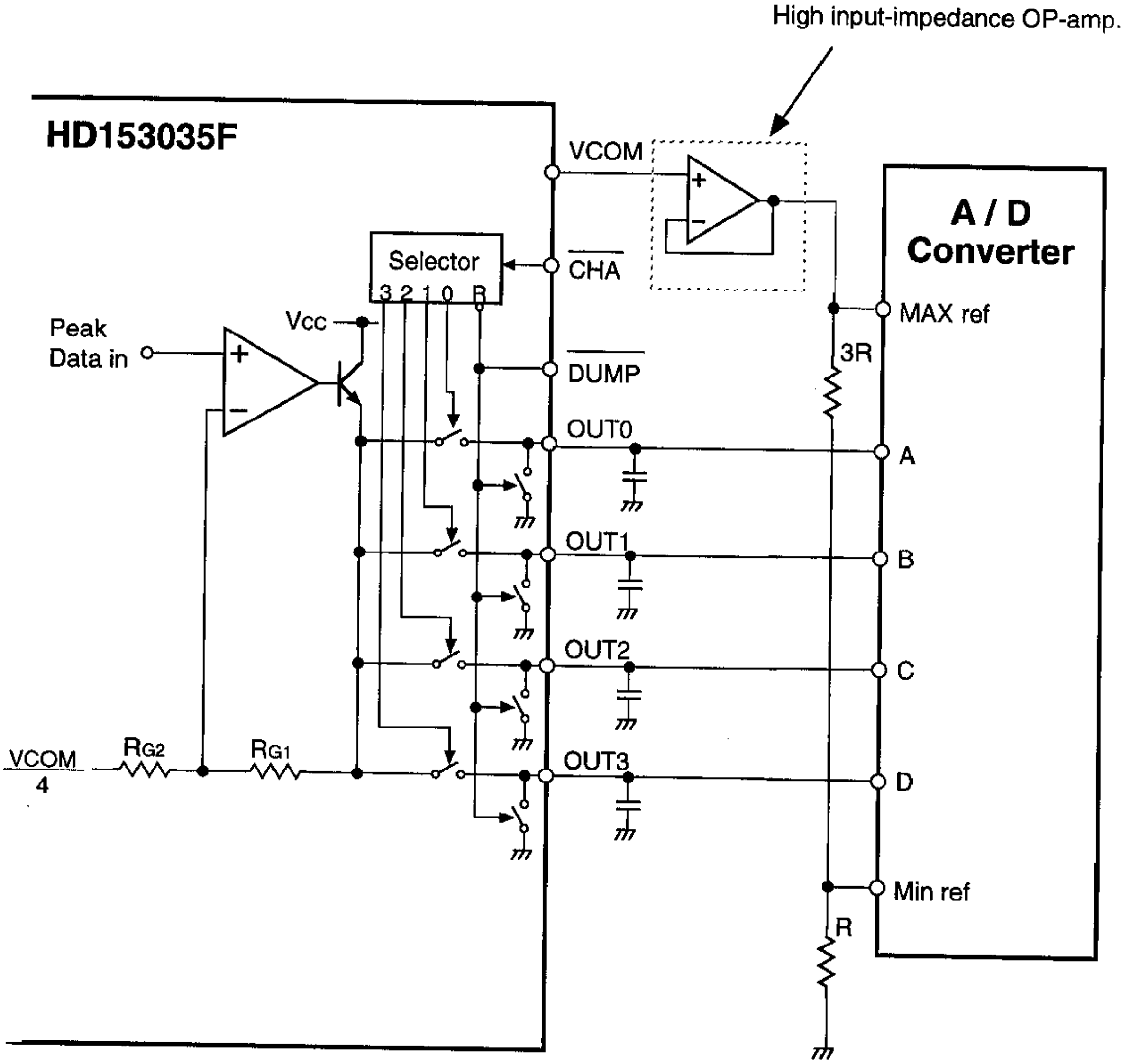
17. Servo application example (external components)

(1) Low input impedance Digital to Analog Converter application

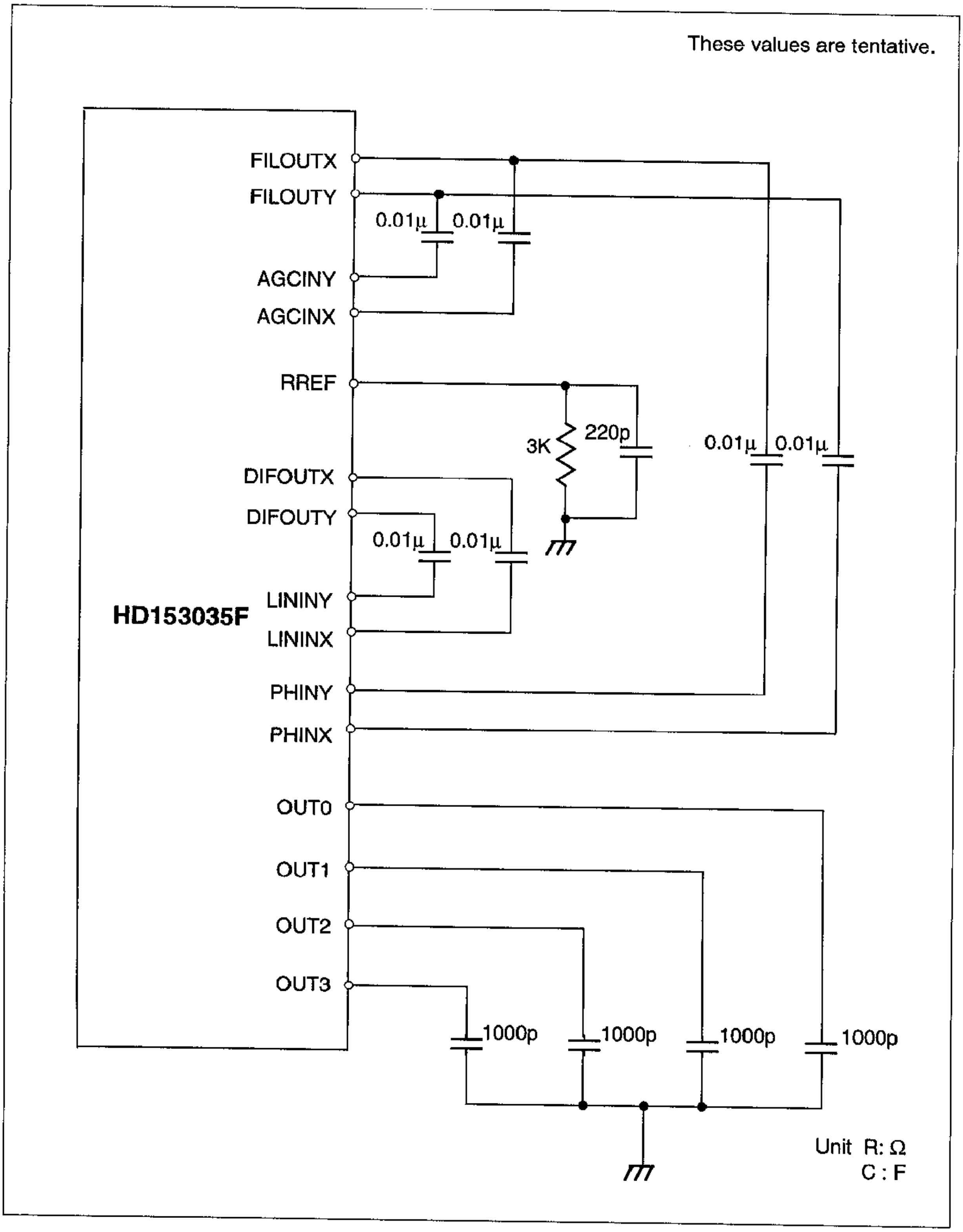


High input-impedance OP-amp.

(2) High input impedance Digital to Analog Converter application

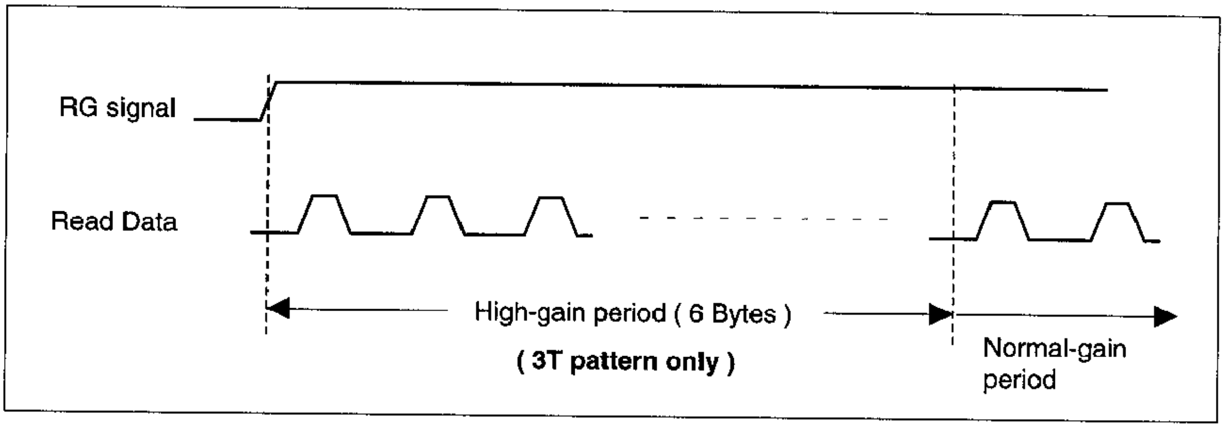


17. Example of External Components Connected to the RPD

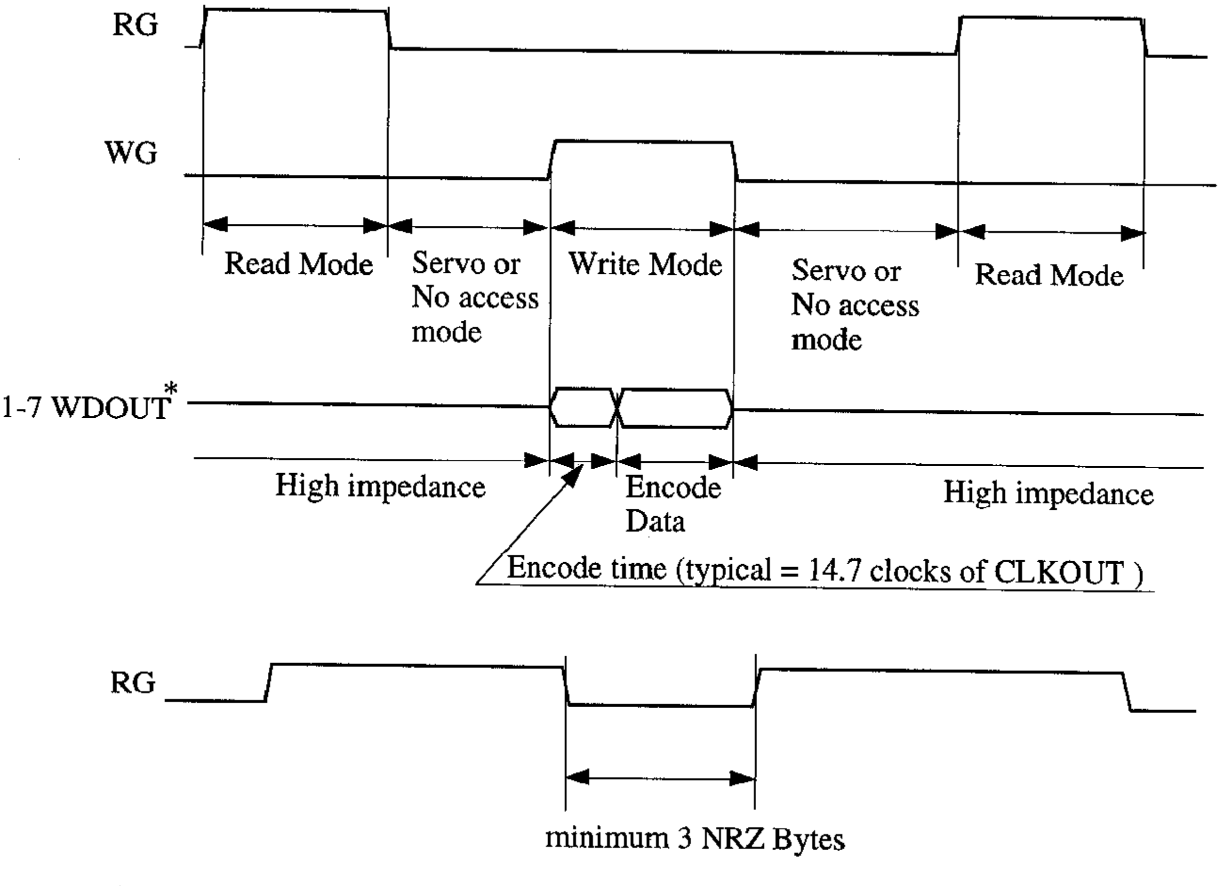


18. Sync Field Detection

The high-gain period can be set to last six NRZ bytes after the RG signal is goes active.



Read and write mode



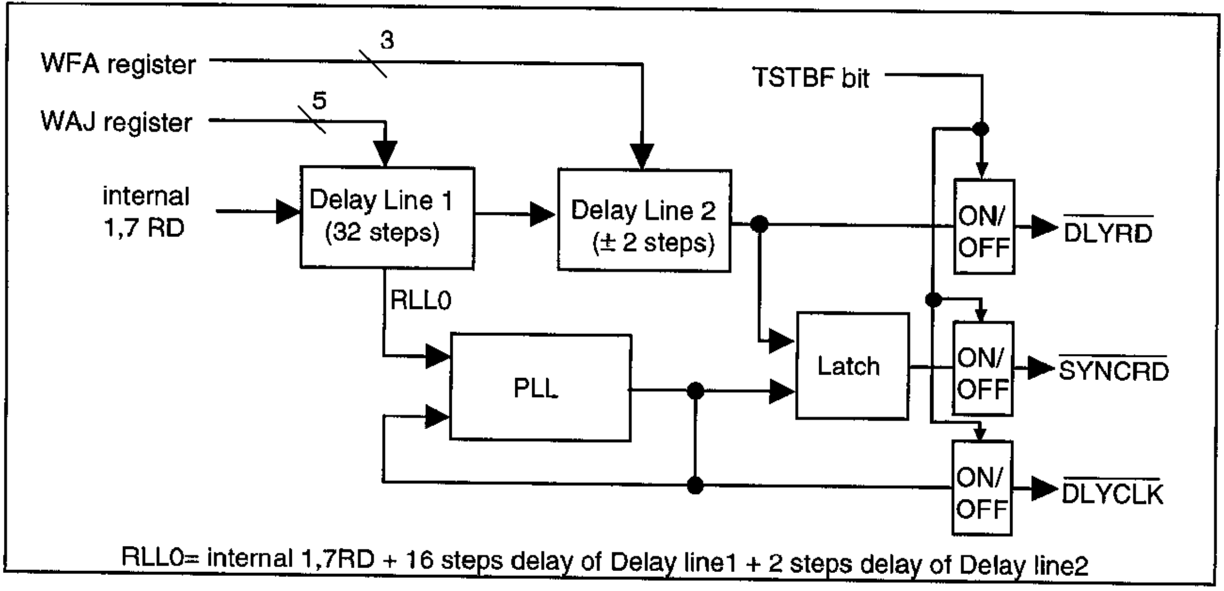
∗) 1-7 WDOUT is synchronized with the rising edge of CLKOUT

19. Window Adjustment Circuit

The HD153035F has two on-chip delay lines for centering the decode window. First delay line has 32 taps for coarse adjustment that can be selected by register WAJ. Second delay line has 5 taps for fine adjustment that can be selected by register WFA.

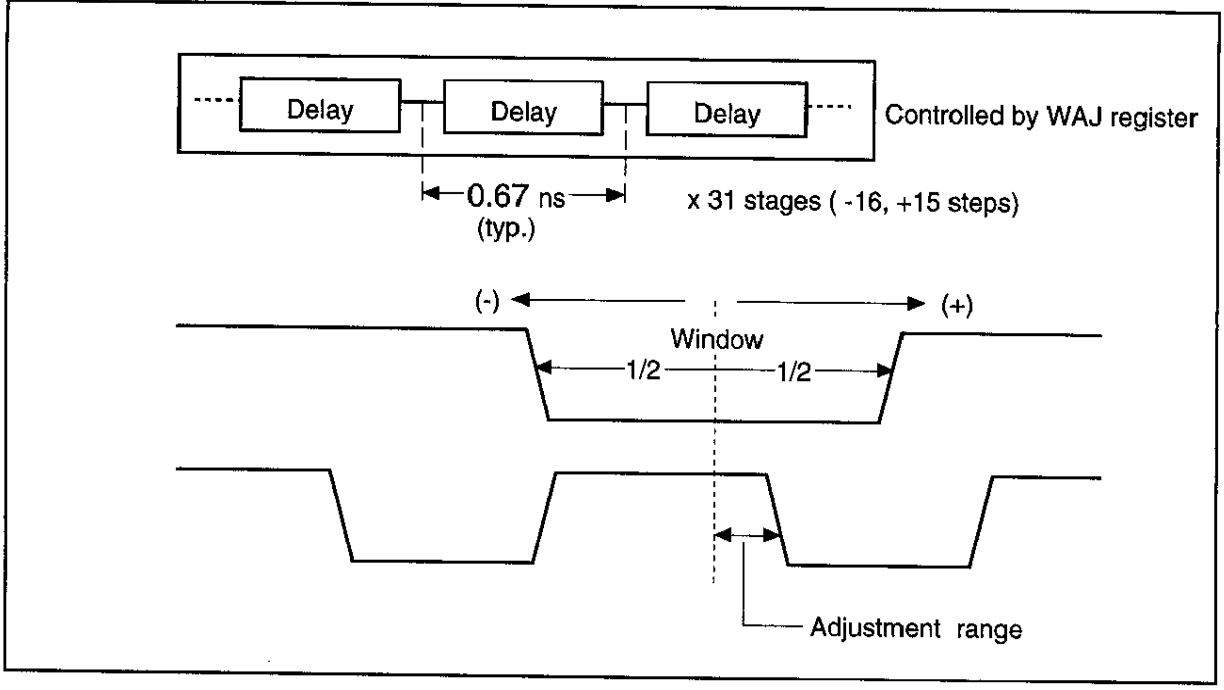
Window centering adjustment can be performed automatically by a microcontroller. This adjustment function can also be used for preshipment window margin test.

(1) Circuit Configuration



RLLO= internal 1,7RD + 16 steps delay of Delay line1 + 2 steps delay of Delay line2

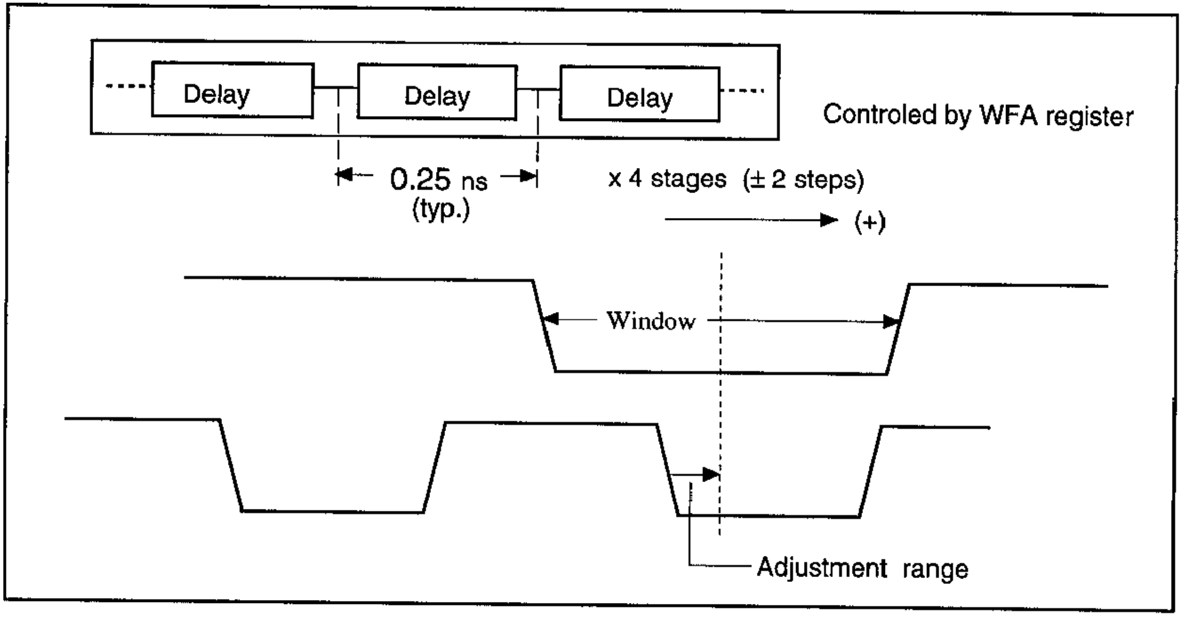
(2) Delay Line 1 (Coarse Window Adjustment)



WAJ Register

MSB 4	3	2	1	LSB 0	Delay line 1 tap No.
0	0	0	0	0	– 16 (- 10.72 ns typ.)
	⋮				⋮
0	1	1	1	0	– 2 (- 1.34 ns typ.)
0	1	1	1	1	– 1 (- 0.67 ns typ.)
1	0	0	0	0	0
1	0	0	0	1	+ 1 (+ 0.67 ns typ.)
1	0	0	1	0	+ 2 (+ 1.34 ns typ.)
	⋮				⋮
1	1	1	1	1	+ 15 (+ 10.05 ns typ.)

(3) Delay Line 2



WFA Register

MSB 7	6	LSB 5	Delay line 2 tap No.
0	1	0	– 2 (- 0.50 ns typ.)
0	0	1	– 1 (- 0.25 ns typ.)
0	0	0	0
1	0	1	+ 1 (+ 0.25 ns typ.)
1	1	0	+ 2 (+ 0.50 ns typ.)

20. Decode Clock Generator's VFO

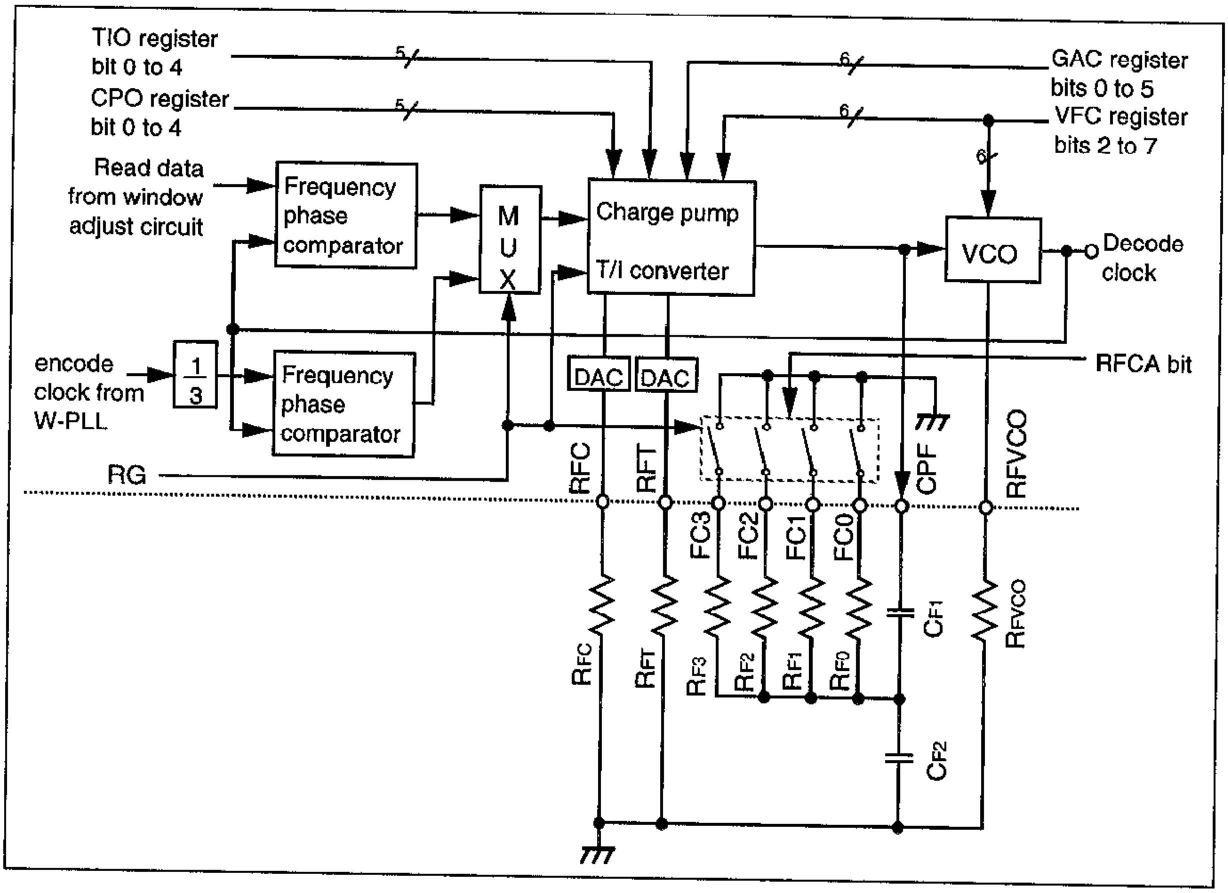


Fig. 20.1 R-PLL Block Diagram

Function

- The phase of the VCO clock is synchronized to the read data from the window adjust circuit.
- The frequency-phase comparator operates in the frquency-phase comparison mode while acquiring phase lock during the sync field, and in phase comparison mode during synchronization in the data field.
- The charge pump and T/I converter circuits both operate while the phase lock is being acquired. During synchronization, only the T/I converter operates.
- The VFO is synchronized with the encode clock until the read gate signal (RG) is asserted.
- The VCO center frequency can be programmed by rewriting bits 0 to 7 of the VFC register, so multiple zone recording can be implemented with a single external resistor.
- The charge pump can select eight levels currents, the reference value of which is controlled by external resistor R_{FC}. Bit 3 to 5 in register GAC selects these eight levels.
- The T/I converter provides one of eight output currents as selected by bits 0 to 2 of the GAC register.
- The loop filter attenuation ζ can be selected by bit 6 (RFCA bit) of register GAC (two selections). Independent settings can be made for high gain and normal gain.

21. Encode Clock Generator's Frequency Synthesizer

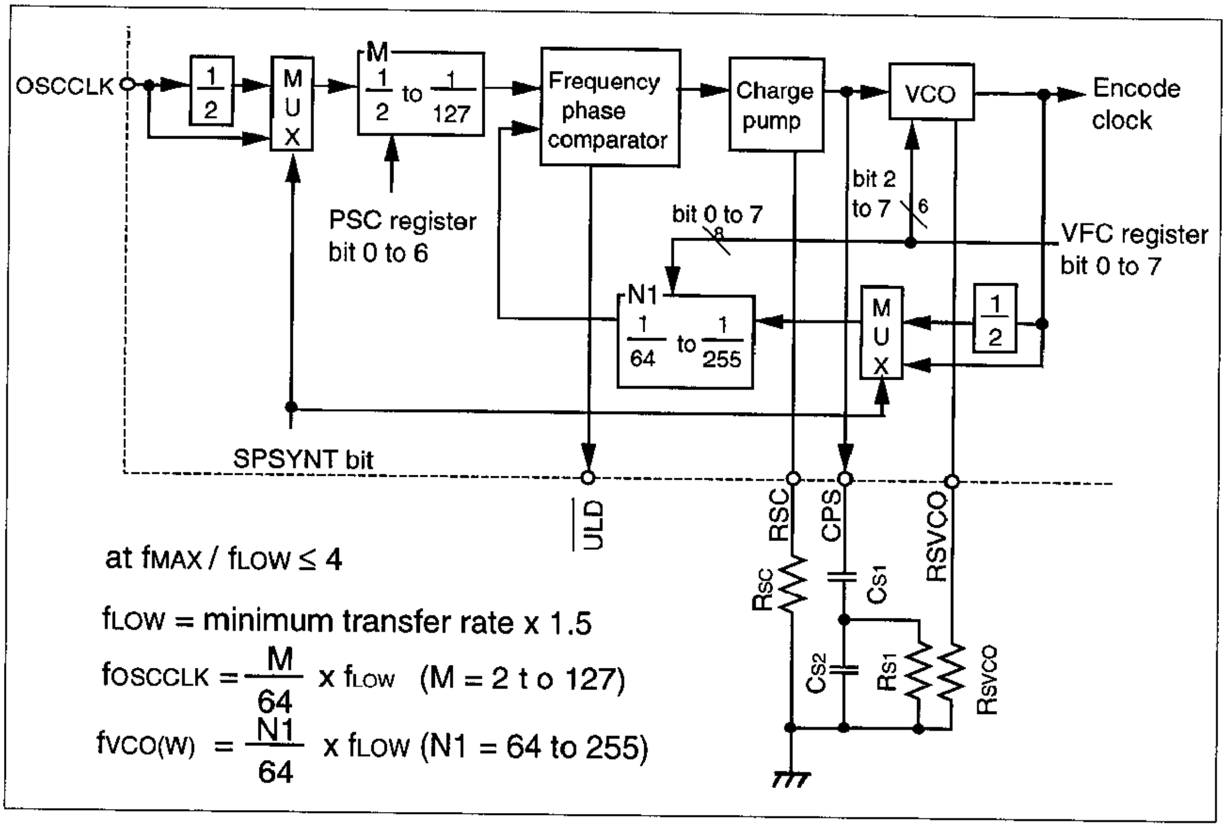


Fig. 21.1 W-PLL Block Diagram

Function

- A PLL-type frequency synthesizer generates the encode clock.
- The encode clock frequency can be set by bits 0 to 7 of register VFC to a value of N/64 times the minimum data transfer rate (innermost track on the disk), where $64 \leq N \leq 255$.
- The lock/$\overline{\text{unlock}}$ monitor function (ULD line) can prevent data from being written when a drive fault occurs.
- The VCO center frequency can be selected by bits 0 to 7 of register VFC, so a single external resistor RSC covers the entire setting range.
- The operating mode can be selected by bit 7 (SPYNT bit) of GACregister. When use over 50 Mbps, this bit has to be set low.

Operation

- Input a reference clock to OSCCLK at (1.5 xM)/64 times the driver's minimum transfer rate.
This signal input to the frequency-phase
- comparator at 1/M .
The VCO clock is divided by 1/64 to 1/255,
- depending on bits 0 to 7 of VFC register, and input to the frequency-phase comparator.

$$2 \leq M \leq 127 \text{ , } 64 \leq N1 \leq 255.$$

$f_{VCO(W)}$: VCO output frequency

f_{LOW} : Encoder clock frequency corresponding to the minimum transfer rate.

22. Calculation of PLL Constants

I. Decode Clock Generator's VFO (R-PLL)

1. VCO center frequency f_{OR}

$$f_{OR} = \frac{(3.375 \times 10^9) \bullet N}{R_{FVCO}} \quad (Hz) \cdots\cdots (I.1)$$

2. VCO gain K_{OR}

$$K_{OR} = (1.536 \times 10^9) \bullet \sqrt{\frac{N}{R_{FVCO}}} \quad \left(\frac{rad}{sec \bullet V}\right) \cdots\cdots (I.2)$$

3. Charge pump current I_{CR}

$$I_{CR} = \frac{2.5 \times 10^4}{R_{FC}} \bullet \frac{P}{8} \quad (mA) \cdots\cdots (I.3)$$

where $1 \leq P \leq 8$

4. T/I converter current I_{TR}

$$I_{TR} = (3.52 \times 10^3) \bullet \frac{N \bullet L}{500 + R_{FT}} \quad (\mu A) \cdots\cdots (I.4)$$

where $0 \leq L \leq 7$

5. Characteristic frequency (high gain) ω_{nRH}

$$\omega_{nRH} = \sqrt{\frac{K_{OR} \bullet \left(\frac{I_{CR}}{6} + I_{TR}\right)}{\pi \bullet C_{F1}}} \quad \left(\frac{rad}{sec}\right) \cdots\cdots (I.5)$$

6. Characteristic frequency (normal gain) ω_{nRN}

$$\omega_{nRN} = \sqrt{\frac{K_{OR} \bullet I_{TR}}{\pi \bullet C_{F1}}} \quad \left(\frac{rad}{sec}\right) \cdots\cdots (I.6)$$

7. Attenuation (high gain) ζ_{RH}

$$\zeta_{RH} = \frac{(C_{F1} + C_{F2})}{2} \bullet \frac{1}{\frac{1}{R_{FA}} + \frac{1}{R_{FB}}} \bullet \omega_{nRH} \cdots\cdots (I.7)$$

where R_{FA} and R_{FB} = R_{F0} and R_{F1} when GAC register bit 6 = 0
R_{F2} and R_{F3} when GAC register bit 6 = 1

8. Attenuation (normal gain) ζ_{RN}

$$\zeta_{RN} = \frac{(C_{F1} + C_{F2})}{2} \cdot R_{FA} \cdot \omega_{nRN} \quad \cdots\cdots (\text{I}.8)$$

where R_{FA} = R_{F0} when GAC register bit 6 = 0
R_{F2} when GAC register bit 6 = 1

II. Encode Clock Generator's Frequency Synthesizer (W-PLL)

1. VCO center frequency f_{ow}

$$f_{ow} = \frac{(6.975 \times 10^{9}) \cdot N}{R_{SVCO}} \ (\text{Hz}) \quad \cdots\cdots (\text{II}.1)$$

2. VCO gain K_{ow}

$$K_{ow} = (1.056 \times 10^{9}) \cdot \sqrt{\frac{N}{R_{SVCO}}} \left(\frac{\text{rad}}{\text{sec} \cdot \text{V}}\right) \quad \cdots\cdots (\text{II}.2)$$

3. Charge pump current ratio N_C

$$N_C = \overset{\text{Note1}}{\text{int}}\left[\, 16 \cdot \sqrt{\frac{N1}{N1_{MAX}}} - 8 \,\right] \quad \cdots\cdots (\text{II}.3)$$

When $N1 = N1_{MAX}$, set the N_C=7

Note1: int[ ] is the integer value calculated by discarding the fractional part of the value.

4. Charge pump current I_{CW}

$$I_{CW} = \frac{5.3}{R_{SC}} \cdot \left(1 + \frac{N_C}{8}\right) \quad (\text{A}) \quad \cdots\cdots (\text{II}.4)$$

5. Characteristic frequency ω_{nW}

$$\omega_{nW} = \sqrt{\frac{K_{ow} \cdot I_{CW}}{2\pi \cdot N1 \cdot C_{S1}}} \left(\frac{\text{rad}}{\text{sec}}\right) \quad \cdots\cdots (\text{II}.5)$$

6. Attenuation ζ_W

$$\zeta_W = \frac{(C_{S1} + C_{S2})}{2} \cdot R_{S1} \cdot \omega_{nW} \quad \cdots\cdots (\text{II}.6)$$

Table 22. 1 VCO Oscillation Frequency and Transfer Speed for Settings of Register VFC

(at fMAX / fLOW = 3.98)

N1	VFC register MSB LSB 7 6 5 4 3 2 1 0	N	Transfer speed (Mbps)	Transfer speed ratio	1-7 clock frequency (MHz)	Example: R_{FVCO}= 2.55 kΩ, R_{SVCO} = 5.24 kΩ	
						R-VCO setting frequency (MHz)	W-VCO setting frequency (MHz)
0	Inhibit						
•							
•							
63							
64	0 1 0 0 0 0 0 0	16	14.00	1.000	21.00	21.18	21.30
65	0 1 0 0 0 0 0 1	16	14.22	1.016	21.33	21.18	21.30
66	0 1 0 0 0 0 1 0	16	14.44	1.031	21.66	21.18	21.30
67	0 1 0 0 0 0 1 1	16	14.66	1.047	21.98	21.18	21.30
68	0 1 0 0 0 1 0 0	17	14.88	1.063	22.31	22.50	22.63
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
127	0 1 1 1 1 1 1 1	31	27.78	1.984	41.67	41.03	41.26
128	1 0 0 0 0 0 0 0	32	28.00	2.000	42.00	42.35	42.60
129	1 0 0 0 0 0 0 1	32	28.22	2.016	42.33	42.35	42.60
130	1 0 0 0 0 0 1 0	32	28.44	2.031	42.66	42.35	42.60
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
253	1 1 1 1 1 1 0 1	63	55.34	3.95	83.02	83.38	83.86
254	1 1 1 1 1 1 1 0	63	55.56	3.97	83.34	83.38	83.86
255	1 1 1 1 1 1 1 1	63	55.78	3.98	83.67	83.38	83.86

Table 22. 2 Charge pump Output Current Settings with GAC Register

	GAC register					Example: R_{FC} = 5.1kΩ
Bits	5	4	3	P	Charge pump output current ratio	Charge pump output current (mA)
1	0	0	0	1	1	0.613
2	0	0	1	2	2	1.226
3	0	1	0	3	3	1.838
4	0	1	1	4	4	2.451
5	1	0	0	5	5	3.064
6	1	0	1	6	6	3.677
7	1	1	0	7	7	4.289
8	1	1	1	8	8	4.902

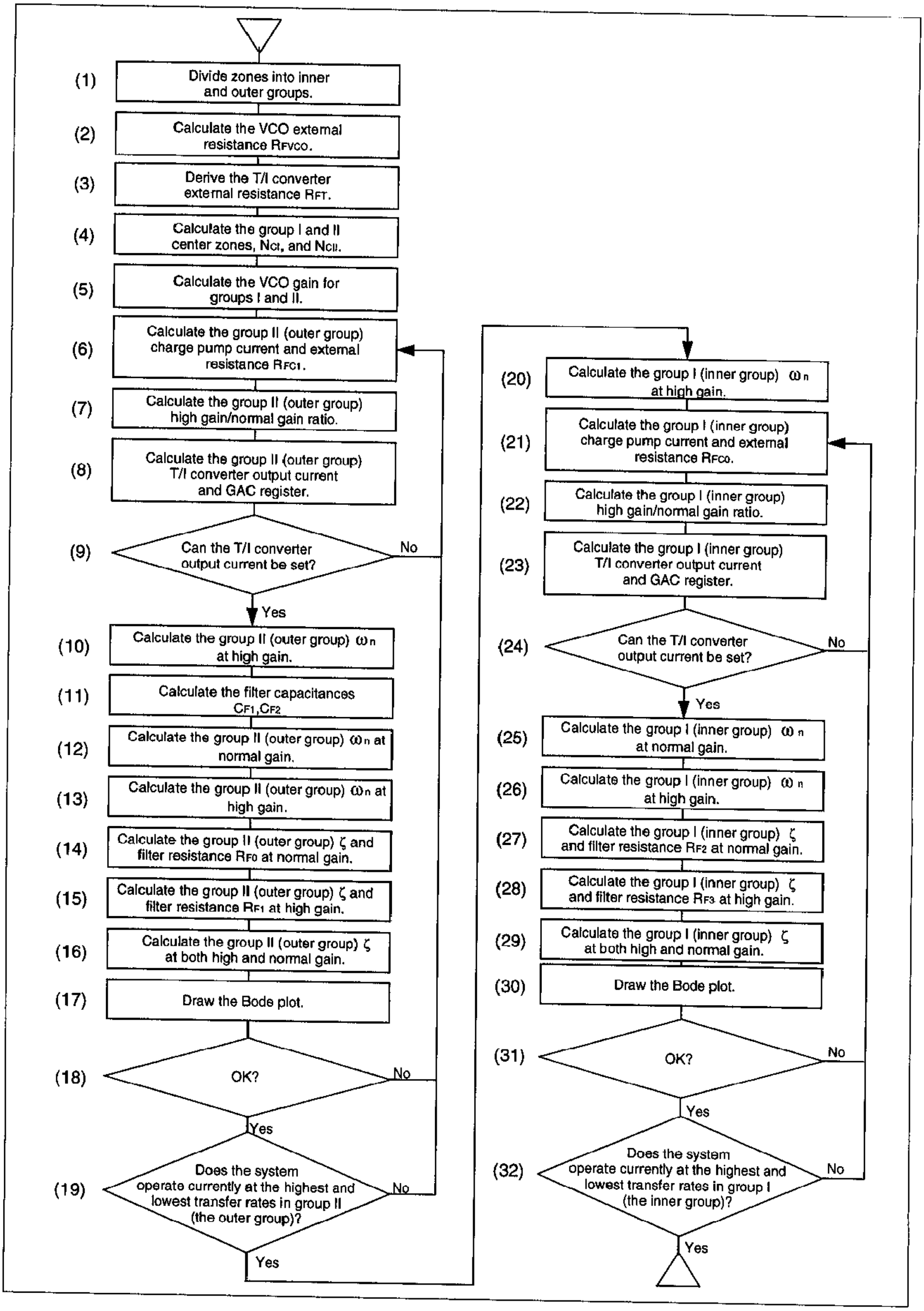
$$I_{CR} = \frac{2.5 \times 10^4}{R_{FC}} \bullet \frac{P}{8} \quad \text{(mA)}$$

Table 22. 3 T/I Output Current Settings with GAC Register

	GAC register					Example: R_{FT} =11kΩ N=63
Bits	2	1	0	L	T/I output current ratio	T/I output current (μA)
1	0	0	0	0	0	0.0
2	0	0	1	1	1	19.3
3	0	1	0	2	2	38.6
4	0	1	1	3	3	57.9
5	1	0	0	4	4	77.1
6	1	0	1	5	5	96.4
7	1	1	0	6	6	115.7
8	1	1	1	7	7	135.0

$$I_{TR} = (3.52 \times 10^3) \bullet \frac{N \bullet L}{500 + R_{FT}} \quad (\mu A)$$

23. Flowchart of Procedure for Setting Decode Clock Generator VFO (R-PLL) Constants



24. Flowchart Explanation (R-PLL)

(1) Divide zones into groups

Divide the zones selected in synthesizer step (1) into two groups (I and II) having equal frequency ranges. Divide the groups at the following transfer rate TRgr:

$$TRgr = \sqrt{TRmin \bullet TRmax}$$

(2) VCO external resistance R_{FVCO}

Use equation (I.1) to calulate the external resistance R_{FVCO} that makes the VCO oscillate at 1.5 times the minimum transfer rate (N=16)

(3) T/I converter external resistance R_{FT}

Find the R_{FT} values at the minimum transfer rate as shown in Fig. 24.2.(R_{FT} vs Data transfer rate).

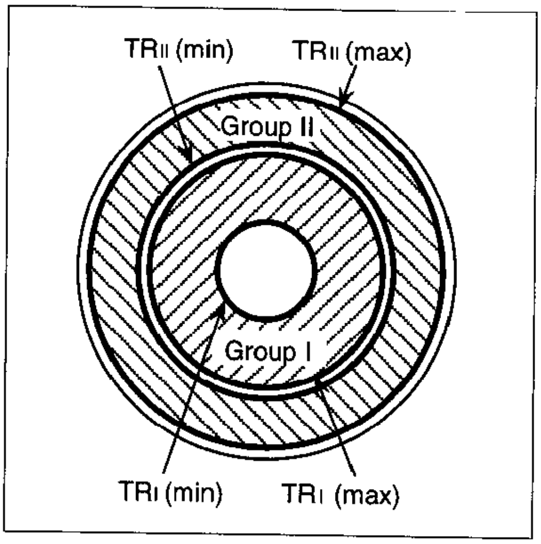


Fig. 24.1. Divide zone image

(4) Center zones TR_{CI} and TR_{CII} of group I and II

Calculate the midpoint (TR_{CI} & TR_{CII}) between the minimum transfer rate (TRmin) and maximum transfer rate (TRmax) at each groups (caluculate at step (1)), and from the zones selected in step (1), find the value of N (N_{CI} & N_{CII}) that comes closest toTR_{CI} & TR_{CII}.

$$TR_{CI} = \frac{TR_I(min)+TR_I(max)}{2}, \quad TR_{CII} = \frac{TR_{II}(min)+TR_{II}(max)}{2}$$

(5) VCO gain K_{OR} in groups I and II

Use equation (I.2) to calculate the VCO gain K_{OR} at the center zones ($N=N_{CI}$ and $N=N_{CII}$) in groups I and II.

(6) Charge pump current I_{CR} in group II

Select the charge pump current level within the following range:

$$I_{CR} \leq 5.0 \quad (mA)$$

Calculate the values for the external resistances R_{FC} and P from equation (I.3). So that the current has the desired value. See Table 22.2 for the relationship between the value of P and GAC register.

(7) High gain/normal gain ratio in group II.

Set the current ratio g_G between high and normal gain. This value is depend on HDA system. Normally,

$g_G = 16$ (Adjust so that this value is in the range 11 to 21.)

(8) Group II T/I conversion output current I

Determine the value of $L(0 \leq L \leq 7)$ using equation (I.4), so that the following equation is satisfied :

$$I_{TR} = \frac{I_{CR}}{6(g_G-1)}$$

See Table 22.3 for the relationship between the value of L and GAC register.

(9) Analysis

Determine if the T/I converter output current can be set.

(10) Group II High Gain ω_n

After determining the group II center zone N_{CII} phase pull-in time Taq taking into consideration the high gain set time, and determine the high gain characteristic frequency ω_{nRH}. using the following equation.

$$\omega_{nRH} \bullet T_{aq} = 2.5$$

(Adjust so that this value is in between 2 to 4.)

(11) Filter Capacitances C_{F1} and C_{F2}

Calculate the filter capacitance C_{F1} by substituting the high gain characteristic frequency ω_{nRH} calculated in item (10) above in formula I.5.

Also, set the ratio between C_{F1} and C_{F2} taking into consideration high region jitter suppression and phase margin. We recommend deriving C_{F2} using the following equation.

$$C_{F2} = \frac{1}{45} \bullet C_{F1}$$

(Adjust so that this value is in between 1/20 to 1/100.)

(12) Group II Normal Gain ω_n

Compute the normal gain characteristic frequency ω_{nRN} by substituting the derived value of C_{F1} into formula I.6.

(13) Group II High Gain ω_n

Compute the high gain characteristic frequency ω_{nRH} by substituting the derived value of C_{F1} into formula I.5.

(14) Group II Normal Gain ζ_{RN} and Filter Resistance R_{F0}

Set the normal gain attenuation ratio ζ_{RN} with stability as the main criteria.

The equation below indicate the recommend value . $\zeta_{RN} \cong 1.0$
Calculate the filter resistance R_{F0} by substituting that value into formula I.8

(15) Group II High Gain ζ_{RH} and Filter Resistance R_{F1}

Set the normal gain attenuation ratio ζ_{RH} with stability as the main criteria.

The equation below indicate the recommend value . $\zeta_{RH} \cong 0.8$
Calculate the filter resistance R_{F1} by substituting that value into formula I.7.

(16) Group II High Gain ζ_{RH} and Normal Gain ζ_{RN}

Calculate the attenuation ratios ζ_{RH} and ζ_{RN} by substituting the values of R_{F0} and R_{F1} into equations I.7 and I.8.

(17) Bode Plot Construction

Compute the open loop transfer function G(s) and construct the Bode plot.

(18) Analysis

Determine if the system is suitable from the open and closed loop characteristics.

(19) Analysis at TRmin and TRmax

Repeat the analysis of item (17) and (18) for group II TRmin and TRmax.

(20) Group I High Gain ω_n

After determining the group I center zone N_{CI} phase pull-in time Taq, taking into consideration the high gain set time, and determine the high gain chracteristic frequency ω_{nRH} using the following equation

$\omega_{nRH} \bullet Taq = 2.9$

(Adjust so that this value is in between 2 to 4.)

(21) Group I Charge Pump Current I_{CR}

Calculate the charge pump current I_{CR} by substituting the high gain characteristic frequency ω_{nRH} computed in item (20) above into formula I.5.

Here, set the charge pump current level within the following range:

$I_{CR} \leq 5.0mA$

Now , derive a value for P using equation I.3 so that the desired charge pump current is achieved.

See Table 22.2 for the relationship between the value P and GAC register.

(22) Group I High gain / Normal Gain Ratio

Set the high gain to normal gain current ratio g_G.

$g_G = 16$ (Adjust so that this value is in between 11 to 21.)

(23) Group I T/I Converter Output Current I_{TR}

Determine a value of L ($0 \leq L \leq 7$) using equation (I.4) so that the following equation

$$I_{TR} = \frac{I_{CR}}{6(g_G-1)}$$

See Table 22.3 for the relationship between the value L and GAC register.

(24) Analysis

Determine if the T/I converter output current should be set .

(25) Group I Normal Gain ω_n

Calculate the normal gain characteristic frequeny ω_{nRN} by substituting the I_{TR} derived above into formuia I.6.

(26) Group I High Gain ω_n

Calculate the high gain characteristic frequeny ω_{nRH} by substituting the I_{CR} derived above into formuia I.5.

(27) Group I Normal Gain ζ_{RN} and Filter Resistance R_{F2}

Set the normal gain attenuation ration ζ_{RN} with stability as the main criteria.
The equation below indicate the recommend value.
$\zeta_{RN} \cong 1.0$
Calculate the filter resistance R_{F2} by substituting that value into formula I.8.

(28) Group I High Gain ζ_{RH} and Filter Resistance R_{F3}

Set the high gain attenuation ration ζ_{RH} with stability as the main criteria.
The equation below indicate the recommended value.
$\zeta_{RH} \cong 0.8$
Calculate the filter resistance R_{F3} by substituting that value into formula I.7.

(29) Group I High Gain ζ_{RH} and Normal Gain ζ_{RN}

Calculate the attenuation ratios ζ_{RH} and ζ_{RN} by substituting the values of R_{F2} and R_{F3} into equations I.7 and I.8.

(30) Bode Plot Construction

Compute the open loop transfer function G(s) and construct the Bode plot.

(31) Analysis

Determine if the system is suitable from the open and closed loop characteristics.

(32) Analysis to determine TRmin and TRmax

Repeat the analysis of items (30) and (31) for group I TRmin and TRmax.

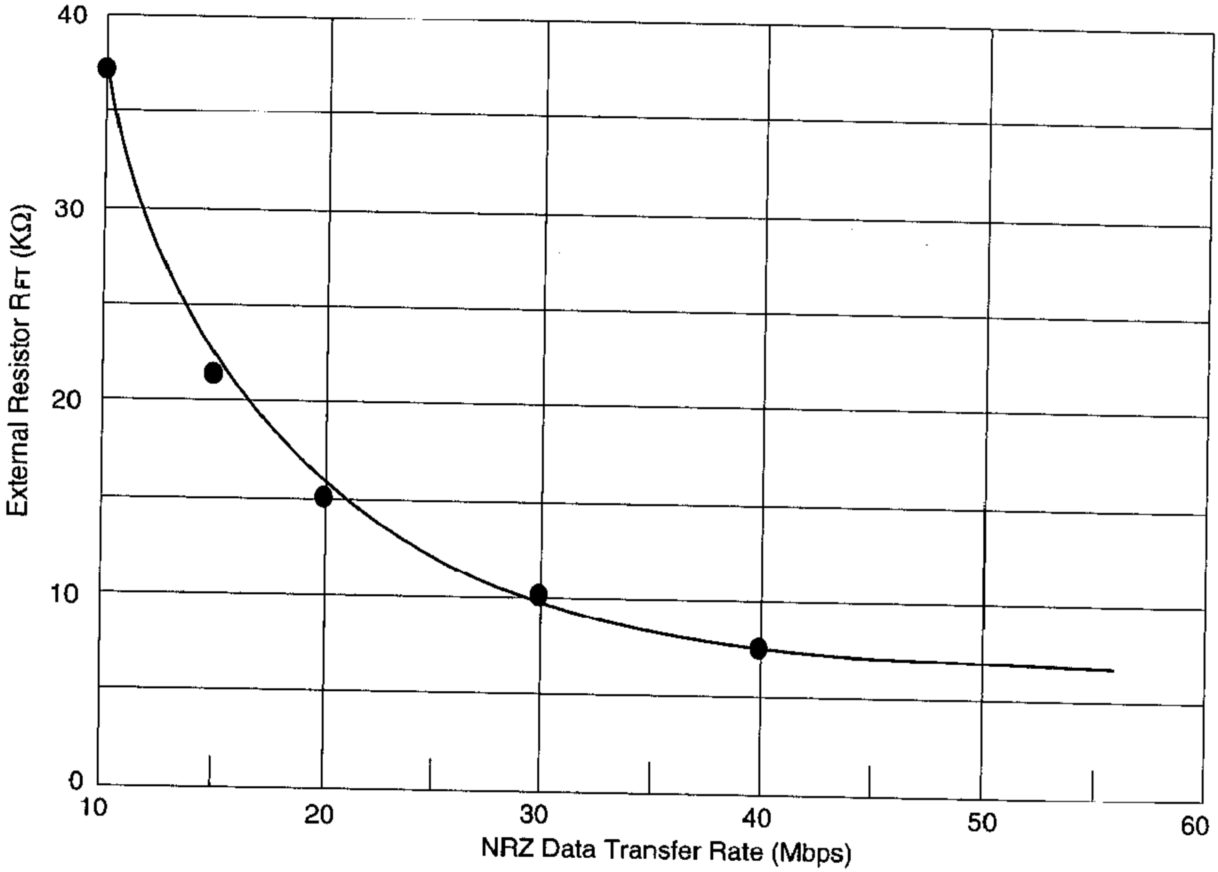


Fig 24. 2 T/I Converter Circuit External Resistor RFT vs NRZ Data Transfer Rate

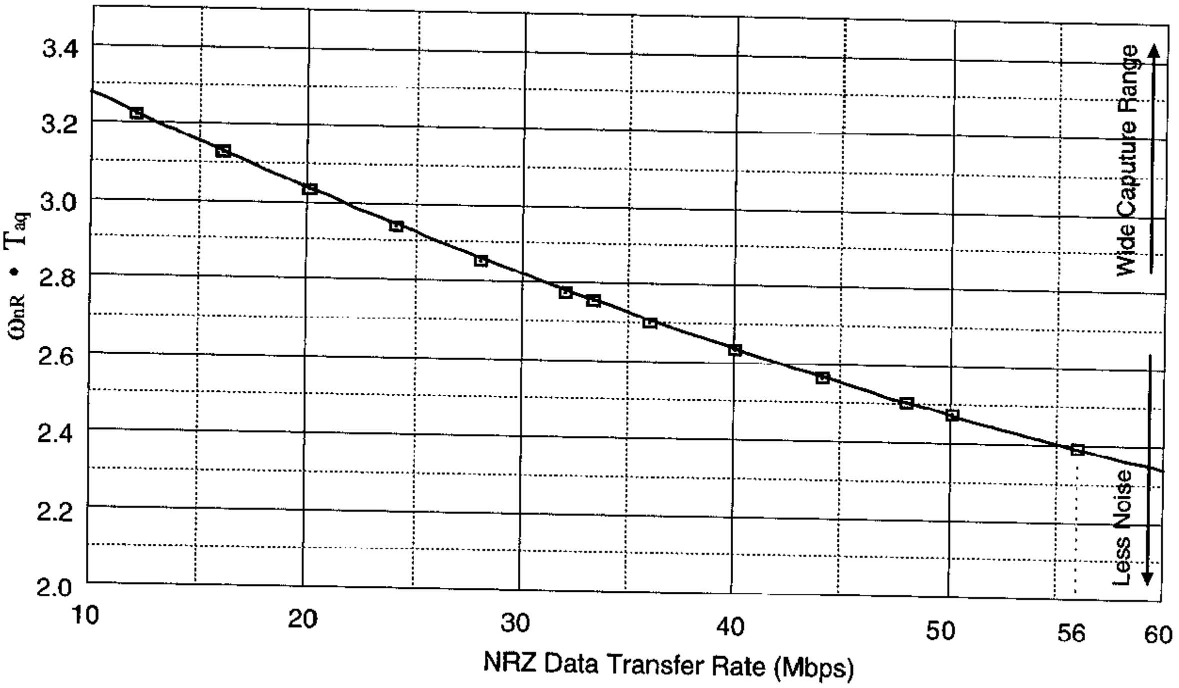


Fig 24. 3 $\omega_{nR} \cdot T_{aq}$ vs NRZ Data Transfer Rate (R-PLL)

25. Calculation example of HD153035F R-PLL Constants

Transfer rate ; 28Mbps , 56Mbps 2 zones

(1) R_{FVCO}

Oscillation frequency (f_o)= 36 MHz at R_{FVCO} = 3 kΩ • • • • 24 Mbps

At 28 Mbps case, f_o = 42 MHz

42 MHz x R_{FVCO} = 36 MHz x 3 kΩ

R_{FVCO} = 2.57 kΩ

∴ R_{FVCO} = 2.55KΩ • • • • f_{OSCR} = 42.4 MHz

Error of oscillation frequency is

$(f_{osc} - f_o) \div f_o = 0.84\ \% \leq 5\ \%$

(2) R_{FT} = 11KΩ

See Fig. 24.2

(3) VCO Gain K_{OR}

$$K_{OR\,28} = 1.536 \times 10^9 \sqrt{\frac{32}{2.55 \times 10^3}} = 172.1\ \mathrm{Mrad/s \bullet V}$$

$$K_{OR\,56} = 1.536 \times 10^9 \sqrt{\frac{63}{2.55 \times 10^3}} = 241.4\ \mathrm{Mrad/s \bullet V}$$

(4) Charge Pump Current I_{CR}

R_{FC} = 5.1 KΩ

$$I_{CR\,56} = \frac{2.5\mathrm{x}10^4}{5.1 \times 10^3} \bullet \frac{P}{8} \leq 5\ \mathrm{mA}$$

$I_{CR\,56}$ = 4.9 mA (P=8)

(5) T/I Current I_{TR}

$$I_{TR\,56} = \frac{4.9}{6 \bullet (16 - 1)} = 54.4\ \mu\mathrm{A}$$

R_{FT} = 11 KΩ

$$I_{TR\,56} = 3.52 \times 10^3 \bullet \frac{N \bullet L}{500 + R_{FT}}$$

∴ $I_{TR\,56}$ = 57.9 μA (N=63,L=3)

(6) $\omega_{nRH} \bullet T_{aq\,56} = 2.4$

$T_{aq\,56}$ = 0.57μ s (6 bytes x 2/3)

ω_{nRH} = 4.21 Mrad / s

$$\omega_{nRH\,56} = \sqrt{\frac{K_{OR\,56} \bullet \left(\frac{I_{CR\,56}}{6} + I_{TR\,56}\right)}{\pi \bullet C_{F1}}}$$

$$4.21 \times 10^{6} = \sqrt{\frac{241.4 \times 10^{6} \bullet \left(\frac{4.9 \times 10^{-3}}{6} + 57.9 \times 10^{-6}\right)}{\pi \bullet C_{F1}}}$$

$C_{F1} = 3792$ pF

$C_{F2} = C_{F1} \div 45 = 84$ pF

$\therefore$ $C_{F1} = 3900$ pF, $C_{F2} = 82$ pF

$$\omega_{nRH\,56} = \sqrt{\frac{241.4 \times 10^{6} \bullet \left(\frac{4.9 \times 10^{-3}}{6} + 57.9 \times 10^{-6}\right)}{\pi \times 3900 \times 10^{-12}}} = 4.15 \text{ Mrad / s}$$

$$\omega_{nRN\,56} = \sqrt{\frac{241.4 \times 10^{6} \times 57.9 \times 10^{-6}}{\pi \times 3900 \times 10^{-12}}} = 1.07 \text{ Mrad / s}$$

(7) $\zeta_{RN\,56} = 1.0$, $\zeta_{RH\,56} = 0.8$

$R_{F2} = 1.0 \div \{ (3900 \times 10^{-12} + 82 \times 10^{-12}) \div 2 \times 1.07 \times 10^{6} \} = 469.4\ \Omega$

$R_{F3} = 122\ \Omega$

$\therefore$ $R_{F2} = 470\ \Omega$, $R_{F3} = 120\ \Omega$

$\zeta_{RN\,56} = 1.0$, $\zeta_{RH\,56} = 0.79$

(8) $\omega_n \bullet T_{aq\,28} = 2.86$

$T_{aq\,28} = 1.14\ \mu s$ (6 bytes x 2/3)

$\omega_{nH\,24} = 2.51$ Mrad / s

(9) Charge Pump Current I_{CR}

$$I_{CR\,28} = \frac{6\pi \bullet C_{F1} \bullet \omega_{nH}^{2}}{K_{OR\,28}} \bullet \frac{g_G - 1}{g_G} = 2.52 \text{ mA}$$

$\therefore$ $I_{CR\,28} = 2.45$ mA (P= 4)

(10) T/I Current I_{TR}

$I_{T\,28} = 2.45 \div 6 \div (16 - 1) = 27.2\ \mu A$

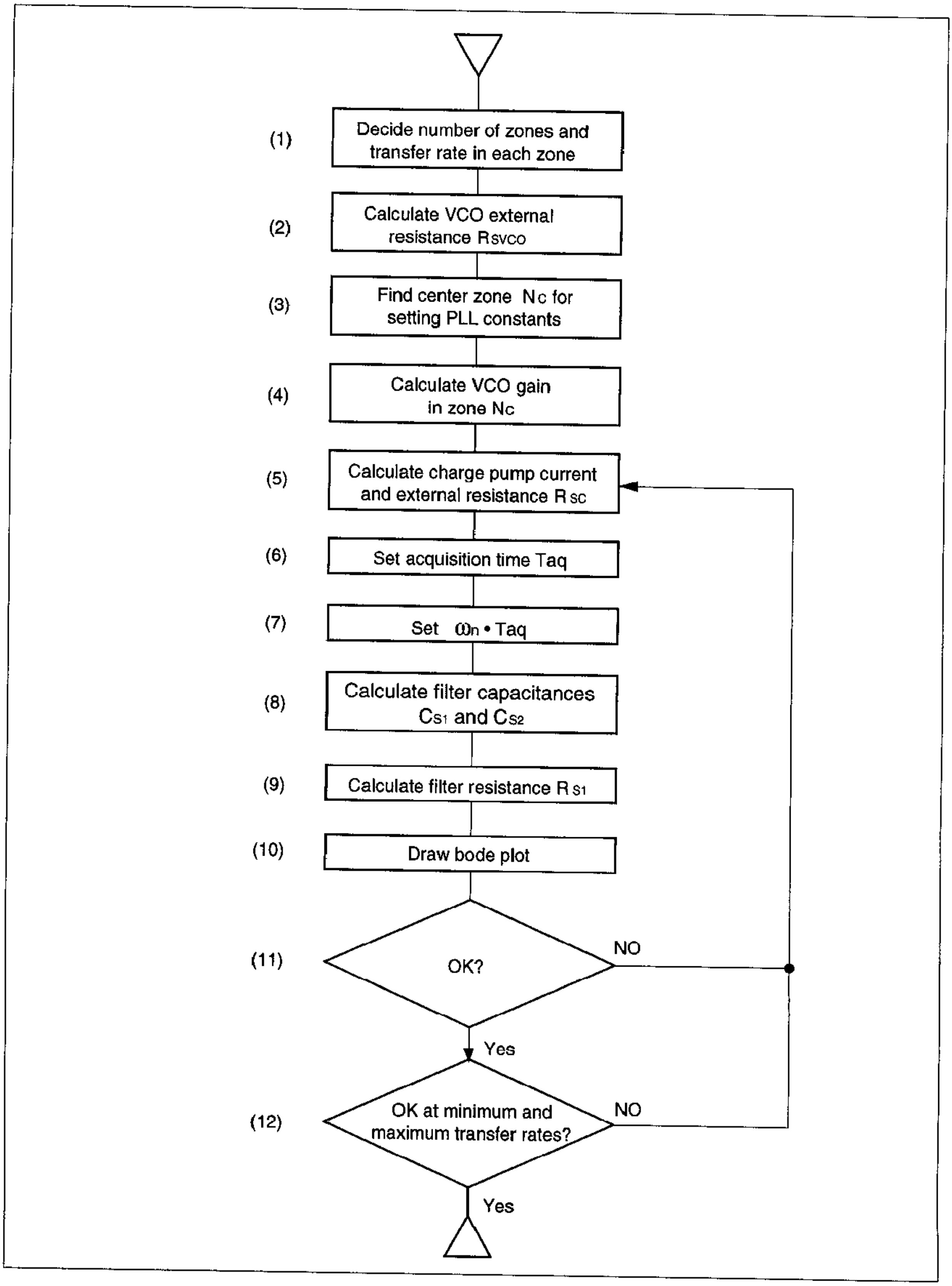
$\therefore$ $I_{T\,28} = 29.4\ \mu A$ (N = 32, L = 3), $\omega_{nH\,28} = 2.47$ Mrad / s, $\omega_{nN\,28} = 0.64$ Mrad / s

(11) $\zeta_{RN\,28} = 1.0$, $\zeta_{RH\,28} = 0.8$

$R_{F0} = 820\ \Omega$, $R_{F1} = 200\ \Omega$

$\zeta_{RN\,28} = 1.04$, $\zeta_{RH\,56} = 0.79$

26. Flowchart for Setting Encode Clock Generator's Frequency Synthesizer (W-PLL) Constants



27. Flowchart Explanation (W-PLL)

(1) Decide the number of zones and transfer rate in each zone

The HD153035F uses a frequency synthesizer to generate the reference clock, so the value of the transfer rate is quantized. If the lowest rate corresponds to N=16, the available rates are given by the formula:

$$TR_N = \quad TR_{min}, \quad 16 \le N \le 63$$

where, TR_N : Transfer rates in different zones
TR_{min} : Minimum transfer rate (innermost track)

(2) Calculate VCO external resistance R_{svco}

Use equation (II.1) to calculate the external resistance R_{svco} that makes the VCO oscillate at 1.5 times the minimum transfer rate (N=16)

(3) Find center zone (TRcen)

Calculate the midpoint (TRcen) between the minimum transfer rate (TRmin) and maximum transfer rate (TRmax), and from the zones selected in step (1), find the value of N (N_c) that comes closest to TRcen.

$$TRcen = \frac{TRmin+TRmax}{2}$$

(4) VCO gain K_{ow}

Use equation (II.2) to calculate the VCO gain ζ in the center zone ($N=N_c$)

(5) Charge pump current I_{cw}

Select the charge pump current within the following range:

$$I_{cw} \le 500 \ (\mu A)$$

Calculate the necessary external resistance R_{sc} from equation (II.4).

(6) Setting phase-lock acquisition time Taq

Decide the phase-lock acquisition time Taq, considering the change in characteristic frequency from zone to zone and the head seek time.

(7) Setting $(\omega_n \bullet T_{aq})$

Decide $(\omega_n \bullet T_{aq})$ the end of the phase-lock acquisition.

(8) Filter capacitances C_{S1} and C_{S2}

Decide the phase-lock acquisition time Taq, considering the charge in characteristic frequency from zone to zone and the head seek time.The value used in this data sheet is:

$$Taq = 0.1 \quad (ms)$$

The following formula gives an estimate of the acquisition time:

$$\omega_{nW} \bullet Taq = 2.25$$

Substitute the values of K_{CW} and Iow into equation (II.5) and combine this with the formula above to calculate the filter capacitance C_{S1}. To suppress jitter and allow enough phase margin, the following value is recommended for C_{S2} :

$$C_{S2} = \frac{1}{45} \bullet C_{S1}$$

(9) Filter resistance R_{S1}

To ensure loop stability, set the attenuation to approximately:

$$\zeta_{nw} = 1.0$$

Substitute this value into equation (I.6) to calculate the filter resistance R_{S1}.

(10) Bode plot

Calculate the open-loop transfer function G(s) and draw a Bode plot.

(11) OK?

Decide whether the open -loop and closed -loop characteristics are satisfactory.

(12) OK at TRmin and TRmax?

Repeat steps (8) and (9) for the minimum and maximum transfer rates.

28. Calculation example of HD153035F W-PLL Constants

NRZ transfer rate ; 28Mbps , 56Mbps (2 zones)

(1) Oscillation frequency f_{OW} = 42MHz (28 x 1.5), N=32

$$Rsvco = \frac{(6.975 \times 10^{9}) \bullet 32}{fow} = 5.31 \text{ k}\Omega$$

$\therefore$ Rsvco = 5.24 kΩ ••••• f_{OSCW} = 42.60 MHz

Error of oscillation frequency is

$| (foscw - fow) \div fow | = 1.4 \% \leq 5 \%$

(2) VCO gain Kow

$$\text{Kow}_{28} = 1.056 \times 10^{9} \sqrt{\frac{32}{5.24 \times 10^{3}}} = 82.5 \text{ Mrad / s} \bullet \text{V}$$

$$\text{Kow}_{56} = 1.056 \times 10^{9} \sqrt{\frac{63}{5.24 \times 10^{3}}} = 115.8 \text{ Mrad / s} \bullet \text{V}$$

(3) Charge Pump Current I_{cw}

$\text{Rcs} = 20\text{K}\Omega$

$$\text{Icw}_{28} = \frac{5.3}{20 \times 10^{3}} \left(1 + \frac{3}{8}\right) = 364.4\ \mu\text{A} \quad (\text{NC}=3)$$

$$\text{Icw}_{56} = \frac{5.3}{20 \times 10^{3}} \left(1 + \frac{7}{8}\right) = 496.9\ \mu\text{A} \quad (\text{NC}=7)$$

(4) Cs_1, Cs_2

$\omega_n \bullet T_{aq} = 2.25$

$(\omega_n = 22.5 \text{ Krad / s})$ $(\text{taq} = 0.1 \text{ ms})$

$$22.5 \times 10^{3} = \sqrt{\frac{81.7 \times 10^{6} \times 364.4 \times 10^{-6}}{2\pi \bullet 128 \bullet \text{Cs}_{1\,28}}}$$

$\text{Cs}_{1\,28} = 76483 \text{ pF}$

$$22.5 \times 10^{3} = \sqrt{\frac{114.6 \times 10^{6} \times 496.9 \times 10^{-6}}{2\pi \bullet 255 \bullet \text{Cs}_{1\,56}}}$$

$\text{Cs}_{1\,56} = 73432 \text{ pF}$

$\therefore$ $\underline{\text{Cs}_1} = (76483 + 73432)/2 = 74958$

$\approx \underline{75000 \text{ pF}}$

$$\text{Cs}_2 = \frac{1}{45} \bullet \text{Cs}_1 = 1667$$

$\therefore$ $\underline{\text{Cs}_2 \approx 1600 \text{ pF}}$ RS1 = 1

(5) Rs_1

Attenuation $\zeta_{nw} = 1$

$$\zeta_{nw} = \frac{(75000+1600) \times 10^{-12}}{2} \bullet \text{Rs}_1 \bullet \omega_{nw}$$

$$\text{Rs}_1 = 1 \div \left\{ \frac{(75000+1600) \times 10^{-12}}{2} \times 22.0 \times 10^{3} \right\} = 1187\ \Omega$$

$\therefore$ $\underline{\text{Rs}_1 \cong 1.2 \text{ k}\Omega}$

$\omega_{nw\,28} = 22.22 \text{ Krad / s}$, $\zeta_{nw\,28} = 1.021$

$\omega_{nw\,56} = 21.77 \text{ Krad / s}$, $\zeta_{nw\,56} = 1.000$

29. Setting value of M and N1 for R-PLL and W-PLL

$$f_{1-7} \text{ (1-7 clock frequency)} = \frac{\text{OSCCLK}}{\text{M}} \times \text{N1}$$

$$\text{Errfw} = \frac{| f_{1-7} - \text{foscw} |}{\text{foscw}} \leq 5\ \%$$

$$\text{Errf}_{\text{R}} = \frac{| f_{1-7} - \text{fosc}_{\text{R}} |}{\text{fosc}_{\text{R}}} \leq 5\ \%$$

example : OSCCLK = 21 MHz, RFVCO = 2.55 kΩ, RSVCO = 5.24 kΩ, f_{1-7} = 42 MHz, 63 MHz, 84 MHz

M = 64, N1 = 128, N = 32 •••• f_{1-7} = 42.0 MHz, foscw = 42.60 MHz, fosc_{R} = 42.35 MHz
Errfw = 1.4 % < 5 %
Errf_{R} = 0.8 % < 5 %

M = 64, N1 = 192, N = 48 •••• f_{1-7} = 63.0 MHz, fosc = 63.89 MHz, fosc_{R} = 63.53 MHz
Errfw = 1.4 % < 5 %
Errf_{R} = 0.8 % < 5 %

M = 63, N1 = 252, N = 63 •••• f_{1-7} = 84.0 MHz, fosc = 83.86 MHz, fosc_{R} = 83.38 MHz
Errfw = 0.2 % < 5 %
Errf_{R} = 0.7 % < 5 %

30. Example of HD153035F PLL's external parts (28/42/56Mbps)

OSCCLK = 21 MHz

(A) R-PLL

R_{FVCO} = 2.55 kΩ
R_{FC} = 5.1 kΩ
R_{FT} = 11 kΩ
C_{F1} = 3900 pF
C_{F2} = 82 pF
R_{F3} = 120 Ω
R_{F2} = 470 Ω
R_{F1} = 200 Ω
R_{F0} = 820 Ω

Register Value

	28Mbps	42 Mbps	56 Mbps
VFC	1000 0000	1100 0000	1111 1100
GAC	0001 1011	0110 1011	0111 1011

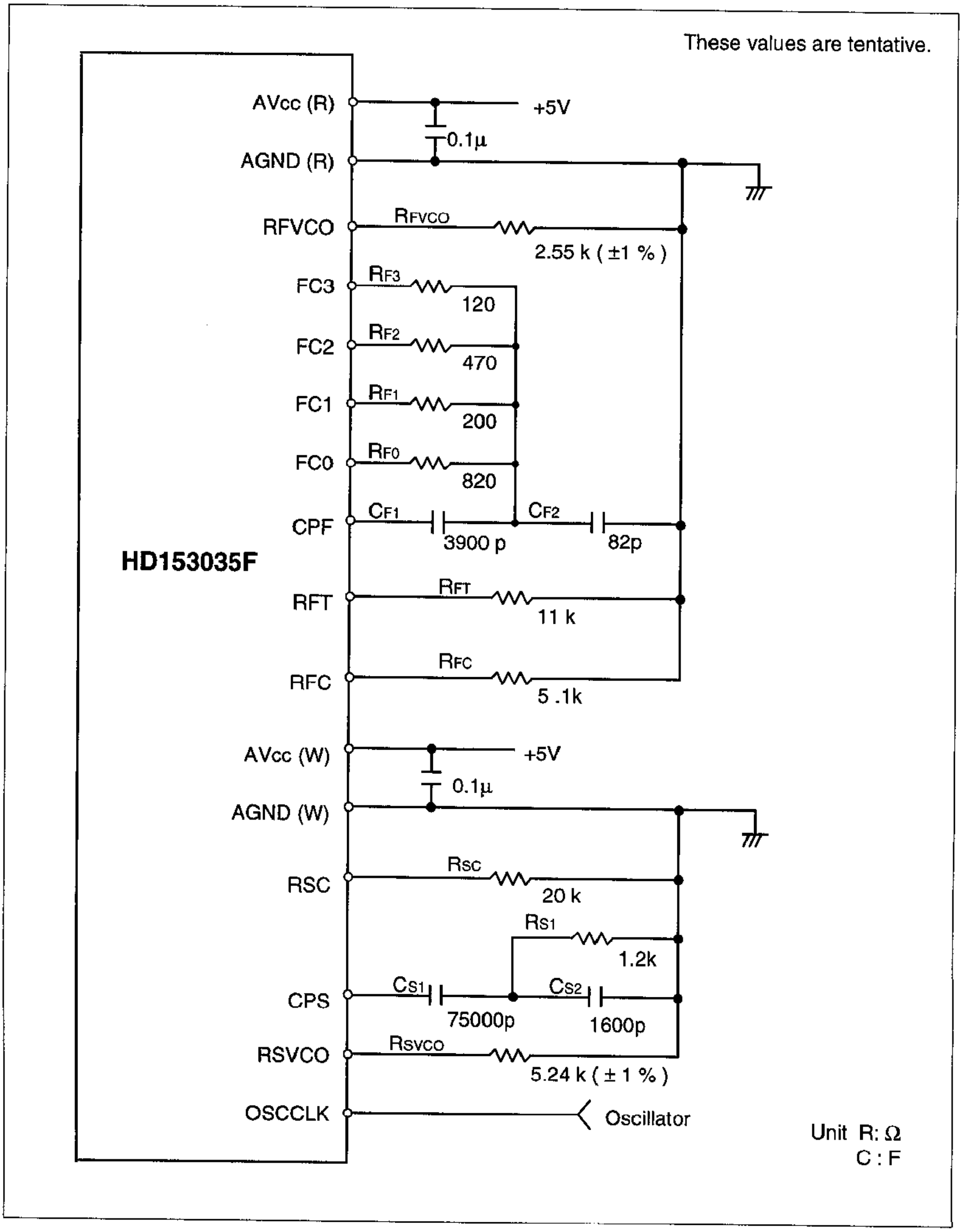
(B) W-PLL

R_{SVCO} = 5.24 kΩ
R_{CS} = 20 kΩ
C_{S1} = 75000pF
C_{S2} = 1600pF
R_{S1} = 1.2 kΩ

Register Value

	28Mbps	42 Mbps	56 Mbps
VFC	1000 0000	1100 0000	1111 1100
SGC	0000 0011	0000 0101	0000 0111
PSC	0010 0000	0010 0000	0011 1111

31. Example of External Components Connected to the Read PLL and Write PLL



32. 1-7 ENDEC

Encoder and Decoder

The encoder converts an NRZ signal to a (1,7) encoding, and the decoder converts a (1,7) signal back to an NRZ signal. The conversion table is shown in Table32.1.

The NRZ signal is encoded after being inverted. The inverted $\overline{\text{NRZ}}$ signal is encoded according to the conversion rules shown in fig. 32.1.

Therefore the disk controller should input the sequence "0000..." in the sync region. This will be converted to the (1,7) encoding 3T pattern "10010 0...".

The NRZ signal is encoded after being inverted.

For example, if the $\overline{\text{NRZ}}$ data 00 is to be (1,7) encoded, it is first inverted to 11.

Next, since the last bit of the previous conversion result A (100) was 0, and the next state of the NRZ data C is 01 ($\overline{C}$=10) , the NRZ data B (00) is converted to the (1,7) code 100.

In decoding the (1,7) code I (=100) to NRZ data (see Fig 32.2), since the previous data H was 100 and the next data J is 010, the decoding table gives 1 1 as the $\overline{\text{NRZ}}$ data. Inverting this gives the NRZ data 00, which is then output.

Table 32.1 Encoding Table (NRZ to (1,7) Code)

No.	Last Bit of the Previous (1,7) Code	$\overline{\text{NRZ}}$ Data Bit				(1,7) Code Bits (C_2,C_3,C_4)		
		Current (D_1,D_2)		Next (D_3,D_4)				
1	0	1	0	0	X	1	0	1
2	0	1	0	1	X	0	1	0
3	0	1	1	0	0	0	1	0
4	0	1	1	$\overline{0}$	$\overline{0}$	1	0	0
5	0	0	0	0	X	0	0	1
6	0	0	0	1	X	0	0	0
7	0	0	1	0	X	0	0	1
8	0	0	1	1	X	0	0	0
9	1	0	0	0	X	0	0	1
10	1	0	0	1	X	0	1	0
11	1	0	1	0	0	0	1	0
12	1	0	1	$\overline{0}$	$\overline{0}$	0	0	0

$\overline{0\ 0}$: Anything other than 0 0

X : Don't care

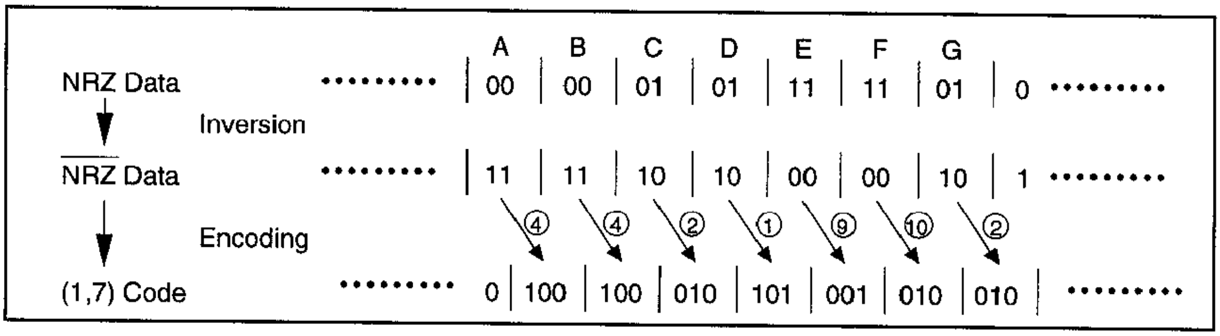


Fig. 32. 1 Shows an Example of NRZ to (1,7) Code Conversion.

Table 32. 2 Decoding Table ((1,7) Code to NRZ)

	(1,7) Code Bits										
No.	Previous			Current			Next			$\overline{\text{NRZ}}$ Data Bit	
1	X	1	0	0	0	0	X	X	X	0	0
2	X	0	0	0	0	0	X	X	X	0	1
3	X	X	X	1	0	0	X	X	X	1	1
4	X	X	0	0	1	0	$\overline{0}$	$\overline{0}$	X	1	0
5	X	X	0	0	1	0	0	0	X	1	1
6	X	X	X	1	0	1	X	X	X	1	0
7	X	0	0	0	0	1	X	X	X	0	1
8	X	1	0	0	0	1	X	X	X	0	0
9	X	X	1	0	0	1	X	X	X	0	0
10	X	X	1	0	1	0	$\overline{0}$	$\overline{0}$	X	0	0
11	X	X	1	0	1	0	0	0	X	0	1
12	X	X	1	0	0	0	X	X	X	0	1

$\overline{0\ 0}$: Anything other than 0 0
X : Don't care

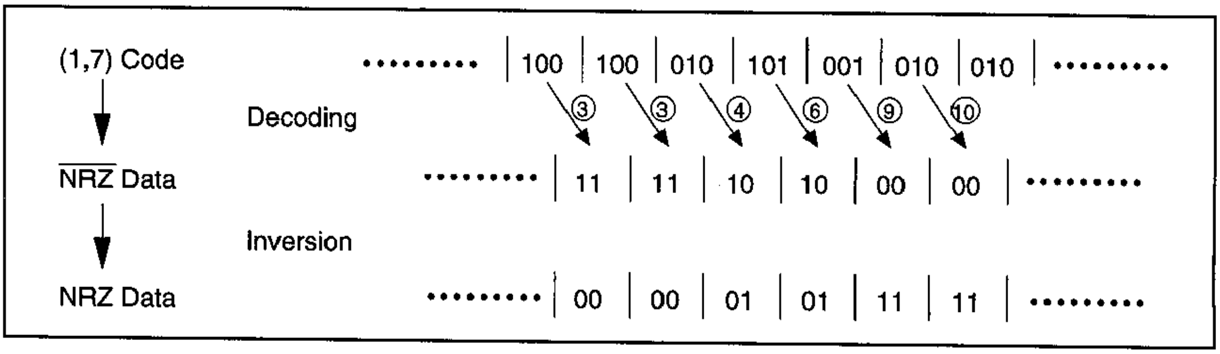
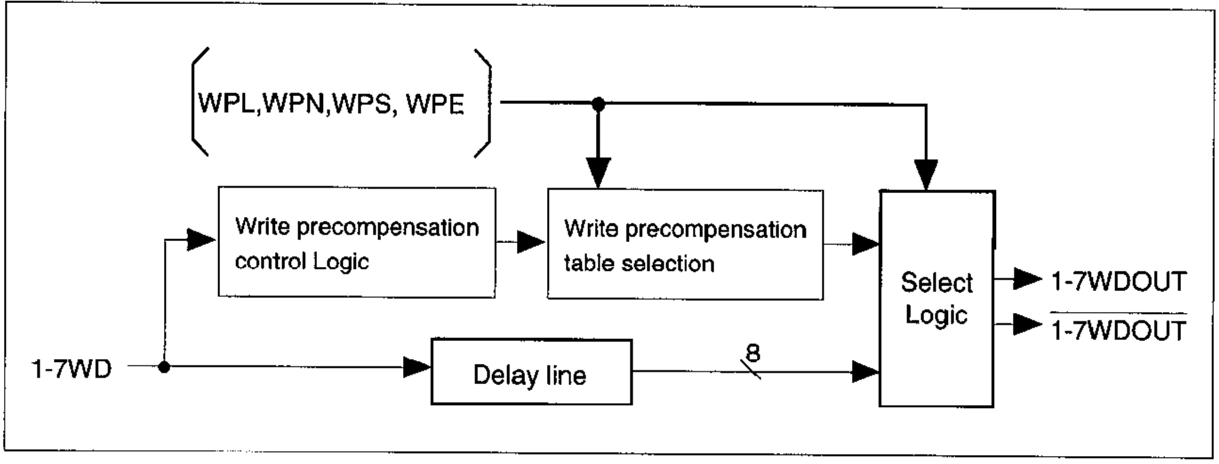


Fig. 32.2 (1,7) Code to NRZ Decoding Example

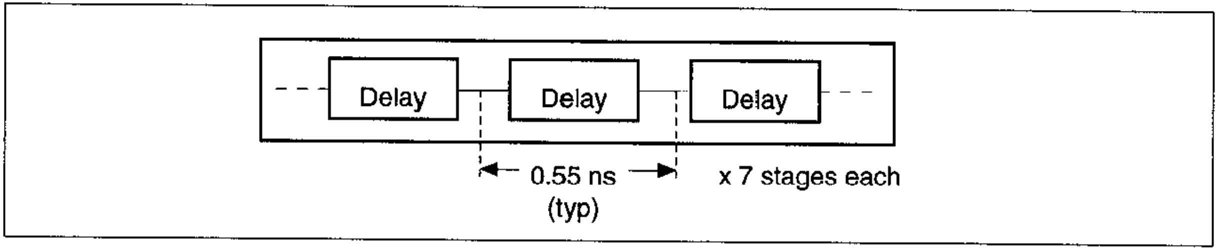
33. Write Precompensation Circuit

The HD153035F has a built-in synchronous write precompensation circuit, and the 4 matrix delay levels from the write precompensation table shown below can be selected independently for the EARLY and LATE sides. Each delay group of the table can select delay value independently.

(1) Circuit Configuration



(2) Programmable Delay Line



(3) Table

n \ m	1	2	3	4	5	6	7
1	N	E					
2	L	S					
3							
4							
5							
6							
7							

```
       n              m
   ┌──────┐       ┌──────┐
1 0 ••• 0 1 0 ••• 0 1 0
Previous     Current     Next
```

n: The number of zero's between the current 1 bit and the previous 1 bit

m: The number of zero's between the current 1 bit and the next 1 bit

The precompensation delay time for each the 4 matrix entries in the precompensation table (see Table) can be set independently.

The delay time (8 levels) is selected by the each part of register.

34. Idle / $\overline{\text{Servo}}$ input pin for power saving:

With the mode control register(PCN), there are four different modes of operation as shown: 11 = Sleep, 10 = Power Save, 00 = Normal (full power).The modes are defined as followed:

a) When bits 5,4 = 00 : **Normal** mode. All circuitries are powered.

b) When bits 5,4 = 11 : **Sleep** mode. Everythings powered down except the I/O and the logic section of the chip.

c) When bits 5,4 = 10 : **Power Save** mode. In this mode, the Idle/$\overline{\text{Servo}}$ pin will select which of the two power save modes to be used. If Idle = 1 then Idle mode is selected and all modules will be powered down except for the I/O, logic, and the bias circuitries.. If Idel/$\overline{\text{Servo}}$ = 0 then Servo mode will be selected and all blocks will be kept on except the clock syncthesizer (WR PLL) and the synchronizer (RD PLL).

	Mode	A14 D5,4	I/$\overline{\text{S}}$ pin	I/O	Logic	Bias	RD PLL	WR PLL	AGC	AF	RPD	PH
	Normal	00	X	ON	ON	ON	ON	ON	ON	ON	ON	ON
Power Save	Servo	10	0	ON	ON	ON			ON	ON	ON	ON
	Idle	10	1	ON	ON	ON						
	Sleep	11	X	ON	ON							

35. Recommendation for PCB layout

To reduce Ground noise for proper chip operation, the following PCB board layout is recommended:

(1) Dedicate 1 layer for Ground plane.
(2) Divide the ground plane into 4 segments as show fig. 35.1
(3) System ground is connected Master GND.

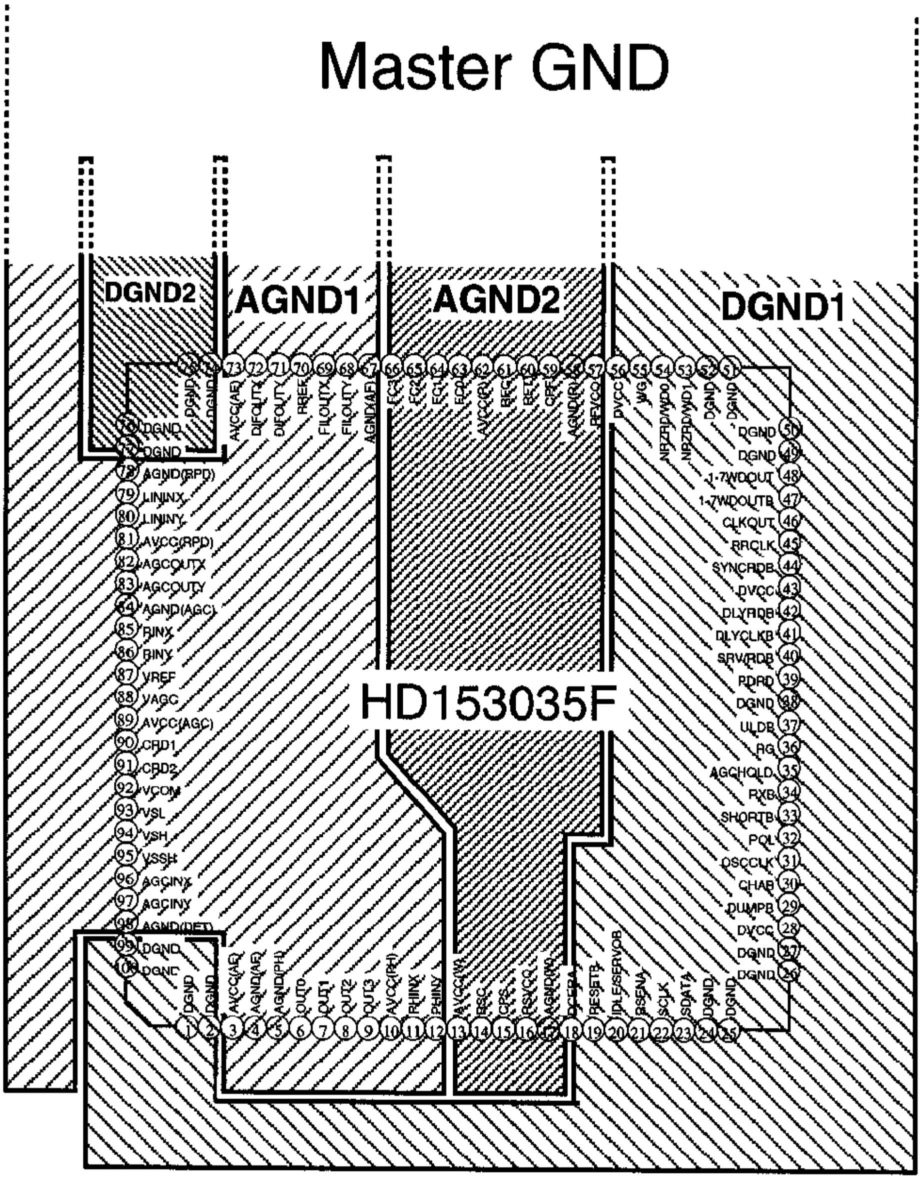


Fig. 35.1 Recommendation for Ground layout

36. Absolute Maximum Ratings (Ta=25 °C)

Description	Symbol	Ratings	Unit	Applicable pins
Supply voltage	Vcc	7	V	DVcc, AVcc
Input voltage	V_I	- 0.3 to 5.5	V	Note1
Output voltage	V_O	5.5	V	Note2
Operating temperature	Topr	0 to 70	°C	
Storage temperature	Tstg	- 55 to + 125	°C	

Note1: OSCCLK, $\overline{\text{RESET}}$, IDLE/$\overline{\text{SERVO}}$, RSENA, SCLK, SDATA, $\overline{\text{DUMP}}$, $\overline{\text{CHA}}$, $\overline{\text{SHORT}}$, $\overline{\text{RX}}$, AGCHOLD, RG, SRV/$\overline{\text{RD}}$, NRZRD/WD0(Write mode), NRZRD/WD1(Write mode), WG, $\overline{\text{DCERA}}$

Note2: SDATA, POL, $\overline{\text{ULD}}$, PDRD, $\overline{\text{DLYCLK}}$, $\overline{\text{DLYRD}}$, $\overline{\text{SYNCRD}}$, RRCLK, CLKOUT, $\overline{\text{1-7WDOUT}}$, 1-7 WDOUT, NRZRD/WD0(Read mode), NRZRD/WD1(Read mode)

37. Electrical Characteristics (Ta=0 to + 70 °C, Vcc = 5.0V ± 10% unless otherwise noted)

General

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
Power supply voltage	Vcc	4.5	5	5.5	V		Note4
Operation temperature	Ta	0	25	70	°C		
NRZ transfer rate		15		56	Mbps		
Power supply current	Icc		850		mW	at 56Mbps, R/W 20% Idle/Servo mode 80%.	Note4
TTL 'H' level intput voltage	V_{IH}	2.2			V	Vcc=4.5V	Note1
TTL 'L' level intput voltage	V_{IL}			0.8	V	Vcc=4.5V	Note1
TTL 'H' level output voltage	V_{OHT}	2.4			V	I_{OH}=-400µA, Vcc=4.5V	Note2
TTL 'L' level output voltage	V_{OLT}			0.5	V	I_{OL}=4mA, Vcc=4.5V	Note2
ECL 'H' level output voltage	V_{OHE}	Vcc -0.95	Vcc -0.8		V	Ta=25°C, RL=510Ω	Note3
ECL 'L' level output voltage	V_{OLE}		Vcc -1.8	Vcc -1.6	V	Ta=25°C, RL=510Ω	Note3
Input current	I_{IH}			20	µA	Vcc=5.5V,Vi=2.7V	Note1
	I_{IL}			-400	µA	Vcc=5.5V,Vi=0.4V	Note1
Output shorted current	I_{OS}	-20		-120	mA	Vcc=5.5V	Note2
Input clamp voltage	V_{IK}			-1.5V	V	Vcc=4.5V,I_{OH}=-18mA	Note1

Note1: OSCCLK,$\overline{\text{RESET}}$,IDLE/$\overline{\text{SERVO}}$,RSENA,SCLK,SDATA,$\overline{\text{DUMP}}$,$\overline{\text{CHA}}$,$\overline{\text{SHORT}}$,$\overline{\text{RX}}$,AGCHOLD,RG, SRV/$\overline{\text{RD}}$,NRZRD/WD0(Write mode),NRZRD/WD1(Write mode),WG,$\overline{\text{DCERA}}$

Note2: SDATA,POL,$\overline{\text{ULD}}$,PDRD,$\overline{\text{DLYCLK}}$,$\overline{\text{DLYRD}}$,SYNCRD,RRCLK,CLKOUT,$\overline{\text{1-7WDOUT}}$(TTL), 1-7WDOUT(TTL), NRZRD/WD0(Read mode),NRZRD/WD1(Read mode)

Note3: $\overline{\text{1-7WDOUT}}$(ECL),1-7WDOUT(ECL)

Note4: DVcc,AVcc(PH),AVcc(W),AVcc(R),AVcc(AF),AVcc(AGC),AVcc(RPD)

38. Encoder/Decoder(Ta=25°C, Vcc=5V,56Mbps)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
NRZRD set-up time (serial)	t_{SNRS}	9.0			ns		NRZRD/WD0
NRZRD set-up time (parallel)	t_{SNRP}	16.0			ns		NRZRD/WD0,1
NRZRD hold time (serial)	t_{HNRS}	8.0			ns		NRZRD/WD0
NRZRD hold time (parallel)	t_{HNRP}	21.0			ns		NRZRD/WD0,1
NRZWD set-up time (serial)	t_{SNWS}	8.0			ns		NRZRD/WD0
NRZWD set-up time (parallel)	t_{SNWP}	17.0			ns		NRZRD/WD0,1
NRZWD hold time (serial)	t_{HNWS}	0			ns		NRZRD/WD0
NRZWD hold time (parallel)	t_{HNWP}	0			ns		NRZRD/WD0,1
RRCLK high time	T/2(H)	14.0			ns		RRCLK
RRCLK low time	T/2(L)	14.0			ns		RRCLK
Decode time	t_{DD}		15	15	RRCLK		NRZRD/WD0
Encode time	t_{ED}		12.5	14.5	RRCLK		1-7WDOUT, $\overline{\text{1-7WDOUT}}$
Write Precomp time step		0.28	0.55	0.82	ns	Not tested	
Write Precomp time width		± 2.0	± 3.85	± 5.7	ns	± 7steps	

39. Register (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
RSENA "L" time	t_{EL}	1650			ns		RSENA
RSENA "H" time	t_{EH}	50			ns		RSENA
RSENA falling edge to the first SCLK rising edge	t_{EFSR}	50			ns		SCLK
SDATA set up time	t_{CDS}	10			ns		SDATA
SDATA hold time	t_{CDH}	10			ns		SDATA
The last SCLK falling edge to RSENA rising edge	t_{SFER}	50			ns		RSENA
SCLK cycle time	t_{CC}	100			ns		SCLK
SCLK "H" time	t_{CH}	40			ns		SCLK
SCLK "L" time	t_{CL}	40			ns		SCLK
SDATA output delay	t_{CDD}			20	ns		SDATA
SDATA output hold time	t_{EDH}	5			ns		SDATA

40. Synchronizer (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Read VCO center frequency 1	fvco1	39.9	42	44.2	MHz	RFVCO=2.47k, Register VFC=7B Hex
Phase lock acquisition time 1		—	—	6	Byte	6 NRZ bytes period at 28Mbps
Capture range 1		±15	—	—	%	at 28Mbps
Lock range 1		±15	—	—	%	at 28Mbps
Read VCO gain 1		129	172	215	Mrad / sec •V	RFVCO=2.47k, Register VFC=7B Hex
Read VCO upper limit clamping frequency 1		—	55	—	MHz	RFVCO=2.47k, Register VFC=7B Hex
Read VCO lower limit clamping frequency 1		—	30	—	MHz	RFVCO=2.47k, Register VFC=7B Hex
Read VCO center frequency 2	fvco2	79.9	84	88.3	MHz	RFVCO=2.47k, Register VFC=F6 Hex
Phase lock acquisition time 2		—	—	6	Byte	6 NRZ bytes period at 56Mbps
Capture range 2		±15	—	—	%	at 56Mbps
Lock range 2		±15	—	—	%	at 56Mbps
Read VCO gain 2		178	236	296	Mrad / sec •V	RFVCO=2.47k, Register VFC=F6 Hex
Read VCO upper limit clamping frequency 2		—	109	—	MHz	RFVCO=2.47k, Register VFC=F6 Hex
Read VCO lower limit clamping frequency 2		—	55	—	MHz	RFVCO=2.47k, Register VFC=F6 Hex
Window margin loss		0		3	ns	at any data rate
Window adjust step		0.34	0.67	1.0	ns	31 steps, Not tested
Window adjust width		+5.5 -5.9	+10.0 -10.7	+14.5 -15.5	ns	+15 step, -16step
Window fine adjust width		0.12	0.25	0.5	ns	total 4 steps
Read VCO maximum oscillate frequency		90	108	—	MHz	RFVCO=1k, Register VFC=80Hex
Decode window center accuracy		-3 -2		3 2	ns	at 28Mbps at 56Mbps
T/I offset accuracy		-6 -15		6 15	µs	at 28Mbps at 56Mbps
C/D offset accuracy		-15		+15	%	at GAC=20Hex
Oscillation start voltage				4.0	V	Ta=25°C fosc ≧100kHz

41. **Synthesizer** (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Write VCO center frequency	fwvco	80.0	84.0	88.3	MHz	RSVCO=5.1k, Register VFC=F6 Hex
Write VCO upper limit clamping frequency		—	100.9	—	MHz	RSVCO=5.1k, Register VFC=F6 Hex
Write VCO lower limit clamping frequency		—	67.3	—	MHz	RSVCO=5.1k, Register VFC=F6 Hex
Phase lock acquisition time		—	—	1	ms	tested at 28Mbps, 56Mbps
Capture range		±10	—	—	%	tested at 28Mbps, 56Mbps
Lock range		±10	—	—	%	tested at 28Mbps, 56Mbps
VCO frequency step		—	1.0	—	%	at fMAX / fLOW = 2.55
VCO gain		84	115	140	Mrad / sec • V	RSVCO=5.1k, Register VFC=F6 Hex

42. **RPD & PH** (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
Max peak-peak Input signal				2.0	Vpp	differential inputs	PHINX/Y
PDRD pulse width		4.5	9	13.5	ns	at 40Mbps, PW[1:0]=00	
PDRD pulse rise time	tr	0.5	2	4	ns	CL=15pF,20%-80%, Not tested	
PDRD pulse fall time	tf	0.5	2	4	ns	CL=15pF,80%-20%, Not tested	
P/H output voltage swing		2.0	2.3	2.6	V	fin=6.5MHz, Vin=2Vpp **	
P/H output leakage current		-0.2	0	+0.2	µA		OUT0 ~ OUT3
P/H Channel Offset		-50		+50	mV		OUT0 ~ OUT3
P/H Reference Voltage			VCOM x 25%		V	PHINX/Y=0Vpp	OUT0 ~ OUT3
P/H Discharge time	tDSCG			2.0	µS	COUT0 ~ COUT3 =1000pF	OUT0 ~ OUT3 $\overline{\text{DUMP}}$
P/H Sampling time ($\overline{\text{CHA}}$ = "L" time)	tSPL	2.0			µS		$\overline{\text{CHA}}$
$\overline{\text{CHA}}$ Switching time	tSWT	200			ns		$\overline{\text{CHA}}$

** : differential input for PHINX and PHINY.

43. **Active Filter** (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Filter cutoff frequency	fc	5		25	MHz	
fc Accuracy	fca	- 15		+15	%	
Filter boost level	Fb	0		10	dB	
Filter boost Accuracy	Fba	- 1		1	dB	Fb = 10dB
Output dynamic range				1.7	Vpp	diff. outputs, THD < 2%
Output noise(normal)			3	5.5	mVRms	Not tested
Output noise(differential)			6	10	mVRms	Not tested
Group delay variation (0)			± 3		%	Fb=0, condition 1
Group delay variation (1)			± 3		%	Fb=10, condition 1
Power noise rejection	PSRR		- 45		dB	Not tested

Condition 1: fc =18MHz, range = 0.2fc to fc, measured from AGCOUTX/Y to FILOUTX/Y.

44. **AGC** (Ta=25°C, Vcc=5V)

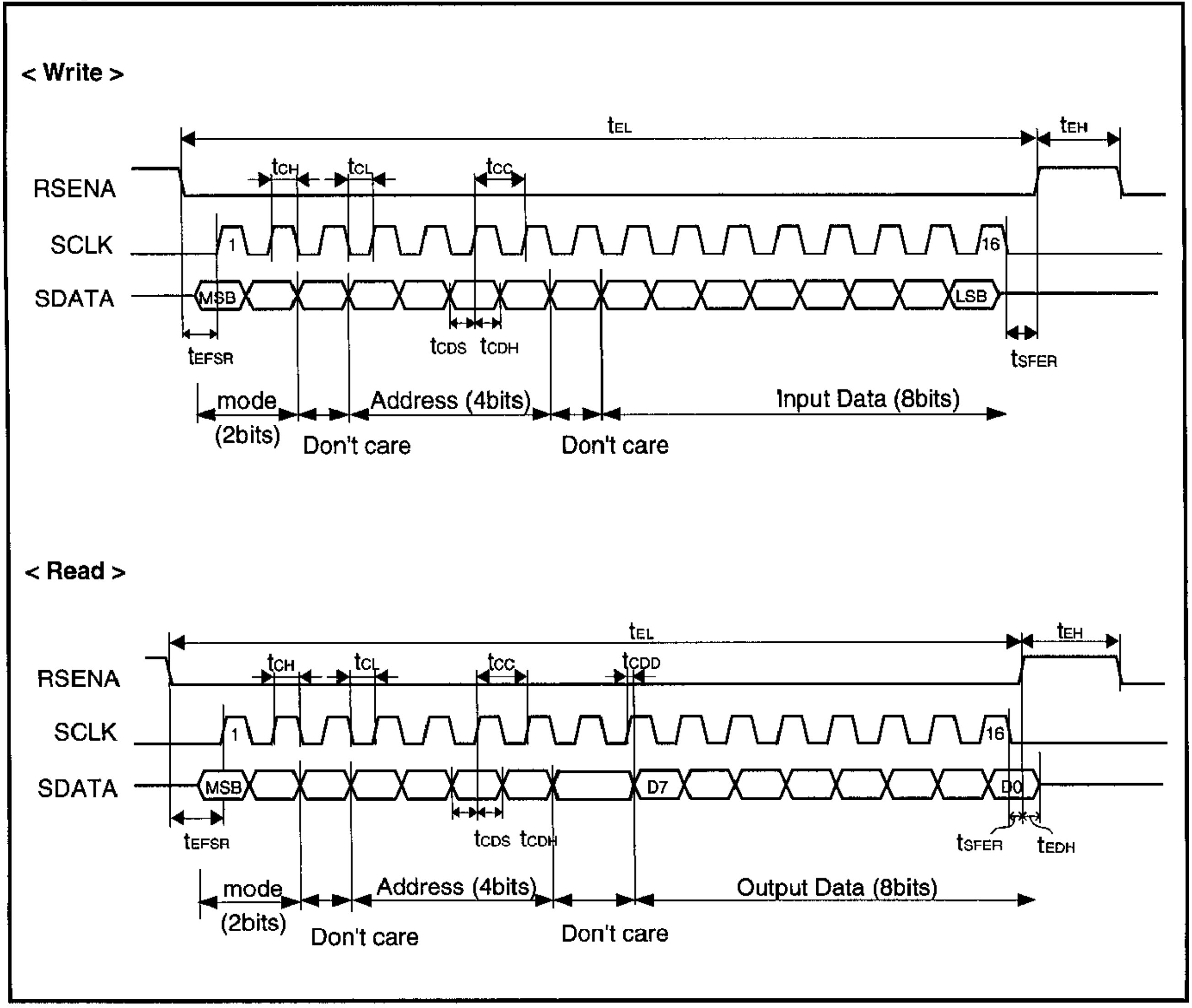
Item	Symbol	min	typ	max	unit	conditions
AGC max gain		(39)	43		dB	RINX/Y to FILOUTX/Y
AGC min gain				0	V/V	
Input dynamic range		20		200	mV	Distortion <2%
Band width(-3dB)	Bw	50			MHz	
Output DC offset	Voff		100	200	mV	AGCOUTX/Y
Input noise(max gain)			5	15	$nV/\sqrt{Hz}$	Not tested
Write to read recovery time	twrr		1	2	µs	write($\overline{RX}$=L) to read cycle
Read recovery time	trr			5	µs	recovery from max gain

45. **P/H of servo mode** (Ta=25°C, Vcc=5V)

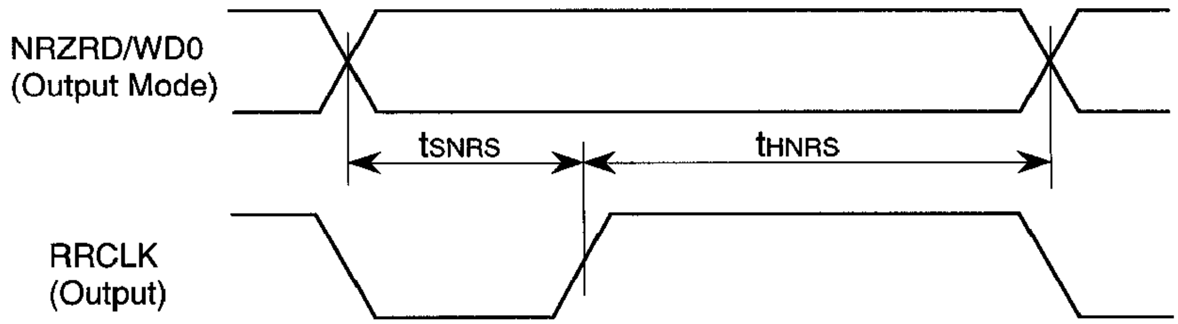
Item	Symbol	min	typ	max	unit	conditions
AGC initialize time	t_{XS}	150			ns	
AGC gain attack time	t_{AGCA}			2	µs	CRD=3300pF
P/H discharge time	t_{DSCG}			2	µs	COUT0~COUT3=1000pF
$\overline{\text{CHA}}$ sample waiting time	t_{SWT}	200			ns	
P/H sample time	t_{SPL}	2			µs	

46. AC Timing Chart

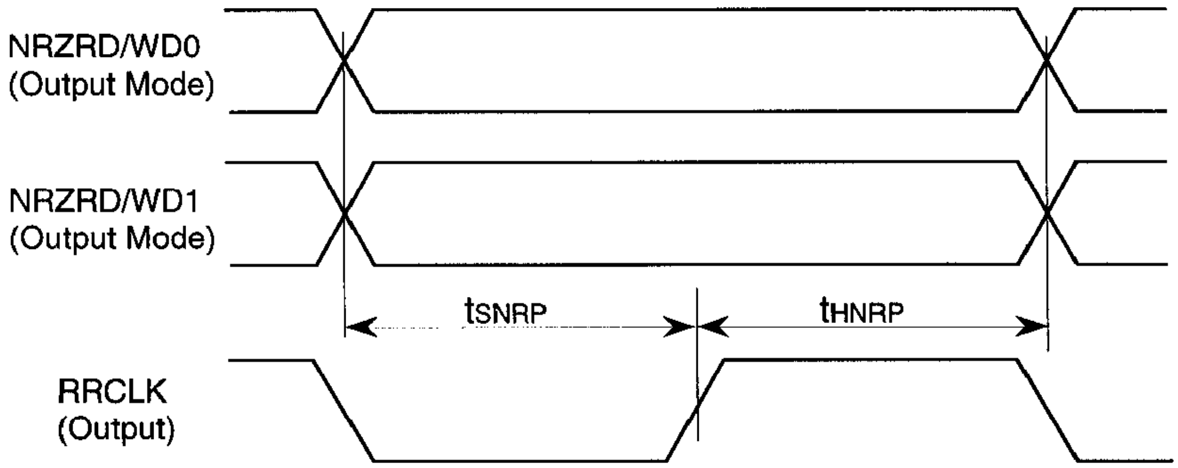
(1) Register read / write



(2) Read for NRZ data



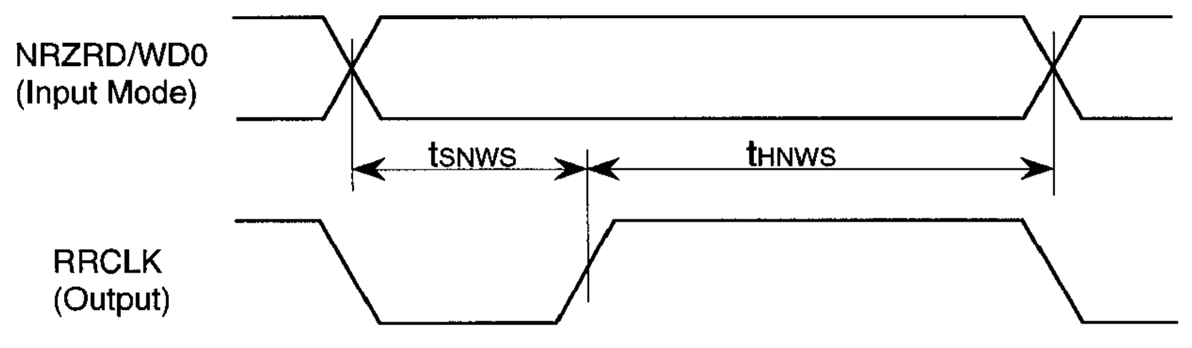
NRZ Read Data(Serial Mode)



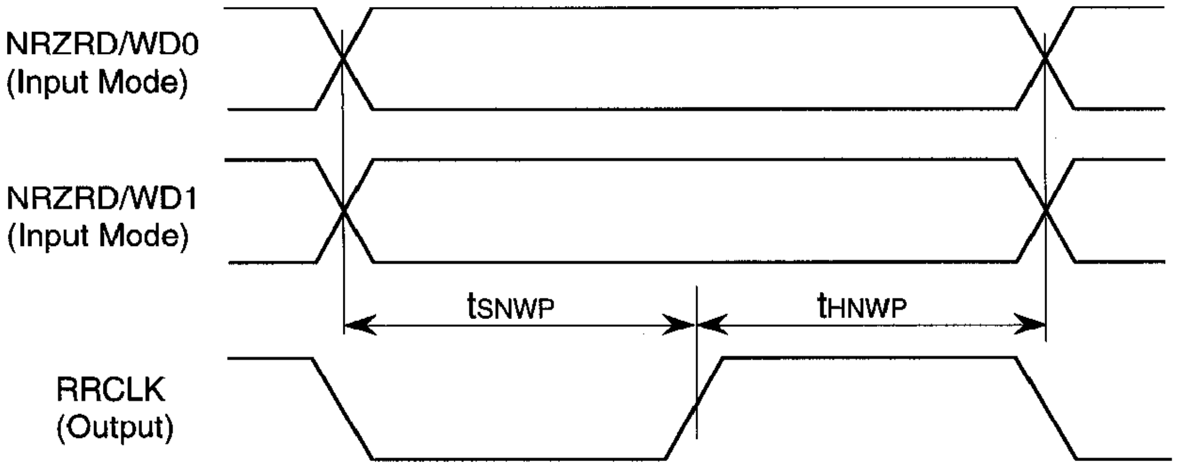
NRZ Read Data(Parallel Mode)

Note1: When data transfer rate is 40Mbps(Serial Mode),NRZ and RRCLK Output is 40MHz. RRCLK clock duty "L":"H" =1:2.
When data transfer rate is 40Mbps(Parallel Mode),NRZ and RRCLK Output is 20MHz. RRCLK clock duty "L":"H" =1:1
We recommend that more than 40Mbps,please select the "Parallel" mode.

(3) Write for NRZ data



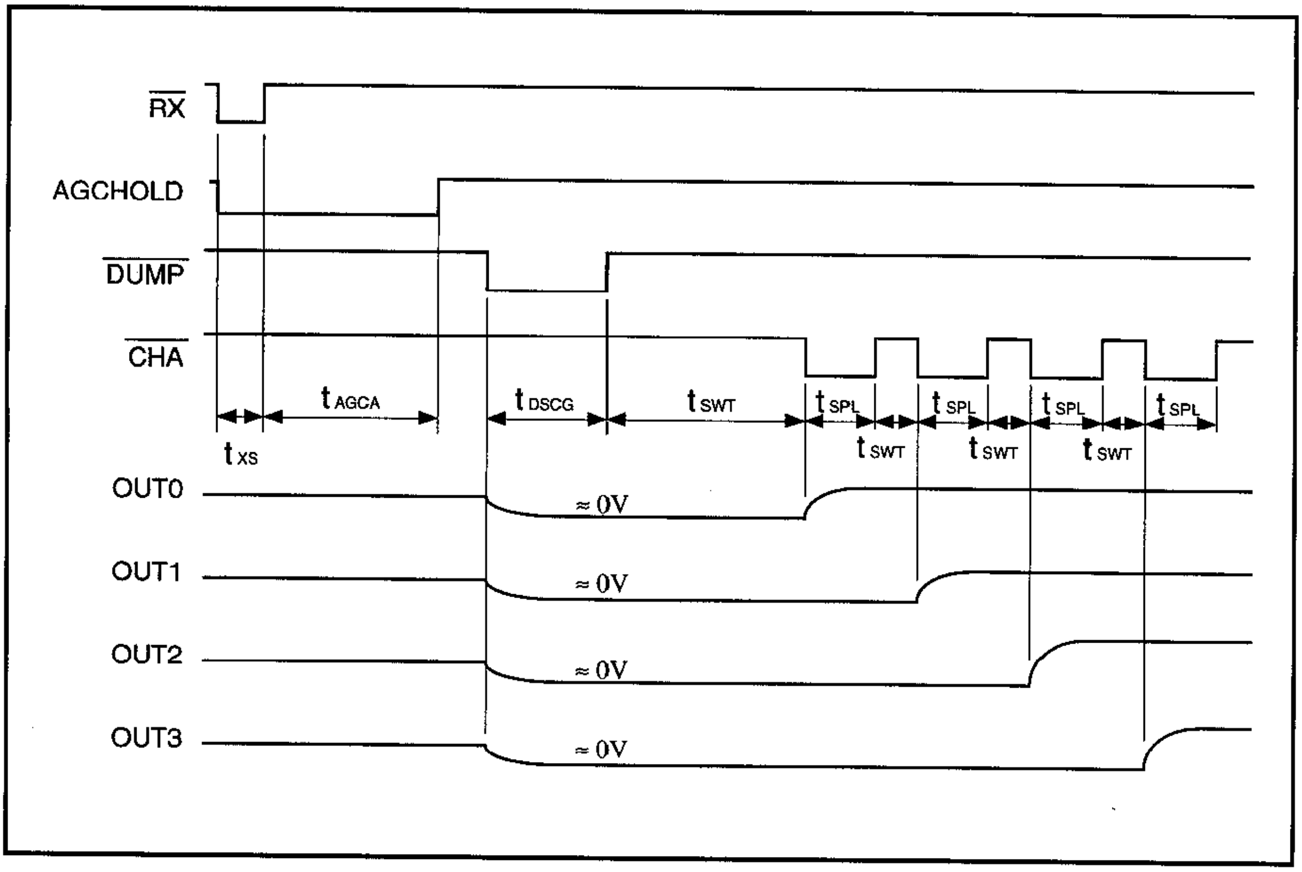
NRZ Write Data(Serial Mode)



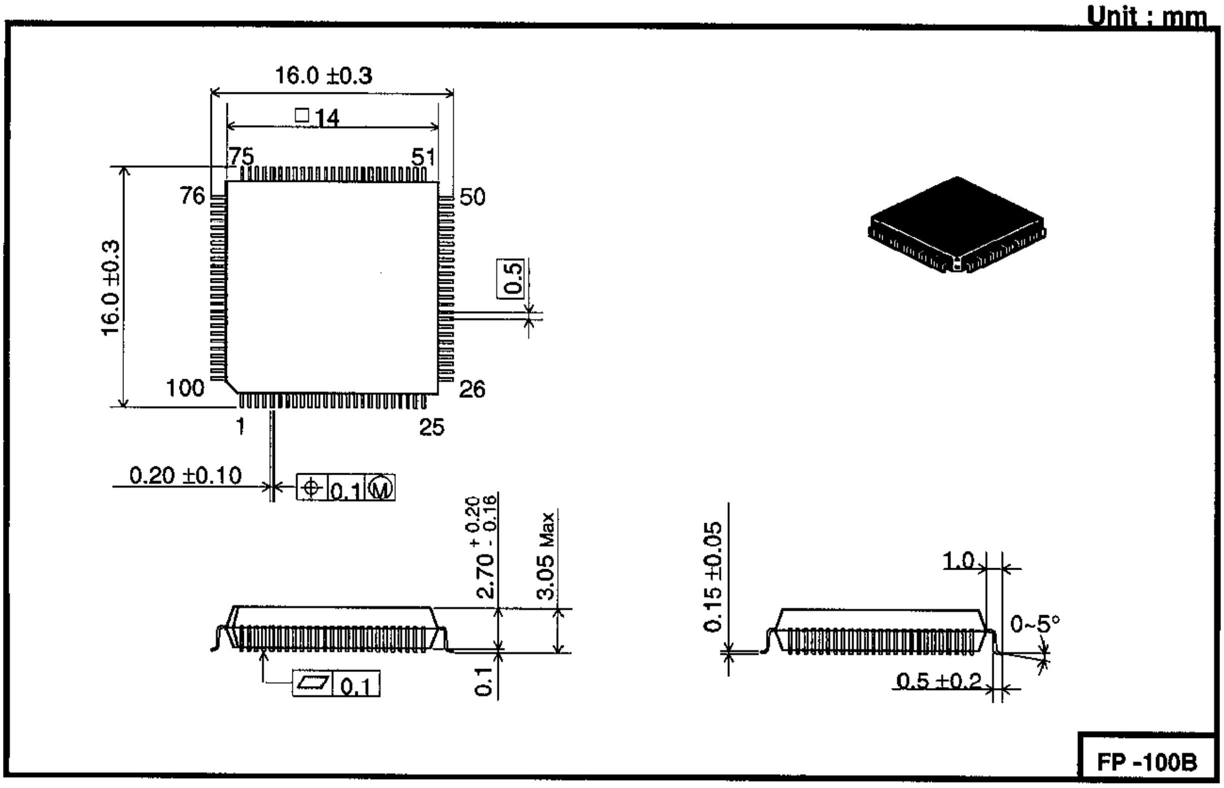
NRZ Write Data(Parallel Mode)

Note2: When data transfer rate is 40Mbps(Serial Mode), RRCLK Output is 40MHz .
RRCLK clock duty "L":"H" =1:2.
When data transfer rate is 40Mbps(Parallel Mode), RRCLK Output is 20MHz .
RRCLK clock duty "L":"H" =1:1
We recommend that more than 40Mbps,please select the "Parallel" mode.

(4) Timing for servo functions



47. PACKAGE DIMENSIONS



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