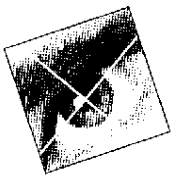


CIRCUIT DESCRIPTION

Pin Descriptions

This chapter begins with a table describing each pin and its function (Table 1), followed by pinout diagrams of each package (Figures 1 and 2), and a detailed functional block diagram (Figure 3).

Table 1. Pin Descriptions *(1 of 3)*

Pin Name	I/O	68 PLCC Pin #	52 PQFP Pin #	Description
CLK	I		49	Pixel clock input (TTL compatible). A clock frequency 2 times the luminance sample rate should be applied. Available on 52-pin PQFP only.
CLK	I/O	38		Pixel clock input/output (TTL compatible). A clock frequency 2 times the luminance sample rate should be applied. Absolute minimum loading should be observed. Available on 68-pin PLCC only.
CLK_DIR	I	36		Clock direction pin. (TTL compatible). A logical one configures the CLK pin as an input; a logical zero enables CLK as an output. Available on 68-pin PLCC only.
XTAL_IN, XTAL_OUT	I/O	41, 40		Crystal I/O pins. A crystal is connected to XTAL_IN and XTAL_OUT to provide the 2x pixel clock. A TTL version of this clock is output onto the pin if CLK_DIR is a logical zero. Available on 68-pin PLCC only.
RESET*	I	57	11	Reset control input (TTL compatible). Must be a logical one for normal operation. A logical zero for one CLK cycle resets video timing (horizontal, vertical subcarrier counters to the start of VSYNC of first field).
VSYNC*	I/O	6	25	Vertical synchronization input/output (TTL compatible). VSYNC* is registered by the rising edge of CLK.
HSYNC*	I/O	7	26	Horizontal synchronization input/output (TTL compatible). HSYNC* is registered by the rising edge of CLK.
VSYNCO*	O	29	41	Field synchronization output (TTL compatible). VSYNCO* transitions on the rising edge of CLK. VSYNCO* can output vertical sync or an even/odd field signal, depending on the setting of register HSYNCTE.
HSYNCO*	O	30	42	Horizontal synchronization output (TTL compatible). HSYNCO* transitions on the rising edge of CLK. HSYNCO* can output a pulse which transitions high and low at any specified time during a video line, depending on the setting of register HSYNCTE.

Table 1. Pin Descriptions *(2 of 3)*

Pin Name	I/O	68 PLCC Pin #	52 PQFP Pin #	Description
Y[7:0]	I	63–66, 2–5	15–18, 21–24	Y pixel inputs (TTL compatible). A higher index corresponds to a greater significance. Y[7:0] is registered on the rising edge of CLK. When configured for 8-bit mux mode, these pins should not be left floating.
P[7:0]	I	20–27	33–40	YCrCb pixel inputs (TTL compatible) in 8-bit mode, CrCb inputs in 16-bit mode. P[7:0] is registered on the rising edge of CLK. A higher index corresponds to a greater significance.
OSD[3:0]	I	31–34	43–46	Overlay pins (TTL compatible). The OSD[3:0] inputs are registered on the rising edge of CLK when Y pixels are normally valid.
SLAVE	I	14	29	Timing mode input (TTL compatible). SLAVE is registered by the rising edge of CLK. A logical one configures the device to accept synchronization signals on the HSYNC* and VSYNC* pins; a logical zero allows the device to output sync signals on these pins.
SLEEP	I	16	30	Powerdown control input (TTL compatible). A logical one configures the device for power-down mode. A logical zero configures the device for normal operation. This pin may be connected directly to VAA or GND.
SDA	I/O	60	13	Serial interface data input/output (TTL compatible). Data is written to and read from the device via this serial bus.
SCL	I	59	12	Serial interface clock input (TTL compatible). Maximum clock rate is 100 kHz.
ALTADDR	I	61	14	Alternative slave address input (TTL compatible). A logical one configures the device to respond to an I^2C address of 0x8A; a logical zero configures the device to respond to an I^2C address of 0x88.
TEST	I	12, 13	27, 28	These pins are reserved for testing and must be connected to a logical zero, such as GND, for normal operation.
CVBS	O	53	8	Composite video output.
C	O	49	4	Modulated chrominance output.
Y	O	51	6	Luminance output (with blanking, sync, and, optionally, Macrovision pulses and/or closed-captioning encoding).
FSADJUST		46	1	Full-scale adjust control pin. A resistor (RSET) connected between this pin and GND controls the full-scale output current on the analog outputs. For standard operation, use the nominal RSET values shown under Recommended Operating Conditions.
VBIAS			10	DAC bias voltage. A 0.1 µF ceramic capacitor must be used to bypass this pin to GND. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Available on 52-pin PQFP only.
VREF_IN	I	55		Voltage reference input. VREF_IN must be connected directly to VREF_OUT. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figure 19 in the PC Board Layout section. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Available on 68-pin PLCC only.

Table 1. Pin Descriptions *(3 of 3)*

Pin Name	I/O	68 PLCC Pin #	52 PQFP Pin #	Description
VREF_OUT	O	54	9	Voltage reference output. This pin should only be used to drive the VREF_IN pin. See Figure 19. For the 52-pin PQFP, this pin is internally connected to VREF_IN, and must be decoupled like VREF_IN.
COMP		47	2	Compensation pin. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA	–	17, 37, 48, 50, 67	3, 5, 19, 31, 48	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	–	1, 19, 35, 42–44, 52	7, 20, 32, 47, 50–52	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Figure 1. Bt866/7 68-Pin PLCC Pinout Diagram

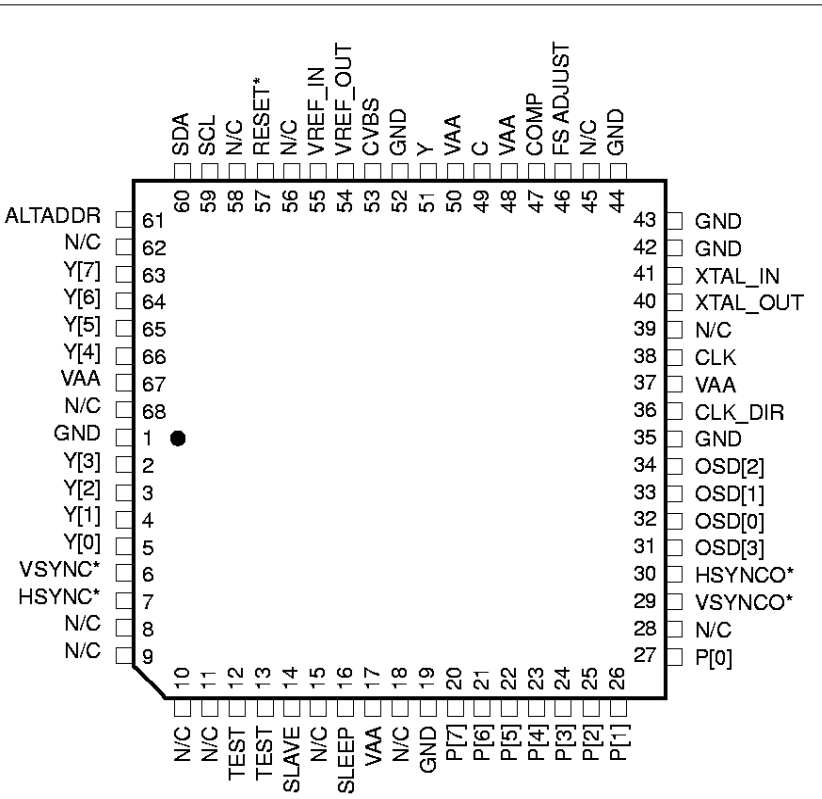


Figure 2. Bt866/7 52-Pin PQFP Pinout Diagram

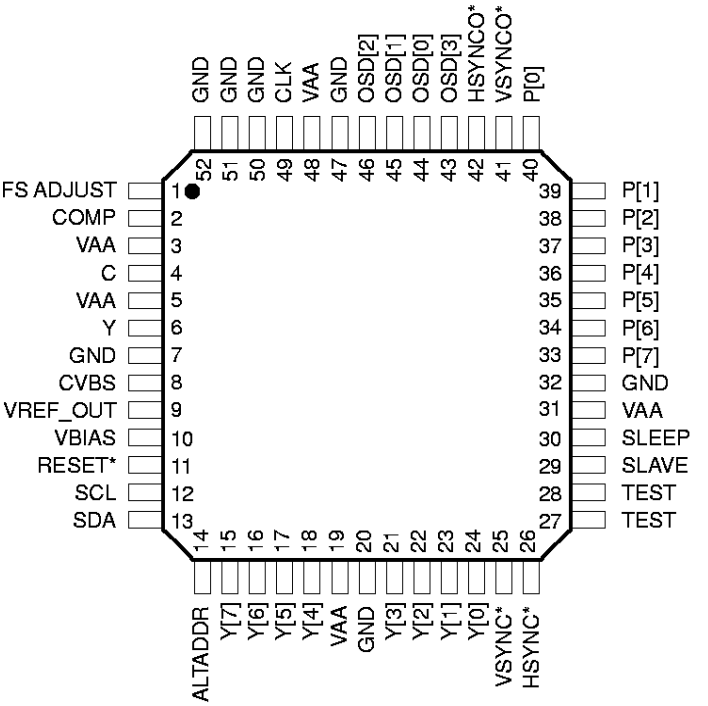
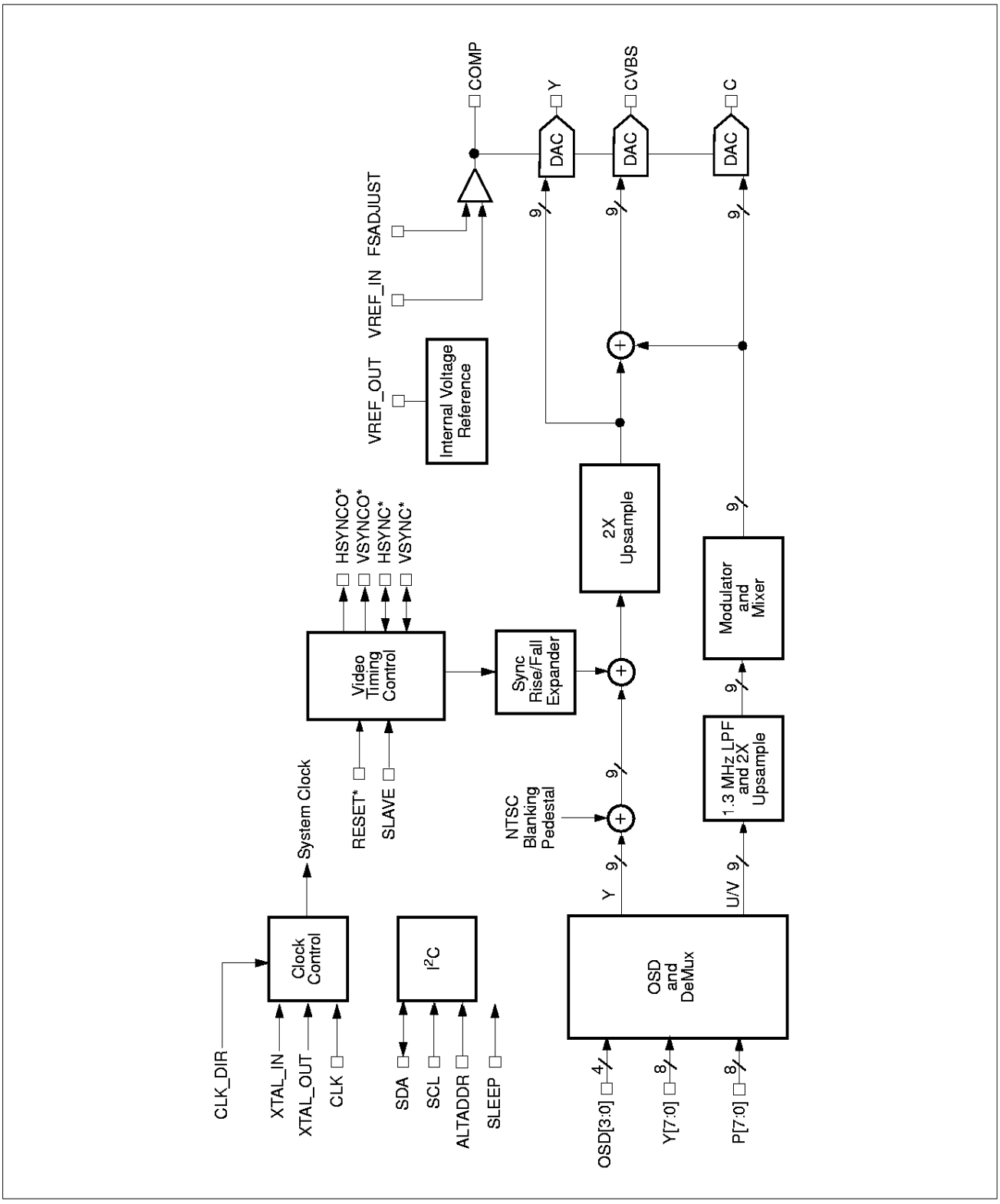


Figure 3. Detailed Block Diagram



Clock Timing

A clock signal with a frequency twice the luminance sampling rate must be present at the CLK pin. All setup and hold timing specifications are measured with respect to the rising edge of this signal.

Pixel Input Timing

8-bit YCrCb Input Mode

The 8-bit YCrCb multiplexed input mode is selected by default. Multiplexed Y, Cb, and Cr data is input through the P[7:0] inputs. By default, the input sequence for active video pixels must be Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc., in accordance with CCIR-656.

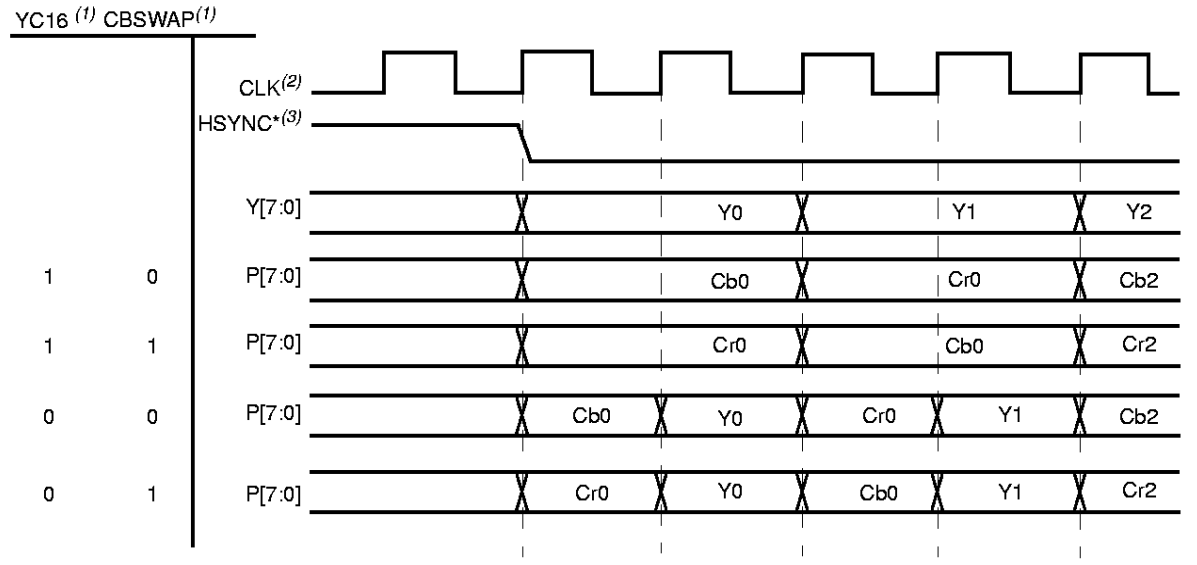
16-bit YCrCb Input Mode

The 16-bit mode is selected by setting register YC16. Y[7:0] data is input via the Y[7:0] inputs; multiplexed Cb[7:0] and Cr[7:0] data is input via the P[7:0] inputs.

Pixel Sequence

By default, the pixel sequence is defined as Cb0-Y0-Cr0-Y1-Cb2. This pattern begins during the first CLK period after the falling edge of HSYNC* (regardless of the setting of SLAVE/MASTER mode). The order of Cb and Cr can be reversed by setting register CBSWAP. Figure 4 illustrates the timing for both multiplexed input modes. If the pixel stream input to the Bt866/7 is off by one CLK period, the Bt866/7 can lock to the pixel stream by setting register YCSWAP. This would solve the problem of having the Y and Cr/Cb pixels swapped.

Figure 4. Pixel Sequence



Notes: (1). YC16 and CBSWAP are programmable registers.
(2). Pixel transitions must occur observing setup and hold timing about the rising edge of CLK.
(3). Pixel sequence will begin with Cb0 at 4 x n clock periods following the falling edge of HSYNC*, where n is an integer.

Video Timing

The width of the analog horizontal sync pulses and the start and end of color burst is automatically calculated and inserted for each mode according to CCIR-624-4 (see Table 3). Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. In addition, rise and fall times of sync, closed-caption data transitions, and the burst envelope are internally controlled. Video timing figures follow the text in this section. Figures 5–10 show the timing characteristics for various Bt866/7 operating modes. Figure 11 illustrates the three-stage chroma filter, Figure 12 illustrates the luminance upsampling filter response.

Reset If the RESET* pin is held low during a single rising edge of CLK, the subcarrier phase is set to zero, and the horizontal and vertical counters are set to the beginning of VSYNC of FIELD1. Counting resumes on the first rising edge of CLK after rising RESET*. A software reset will occur immediately after writing a 1 to register SRESET. This will reset all software-programmable register bits to zero.

On power-up, the Bt866/7 will automatically perform a timing and software reset. The power-up state has the following configuration: interlaced, NTSC CCIR601 black burst (no active video), and zero chroma scaling. Setting register EACTIVE will enable active video.

Video Output Pins

In either slave or master timing mode, HSYNCO* and VSYNCO* are always available as synchronization outputs. HSYNCO* normally outputs the 4.7 µs hsync pulse, exactly like HSYNC* in master mode. By setting register SYNC[0], rising and falling edges of HSYNCO* can be programmed to occur anywhere on the line. There are two 10-bit values that determine the start and end of the hsync pulse. Register HSYNCF programs the hsync falling edge; register HSYNCR programs the rising edge.

To offer a glueless interface to certain MPEG decoders, HSYNCO* can be used as a programmable composite blanking signal by setting the start and end times to specify the active pixel region. To help accomplish this, register SYNC[2] will disable the falling edge of HSYNCO* during the vertical blanking interval. Note that this bit also inverts the field signal on VSYNCO* (if the field signal is enabled).

The VSYNCO* pin normally outputs the field signal. At the beginning of an odd field, VSYNCO* will transition two pixel clock periods before the falling edge of HSYNC* in both interlaced and noninterlaced modes. The polarity of VSYNCO* is normally high for even fields. This can be changed by setting register SYNC[2], so that VSYNCO* will be high for odd fields. Note that this bit also affects programmable HSYNCO* timing by disabling HSYNCO* edges during the vertical blanking interval.

VSYNCO* can also be programmed to output a vsync pulse by setting register SYNC[1]. The vsync pulse has a duration of 3 lines for NTSC or 2.5 lines for PAL, exactly like VSYNC* in master mode.

Sync and Burst Timing

Table 2 lists the resolutions and clock rates for the various modes of operation. Table 3 lists the horizontal counter values for the end of horizontal sync, start of color burst, end of color burst, front porch, back porch, and the first active pixel for the various modes of operation. The front porch is the interval before the next expected falling HSYNC* when outputs are automatically blanked. The PORCH register bit is included in Table 3 for different picture widths.

The horizontal sync width is measured between the 50% points of the falling and rising edges of horizontal sync.

The start of color burst is measured between the 50% point of the falling edge of horizontal sync and the first 50% point of the color burst amplitude (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, N_c above the blanking level).

The end of color burst is measured between the 50% point of the falling edge of horizontal sync and the last 50% point of the color burst envelope (nominally +20 IRE for NTSC/PAL–M and 150 mV for PAL–B, D, G, H, I, N, N_c above the blanking level).

NOTE: PAL-N_c refers to "Combination N," the PAL format used in Argentina.

Table 2. Field Resolutions and Clock Rates for Various Modes of Operation

Operating Mode	Active Resolution (pixels)	Total Resolution (pixels)	CLK Frequency (MHz)
NTSC/PAL–M CCIR601	720 x 240	858 x 262	13.5000
PAL–B, D, G, H, I, N, N_c CCIR601	720 x 288	864 x 312	13.5000
NTSC/PAL–M Square Pixel	640 x 240	780 x 262	12.2727
PAL–B, D, G, H, I, N, N_c Square Pixel	768 x 288	944 x 312	14.7500

Table 3. Horizontal Counter Values for Various Video Timings

Operating Mode	Horizontal Counter Value												
	Horizontal Sync		Start of Burst		End of Burst		First Active Pixel		Back Porch		Front Porch(1)		PORCH Bit
	CNT	µs	CNT	µs	CNT	µs	CNT	µs	CNT	µs	CNT	µs	
NTSC CCIR601	63	4.67	72	5.33	105	7.78	123	9.11	127 123	9.41 9.11	20 15	1.48 1.11	0 1
PAL–M CCIR601	63	4.67	78	5.78	111	8.22	123	9.11	127 123	9.41 9.11	20 15	1.48 1.11	0 1
NTSC Square	58	4.73	65	5.30	96	7.82	115	9.37	115 117	9.37 9.53	18 18	1.47 1.47	0 1
PAL–M Square	58	4.73	78	6.36	111	9.04	115	9.37	115 117	9.37 9.53	18 18	1.47 1.47	0 1
PAL-B CCIR601	63	4.67	76	5.63	106	7.85	133	9.85	142 133	10.52 9.85	20 11	1.48 0.81	0 1
PAL–N_c CCIR601	63	4.67	76	5.63	111	8.22	133	9.85	142 133	10.52 9.85	20 11	1.48 0.81	0 1
PAL–B Square	69	4.68	83	5.63	116	7.86	155	10.51	155 155	10.51 10.51	22 22	1.49 1.49	0 1
PAL-N_c Square(2)	69	4.68	83	5.63	111	7.53	155	10.51	155 155	10.51 10.51	22 22	1.49 1.49	0 1

Notes: (1). In slave mode, since Front Porch timing is triggered by the previous HSYNC pulse, any deviation from nominal line length can affect the front porch duration.
(2). PAL-N_c refers to the PAL format used in Argentina (Combination N).
3. CNT refers to the number of luminance pixel periods; with respect to the CLK pin, there are twice as many CLK periods as CNT periods.

Master Mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are generated from internal timing and optional software bits. HSYNC*, HSYNCO*, VSYNC* and VSYNCO* are output following the rising edge of CLK.

The horizontal counter is incremented on every other rising edge of CLK. After reaching the appropriate value (determined by the mode of operation), it is reset to one, indicating the start of a new line.

The vertical counter is incremented at the start of each new line. After reaching the appropriate value, determined by the mode of operation (see Table 12), it is reset to one, indicating the start of a new field (interlaced operation) or frame (noninterlaced operation). VSYNC* is asserted for 3 or 2.5 scan lines for 262/525 line and 312/625 line, respectively.

HSYNC* indicates the beginning of a new scan line. The beginning of an odd field is indicated by coincident falling edges of VSYNC* and HSYNC*; the beginning of an even field is indicated when VSYNC* falls in between (in the middle of) two falling edges of HSYNC*.

Slave Mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are inputs that are registered on the rising edge of CLOCK. The horizontal counter is incremented on the rising edge of CLOCK. A falling edge of HSYNC* resets it to one, indicating the start of a new line. The vertical counter is incremented on the falling edge of HSYNC*. A falling edge of VSYNC* resets it to one, indicating the start of a new field (interlaced operation) or frame (noninterlaced operation).

A falling edge of VSYNC* occurring within ±1/4 of a scan line from the falling edge of HSYNC* indicates the beginning of an odd field. A falling edge of VSYNC* occurring within ±1/4 scan line from the center of the line indicates the beginning of an even field. Referring to Figures 5–7a/7b start of VSYNC occurs on the falling HSYNC* at the beginning of the next expected odd field and halfway between expected falling HSYNC* edges at the beginning of the next expected even field.

An odd field is detected when VSYNC* falls within one-fourth of a scan line away from the falling edge of HSYNC*; an even field is assumed when VSYNC* falls outside of this time.

The operating mode (NTSC/PAL, interlaced/noninterlaced, Square Pixel/CCIR-601) can be programmed with the MODE[4:0] bits when the SETMODE bit is set high. Alternatively, when SETMODE is low, the mode is automatically detected in slave mode. For example, 525-line operation is assumed, 625-line operation is detected by the number of lines in a field. Interlaced operation is detected by observing the sequence of odd or even fields; if the field timing (odd follows odd, even follows even) is repeated, then noninterlaced mode is assumed. The frequency of operation (square pixels or CCIR-601) for both PAL and NTSC is detected by counting the number of clocks per line. The sampling note is assumed to be 13.5 MHz unless the exact horizontal count for square pixels, ±1 count, is detected in between two successive falling edges of HSYNC*.

NOTE: Square pixel 625-line operation with this sequence requires one frame to stabilize.

Burst Blanking

For interlaced NTSC, color burst information is automatically disabled on scan lines 1–9 and 264–272, inclusive. (SMPTE line numbering convention.)

For interlaced PAL-M, color burst information is automatically disabled on scan lines 1–11 and 263–273, inclusive. (SMPTE line numbering convention.)

For interlaced PAL-B, D, G, H, I, N, N_C, color burst information is automatically disabled on scan lines 1–6, 310–318, and 623–625, inclusive, for fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is disabled on scan lines 1–5, 311–319, and 622–625, inclusive.

For noninterlaced NTSC, color burst information is automatically disabled on scan lines 1–6 and 261–262, inclusive.

For noninterlaced PAL-M, color burst information is automatically disabled on scan lines 1–8 and 260–262, inclusive.

For noninterlaced PAL-B, D, G, H, I, N, N_C, color burst information is automatically disabled on scan lines 1–6 and 310–312, inclusive. See Figures 5–10.

Vertical Blanking Intervals

For interlaced NTSC/PAL-M, scan lines 1–9 and 263–272, inclusive, are always blanked. There is no setup on scan lines 10–21 and 273–284, inclusive, allowing the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately (except for lines controlled by closed caption or Macrovision generation).

For interlaced PAL-B, D, G, H, I, N, N_C, scan lines 1–6, 311–318, and 624–625, inclusive, during fields 1, 2, 5, and 6, are always blanked. During fields 3, 4, 7, and 8, scan lines 1–5, 311–319, and 624–625, inclusive, are always blanked. The remaining scan lines during the vertical blanking interval may be used for the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately.

Normally, all displayed lines in the vertical blanking interval (10–21 and 273–284 for interlaced NTSC/PAL-M; 7–13 and 320–335 for interlaced PAL-B, D, G, H, I, N, N_C) are forced to blank. It is possible to enable active video during the vertical blanking interval by setting register CMC, bit D2.

For noninterlaced NTSC/PAL-M, scan lines 1–9, inclusive, are always blanked. For noninterlaced PAL-B, D, G, H, I, N, N_C, scan lines 1–6 and 311–312, inclusive, are always blanked.

Digital Processing

Once the input data is converted into internal YUV format, the UV components are low-pass filtered with a filter response shown in Figure 11 (linearly scalable by clock frequency). The Y and filtered UV components are upsampled to CLK frequency by a digital filter whose response is shown in Figure 12.

Chrominance Disable

The chrominance subcarrier may be turned off by setting register DCHROMA to a logical one. This kills burst as well, providing luminance only signals on the CVBS outputs and a static blank level on the C output.

Subcarrier Phasing

To maintain correct SC-H phasings, subcarrier phase is set to zero on the falling edge of HSYNC* at the beginning of Field 1 (line 4 for NTSC, line 1 for PAL), unless subcarrier reset is disabled through software (register SCRESET). In slave mode, falling HSYNC* may lead or lag falling VSYNC* by 1/4 scan line.

Setting the SCRESET bit to one may be useful in situations where the ratio of CLK/2 to HSYNC* edges in a color frame is non-integer, which could produce a significant phase impulse by resetting to zero.

For a perfect clock input, the burst frequency is 4.43361875 MHz for PAL-B, D, G, H, I, N, 3.57561149 for PAL-M, 3.58205625 for PAL-N_c (Argentina), 3.579545 MHz for NTSC interlaced, and 3.579515 MHz for NTSC noninterlaced.

Noninterlaced Operation

The device can be operated in noninterlaced mode by setting register MODE1. When in noninterlaced master mode, the Bt866/7 always displays the odd-field, meaning that the falling edges of HSYNC* and VSYNC* will be output coincidentally.

A 30 Hz offset will be added to the color subcarrier frequency while in NTSC mode so that the color subcarrier phase will be inverted from field to field. Subcarrier phase is reset to zero upon rising RESET* and every four fields for NTSC or eight fields for PAL.

Transition from interlaced to noninterlaced in master mode, occurs during odd fields to prevent synchronization disturbance. In slave mode, transition occurs after a subsequent falling edge of VSYNC*.

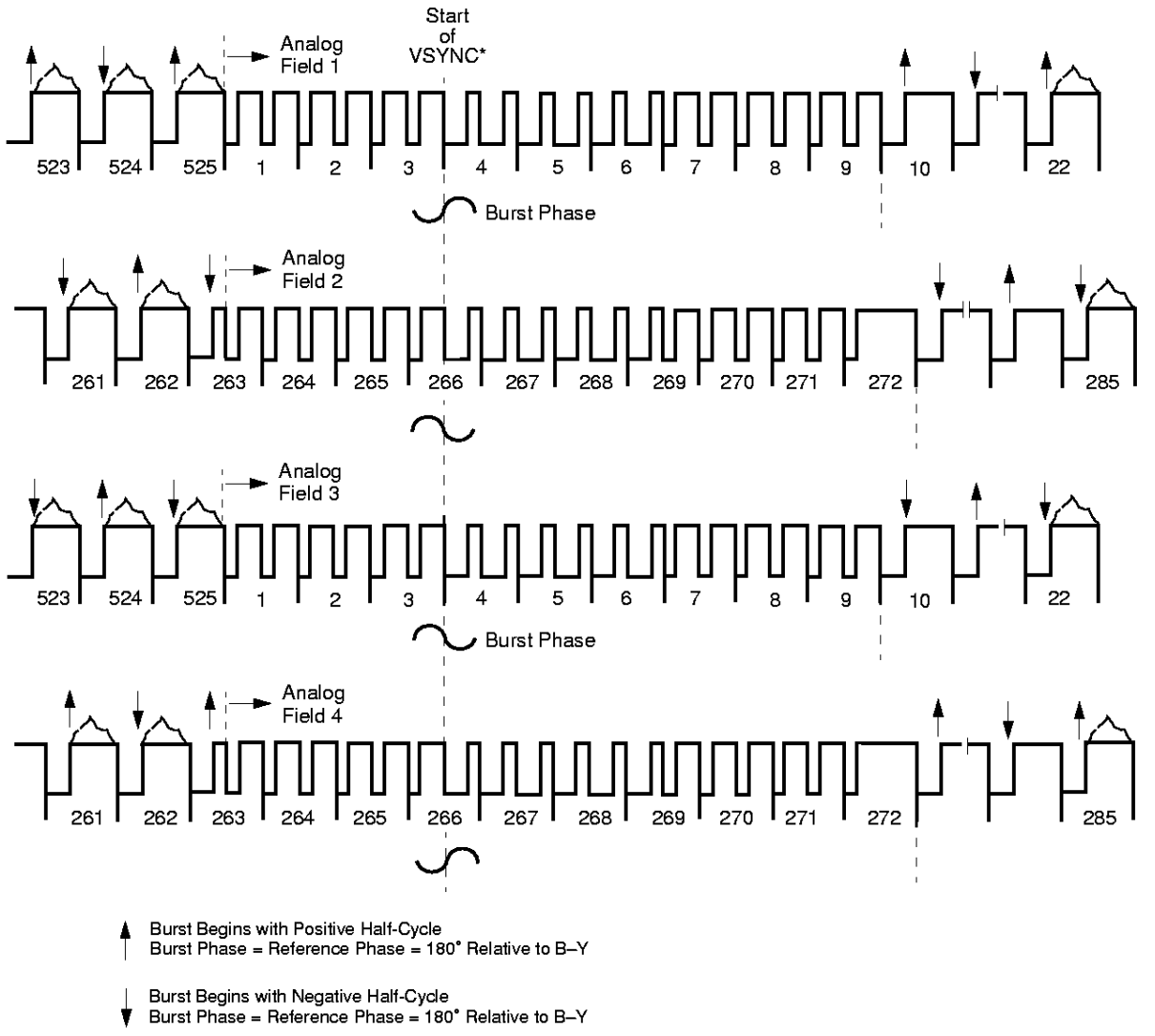
NOTE: Consumer VCRs can record noninterlaced video with minor noise artifacts, but special effects (e.g., scan > 2x) may not function properly.

Power-Down Mode

In power-down mode (SLEEP pin set to 1), register states are preserved, but other chip functionality (including I^2C communication) is disabled. This mode should be set when the Bt866/7 may be subjected to clock and data frequencies outside its functional range.

Register bit DACOFF will power-down the DACs when set high. This will result in the analog current being reduced almost to zero. It will have no effect on the digital current.

Figure 5. Interlaced 525-Line (NTSC) Video Timing



Note: SMPTE line numbering convention rather than CCIR-624 is used.

Figure 6. Interlaced 525-Line (PAL-M) Video Timing

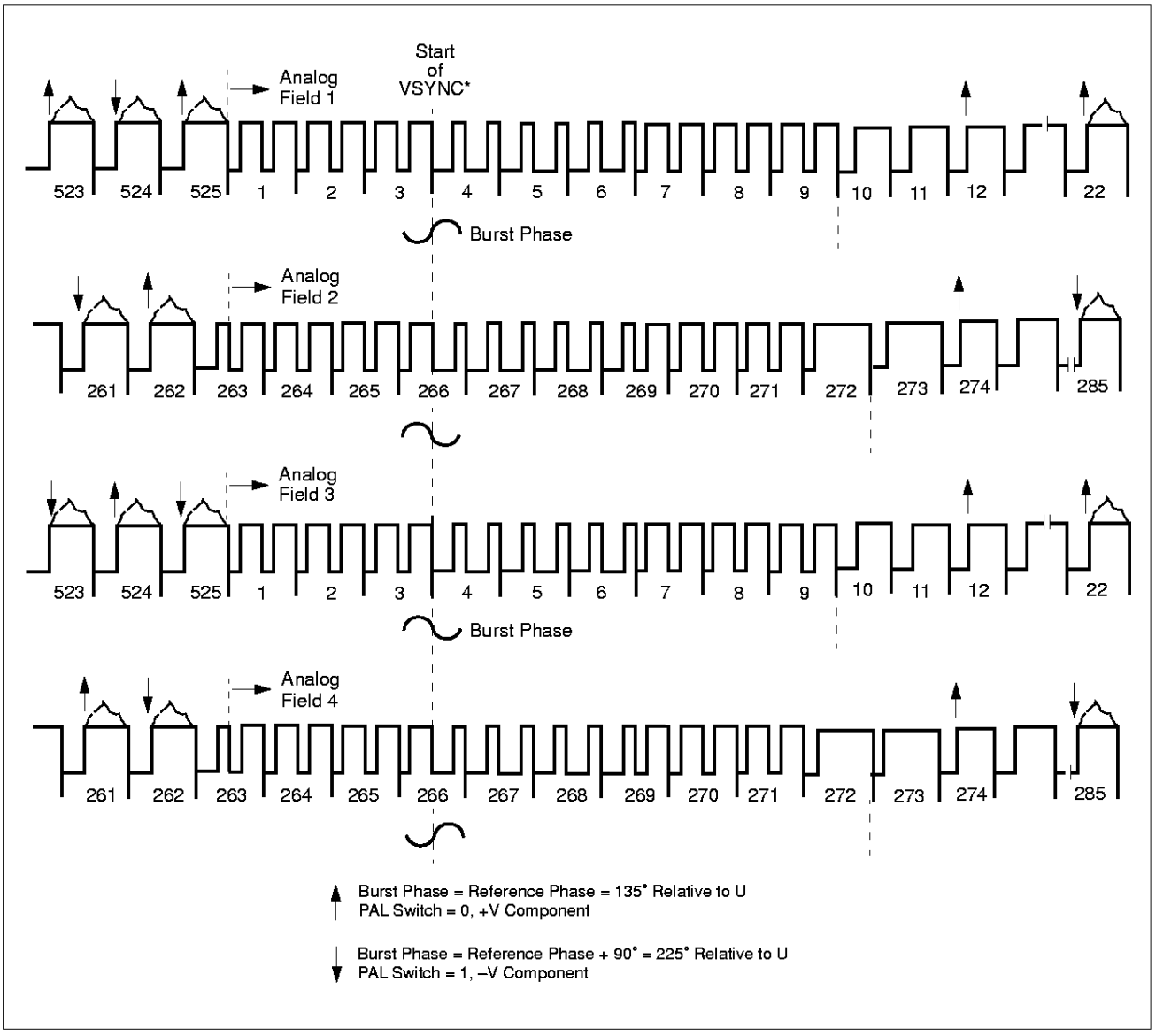


Figure 7a. Interlaced 625-Line (PAL-B, D, G, H, I, N, N_c) Video Timing (Field 1–4)

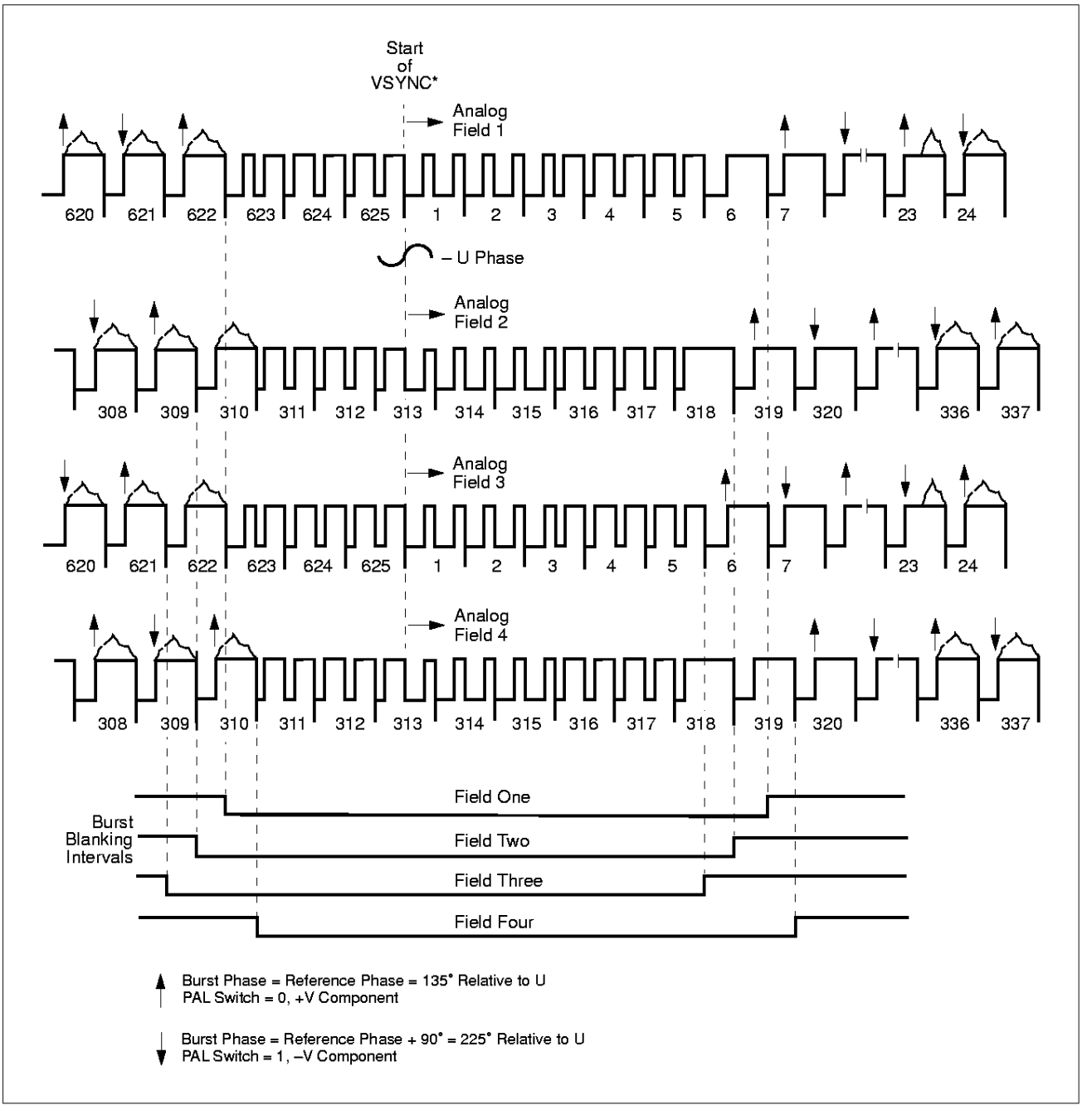


Figure 7b. Interlaced 625-Line (PAL-B, D, G, H, I, N, N_c) Video Timing (Field 5–8)

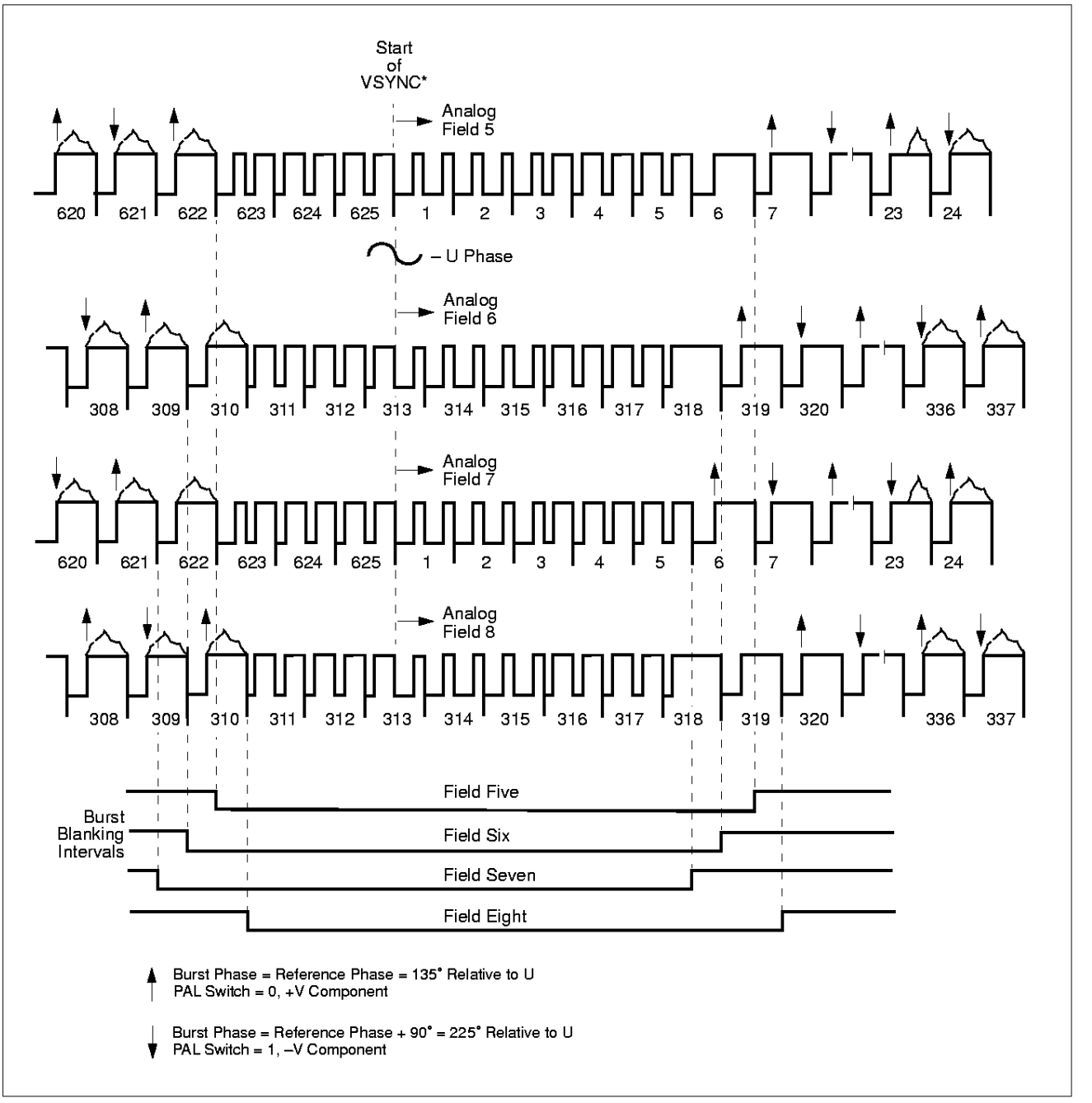


Figure 8. Noninterlaced 262-Line (NTSC) Video Timing

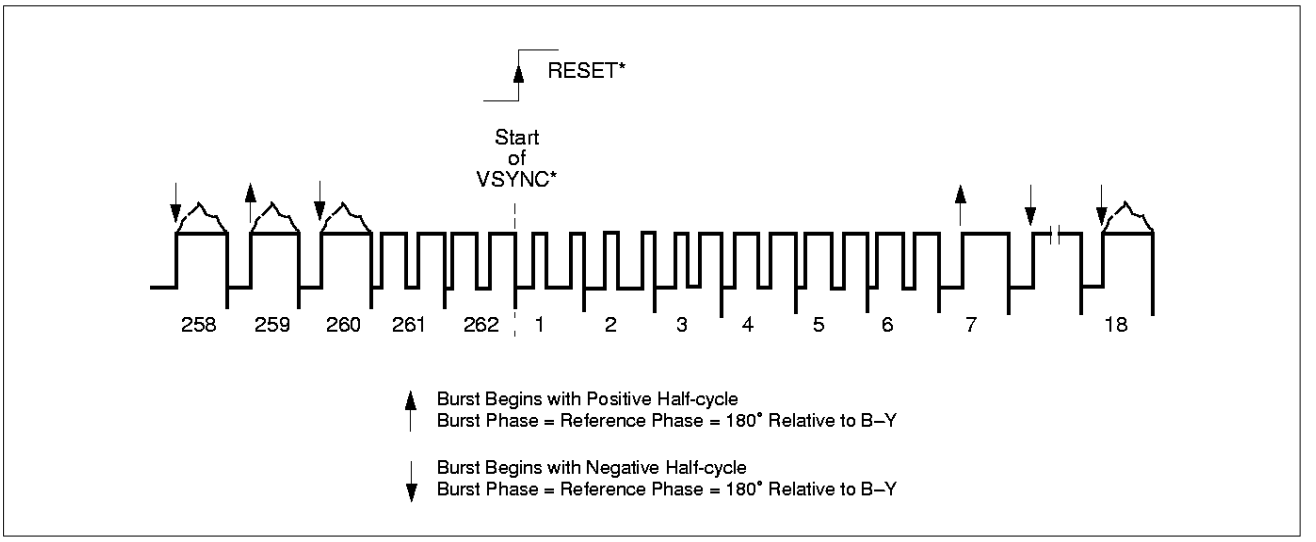


Figure 9. Noninterlaced 262-Line (PAL-M) Video Timing

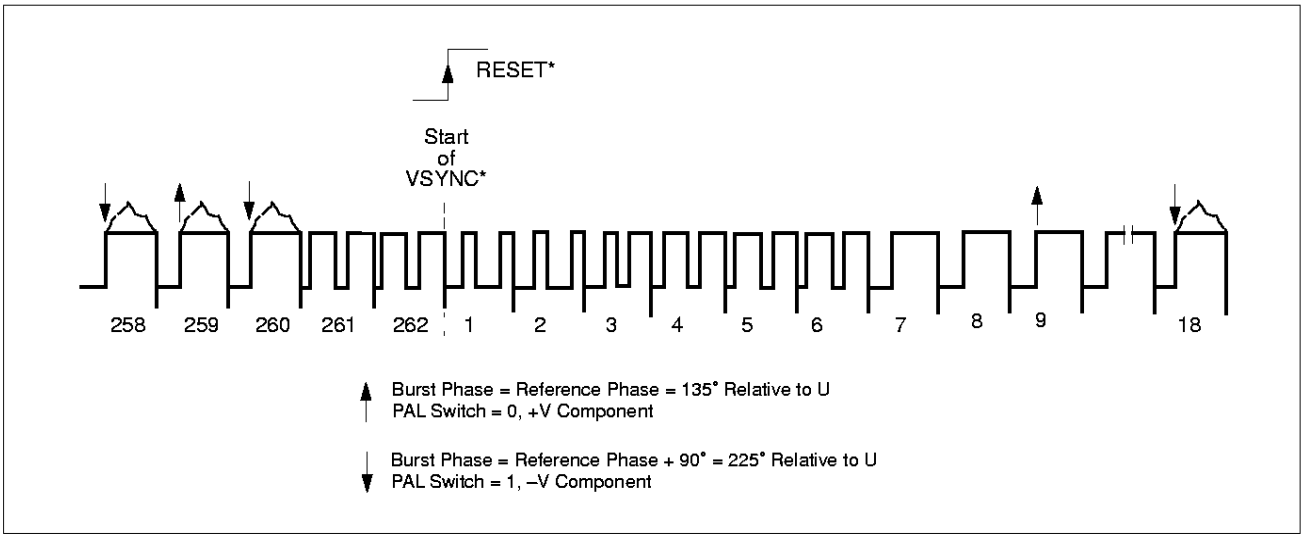


Figure 10. Noninterlaced 312-Line (PAL-B, D, G, H, I, N, N_c) Video Timing

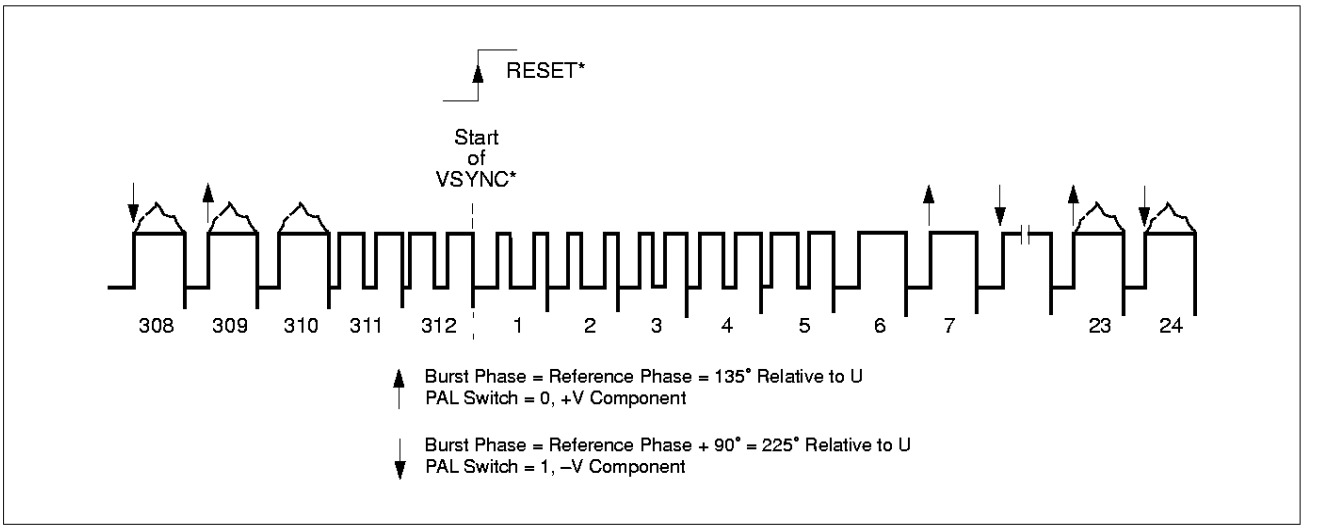


Figure 11. Three-Stage Chroma Filter

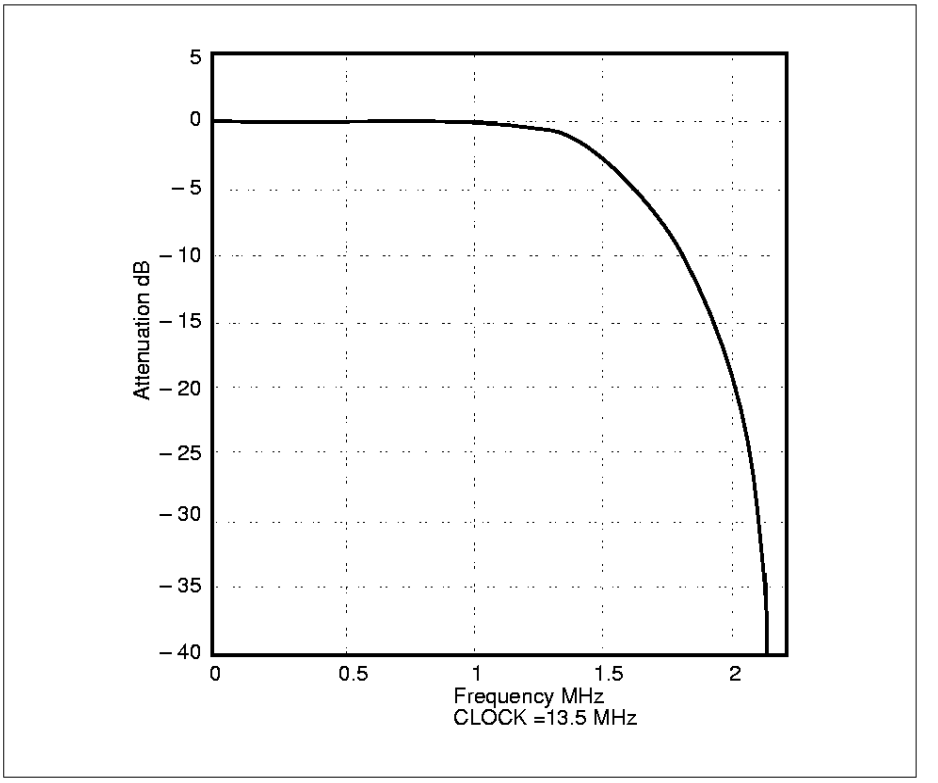
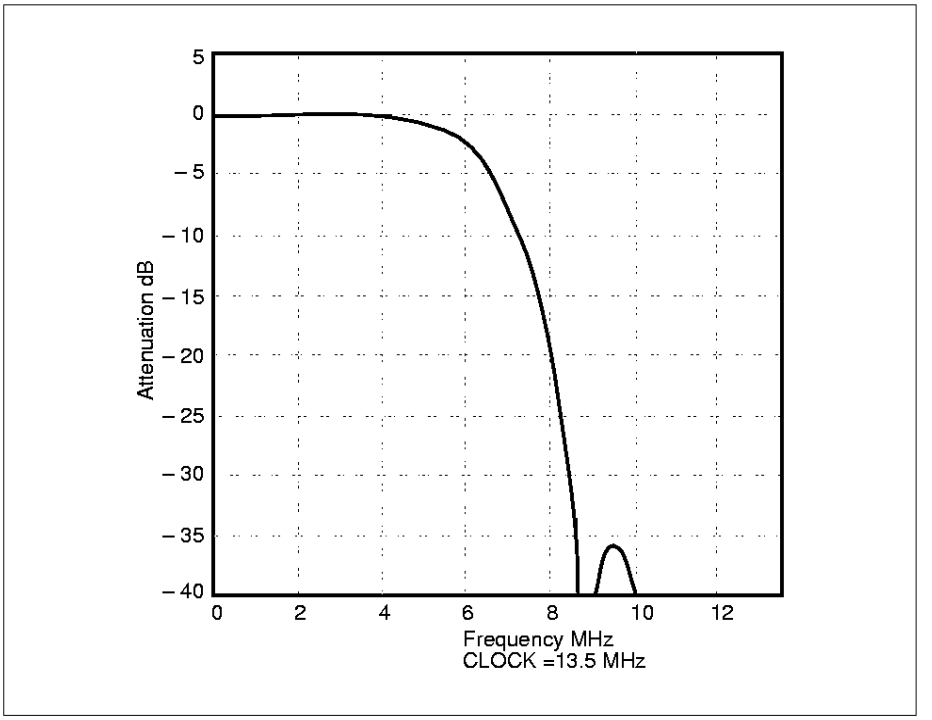


Figure 12. Luminance Upsampling Filter Response



Pixel Input Ranges and Colorspace Conversion

YC Inputs (4:2:2 YCrCb)

Chrominance scaling is programmable. Using the recommended values found in Table 13,Y has a nominal range of 16–235; Cb and Cr have a nominal range of 16–240, with 128 equal to zero. Values of 0 and 255 are interpreted as 1 and 254, respectively. Y values of 1–15 and 236–254, and CrCb values of 1–15 and 241–254, are interpreted as valid linear values.

Alternatively, register bit SETUP, will alter luma scaling and disable or enable the 7.5 IRE setup. Chroma scaling must be programmed with CRSCALE and CBSCALE registers. When the SETUP bit is enabled, PAL-B, D, G, H, I, N, N_c video can be generated using NTSC/PAL-M blanking levels and 7.5 IRE setup, and NTSC/PAL-M pixel scaling is performed (Y range of 16-235 represents 7.5-100 IRE); or, NTSC/PAL-M video can be generated using PAL-B, D, G, H, I, N, N_c scaling (Y range of 16-235 represents 0-100 IRE) without the 7.5 IRE setup. NTSC/PAL-M mode with setup disabled has 2% less black-to-white range than NTSC/PAL-M mode with setup enabled.

Overlays

There are fifteen 24-bit colors that can be written through the serial I^2C port. These lookup tables can then be selected on a pixel-by-pixel basis to control graphics overlays. Internally, overlays are inserted before any video processing, including color space conversion, sync insertion, and modulation. Therefore, all essential registers must be programmed to produce graphics or color bars, just as for normal video. Registers OSDY, OSDCR, and OSDCB contain the LUT values for Y, Cr, and Cb.

Two modes of accessibility for the LUTs are available: 8- and 15-color. The default mode allows access to only 8 colors. In this mode, overlays are enabled only when OSD[3] is high, and are disabled when OSD[3] is low. Pins OSD[2:0] select between 8 different overlay colors, numbered between 8 and 15, during any pixel period. For example, if OSD[2:0] is set to 7, colors OSDY15, OSDCR15, and OSDCB15 will be selected.

The 15-color mode is enabled by setting register bit OSDEXT. In 15-color mode, any nonzero setting of the OSD[3:0] pins will select an overlay color numbered between 1 and 15. Overlays are disabled (transparent mode) whenever all OSD[3:0] pins are set to zero. For example, if OSD[3:0] is set to 1, colors OSDY1, OSDCR1, and OSDCB1 will be selected.

By default, LUT values are 2's complement. Setting register bit OSDNUM will cause the LUTs to be interpreted as straight binary values.

Color bar mode is enabled by setting register bit OSDBAR. In this mode, the OSD pins are ignored, while the Bt867 cycles through colors 8–15. This allows the creation of custom 8-segment color bars, where the width of each color is exactly 1/8th of the active pixel region.

DAC Coding

White is represented by a DAC code of 400. For PAL-B, D, G, H, I, N, N_c, the standard blanking level is represented by a DAC code of 120. For NTSC/PAL-M, with setup enabled (SETUP bit = 0), the standard blanking level is represented by a DAC code of 114, 1 IRE is equivalent to a DAC code of 2.857. For NTSC/PAL-M with setup disabled (SETUP bit = 1), the standard blanking level is represented by a DAC code of 112, 1 IRE is equivalent to a DAC code of 2.800.

Closed Captioning

The Bt866/7 encodes closed captioning on scan line 21 and NTSC/PAL-M extended data services on scan line 284. Four 8-bit registers (CCF1B1, CCF1B2, CCF2B1, CCF2B2) provide the data, while register bits ECCF1 and ECCF2 enable display of the data. A logical zero corresponds to the blanking level of 0 IRE, while a logical one corresponds to 50 IRE above the blanking level.

Closed captioning for PAL-B, D, G, H, I, N, N_c is similar to that for NTSC. Closed caption encoding is performed for 625-line systems according to the system proposed by the National Captioning Institute; clock and data timing is identical to that of NTSC system, except that encoding is provided on lines 22 and 335.

It is possible to safeguard against redundant or incomplete data encoding (register bit ECCGATE). In this mode, encoding is disabled until a new complete pair of data bytes has been written to the CC data registers.

The Bt866/7 generates the clock run-in and appropriate timing automatically. Pixel inputs are ignored during CC encoding. See FCC Code of Federal Regulations (CFR) 47 Section 15.119 (10/91 edition or later) for programming information. EIA608 describes ancillary data applications for Field 2 Line 21 (line 284).

NOTE: Register contents are transferred immediately following the clock run-in; therefore, no register modifications should occur during line 21.

Anticopy Process (Bt867 Only)

The anticopy process contained within the Bt867 is implemented according to the Macrovision revision 6.1 specification developed by Macrovision in Sunnyvale, California. All luminance, chrominance, and composite video waveforms include the Macrovision anticopy process. The Bt867 incorporates an anticopy process technology that is protected by U.S. patents and other intellectual property rights. The anticopy process is licensed for non-commercial, home use only. Reverse engineering or disassembly is prohibited.

Brooktree cannot ship Bt867 units to any customer until that customer has been approved by Macrovision. To obtain approval for shipment of Bt867 samples, a "Macrovision Proprietary Material License Agreement" is required. Contact Macrovision at 408-743-8600 (FAX: 408-743-8610) to facilitate this agreement.

Internal Color Bars

The Bt866/7 can be configured to generate color bars (register bit OSDBAR) with the overlay lookup tables.

I²C Interface

A simplified I²C (7-bit subaddress, 100 Kbps) interface is provided for programming the registers. CLK must be applied and stable for I²C communication. Activating SLEEP or RESET* will disable I²C communication.

Outputs

All digital-to-analog converters are designed to drive standard video levels into an equivalent 37.5 Ω load. Unused outputs should be connected directly to ground to minimize supply switching currents. One composite video plus S-Video (YC) outputs are available. If the SLEEP pin is high, the DACs are essentially turned off and only the leakage current is present. The D/A converter values for 100% saturation, 100% amplitude color bars are shown in Figures 13–18.

Luminance (Y) Analog Output

Digital luminance information drives the 9-bit D/A converter that generates the analog Y video output (Figures 13 and 14 and Tables 4 and 5).

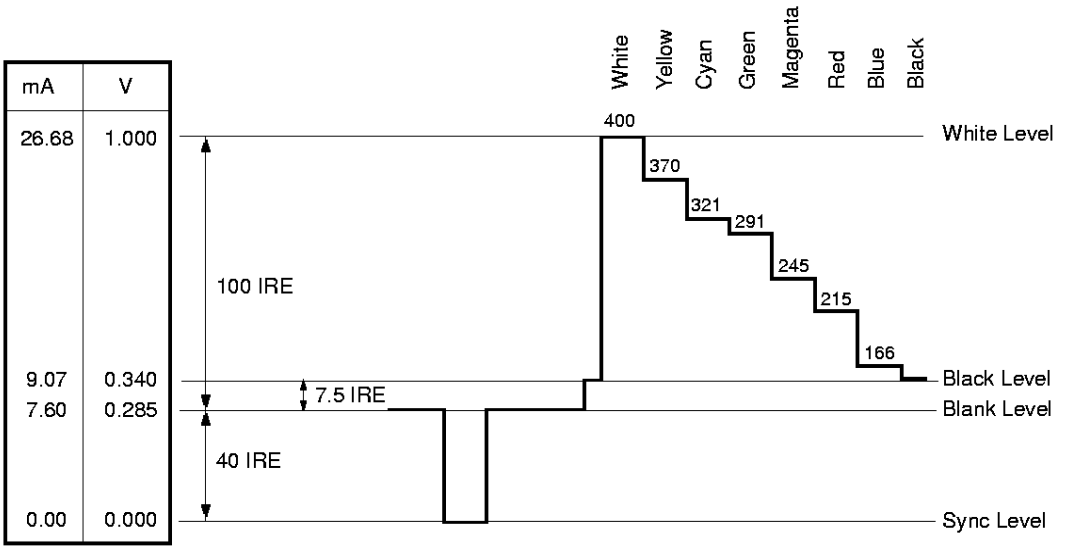
Chrominance (C) Analog Output

Digital chrominance information drives the 9-bit D/A converter that generates the analog C video output (Figures 15 and 16 and Tables 6 and 7).

Composite Video (CVBS) Output

Digital composite video information drives the 9-bit D/A converter that generates the analog NTSC or PAL video output (Figures 17 and 18 and Tables 8 and 9).

Figure 13. 525-Line (NTSC/PAL-M) Y (Luminance) Video Output Waveform



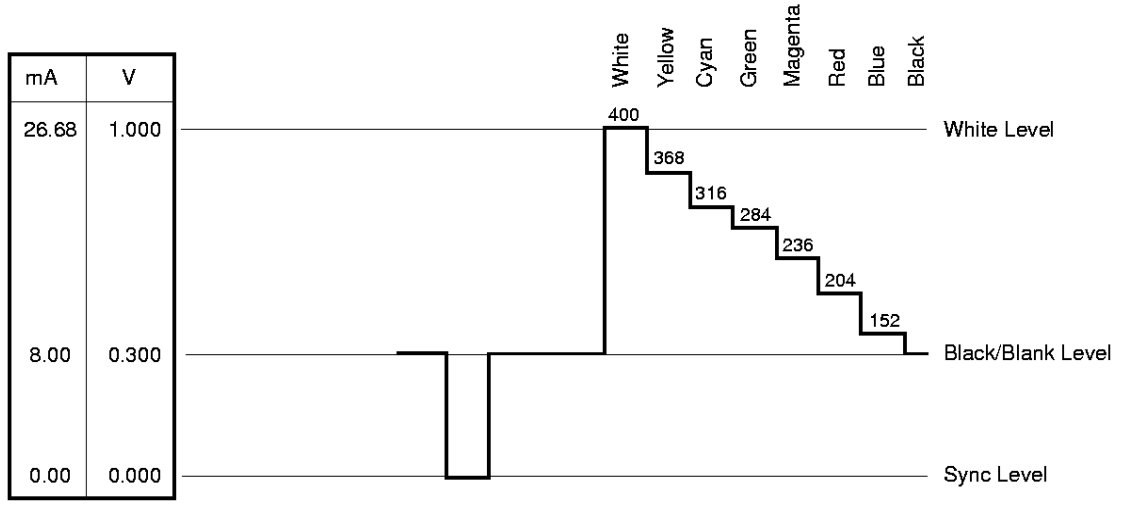
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, and setup on. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 4. 525-Line (NTSC/PAL-M) Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
White	26.68	400	0	1
Black	9.07	136	0	1
Blank	7.60	114	0	0
Sync	0	0	1	0

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, and setup on. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 14. 625-Line (PAL-B, D, G, H, I, N, N_c) Y (Luminance) Video Output Waveform



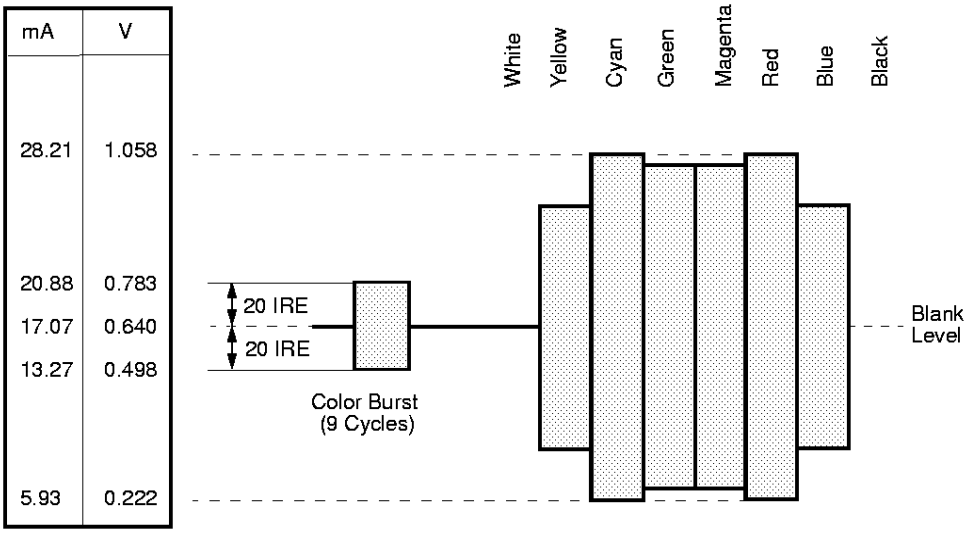
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, setup off, and nominal RSET. CCIR-624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Table 5. 625-Line (PAL-B, D, G, H, I, N, N_c) Y (Luminance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
White	26.68	400	0	1
Black	8.00	120	0	1
Blank	8.00	120	0	0
Sync	0	0	1	0

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, setup off, and nominal RSET. CCIR-624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Figure 15. 525-Line (NTSC/PAL-M) C (Chrominance) Video Output Waveform



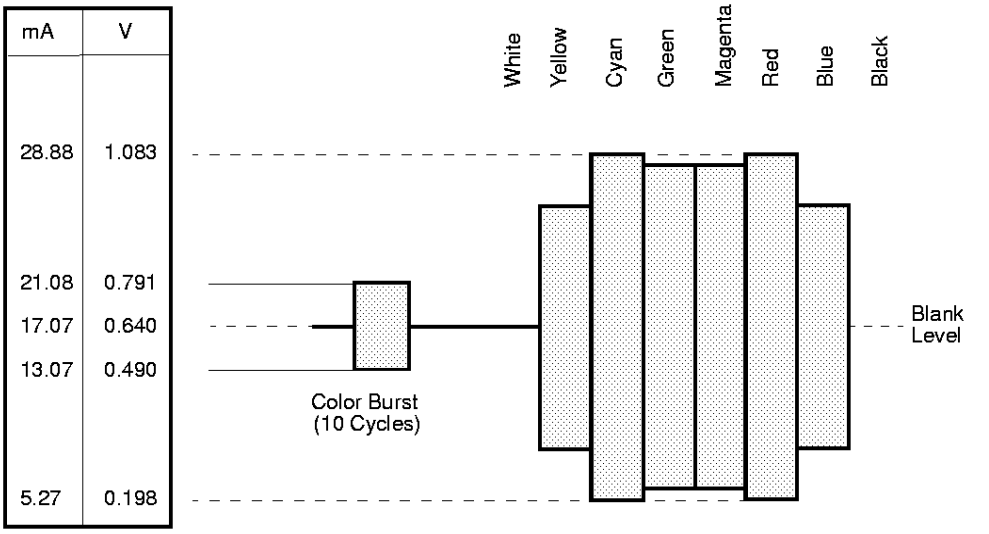
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, chroma on, and setup on. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 6. 525-Line (NTSC/PAL-M) C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
Peak Chroma (High)	28.21	423	x	1
Burst (High)	20.88	313	x	x
Blank	17.07	256	x	0
Burst (Low)	13.27	199	x	x
Peak Chroma (Low)	5.93	89	x	1

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, chroma on, and setup on. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 16. 625-Line (PAL-B, D, G, H, I, N, N_C) C (Chrominance) Video Output Waveform



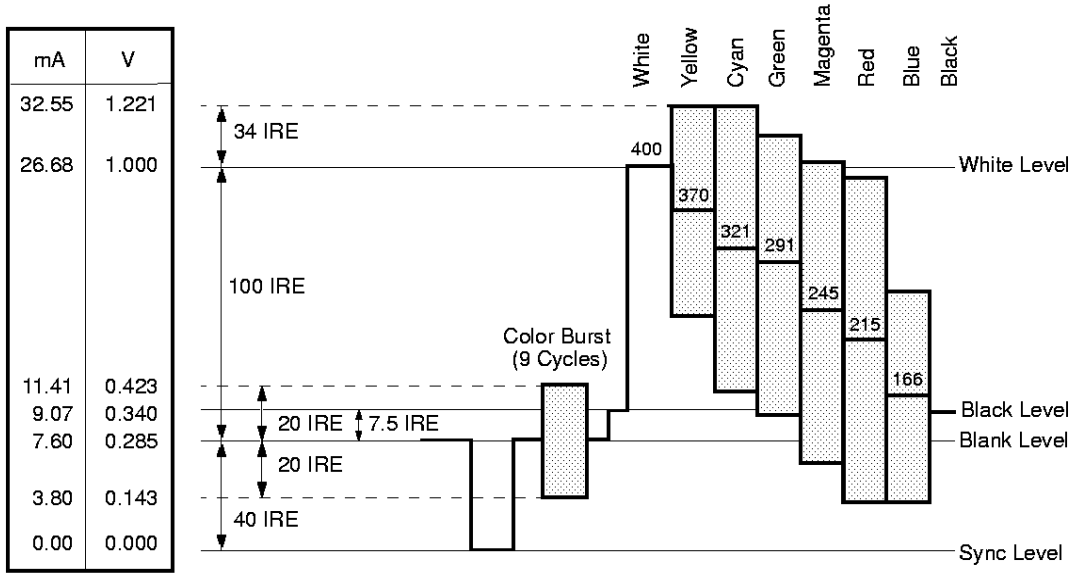
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, chroma on, and setup off. CCIR-624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Table 7. 625-Line (PAL-B, D, G, H, I, N, N_C) C (Chrominance) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
Peak Chroma (High)	28.88	433	x	1
Burst (High)	21.08	316	x	x
Blank	17.07	256	x	0
Burst (Low)	13.07	196	x	x
Peak Chroma (Low)	5.27	79	x	1

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, chroma on, and setup off. CCIR-624 levels are assumed. 100% saturation (100/0/100/0) color bars are shown.

Figure 17. Composite 525-Line (NTSC/PAL-M) Video Output Waveform



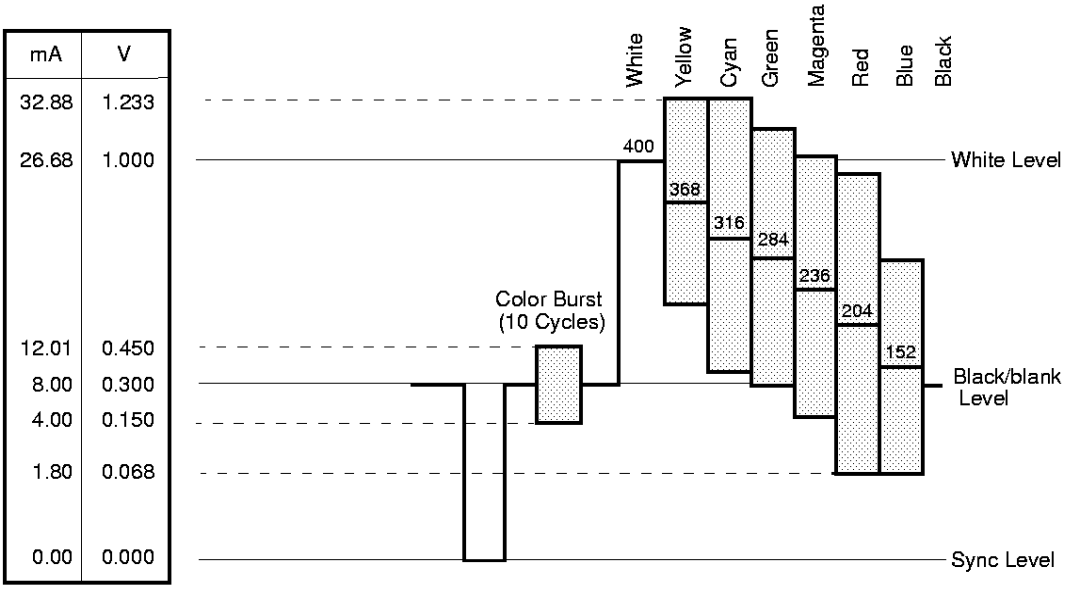
Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, clipping off, chroma on and setup on. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Table 8. Composite 525-Line (NTSC/PAL-M) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
Peak Chroma (High)	32.55	488	0	1
White	26.68	400	0	1
Burst (High)	11.41	171	0	x
Black	9.07	136	0	1
Blank	7.60	114	0	0
Burst (Low)	3.80	57	0	x
Peak Chroma (Low)	3.20	48	0	1
Sync	0	0	1	0

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, clipping off, chroma on and setup on. SMPTE-170 M levels are assumed. 100% saturation color bars (100/7.5/100/7.5) are shown.

Figure 18. Composite 625-Line (PAL-B, D, G, H, I, N, N_c) Video Output Waveform



Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, setup and clipping off. CCIR-624 levels are assumed. 100% amplitude, 100% saturation (100/0/100/0) color bars are shown.

Table 9. Composite 625-Line (PAL-B, D, G, H, I, N, N_c) Video Output Truth Table

Description	Iout (mA)	DAC Data	Sync Interval	BLANK*
Peak Chroma (High)	32.88	493	0	1
White	26.68	400	0	1
Burst (High)	12.01	180	0	x
Black	8.00	120	0	1
Blank	8.00	120	0	0
Burst (Low)	4.00	60	0	x
Peak Chroma (Low)	1.80	27	0	1
Sync	0	0	1	0

Note: Typical with 37.5 Ω load, VREF_IN = VREF_OUT, nominal RSET, setup and clipping off. CCIR-624 levels are assumed. 100% amplitude, 100% saturation (100/0/100/0) color bars are shown.