# SRAM DIE

# 1 MEG SYNCHRONOUS BURST SRAM

64K x 18, 32K x 32 and 32K x 36

## FEATURES

- 3.3V +10%/-5% power supply for D7 version
- 3.3V ±5% power supply for C4 or B2 version
- 5V-tolerant I/O
- SNOOZE MODE for reduced power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications

## GENERAL PHYSICAL SPECIFICATIONS

- Wafer thickness = 14.0 mils ±0.5 mils
- The backside wafer surface is polished bare silicon
- Typical metalization thickness 10.5K angstroms for the top level of metalization
- Typical lower-level metal thickness is 5.7K angstroms
- Metalization composition: 99.5% Al and 0.5% Cu over Titanium
- Typical topside passivation 3K angstroms undoped oxide with 4.5K angstroms of nitride over oxide
- Typical passivation openings: 4.5 x 4.5 mil
  115 x 115 µm

## OPTIONS — ORDER NUMBER

- Speed probing*

| | |
|---|---|
| **Nonpipelined** | |
| No speed probing | None |
| 9ns access | -9† |
| 10ns access | -10† |
| 11ns access | -11 |
| 12ns access | -12 |
| 14ns access | -14 |
| **Fully pipelined** | |
| No speed probing | None |
| 4.5ns access | -4.5† |
| 5ns access | -5† |
| 6ns access | -6† |
| 7ns access | -7 |
| 8ns access | -8 |

- Form

| | |
|---|---|
| Die | D |
| Wafer | W |

**DIE DATA BASE S25A**
**DIE OUTLINE (see page 5)**

**Die size:** 271 x 303 mil
6,883 x 7,696 µm
See Bond Pad Location and Identification Table on page 4.

## OPTIONS — ORDER NUMBER

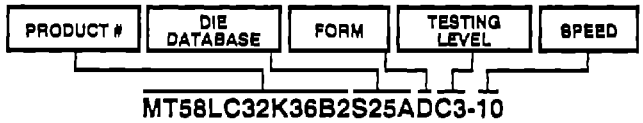
- Testing levels**

| | |
|---|---|
| Standard Probe | C1 |
| Speed Probe | C2 |
| PROBE Plus™ | C3 |
| KGD Plus® (Known Good Die) | C7 |

*Refer to "Speed Probe" section of this data sheet. Speed designator should not be included in die part number for C1 level product.
**Refer to "Die Testing Procedures" section of this data sheet.
† Available as C2 and C3 level product only.

## ORDER INFORMATION

- **Selectable Burst Sequence, Pipelined**
  64K x 18 — MT58LC64K18C4S25A
- **Selectable Burst Sequence, Pipelined, Single-Cycle Deselect**
  64K x 18 — MT58LC64K18D7S25A
- **Selectable Burst Sequence, Flow-Through**
  64K x 18 — MT58LC64K18B2S25A
- **Selectable Burst Sequence, Pipelined**
  32K x 32 — MT58LC32K32C4S25A
- **Selectable Burst Sequence, Pipelined, Single-Cycle Deselect**
  32K x 32 — MT58LC32K32D7S25A
- **Selectable Burst Sequence, Flow-Through**
  32K x 32 — MT58LC32K32B2S25A
- **Selectable Burst Sequence, Pipelined**
  32K x 36 — MT58LC32K36C4S25A
- **Selectable Burst Sequence, Pipelined, Single-Cycle Deselect**
  32K x 36 — MT58LC32K36D7S25A
- **Selectable Burst Sequence, Flow-Through**
  32K x 36 — MT58LC32K36B2S25A



## GENERAL DESCRIPTION

Micron SRAMs are fabricated using an advanced CMOS process. The Micron MT58LC64K18, MT58LC32K32 and MT58LC32K36 are randomly accessed solid-state memories organized in a x18, x32 or x36 configuration.

### DIE TESTING PROCEDURES

Micron has established four testing levels for die products. Most Micron products are tested to Standard Probe (C1) level. Selected products are available as Speed Probe (C2) level. Customers especially concerned with reducing the infant mortality rate may choose the PROBE$^{Plus}$ (C3) level. KGD$^{Plus}$ (Known Good Die) (C7) level product is available on selected products as market demand dictates. Level C2, C3 and C7 products are designed to provide customers with improved yields over C1.

### STANDARD PROBE (C1)

Micron probes wafers at a temperature with limits guardbanded to assure product performance from 0°C to 70°C in Micron's standard packaging. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the die junction temperature remains within specified limits. A high voltage functional stress test will be performed at probe to assure minimum junction breakdown integrity. $V_{BB}$ (substrate bias voltage) is a forced condition at wafer probe.

Wafer probe consists of various functional and parametric tests of each die. Test patterns, timing, voltage margins, limits and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield or performance of the product.

Die users may experience differences in performance relative to our data sheet. This is due to differences in package capacitance, inductance, resistance and trace length.

### SPEED PROBE (C2)

In addition to the testing performed at Standard Probe (C1), Micron also offers Speed Probe (C2). Micron's Hot Chuck Speed Probe assures the speed performance of die products for the fastest speed grades. Speed probing tests for most data sheet parameters and may increase yield over C1-level. C2-level die have not received burn-in and therefore are still subject to infant mortality failures.

### PROBE$^{Plus}$ (C3)

PROBE$^{Plus}$ or burned-in die incorporates all the testing done in the C2-level die as well as a burn-in step. The addition of the intelligent burn-in allows the devices to be operated until they have passed the infant mortality stage.

### KGD$^{Plus}$ (KNOWN GOOD DIE) (C7)

In order to provide the customer with fully warranted die product, Micron has developed a Known Good Die process designed to provide customers with die products of equal quality and reliability to packaged products. Micron's KGD$^{Plus}$ process allows Micron to fully test and burn-in die product after it has been tested to C1 level.

## FUNCTIONAL SPECIFICATIONS

Please refer to the packaged product data sheets found in the applicable Micron data book, for functional and parametric specifications. The specifications are provided for reference only on C1- and C2-level die product. On C2 and C3-level product $^{t}KQ$ is guaranteed. C7-level product is warranted to the data sheet.

## DIE AND WAFER LEVEL CONSIDERATIONS

Only C1- and C2-level products are available in wafer level form. Burned-in die (C3) or KGD die (C7) are available only in die form. C2-level wafers are shipped with a user's wafer map indicating speed. Users should be aware that there may be multiple speed grades on wafers shipped with a C2 level.

## BONDING INSTRUCTIONS

The S25A SRAM die has 100 bond pads. Refer to the bond pad location and identification table for a complete listing of bond pads and coordinates.

The S25A SRAM die is available in three separate configurations: 64K x 18, 32K x 32 or 32K x 36. Each of these configurations allows the user, through bonding options, to customize the feature set for the intended application and processor base. The four feature sets include the linear and interleaved burst sequence with fully pipelined or nonpipelined versions of each. The mode pad selects between the interleaved and linear burst sequences. Table 1 shows various bonding options that must be wired for different versions of the die (see Table 1).

The S25A SRAM die has an internal substrate bias generator for normal operation, bond pad 47 ($V_{BB}$) is used for manufacturing tests only. Normal bonding leaves bond pad 47 open (not bonded). Users must place a bond wire on each VccQ, VssQ, Vcc and Vss bond pad for improved noise immunity. It is important that the back of the die be kept isolated from any other devices sharing a common package or substrate, since the die substrate is internally driven to a negative voltage.

The die also has several pads defined as "Do Not Use" (DNU). These pads are used for engineering purposes and should NOT be used. Bonding these pads could result in non-functional die.

The 1 Meg SRAM device operates from a single +3.3V power supply and all inputs and outputs are fully low-voltage TTL- compatible.

## WAFER SAW

Standard wafer saw cuts the die 100 percent through. Micron holds die dimensions to a maximum tolerance of +0/-1 mil of each cut, as measured from the vertical cut. For clarification purposes, the die size provided is measured from center to center of the die street. A finished die is approximately 1.5 mils smaller on each side due to the sawing operation. As an example, a 340 mil x 411 mil die is approximately 338.5 mil x 409.5 mil after sawing.

## PACKAGING

For packaging, Micron utilizes Gel-Pak®. Please refer to the Micron Technical Note (TN-00-03) "Using Gel-Pak Trays with Micron Die," for more information. We package all die with the top metalization consistently oriented (refer to Figure 1). External packaging is suitable for electrostatic discharge protection. Each package is individually self-locking, or closed with a conductive clip and labeled with the following information:

- Generic device type and data base (Example: 32K36C4S25A)
- Micron fabrication lot number
- Speed grade of the die (optional)
- Quantity of die in package

**Table 1**
**FEATURE SET BONDING OPTIONS**

| PART NUMBER (FEATURE SET) | BOND PAD INSTRUCTIONS | | |
|---|---|---|---|
| | 13 | 36 | 88 |
| MT58LC64K18D7 | Vcc | DNU | DNU |
| MT58LC64K18C4 | Vcc | Vss | DNU |
| MT58LC64K18B2 | DNU | DNU | DNU |
| MT58LC32K32D7 | Vcc | DNU | Vss |
| MT58LC32K32C4 | Vcc | Vss | Vss |
| MT58LC32K32B2 | DNU | DNU | Vss |
| MT58LC32K36D7 | Vcc | DNU | DNU |
| MT58LC32K36C4 | Vcc | Vss | DNU |
| MT58LC32K36B2 | DNU | DNU | DNU |

## STORAGE REQUIREMENTS

Micron die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the Gel-Pak to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times during inspection and assembly.

## PRODUCT RELIABILITY MONITORS

Reliability of KGD$^{Plus}$ or C7 is monitored by ongoing QA reliability evaluations. Micron's QA department samples product families on a continuous basis for reliability studies. These studies include high temperature operating life (HTOL) tests for failure in time (FIT) calculations. A summary of these product family evaluations is published on a regular basis.

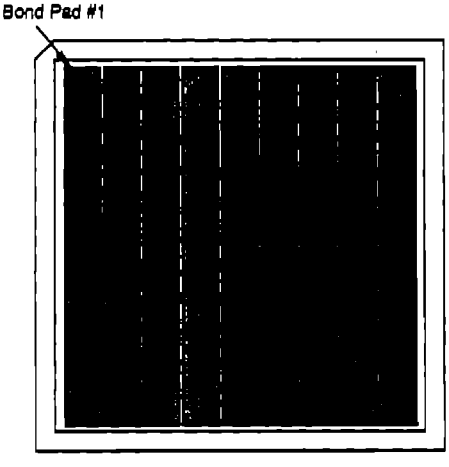



**Figure 1**
**ORIENTATION OF DIE IN GEL-PAK**

## BOND PAD LOCATION AND IDENTIFICATION TABLE

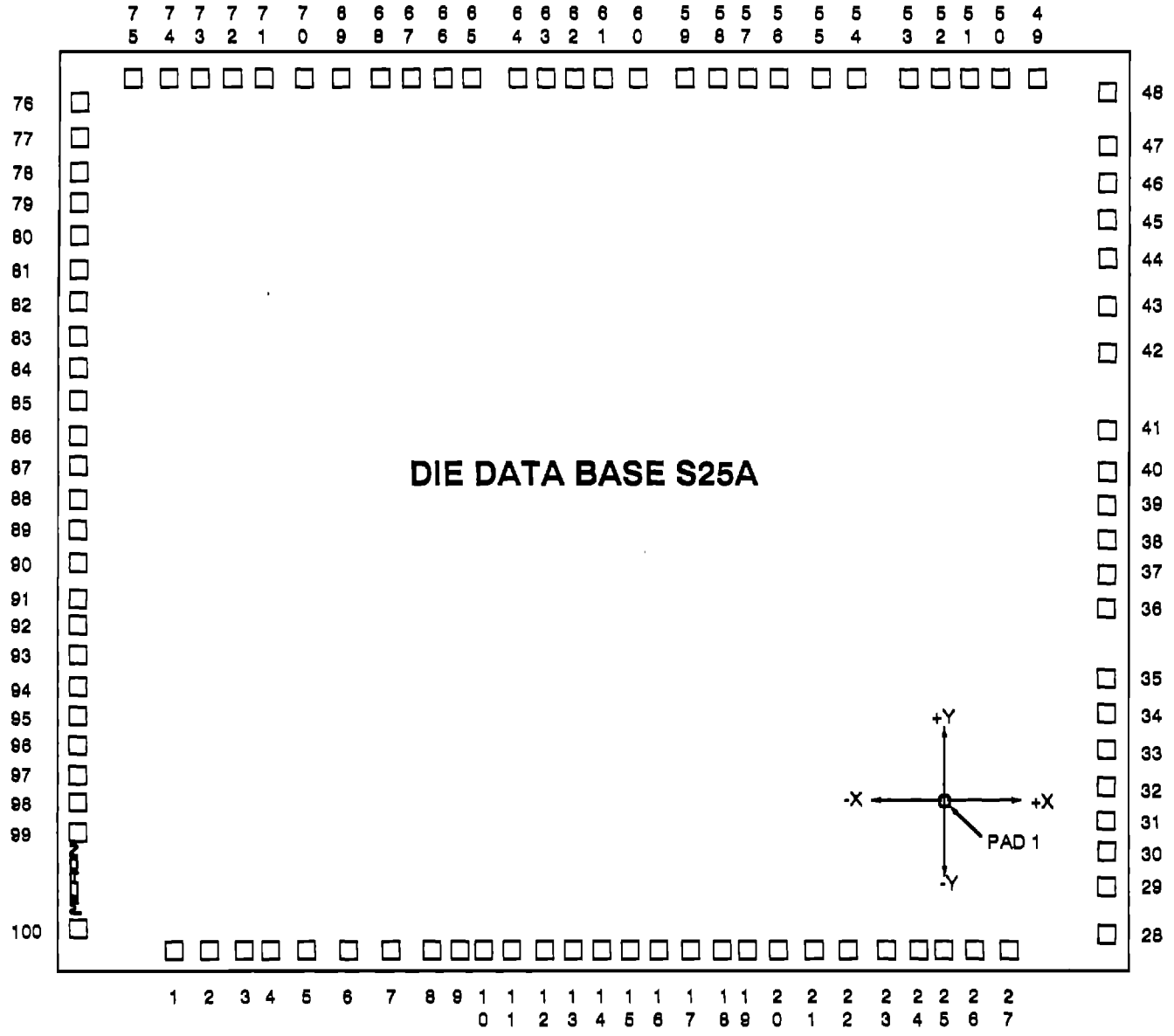
| | | | FROM CENTER OF #1 | | | |
|---|---|---|---|---|---|---|
| PAD # | MT58LC64K18 | MT58LC32K36<br>MT58LC32K32 | "X"[2]<br>INCHES | "Y"[2]<br>INCHES | "X"[2]<br>MICRONS | "Y"[2]<br>MICRONS |
| 1 | DNU[1] | DQ17 | 0.000000 | 0.000000 | 0.0 | 0.0 |
| 2 | DNU | DQ18 | 0.010885 | 0.000000 | 276.5 | 0.0 |
| 3 | VccQ | VccQ | 0.019162 | 0.000000 | 486.7 | 0.0 |
| 4 | VssQ | VssQ | 0.026167 | 0.000000 | 664.6 | 0.0 |
| 5 | DNU | DQ19 | 0.034444 | 0.000000 | 874.9 | 0.0 |
| 6 | DNU | DQ20 | 0.045909 | 0.000000 | 1,166.1 | 0.0 |
| 7 | DQ9 | DQ21 | 0.056491 | 0.000000 | 1,434.9 | 0.0 |
| 8 | DQ10 | DQ22 | 0.067376 | 0.000000 | 1,711.4 | 0.0 |
| 9 | VssQ | VssQ | 0.075654 | 0.000000 | 1,921.6 | 0.0 |
| 10 | VccQ | VccQ | 0.082658 | 0.000000 | 2,099.5 | 0.0 |
| 11 | DQ11 | DQ23 | 0.090935 | 0.000000 | 2,309.8 | 0.0 |
| 12 | DQ12 | DQ24 | 0.101820 | 0.000000 | 2,586.2 | 0.0 |
| 13 | BondOpt[3] | BondOpt[3] | 0.110387 | 0.000000 | 2,803.8 | 0.0 |
| 14 | Vcc | Vcc | 0.118274 | 0.000000 | 3,004.2 | 0.0 |
| 15 | Vss | Vss | 0.126161 | 0.000000 | 3,204.5 | 0.0 |
| 16 | DQ13 | DQ25 | 0.134438 | 0.000000 | 3,414.7 | 0.0 |
| 17 | DQ14 | DQ26 | 0.145323 | 0.000000 | 3,691.2 | 0.0 |
| 18 | VccQ | VccQ | 0.153600 | 0.000000 | 3,901.4 | 0.0 |
| 19 | VssQ | VssQ | 0.160605 | 0.000000 | 4,079.4 | 0.0 |
| 20 | DQ15 | DQ27 | 0.168882 | 0.000000 | 4,289.6 | 0.0 |
| 21 | DQ16 | DQ28 | 0.179767 | 0.000000 | 4,566.1 | 0.0 |
| 22 | DQP2 | DQ29 | 0.190350 | 0.000000 | 4,834.9 | 0.0 |
| 23 | DNU | DQ30 | 0.201814 | 0.000000 | 5,126.1 | 0.0 |
| 24 | VssQ | VssQ | 0.210091 | 0.000000 | 5,336.3 | 0.0 |
| 25 | VccQ | VccQ | 0.217096 | 0.000000 | 5,514.2 | 0.0 |
| 26 | DNU | DQ31 | 0.225373 | 0.000000 | 5,724.5 | 0.0 |
| 27 | DNU | DQ32 | 0.236258 | 0.000000 | 6,001.0 | 0.0 |
| 28 | DNU | DNU/DQP4[4] | 0.264668 | 0.005468 | 6,722.6 | 138.9 |
| 29 | MODE | MODE | 0.264668 | 0.023748 | 6,722.6 | 603.2 |
| 30 | A5 | A5 | 0.264668 | 0.033247 | 6,722.6 | 844.5 |
| 31 | A4 | A4 | 0.264668 | 0.042910 | 6,722.6 | 1,089.9 |
| 32 | A3 | A3 | 0.264668 | 0.052913 | 6,722.6 | 1,344.0 |
| 33 | A2 | A2 | 0.264668 | 0.062413 | 6,722.6 | 1,585.3 |
| 34 | A1 | A1 | 0.264668 | 0.071912 | 6,722.6 | 1,826.6 |
| 35 | A0 | A0 | 0.264668 | 0.080630 | 6,722.6 | 2,048.0 |
| 36 | BondOpt[3] | BondOpt[3] | 0.264668 | 0.107540 | 6,722.6 | 2,731.5 |
| 37 | Vss | Vss | 0.264668 | 0.115830 | 6,722.6 | 2,942.1 |
| 38 | Vss | Vss | 0.264668 | 0.123704 | 6,722.6 | 3,142.1 |
| 39 | Vcc | Vcc | 0.264668 | 0.131578 | 6,722.6 | 3,342.1 |
| 40 | Vcc | Vcc | 0.264668 | 0.139452 | 6,722.6 | 3,542.1 |
| 41 | DNU | DNU | 0.264668 | 0.150791 | 6,722.6 | 3,830.1 |
| 42 | A15 | A10 | 0.264668 | 0.176592 | 6,722.6 | 4,485.4 |
| 43 | A14 | A11 | 0.264668 | 0.188737 | 6,722.6 | 4,793.9 |
| 44 | A13 | A12 | 0.264668 | 0.201474 | 6,722.6 | 5,117.4 |
| 45 | A12 | A13 | 0.264668 | 0.211754 | 6,722.6 | 5,378.6 |
| 46 | A11 | A14 | 0.264668 | 0.221417 | 6,722.6 | 5,624.0 |
| 47 | Vss | Vss | 0.264668 | 0.231874 | 6,722.6 | 5,889.6 |
| 48 | DNU | DNU/DQP1[4] | 0.264668 | 0.249877 | 6,722.6 | 6,346.9 |
| 49 | DNU | DQ1 | 0.236246 | 0.255345 | 6,000.6 | 6,485.8 |
| 50 | DNU | DQ2 | 0.225361 | 0.255345 | 5,724.2 | 6,485.8 |
| 51 | VccQ | VccQ | 0.217083 | 0.255345 | 5,513.9 | 6,485.8 |
| 52 | VssQ | VssQ | 0.210079 | 0.255345 | 5,336.0 | 6,485.8 |
| 53 | DNU | DQ3 | 0.201802 | 0.255345 | 5,125.8 | 6,485.8 |
| 54 | DNU | DQ4 | 0.190337 | 0.255345 | 4,834.6 | 6,485.8 |
| 55 | DQ1 | DQ5 | 0.179754 | 0.255345 | 4,565.8 | 6,485.8 |

## BOND PAD LOCATION AND IDENTIFICATION TABLE

| | | | FROM CENTER OF #1 | | | |
|---|---|---|---|---|---|---|
| PAD # | MT58LC64K18 | MT58LC32K36<br>MT58LC32K32 | "X"[2]<br>INCHES | "Y"[2]<br>INCHES | "X"[2]<br>MICRONS | "Y"[2]<br>MICRONS |
| 56 | DQ2 | DQ6 | 0.168869 | 0.255345 | 4,289.3 | 6,485.8 |
| 57 | VssQ | VssQ | 0.160592 | 0.255345 | 4,079.0 | 6,485.8 |
| 58 | VccQ | VccQ | 0.153587 | 0.255345 | 3,901.1 | 6,485.8 |
| 59 | DQ3 | DQ7 | 0.145310 | 0.255345 | 3,690.9 | 6,485.8 |
| 60 | DQ4 | DQ8 | 0.134425 | 0.255345 | 3,414.4 | 6,485.8 |
| 61 | ZZ | ZZ | 0.125858 | 0.255345 | 3,196.8 | 6,485.8 |
| 62 | Vcc | Vcc | 0.117972 | 0.255345 | 2,996.5 | 6,485.8 |
| 63 | Vss | Vss | 0.110085 | 0.255345 | 2,796.2 | 6,485.8 |
| 64 | DQ5 | DQ9 | 0.101608 | 0.255345 | 2,585.9 | 6,485.8 |
| 65 | DQ6 | DQ10 | 0.090923 | 0.255345 | 2,309.4 | 6,485.8 |
| 66 | VccQ | VccQ | 0.082646 | 0.255345 | 2,099.2 | 6,485.8 |
| 67 | VssQ | VssQ | 0.075641 | 0.255345 | 1,921.3 | 6,485.8 |
| 68 | DQ7 | DQ11 | 0.067364 | 0.255345 | 1,711.0 | 6,485.8 |
| 69 | DQ8 | DQ12 | 0.056479 | 0.255345 | 1,434.6 | 6,485.8 |
| 70 | DQP1 | DQ13 | 0.045896 | 0.255345 | 1,165.8 | 6,485.8 |
| 71 | DNU | DQ14 | 0.034432 | 0.255345 | 874.6 | 6,485.8 |
| 72 | VssQ | VssQ | 0.026154 | 0.255345 | 664.3 | 6,485.8 |
| 73 | VccQ | VccQ | 0.019150 | 0.255345 | 486.4 | 6,485.8 |
| 74 | DNU | DQ15 | 0.010872 | 0.255345 | 276.2 | 6,485.8 |
| 75 | DNU | DQ16 | -0.000013 | 0.255345 | -0.3 | 6,485.8 |
| 76 | A10 | DNU/DQP2[4] | -0.025121 | 0.247609 | -638.1 | 6,289.3 |
| 77 | DNU | DNU | -0.025121 | 0.239282 | -638.1 | 6,077.8 |
| 78 | A9 | A9 | -0.025121 | 0.230728 | -638.1 | 5,860.5 |
| 79 | DNU | DNU | -0.025121 | 0.222488 | -638.1 | 5,651.2 |
| 80 | A8 | A8 | -0.025121 | 0.214299 | -638.1 | 5,443.2 |
| 81 | $\overline{ADV}$ | $\overline{ADV}$ | -0.025121 | 0.204800 | -638.1 | 5,201.9 |
| 82 | $\overline{ADSP}$ | $\overline{ADSP}$ | -0.025121 | 0.195301 | -638.1 | 4,960.6 |
| 83 | $\overline{ADSC}$ | $\overline{ADSC}$ | -0.025121 | 0.185802 | -638.1 | 4,719.4 |
| 84 | $\overline{OE}$ | $\overline{OE}$ | -0.025121 | 0.176302 | -638.1 | 4,478.1 |
| 85 | $\overline{BWE}$ | $\overline{BWE}$ | -0.025121 | 0.166803 | -638.1 | 4,236.8 |
| 86 | $\overline{GW}$ | $\overline{GW}$ | -0.025121 | 0.156523 | -638.1 | 3,975.7 |
| 87 | CLK | CLK | -0.025121 | 0.147605 | -638.1 | 3,754.2 |
| 88 | BondOpt[3] | BondOpt[3] | -0.025121 | 0.137524 | -638.1 | 3,493.1 |
| 89 | Vss | Vss | -0.025121 | 0.127672 | -638.1 | 3,242.9 |
| 90 | Vcc | Vcc | -0.025121 | 0.117581 | -638.1 | 2,986.6 |
| 91 | $\overline{CE2}$ | $\overline{CE2}$ | -0.025121 | 0.106646 | -638.1 | 2,708.8 |
| 92 | $\overline{WEL}$ | $\overline{BW1}$ | -0.025121 | 0.097928 | -638.1 | 2,487.4 |
| 93 | $\overline{WEH}$ | $\overline{BW2}$ | -0.025121 | 0.088428 | -638.1 | 2,246.1 |
| 94 | DNU | $\overline{BW3}$ | -0.025121 | 0.078148 | -638.1 | 1,985.0 |
| 95 | DNU | $\overline{BW4}$ | -0.025121 | 0.068649 | -638.1 | 1,743.7 |
| 96 | $\overline{CE2}$ | CE2 | -0.025121 | 0.059150 | -638.1 | 1,502.4 |
| 97 | $\overline{CE}$ | $\overline{CE}$ | -0.025121 | 0.050432 | -638.1 | 1,281.0 |
| 98 | A7 | A7 | -0.025121 | 0.040151 | -638.1 | 1,019.9 |
| 99 | A6 | A6 | -0.025121 | 0.030652 | -638.1 | 778.6 |
| 100 | DNU | DNU/DQP3[4] | -0.025121 | 0.007735 | -638.1 | 196.5 |

**NOTES:**
1. "DNU" stands for Do Not Use.
2. Reference to center of each bond pad from center of Bond Pad #1.
3. Refer to Table 1 for feature set bonding options.
4. The x36 has a parity pin and the x32 has a DNU pin at these pad locations.

## DIE OUTLINE (Top View)




| | |
|---|---|
| **Wafer thickness:** | 14.0 mil ±0.5 mil |
| **Die size:** | 271 x 303 mil<br>(stepping interval)<br>6,883 x 7,696 µm |
| **Bond pad size:** | 5.1 x 5.1 mil<br>129 x 129 µm |
| **Passivation Openings (typical):** | 4.5 x 4.5 mil<br>115 x 115 µm |