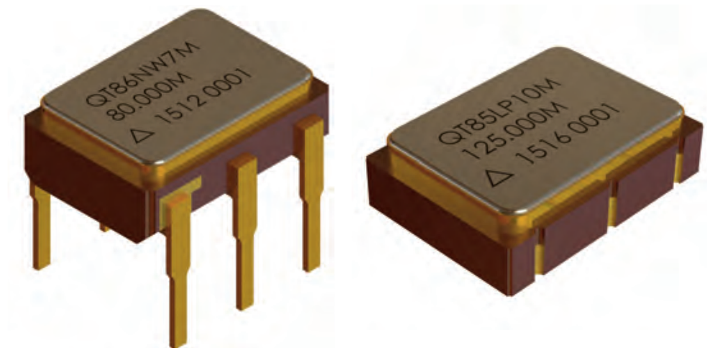
QT86LW & LP SERIES

5x7mm Extreme LVDS and LVPECL Crystal Oscillator
2.5V, 3.3Vdc | 60MHz to 200MHz

Description

Q-Tech's 5x7mm LVDS and LVPECL hybrid oscillators consist of an IC operating at various supply voltages of 2.5V and 3.3Vdc and a miniature strip quartz crystal. The series is offered in various ceramic package configurations from true Surface-Mount SMT to straight leads and formed leads. This is the smallest package offered with either a two-point crystal mount or a four-point for high shock and high reliability military applications.



Features

- Made in the USA
- ECCN: EAR99
- Innovative Four Point Mount Strip Crystal Resonator option
- Broad Frequency Range, 60MHz to 200MHz
- Small Footprint
- Differential LVDS or LVPECL output
- Various Supply Voltages, 2.5Vdc to 3.3Vdc
- Wide Operating Temperature Range, -55°C to 125°C
- Standard Tri-State Output
- Hermetically sealed package
- 3rd Overtone Designs
- Full or Partial Screening per MIL-PRF-55310, Level B
- High Shock Resistant Tested Up to 20,000g Mechanical Shock, Half-Sine, 0.3ms, All Axes with 4-point mount
- Low phase noise, low noise coupling, low emissions
- Optional Hot Solder Dip, Sn60Pb40 or SAC305
- RoHS Compliant

(Sample part number)

Q T 86 F LW 10 M - 80.000MHz

Q	T	86	F	LW	10	M	-	80.000MHz

Solder Dip Options
T = Standard
S = Sn60Pb40
G = SAC305

Package
86=Leaded
87=Formed Leads
80=Formed Leads
85=SMT

4-Point Mount	
F	= Four-point mount (High Shock)
Blank	= Standard two-point mount

Logic & Supply Voltage:
LW = LVDS +3.3Vdc
NW = LVDS +2.5Vdc
LP = LVPECL+3.3Vdc
NP = LVPECL+2.5Vdc

Frequency vs. Temperature Code
7 = ± 75ppm at -55ºC to +125°C
9 = ± 50ppm at -55ºC to +125°C
10 = ± 100ppm at -55ºC to +125°C
11 = ± 50ppm at -40ºC to +85°C
12 = ± 100ppm at -40ºC to +85°C
17 = ± 75ppm at -60ºC +125°C
18 = ± 100ppm at -60ºC to +125°C

Screening Option:	
Blank	= No Screening
M	= Screening per MIL-PRF-55310, Level B

Output Frequency

1/ Please contact Q-Tech for higher frequencies

Applications

- SONET/SDH
- Missile Launch
- Gun-Launched Munitions and Systems
- Clock generation and distribution
- Broadband access
- Ethernet, Gigabit Ethernet

Packaging Options

- Standard ESD packaging

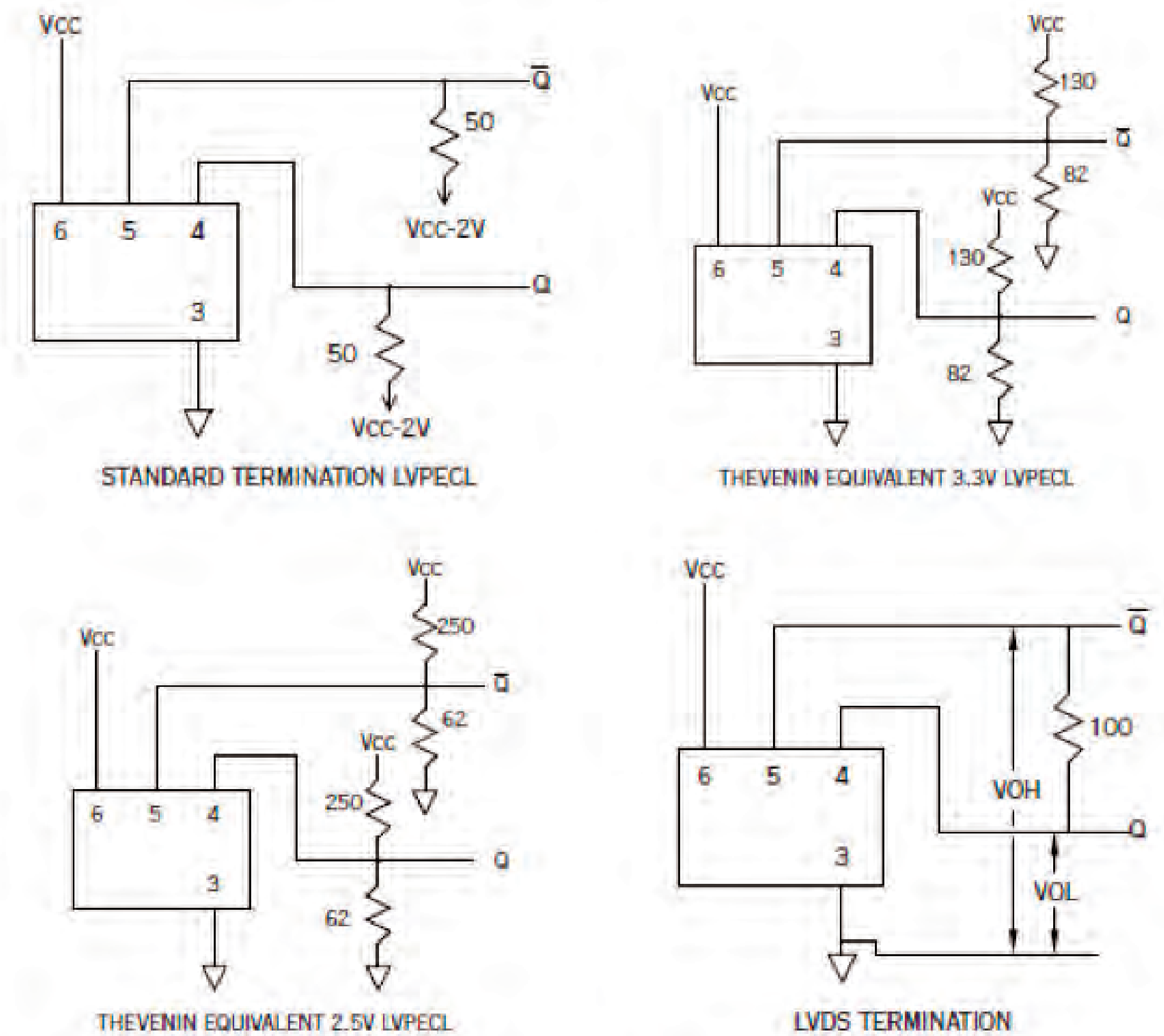
TABLE I - ELECTRICAL CHARACTERISTICS LVDS (+2.5VDC AND +3.3VDC)

PARAMETERS	LIMITS	COMMENTS
Output Frequency Range (Fo)	500kHz – 60MHz – 200MHz	Consult Factory for Lower and Higher Frequencies
Supply Voltage (Vdd)	+2.5Vdc ± 5% +3.3Vdc ± 5%	
Maximum Applied Voltage (Vdd max.)	+5Vdc	
Operating Temperature (Top)	See Ordering Information	
Storage temperature (Tsto)	-62°C to +125°C	
Supply current (Idd)	66mA max.	No Load
Load	100Ω	Note 1/
Duty Cycle (Sym)	45/55%	Measured at ½ waveform
Rise and Fall Times (Tr/Tf)	0.7ns max.	Measured Between 20% and 80% or 80% and 20% differential output swing
Start-Up Time (Tstup)	10ms Max.	
Output Voltage High (VOH)	1.43Vdc typ., 1.6Vdc max.	
Output Voltage Low (VOL)	0.9Vdc min., 1.1Vdc typ.	
Enable/Disable	VIH ≥ 0.7Vcc Oscillation VIL ≤ 0.3Vcc High Impedance	
Differential Output Voltage (VOD)	247mV min., 454mV max.	
Differential Output Error (ΔVOD)	50mV max.	
Offset Voltage (VOS)	1.125V min., 1.375V max.	
Output Current (IOH/IOL)	3.5mA typ.	
Aging at +70°C ± 3°C	±5ppm First Year Max. ±2ppm Max. Each Year Thereafter	
Period Jitter 1σ (RMS) Integrated Phase Jitter	5ps Typ. 1ps Max.	By Design; Not Tested 12kHz to 20MHz
Phase Noise (Typical)	10Hz Offset -65dBc/Hz 100Hz Offset -95dBc/Hz 1kHz Offset -130dBc/Hz 10kHz Offset -135dBc/Hz 100kHz Offset -140dBc/Hz 1MHz Offset -145dBc/Hz	Typical by Design Not Tested Unless Specified

TABLE II - ELECTRICAL CHARACTERISTICS LVPECL (+2.5VDC AND +3.3VDC)

PARAMETERS	LIMITS	COMMENTS
Output Frequency Range (Fo)	60MHz – 200MHz	Consult Factory for Lower and Higher Frequencies
Supply Voltage (Vdd)	+2.5Vdc ± 5% +3.3Vdc ± 5%	NP LP
Maximum Applied Voltage (Vdd max.)	+5Vdc	
Operating Temperature (Top)	See Ordering Information	
Storage temperature (Tsto)	-62°C to +125°C	
Supply current (Idd)	80mA max.	No Load
Load	50Ω to Vcc-2Vdc	Between each output and Vcc-2Vdc
Duty Cycle (Sym)	45/55%	Measured at ½ waveform
Rise and Fall Times (Tr/Tf)	1ns max.	Measured Between 20% and 80% or 80% and 20% differential output swing
Start-Up Time (Tstup)	10ms Max.	
Output Voltage High (VOH)	2.215 min., 2.420V max. 1.415V min., 1.76V max.	LP (+3.3Vdc) NP (+2.5Vdc)
Output Voltage Low (VOL)	1.47V min., 1.745V max. 0.67V min., 1.195V max.	LP (+3.3Vdc) NP (+2.5Vdc)
Enable/Disable	VIH ≥ 0.7Vcc Oscillation VIL ≤ 0.3Vcc High Impedance	
Offset Swing (VOpp)	0.4V min.	
Output Current (IOH/IOL)	22mA typ.	
Aging at +70°C ± 3°C	±5ppm First Year Max. ±2ppm Max. Each Year Thereafter	
Period Jitter 1σ (RMS) Integrated Phase Jitter	5ps Typ. 1ps Max.	By Design; Not Tested 12kHz to 20MHz
Phase Noise (Typical)	10Hz Offset -65dBc/Hz 100Hz Offset -95dBc/Hz 1kHz Offset -130dBc/Hz 10kHz Offset -135dBc/Hz 100kHz Offset -140dBc/Hz 1MHz Offset -145dBc/Hz	Typical by Design Not Tested Unless Specified

Test Circuit



The Tristate function on pin 1 has a built-in pull-up resistor so it can be left floating or tied to Vcc without deteriorating the electrical performance.

FIGURE 1 – CIRCUIT DIAGRAM

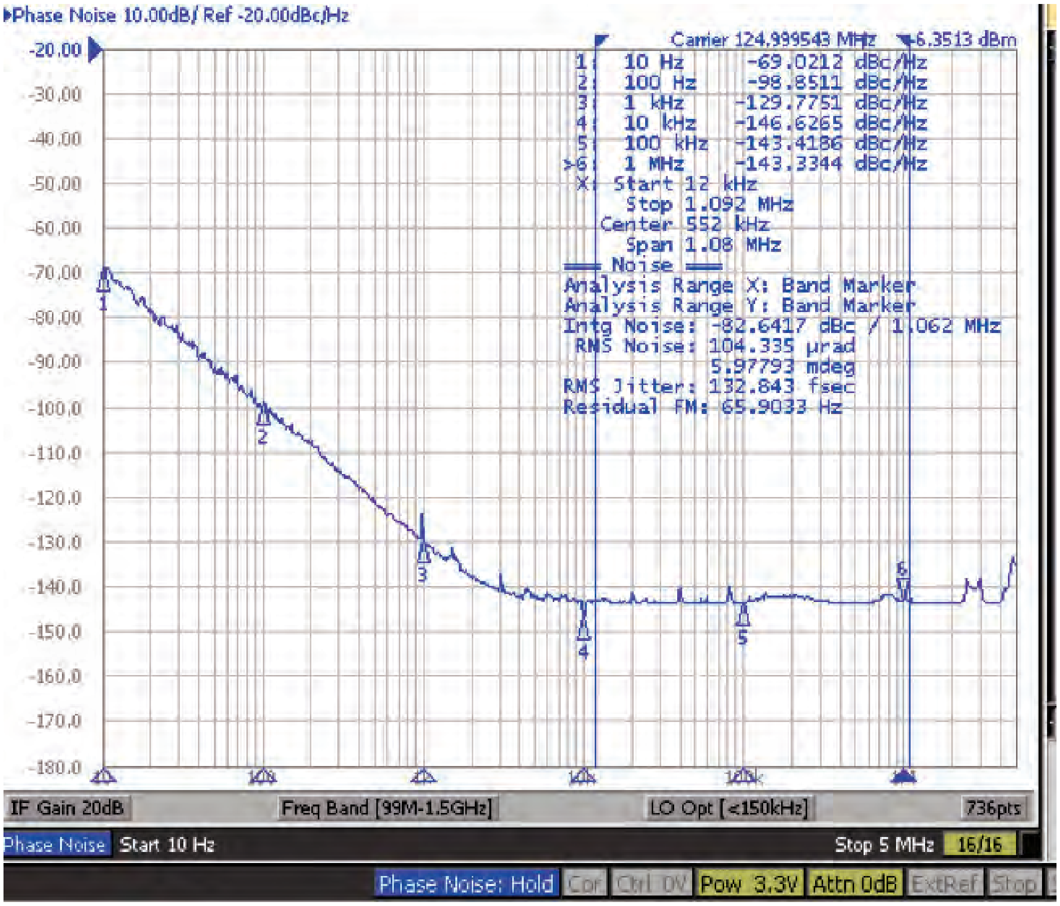


Figure 2 – TYPICAL PHASE NOISE OF A QT86LW-125MHz

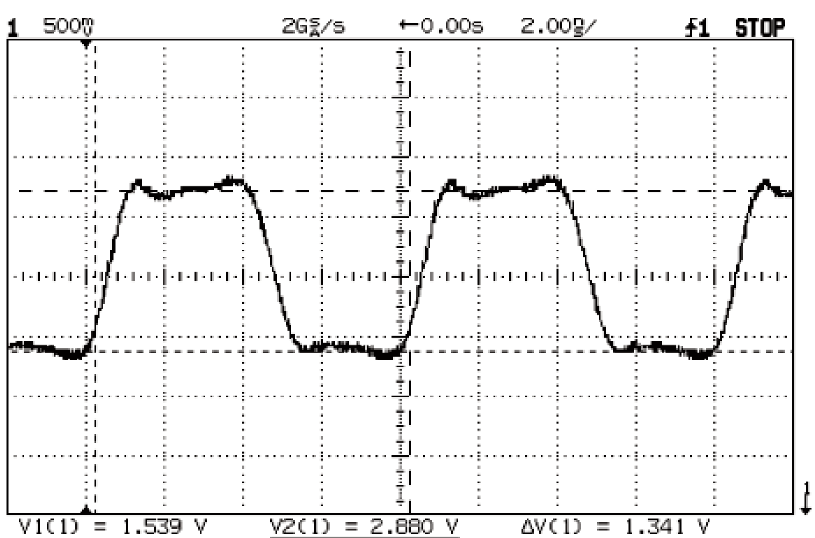


Figure 3 – TYPICAL WAVEFORM OF A QT86LP-125MHz

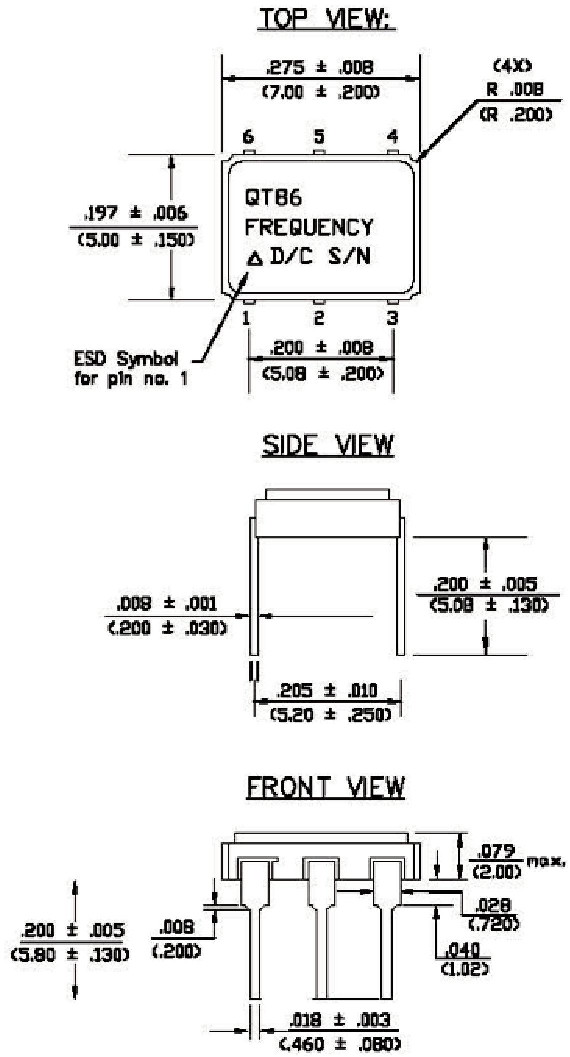


Figure 4 – QT86 DRAWING AND PIN OUTPUTS

QT86 (6 Leads)	
Pin No.	**Function**
1	ED
2	NC
3	GND/CASE
4	OUTPUT -
5	OUTPUT +
6	VDD

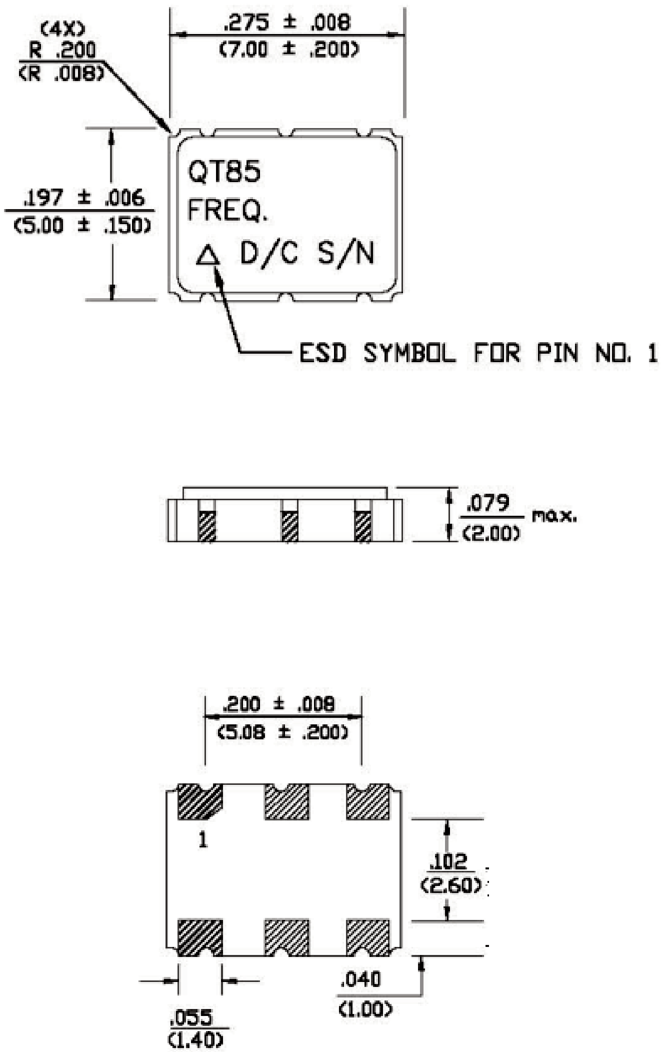


Figure 5 – QT85 DRAWING AND PIN OUTPUTS

QT85 (SMT 6 Pads)	
Pin No.	**Function**
1	ED
2	NC
3	GND/CASE
4	OUTPUT -
5	OUTPUT +
6	VDD

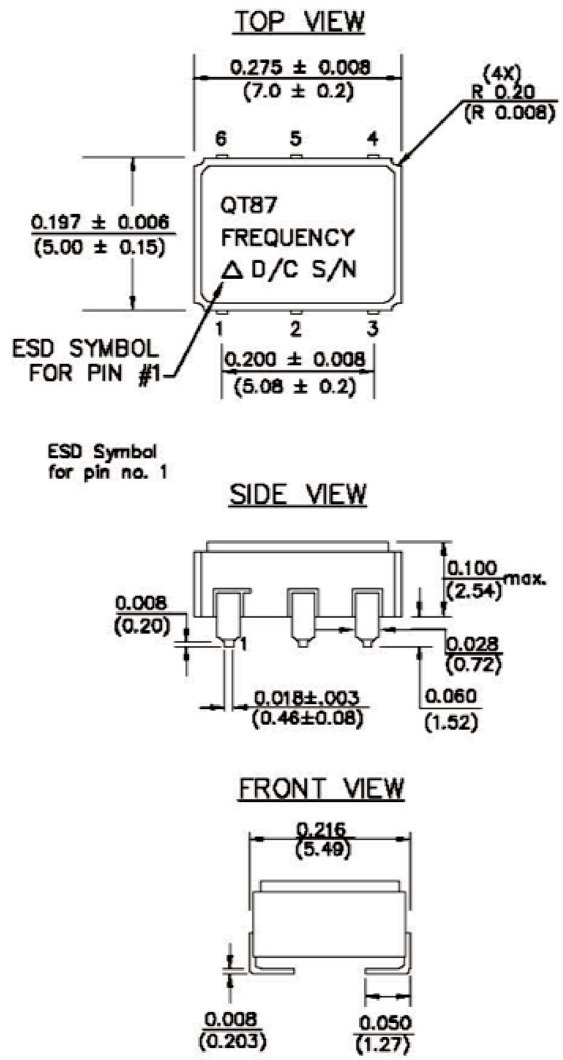


Figure 6 – QT87 DRAWING AND PIN OUTPUTS

QT87 (Lead Formed, 6 Leads)	
Pin No.	**Function**
1	ED
2	NC
3	GND/CASE
4	OUTPUT -
5	OUTPUT +
6	VDD

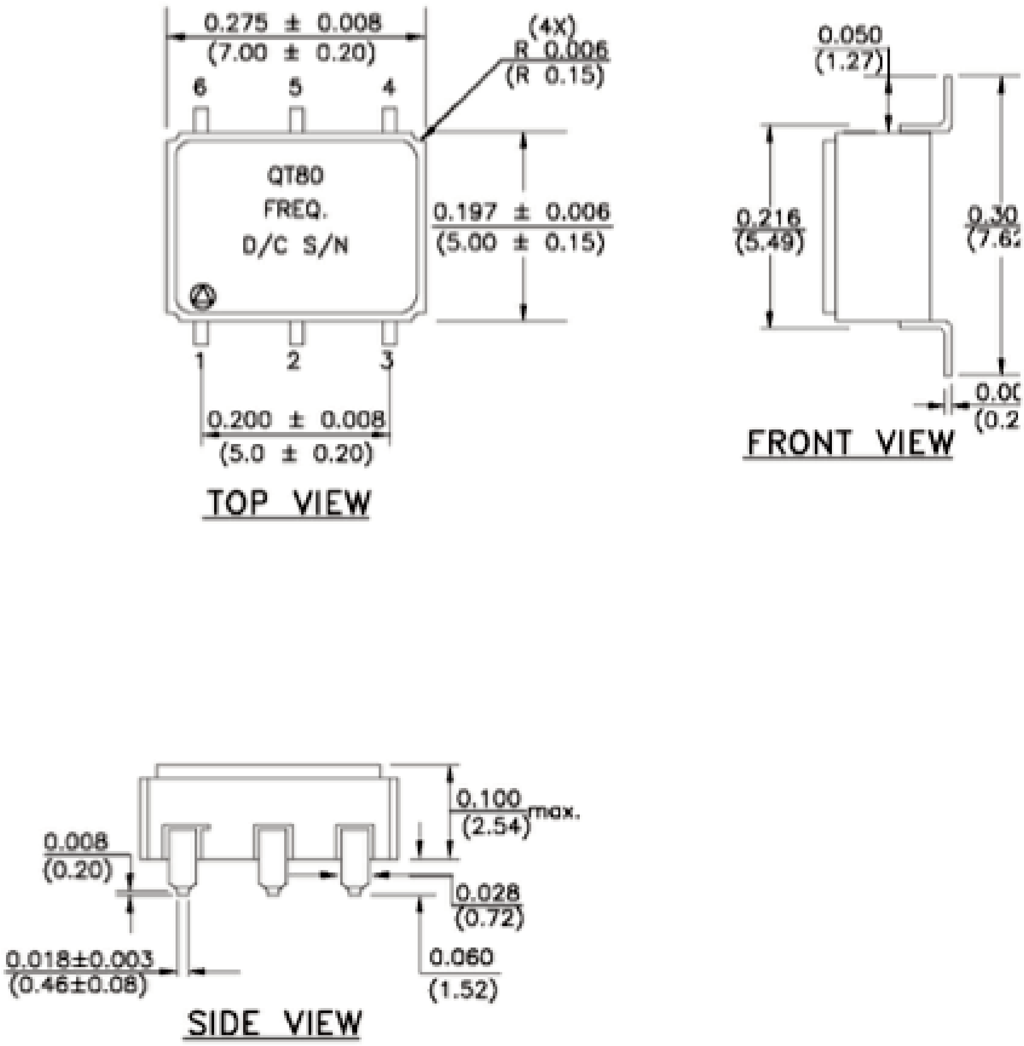


Figure 7 – QT80 DRAWING AND PIN OUTPUTS

QT80 (Lead Formed, 6 Leads)	
Pin No.	**Function**
1	NC or ED
2	NC
3	GND/CASE
4	OUTPUT -
5	OUTPUT +
6	VDD

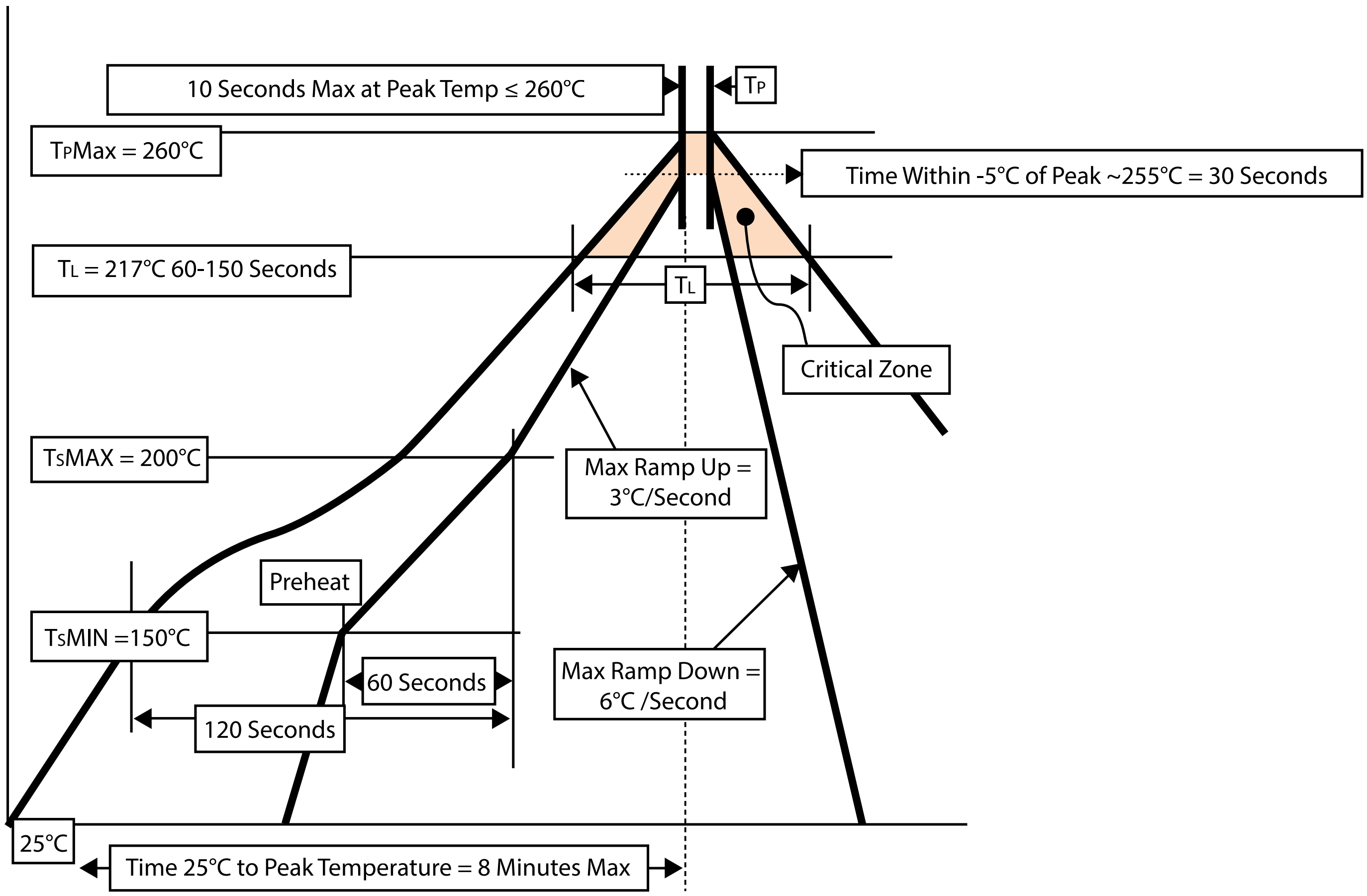


Figure 8 – Solder Reflow Profile Reflow Profile per IPC/JEDEC J-STD-020D.1, 240°C Reflow Profile Also Acceptable

ENVIRONMENTAL AND MECHANICAL TEST SPECIFICATIONS

TEST	SPECIFICATION
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Solderability	MIL-STD-883, Method 2003
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition B
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Mechanical Vibration	MIL-STD-883, Method 2007, Condition A
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A1
Solvent Resistance	MIL-STD-202, Method 215
Moisture Sensitivity Level	MSL = 1
Contact Pads	Gold (Au 60µin) Over Nickel (Ni 100-250µin) or Solder Dip Sn60Pb40/SAC305 Lead Free
ESD	Proper ESD Precautions Should be Taken When Handling and Mounting Crystal Oscillators. Built in ESD Protection Circuitry Ratings are as Follows: HBM Class 1C 1,999V per MIL-STD-883, Method 3015.7

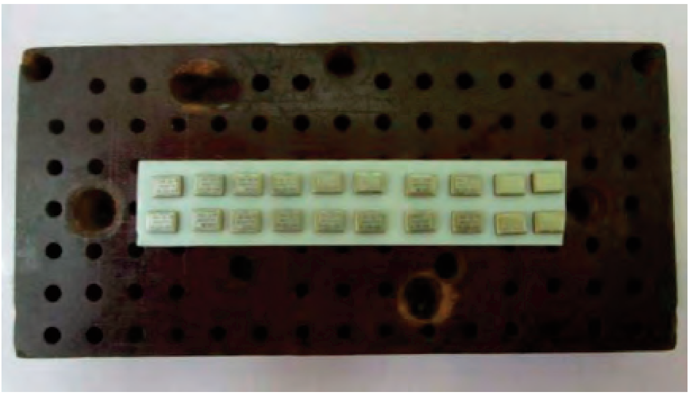


Figure 9 – UNITS TO BE TESTED

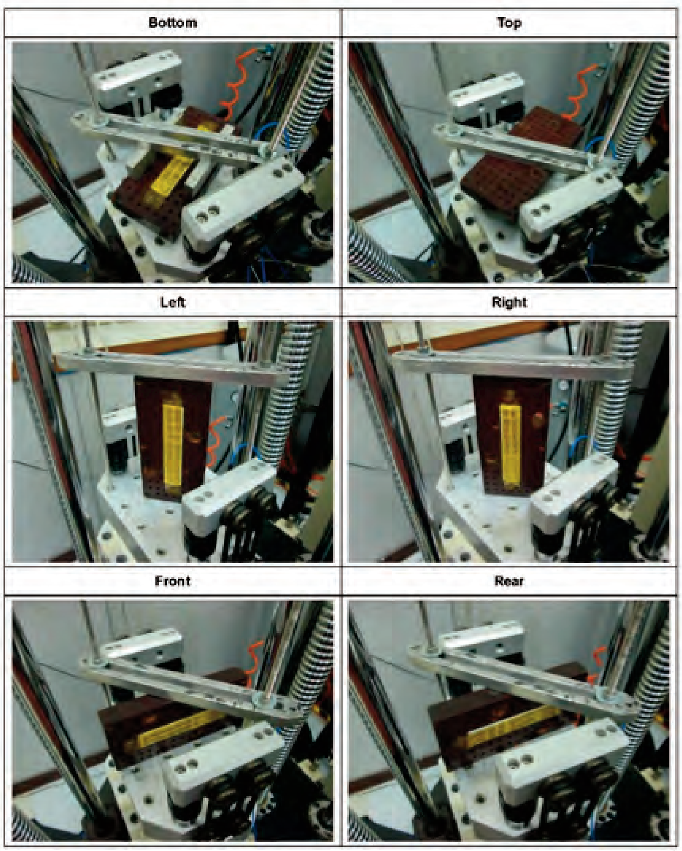


Figure 10 – MECHANICAL SHOCK TEST SET UP

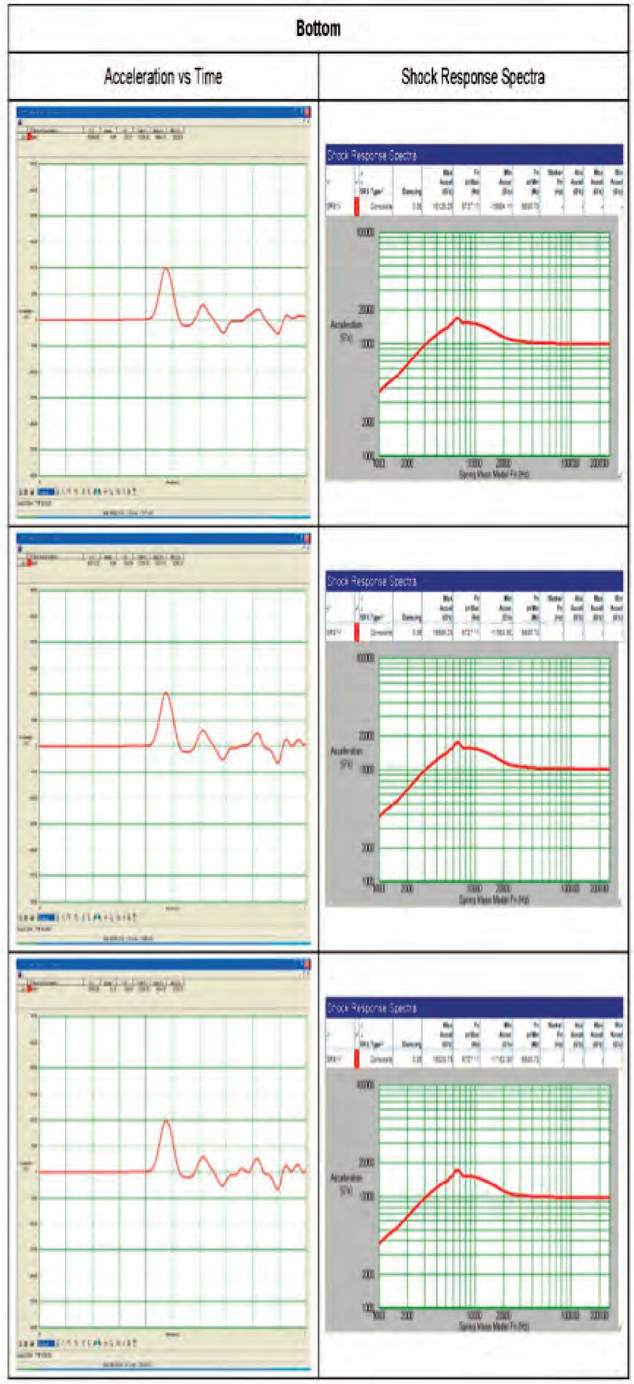


Figure 11 – GRAPH OF MECHANICAL SHOCK TEST