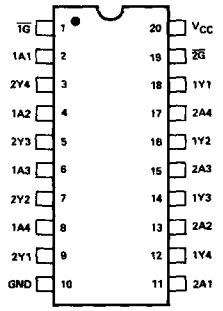
AmZ8165 • AmZ8166

Octal Dynamic Memory Drivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- **Controlled rise and fall characteristics**
  Internal resistors provide symmetrical drive to HIGH and LOW states, eliminating need for external series resistor.
- **Output swings designed to drive 16K and 64K RAMs**
  V_{OH} guaranteed at V_{CC} – 1.15V. Undershoot going LOW guaranteed at less than 0.5V.
- **Large capacitive drive capability**
  35mA min source or sink current at 2.0V. Propagation delays specified for 50pF and 500pF loads.
- **Pin-compatible with 'S240 and 'S244**
  Non-inverting AmZ8166 replaces 74S244; inverting AmZ8165 replaces 74S240. Faster than 'S240/244 under equivalent load.
- **No-glitch outputs**
  Outputs forced into OFF state during power up and down.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-210

FUNCTIONAL DESCRIPTION

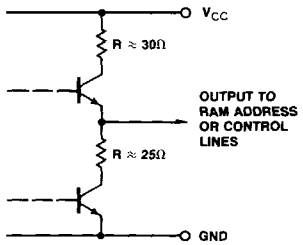
The AmZ8165 and AmZ8166 are designed and specified to drive the capacitive input characteristics of the address and control lines of MOS dynamic RAMs. The unique design of the lower output driver includes a collector resistor to control undershoot on the HIGH-to-LOW transition. The upper output driver pulls up to V_{CC} – 1.15V to be compatible with MOS memory and is designed to have a rise time symmetrical with the lower output's controlled fall time. This allows optimization of Dynamic RAM performance.

The AmZ8165 and AmZ8166 are pin-compatible with the popular 'S240 and 'S244 with identical 3-state output enable controls. The AmZ8165 has inverting drivers and the AmZ8166 has non-inverting drivers.

The inclusion of an internal resistor in the lower output driver eliminates the requirement for an external series resistor, therefore reducing package count and the board area required. The internal resistor controls the output fall and undershoot without slowing the output rise.

These devices are designed for use with the AmZ8164 Dynamic Memory Controller where large dynamic memories with highly capacitive input lines require additional buffering. Driving eight address lines or four $\overline{RAS}$ and four $\overline{CAS}$ lines with drivers on the same silicon chip also provides a significant performance advantage by minimizing skew between drivers. Each device has specified skew between drivers to improve the memory access worst case timing over the min and max t_{PD} difference of unspecified devices.

TYPICAL OUTPUT DRIVER

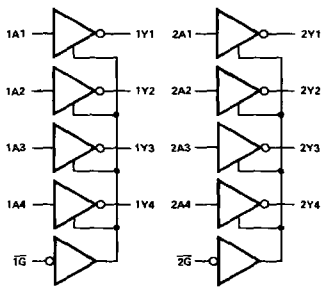


BLI-211

LOGIC DIAGRAMS

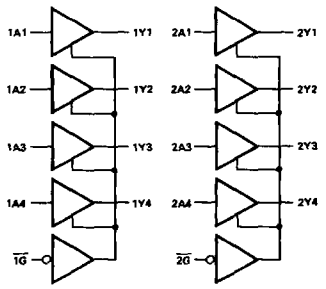
BLI-212

AmZ8165



Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

AmZ8166



Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

BLI-213

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +7.0V
DC Output Current, into Outputs	30mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)
MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1mA	V_{CC}−1.15	V_{CC}−0.7V		Volts
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.5	Volts
				I_{OL} = 12mA			0.8	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.4V				−200	μA
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZH}	Off-State Current		V_O = 2.7V				100	μA
I_{OZL}	Off-State Current		V_O = 0.4V				−200	μA
I_{OL}	Output Sink Current		V_{OL} = 2.0V		35			mA
I_{OH}	Output Source Current		V_{OH} = 2.0V		−35			mA
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−60 (see I_{OH})		−200	mA
I_{CC}	Supply Current	AmZ8165	All Outputs HIGH	V_{CC} = MAX Outputs Open		24	50	mA
			All Outputs LOW			86	125	
			All Outputs Hi-Z			86	125	
		AmZ8166	All Outputs HIGH	V_{CC} = MAX Outputs Open		53	75	
			All Outputs LOW			92	130	
			All Outputs Hi-Z			116	150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

8

AmZ8165 • AmZ8166
SWITCHING CHARACTERISTICS
(T_A = +25°C, VCC = 5.0V)

Parameters	Description	Test Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Output	Figure 1 Test Circuit Figure 3 Voltage Levels and Waveforms	C_L = 0pF		6	(Note 4)	ns
			C_L = 50pF	6	9	15	
			C_L = 500pF	15	22	35	
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Output		C_L = 0pF		4	(Note 4)	ns
			C_L = 50pF	6	12	20	
			C_L = 500pF	20	30	45	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4, S = 1			13	20	ns
t_{PHZ}		Figures 2 and 4, S = 2			8	12	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4, S = 1			13	20	ns
t_{PZH}		Figures 2 and 4, S = 2			13	20	
t_{SKEW}	Output-to-Output Skew	Figures 1 and 3, C_L = 50pF			±0.5	±3.0 (Note 5)	ns
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			0	−0.5	Volts

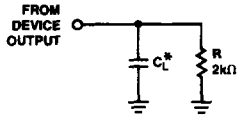
SWITCHING CHARACTERISTICS
OVER OPERATING RANGE (Note 6)

Parameters	Description	Test Conditions		COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±10% Min	COM'L Max	MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% Min	MIL Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	Figures 1 and 3	C_L = 50pF	4	20	4	20	ns
			C_L = 500pF	13	40	13	40	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output	Figures 1 and 3	C_L = 50pF	4	24	4	24	ns
			C_L = 500pF	17	50	17	50	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4	S = 1		24		24	ns
t_{PHZ}			S = 2		16		16	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4	S = 1		28		28	ns
t_{PZH}			S = 2		28		28	
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			−0.5		−0.5	Volts

Notes: 4. Typical time shown for reference only – not tested.
5. Time Skew specification is guaranteed by design but not tested.
6. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING TEST CIRCUITS

BLI-214



*t_{pd} specified at C = 50 and 500pF.

Figure 1. Capacitive Load Switching.

BLI-215

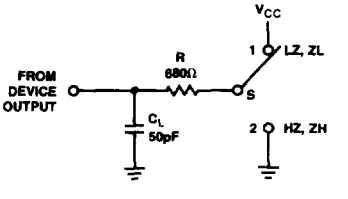
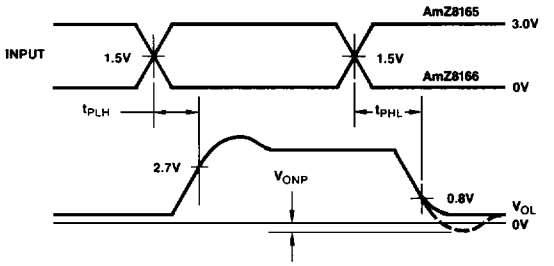


Figure 2. Three-State Enable/Disable.

TYPICAL SWITCHING CHARACTERISTICS

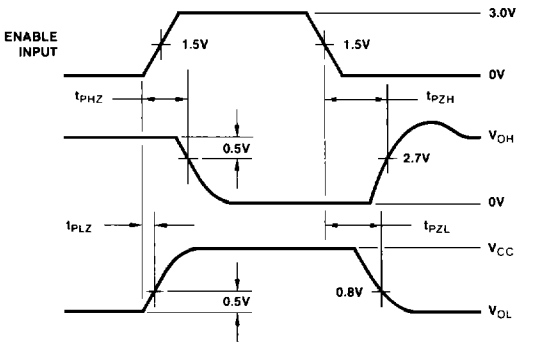
VOLTAGE WAVEFORMS



$t_r = t_f = 2.5ns$
$f = 2.5MHz$
$t_{pw} = 200ns$

BLI-217

Figure 3. Output Drive Levels.



$t_r = t_f = 2.5ns$
$f = 1MHz$
$t_{pw} = 800ns$

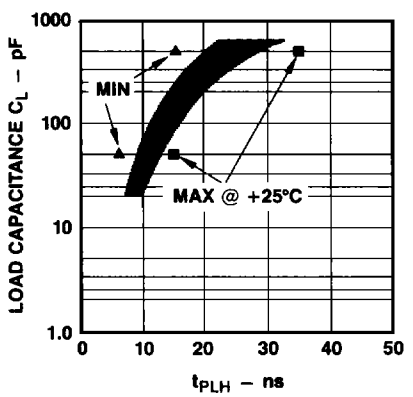
BLI-218

Figure 4. Three-State Control Levels.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈33Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels (V_{CC} – 1.15V). External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.

The curves shown below provide performance characteristics typical of both the inverting (AmZ8165) and non-inverting (AmZ8166) RAM Drivers.



BLI-219

Figure 5. t_{PLH} vs. C_L.

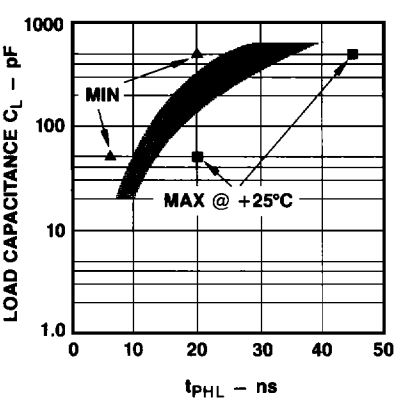


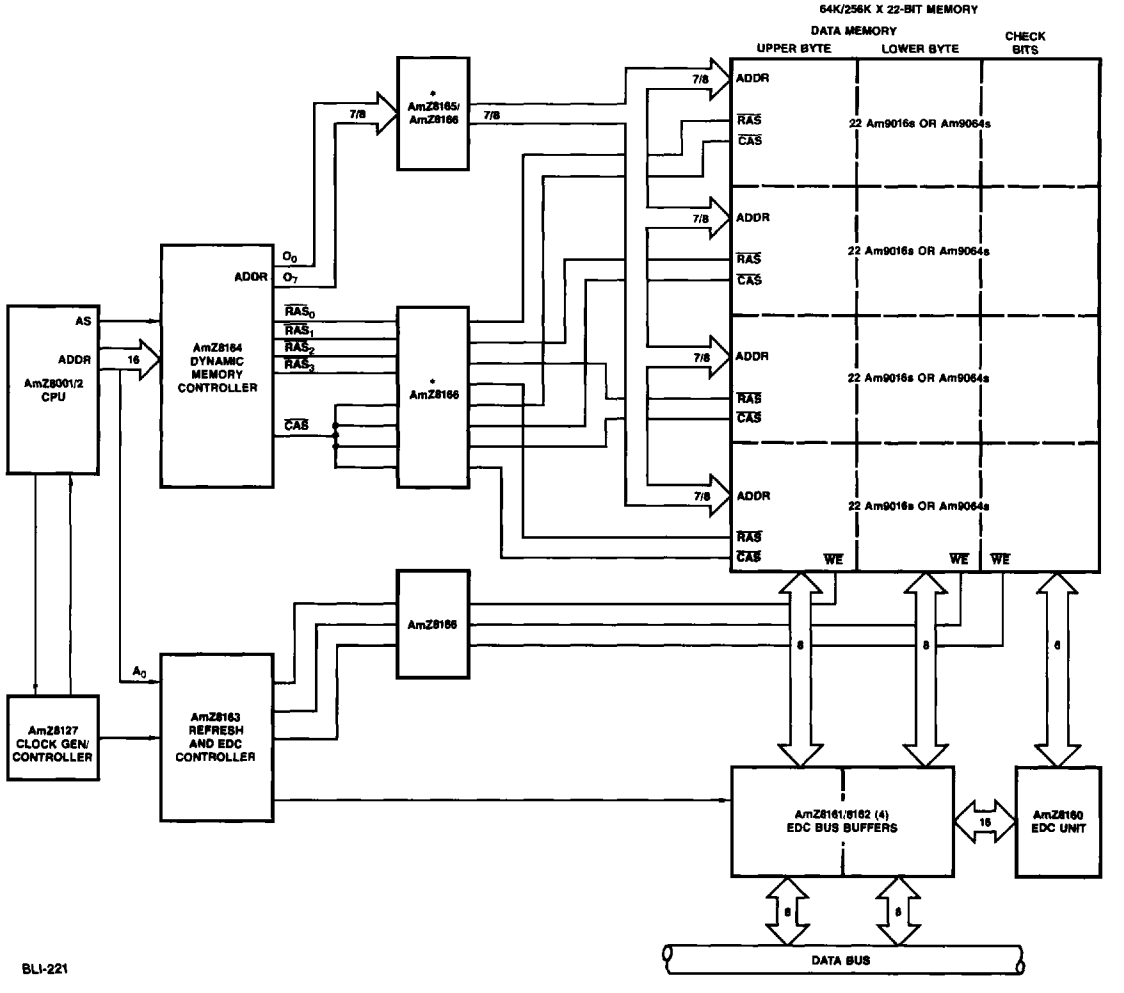
Figure 6. t_{PHL} vs. C_L.

BLI-220

The curves above depict the typical t_{PLH} and t_{PHL} for the RAM Driver outputs as a function of load capacitance. The minimums and maximums are shown for worst case design. The typical band is provided as a guide for intermediate capacitive loads.

8

APPLICATION

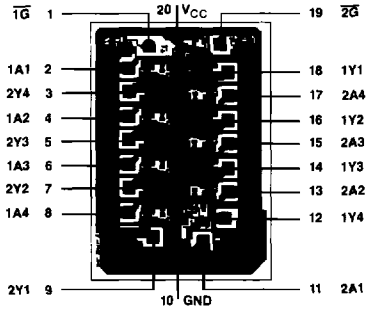


*Address and $\overline{RAS}$/$\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}$/$\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

DYNAMIC MEMORY CONTROL WITH ERROR DETECTION AND CORRECTION

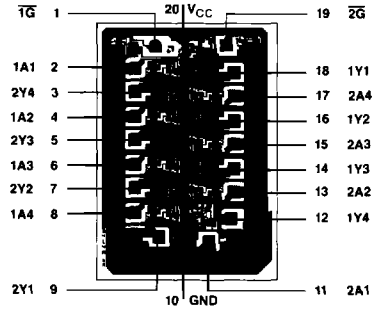
Metallization and Pad Layouts

AmZ8165



DIE SIZE 0.094" X 0.060"

AmZ8166



DIE SIZE 0.094" X 0.060"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

AmZ8165 Order Number	AmZ8166 Order Number	Package Type	Temperature Range	Screening Level
AMZ8165PC	AMZ8166PC	P-20	C	C-1
AMZ8165DC	AmZ8166DC	D-20	C	C-1
AMZ8165DM	AMZ8166DM	D-20	M	C-3
AMZ8165XC	AMZ8166XC	Dice	C	Visual Inspection to MIL-STD-883 Method 2010B.
AMZ8165XM	AMZ8166XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP. Number following letter is number of leads.
2. C = 0 to 70°C, V_{CC} = 4.50 to 5.50V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

8