High-Speed CMOS 64Kx4 SRAM with Separate I/O

QS8821
QS8822
ADVANCE INFORMATION

FEATURES/BENEFITS

- High Speed Access and Cycle times
- 15ns/20ns/25ns Commercial
- 20ns/25ns/35ns Military
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 6-Transistor cell for high reliability
- Ideal for reliable,dense memory systems
- Available in 28-pin DIPs, 28-pin 300 mil SOJ & SOIC
- Low Standby current
- JEDEC standard pinout

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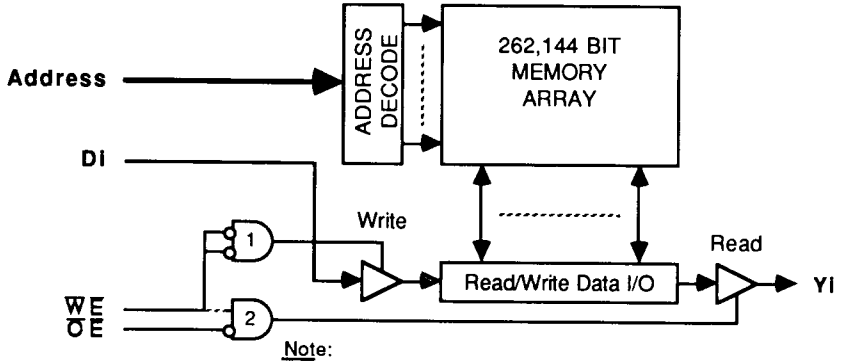
DESCRIPTION

The QS8821 and QS8822 are high-speed 256K SRAMs organized as 64Kx4 with separate read and write data buses. In the 8821, the read data outputs follow the inputs during a write; in the 8822, the outputs are disabled during a write. The 8821 and 8822 are manufactured in a high-performance CMOS process, and they are based on a 6-transistor cell design for high reliability of data retention. Their high-speed access times make them useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



Note:
WE is not connected to Output Enable Gate 2 in the 8821.
WE is connected to Output Enable Gate 2 as shown in the 8822.

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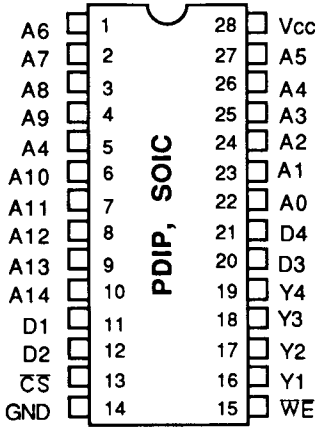
PIN CONFIGURATIONS



ALL PINS TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
D	I	Write Data In
Y	O	Read Data Out
$\overline{CS}$	I	Chip Select
$\overline{WE}$	I	Write Enable
$\overline{OE}$	I	Output Enable

FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Y Outputs		Power	Function
			8821	8822		
H	X	X	High Z	High Z	Standby	Deselect
L	H	X	High Z	High Z	Active	Deselect
L	L	H	Data Out	Data Out	Active	Read
L	L	L	Data In	High Z	Active	Write