Data Sheet
February 1997

microelectronics group

Lucent Technologies
Bell Labs Innovations

T7295-1 E3 Integrated Line Receiver

Features

- Fully integrated receive interface for E3 signals
- Integrated equalization (optional) and timing recovery
- Loss-of-signal and loss-of-lock alarms
- Variable input sensitivity control
- Single 5 V power supply

Applications

- Interface to E3 networks
- CSU/DSU equipment
- PCM test equipment
- Fiber-optic terminals
- Companion device to T7296 transmitter

Description

The T7295-1 E3 Integrated Line Receiver is a fully integrated receive interface that terminates a bipolar E3 (34.368 Mbits/s) signal transmitted over coaxial cable. This device can be used with the T7296 Integrated Line Transmitter.

The device provides the functions of receive equalization (optional), automatic-gain control (AGC), clock recovery and data retiming, and loss-of-signal and loss-of-frequency-lock detection. The digital system interface is dual rail, with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable losses up to 15 dB. The receive input has a variable input sensitivity control, providing three different sensitivity settings. High input sensitivity allows for significant amounts of flat loss within the system. Figure 1 shows the block diagram of the device.

The T7295-1 device is manufactured by using linear CMOS technology and is packaged in a 20-pin, plastic DIP or 20-pin, plastic SOJ package for surface mounting. Figure 2 shows the pin layout for both package types.

Description (continued)

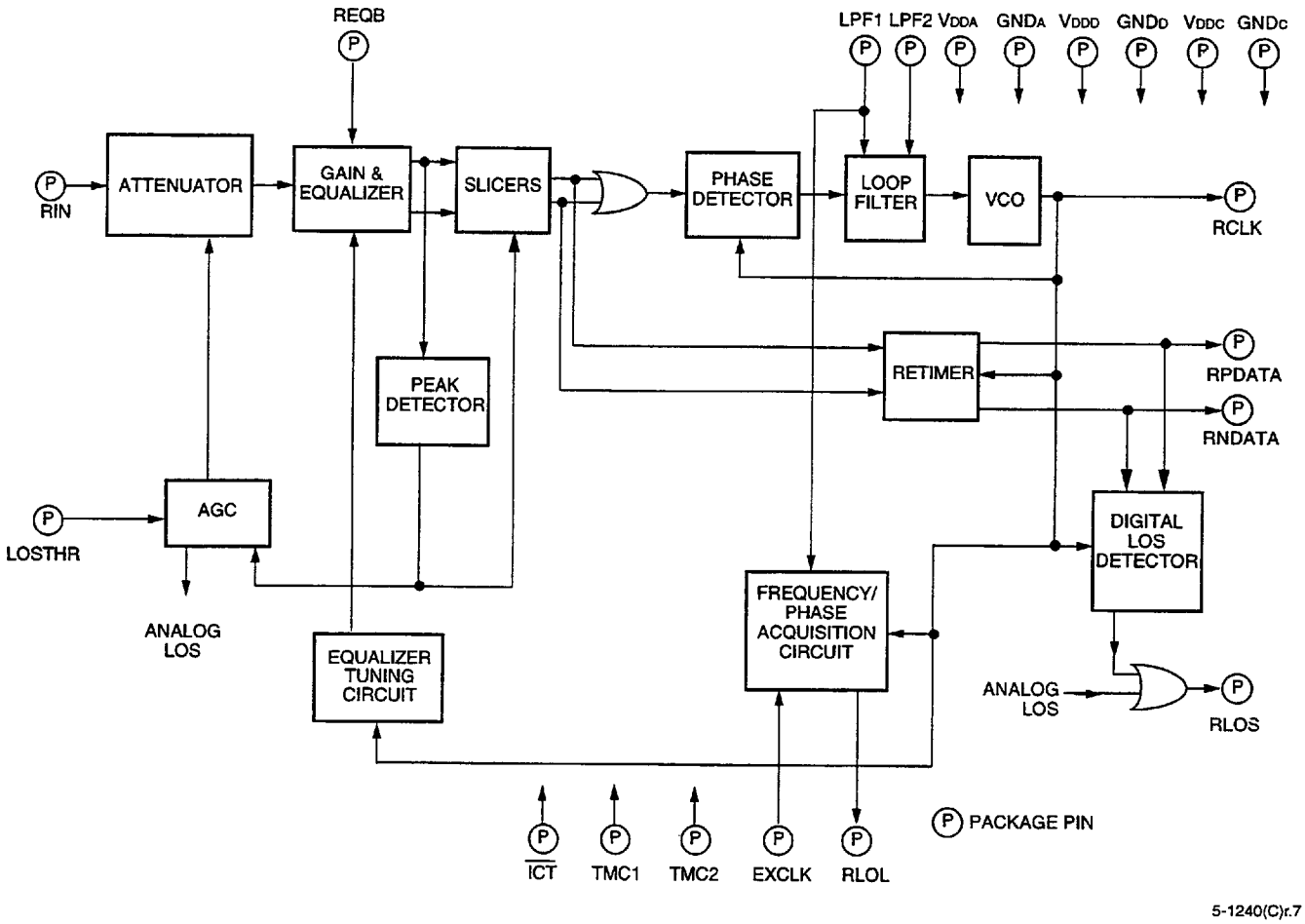

Figure 1. Block Diagram

Pin Information

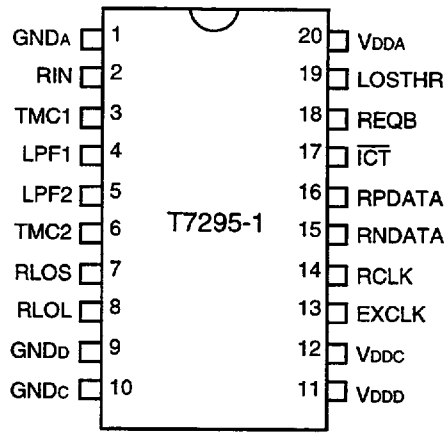

Figure 2. Pin Assignment

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Description
1	GNDA	—	**Analog Ground.**
2	RIN	I	**Receive Input.** Single-ended analog receive input. This pin is internally biased at approximately 1.5 V in series with 50 kΩ.
3, 6	TMC1, TMC2	I	**Test Mode Control 1 and 2.** Internal test modes are enabled within the device using TMC1 and TMC2. Users must tie these pins to the ground plane.
4, 5	LPF1, LPF2	I	**PLL Filter 1 and 2.** An external capacitor (0.1 µF ± 20%) is connected between these pins. The capacitor should be mounted as close to the pins as possible (within 1.2 cm is recommended).
7	RLOS	O	**Receive Loss of Signal.** This pin is set high on loss of the data signal at the receive input.
8	RLOL	O	**Receive PLL Loss of Lock.** This pin is set high on loss of PLL frequency lock.
9	GNDD	—	**Digital Ground for PLL Clock.** Ground lead for all circuitry running synchronously with PLL clock.
10	GNDC	—	**Digital Ground for EXCLK.** Ground lead for all circuitry running synchronously with EXCLK.
11	VDDD	—	**5 V Digital Supply (±10%) for PLL Clock.** Power for all circuitry running synchronously with PLL clock.
12	VDDC	—	**5 V Digital Supply (±10%) for EXCLK.** Power for all circuitry running synchronously with EXCLK.
13	EXCLK	I	**External Reference Clock.** A valid E3 (34.368 MHz ± 100 ppm) or clock must be provided at this input. EXCLK must be an independent clock to guarantee device performance for all specifications. The duty cycle of EXCLK, referenced to VDD/2 levels, must be 40% to 60% with a maximum rise and fall time (10% to 90%) of 5 ns.
14	RCLK	O	**Receive Clock.** Recovered clock signal to the terminal equipment.
15	RNDATA	O	**Receive Negative Data.** Negative pulse data output to the terminal equipment.
16	RPDATA	O	**Receive Positive Data.** Positive pulse data output to the terminal equipment.
17	$\overline{\text{ICT}}$	I	**In-Circuit Test Control (Active-Low).** If $\overline{\text{ICT}}$ is forced low, all digital output pins (RCLK, RPDATA, RNDATA, RLOS, RLOL) are placed in a high-impedance state to allow for in-circuit testing. A nominal 50 kΩ pull-up is provided on this pin.
18	REQB	I	**Receive Equalization Bypass.** A high on this pin bypasses the internal equalizer. A low places the equalizer in the data path.
19	LOSTHR	I	**Loss-of-Signal Threshold Control.** The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing GND, VDD/2, or VDD. This pin must be set to the desired level upon powerup and should not be changed during operation.
20	VDDA	—	**5 V Analog Supply (±10%).**

Overview

Receive Path Configuration

The diagram in Figure 3 shows a typical system application for the T7295-1 device. In the receive signal path (see Figure 1), the internal equalizer can be included by setting REQB = 0 or bypassed by setting REQB = 1. The equalizer bypass option allows easy interfacing of the T7295-1 device into systems already containing external equalizers. Figure 4 illustrates the receive path options for two separate cases.

In case 1, the signal from the coaxial cable feeds directly into the RIN input. In this mode, the user should set REQB = 0, engaging the equalizer in the data path if the cable loss is greater than 6 dB. If the cable loss is less than 6 dB, the equalizer is bypassed by setting REQB = 1.

In case 2, an external line and equalizer network precedes the T7295-1 device. In this mode, the signal at RIN is already equalized, and the on-chip equalizer should be bypassed by setting REQB = 1. In both case 1 and case 2, the signal at RIN must meet the amplitude limits described in Table 2.

The recommended receive termination is shown in Figure 4. The 75 Ω resistor terminates the coaxial cable with its characteristic impedance. In Figure 4, case 2, if the fixed equalizer includes the line termination, the 75 Ω resistor is not required. The signal is ac-coupled through the 0.01 µF capacitor to RIN. The dc bias at RIN is generated internally. The input capacitance at the RIN pin is typically 2.8 pF (SOJ package) and 3.6 pF (DIP package).

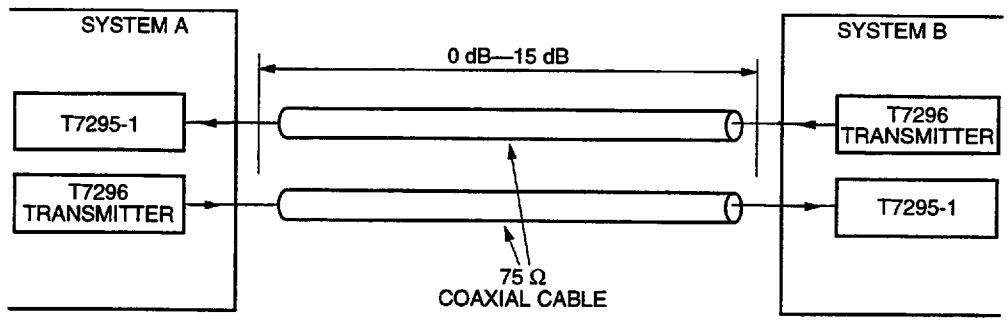

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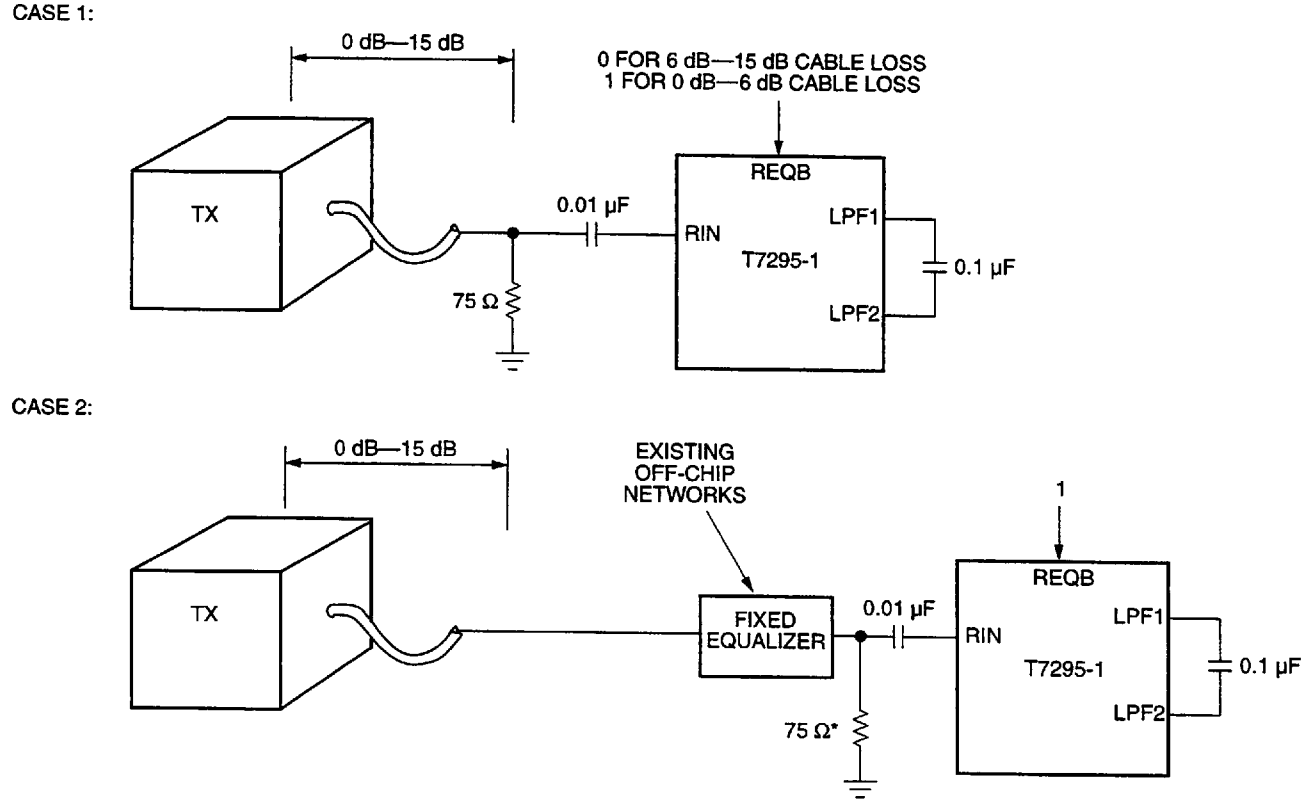
Figure 3. Application Diagram

Overview (continued)

External Loop Filter Capacitor

Figure 4 shows the connection to an external 0.1 µF ± 20% capacitor at the LPF1/LPF2 pins. This capacitor is part of the PLL filter. A nonpolarized, low-leakage capacitor should be used.



* Optional, see Receive Path Configuration section.

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Figure 4. Receiver Configurations

Table 2. Receive Input Signal Amplitude Requirements

Maximum input amplitude under all conditions is 1.1 V pk.

REQB	LOSTHR	Minimum Signal		Unit†
		SOJ*	DIP	
0	0	80	115	mV pk
	$V_{DD}/2$	60	85	mV pk
	V_{DD}	40	60	mV pk
1	0	80	115	mV pk
	$V_{DD}/2$	80	115	mV pk
	V_{DD}	80	115	mV pk

* The SOJ device performance is enhanced by decreased package parasitics.
† Although system designers typically use power in dBm to describe input levels, the T7295-1 responds to peak input signal amplitude. Therefore, the T7295-1 input signal limits are given in mV pk.

Overview (continued)

E3 Signal Requirements

The T7295-1 E3 is designed to recover pulses that conform to ITU-T recommendation G.703. Figure 5 shows the E3 pulse mask requirement recommended in G.703, and Table 3 shows the pulse specifications.

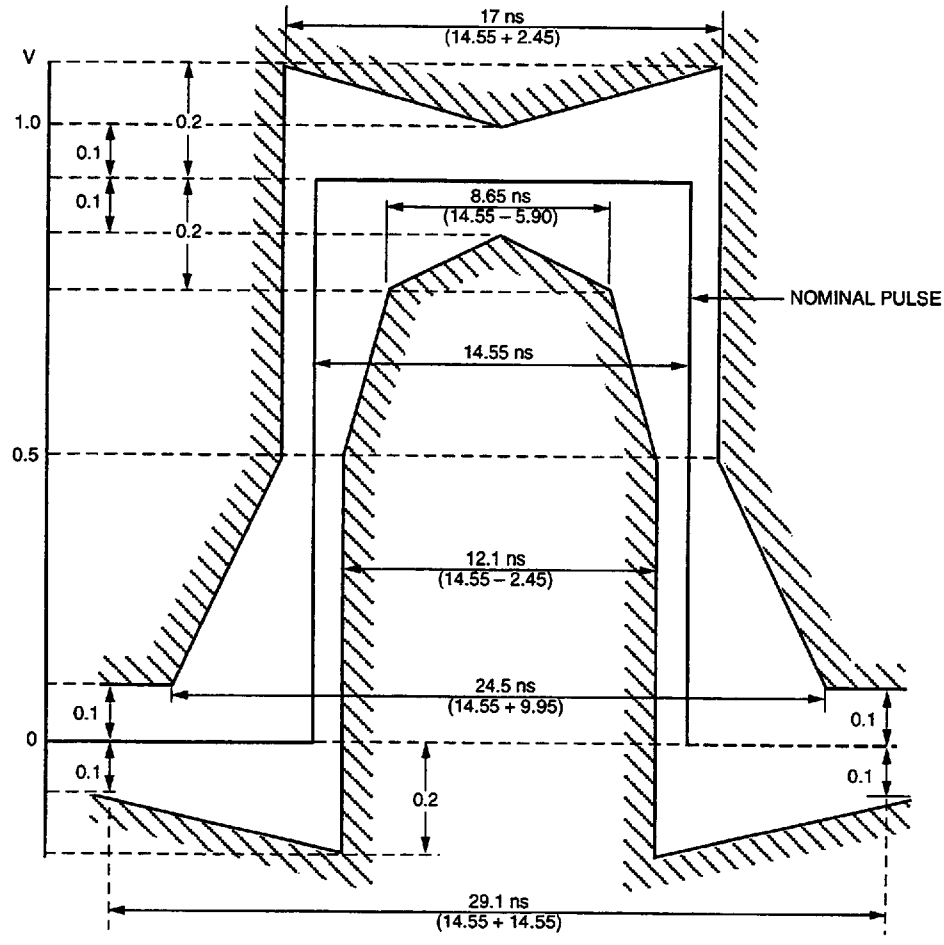

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Figure 5. Isolated E3 Pulse Template

Table 3. E3 Pulse Specification

Parameter	Value
Pulse Shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 5), regardless of the sign.
Test Load Impedance	75 Ω resistive.
Nominal Peak Voltage of a Mark (pulse)	1.0 V.
Peak Voltage of a Space (no pulse)	0 V ± 0.1 V.
Nominal Pulse Width	14.55 ns.
Ratio of the Amplitudes of Positive and Negative Pulses at the Center of a Pulse Interval	0.95 to 1.05.
Ratio of the Widths of Positive and Negative Pulses at the Nominal Half Amplitude	0.95 to 1.05.

Timing Recovery

Output Jitter

The total jitter appearing on the RCLK output during normal operation consists of two components. First, some jitter appears on RCLK because of jitter on the incoming signal. (The next section discusses the jitter transfer characteristic, which describes the relationship between input and output jitter.) Second, noise sources, both within the T7295-1 device and those that are coupled into the device through the power supplies, create jitter on RCLK. The magnitude of this internally generated jitter is a function of the PLL bandwidth, which, in turn, is a function of the input 1s density. For higher 1s densities, the amount of generated jitter decreases. Generated jitter also depends on the quality of the power supply bypassing networks used. Table 4 lists the typical generated jitter performance achievable with the suggested bypassing network shown in Figure 8.

Jitter Transfer Characteristic

The jitter transfer characteristic indicates the fraction of input jitter that reaches the RCLK output as a function of input jitter frequency. Table 4 shows important jitter transfer characteristic parameters.

Table 4. Generated Jitter and Jitter Transfer Characteristics

Parameter	Typ	Max	Unit
Generated Jitter:*			
All-1s Pattern	1.0	—	ns pk-to-pk
Repetitive 1000 Pattern	1.5	—	ns pk-to-pk
Jitter Transfer Characteristic:†			
Peaking	0.05	0.1	dB
f3dB	115	—	kHz

* Nominal E3 levels with V_{DD} = 5 V, T_A = 25 °C.
† Repetitive 1000 input pattern at nominal E3 levels with V_{DD} = 5 V, T_A = 25 °C.

Jitter Accommodation

Under all allowable operating conditions, the jitter accommodation of the T7295-1 device exceeds the system requirements for error-free operation (BER < $1e^{-9}$). The typical (V_{DD} = 5.0 V, T_A = 25 °C, E3 nominal signal level) jitter accommodation of the T7295-1 is also shown in Figure 6.

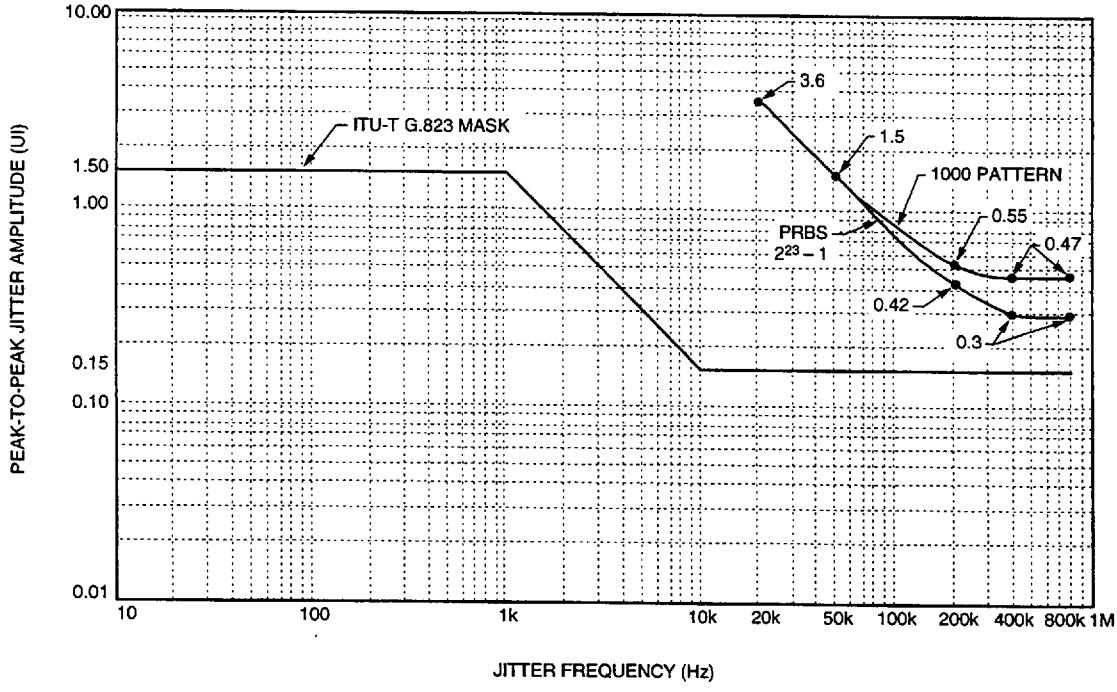

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Figure 6. Typical Jitter Accommodation of the T7295-1 E3 Device

Timing Recovery (continued)

Acquisition Time

If a valid input signal is already present at the RIN input, the maximum time between the application of device power at 4.5 V and error-free operation is 20 ms. If power has already been applied, the interval between the application of valid data and error-free operation is 4 ms.

False Lock Immunity

False lock is defined as the condition where a PLL recovered clock obtains stable phase-lock at a frequency not equal to the incoming data rate. The T7295-1 device uses a combination frequency/phase-lock architecture to prevent false lock. The PLL acquisition aid circuitry monitors the PLL clock frequency relative to the EXCLK reference frequency. If the frequency difference between the EXCLK and PLL clock exceeds approximately ±0.5%, correction circuitry forces reacquisition of the proper frequency and phase.

Loss-of-Lock Indication

The RLOL alarm is activated if the difference between the PLL clock and the EXCLK frequency exceeds approximately ±0.5%. A high RLOL output indicates that the PLL acquisition circuit is working to bring the PLL into proper frequency lock. RLOL remains high until frequency lock has occurred; however, the minimum RLOL pulse width is 32 clock cycles.

Loss-of-Signal Detection

Figure 1 shows that analog and digital methods of loss-of-signal (LOS) detection are combined to create the RLOS alarm output. RLOS is set if either the analog or digital detection circuitry indicates LOS has occurred.

Analog LOS Detection

The analog LOS detector monitors the peak input signal amplitude. RLOS makes a high-to-low transition (input signal regained) when the input signal amplitude exceeds the loss-of-signal threshold defined in Table 5. The RLOS low-to-high transition (input signal lost) occurs at a level typically 1.0 dB below the high-to-low transition level. This hysteresis prevents RLOS chattering. Once set, the RLOS alarm remains high for at least 32 clock cycles, allowing for system detection of a loss-of-signal condition without the use of an external latch.

To allow for varying levels of noise and crosstalk in different applications, three loss-of-signal threshold settings are available using the LOSTHR pin. Setting LOSTHR = V_{DD} provides the lowest loss-of-signal threshold; LOSTHR = $V_{DD}/2$ (can be produced using two 50 kΩ ± 10% resistors as a voltage divider between V_{DDD} and GND_D) provides an intermediate threshold; and LOSTHR = GND provides the highest threshold. The LOSTHR pin must be set to its desired value at powerup and must not be changed during operation.

Table 5. Analog Loss-of-Signal Thresholds

Data Rate	REQB	LOSTHR	Threshold		Unit
			Min	Max	
E3 34.368 Mbits/s	0	0	60	220	mV pk
		$V_{DD}/2$	40	145	mV pk
		V_{DD}	25	90	mV pk
	1	0	45	175	mV pk
		$V_{DD}/2$	30	115	mV pk
		V_{DD}	20	70	mV pk

Notes:
The RLOS alarm is an indication of the presence of an input signal, not a bit error rate indication. Table 2 gives the minimum input amplitude needed for error-free operation (BER < $1e^{-9}$). Independent of the RLOS state, the device will attempt to recover correct timing and data.

The RLOS low-to-high transition typically occurs 1 dB below the high-to-low transition.

Digital LOS Detection

In addition to the signal amplitude monitoring of the analog LOS detector, the digital LOS detector monitors the recovered data 1s density. The RLOS alarm goes high if 160 ± 32 or more consecutive 0s occur in the receive data stream. The alarm goes low when at least eight 1s occur in a string of 32 consecutive bits. This hysteresis minimizes RLOS chattering and guarantees a minimum RLOS pulse width of 32 clock cycles.

Note, however, that RLOS chatter can still occur. When REQB = 1, input signal levels above the analog RLOS threshold can still be low enough to result in a high bit error rate. The resultant data stream (containing errors) can temporarily activate the digital LOS detector, and RLOS chatter can occur. Therefore, RLOS should not be used as a bit error rate monitor. RLOS chatter can also occur when RLOL is activated (high).

The T7295-1EL and T7295-1PL devices do not meet the digital LOS detection requirements for HDB3 encoding. This is corrected in the version of silicon that is code marked T7295-1EL2 and T7295-1PL2.

Timing Recovery (continued)

Loss-of-Signal Detection (continued)

Phase Hits

In response to a 180 degree phase hit in the input data, the T7295-1 returns to error-free operation in less than 2 ms. During the reacquisition time, RLOS may temporarily be indicated.

Interference Immunity

The T7295-1 complies with the interference test detailed in G.703 and detailed in Figure 7. The two data generators are asynchronous.

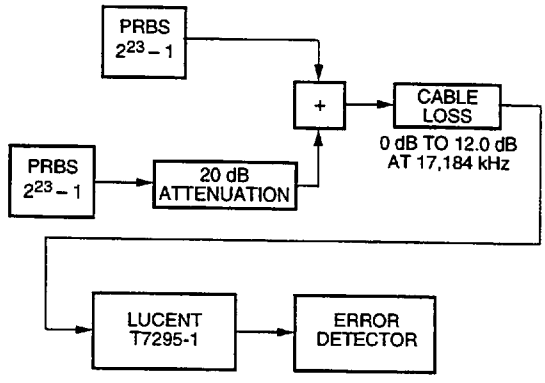


Figure 7. Test Setup for Interference Immunity

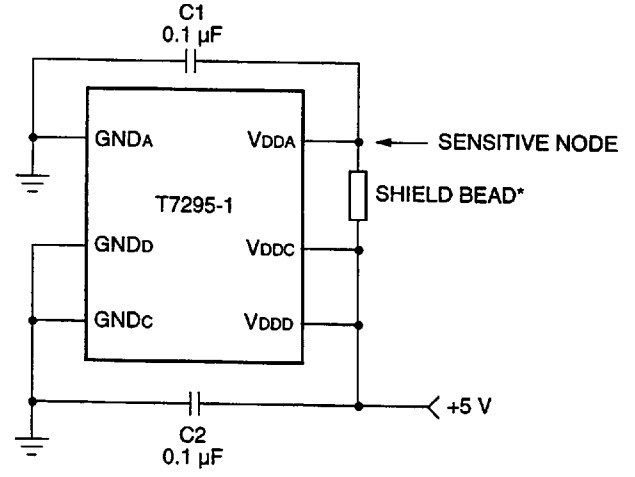
In-Circuit Test Capability

When pulled low, the $\overline{\text{ICT}}$ pin forces all digital outputs (RCLK, RPDATA, RNDATA, RLOS, RLOL pins) into a high output impedance state. This feature allows in-circuit testing to be done on neighboring devices without concern for T7295-1 device output damage. When forced high, the $\overline{\text{ICT}}$ pin does not affect device operation. An internal pull-up device (nominally 50 kΩ) is provided on this pin; therefore, users can leave this pin unconnected for normal operation. This is the only pin for which internal pull-up/pull-down is provided.

Board Layout Considerations

Power Supply Bypassing

Figure 8 illustrates the recommended power supply bypassing network. A 0.1 µF (C2) capacitor bypasses the digital supplies. The analog supply V_{DDA} is bypassed by using a 0.1 µF (C1) capacitor and a shield bead that removes significant amounts of high-frequency noise generated by the system and by the device logic. Good-quality, high-frequency (low lead inductance) capacitors should be used. Finally, it is most important that all ground connections be made to a low-impedance ground plane.



* Recommended shield beads are the *FairRite*† 2643000101 or the *FairRite* 2743019446 (surface mount) or equivalent.
† *FairRite* is a registered trademark of FairRite Products Corporation.

Figure 8. Recommended Power Supply Bypassing Network

Receive Input

The connections to the receive input pin must be carefully considered. Noise coupling must be minimized along the path from the signal entering the board to the input pin. Any noise coupled into the T7295-1 input directly degrades the signal-to-noise ratio of the input signal and may degrade sensitivity.

PLL Filter Capacitor

The PLL filter capacitor between pins LPF1 and LPF2 must be placed as close to the chip as possible (within 1.2 cm is recommended). The LPF1 and LPF2 pins are adjacent, allowing for short-lead lengths with no crossovers to the external capacitor. Noise coupling into the LPF1 and LPF2 pins may degrade PLL performance.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability. External leads can be soldered safely at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
Power Supply	V_{DD}	–0.5	6.5	V
Power Dissipation, Package Limit	P_D	—	700	mW
Storage Temperature	T_{stg}	–40	125	°C
Maximum Voltage (any pin) with Respect to V_{DD}	—	—	0.5	V
Minimum Voltage (any pin) with Respect to GND	—	–0.5	—	V
Maximum Allowable Voltages (RIN) with Respect to GND	—	–0.5	5.0	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold	
Device	**Voltage**
T7295-1	>1000 V

Electrical Characteristics

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	T_A	–40	85	°C
Power Supply	V_{DD}	4.5	5.5	V

Table 7. Electrical Characteristics

Typical values are for V_{DD} = 5.0 V, T_A = 25 °C, and random data. Maximum values are for V_{DD} = 5.5 V at T_A = 85 °C, and all 1s data.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current:	I_{DD}				
REQB = 0		—	82	106	mA
REQB = 1		—	79	103	mA

Electrical Characteristics (continued)

Table 8. Logic Interface Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage:					
Low	V_{IL}	—	GND_D	0.5	V
High	V_{IH}	—	$0.7V_{DDD}$	V_{DDD}	V
Input Leakage	I_L	–0.5 to V_{DD} + 0.5 V (all input pins except 2 and 17)	–10	10	µA
		Pin 17, 0 V	20	500	µA
		Pin 2, V_{DD}	10	100	µA
		Pin 2, GND_D	–50	–5	µA
Output Voltage					
Low	V_{OL}	–5.0 mA	GND_D	0.4	V
High	V_{OH}	5.0 mA	V_{DDD} – 0.5	V_{DDD}	V
Input Capacitance	C_I	—	—	10	pF
Load Capacitance	C_L	—	—	10	pF

Timing Characteristics

Recovered Clock and Data Timing

Table 9 and Figure 9 summarize the timing relationships between the high-speed logic signals RCLK, RPDATA, and RNDATA. RPDATA and RNDATA change on the rising edge of RCLK and are valid during the falling edge of RCLK. A positive pulse at RIN creates a high level on RPDATA and a low level on RNDATA. A negative pulse creates a high level on RNDATA and a low level on RPDATA, and a received zero produces low levels on both RPDATA and RNDATA.

Table 9. System Interface Timing Characteristics

All timing characteristics are measured with 10 pF loading.

Symbol	Parameter	Min	Typ	Max	Unit
tRCH1RCH2	Receive Clock Rise Time (10% to 90%)	—	—	3.5	ns
tRCL2RCL1	Receive Clock Fall Time (90% to 10%)	—	—	2.5	ns
tRDVRCL	Receive Data Setup Time	5.0	—	—	ns
tRCLRDX	Receive Data Hold Time	8.5	—	—	ns
tRCHRDV	Receive Propagation Delay	0.6	—	3.7	ns
—	Receive Clock Duty Cycle	45	50	55	%

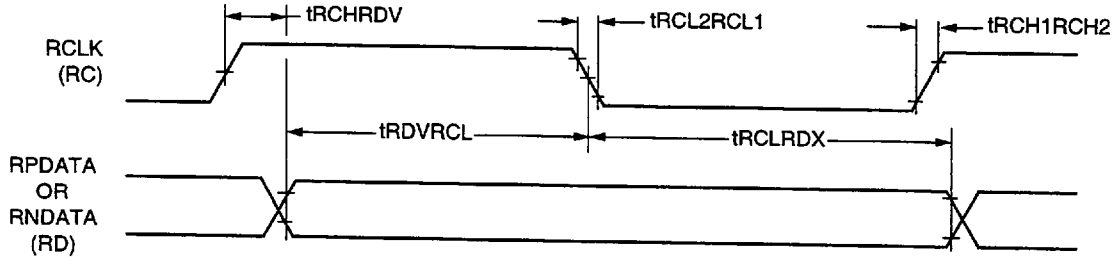


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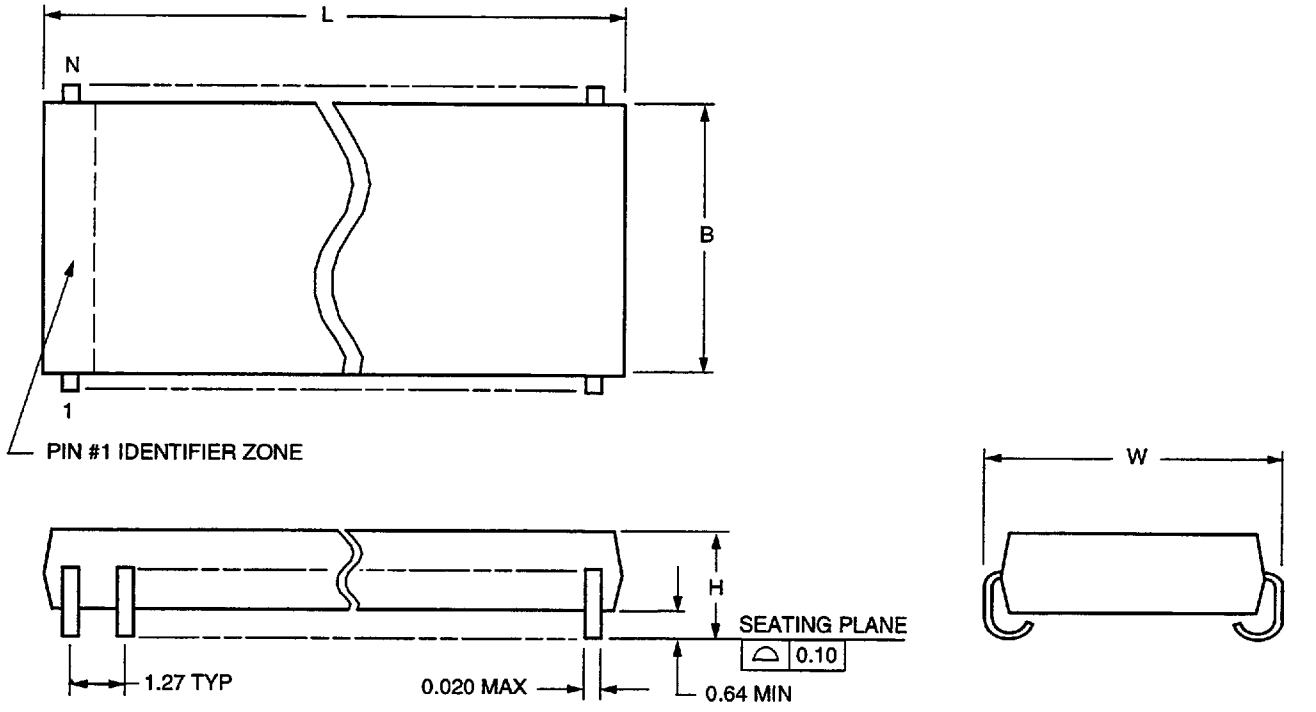
Figure 9. Timing Diagram for System Interface

Outline Diagrams

20-Pin, Plastic SOJ

Dimensions are in millimeters.

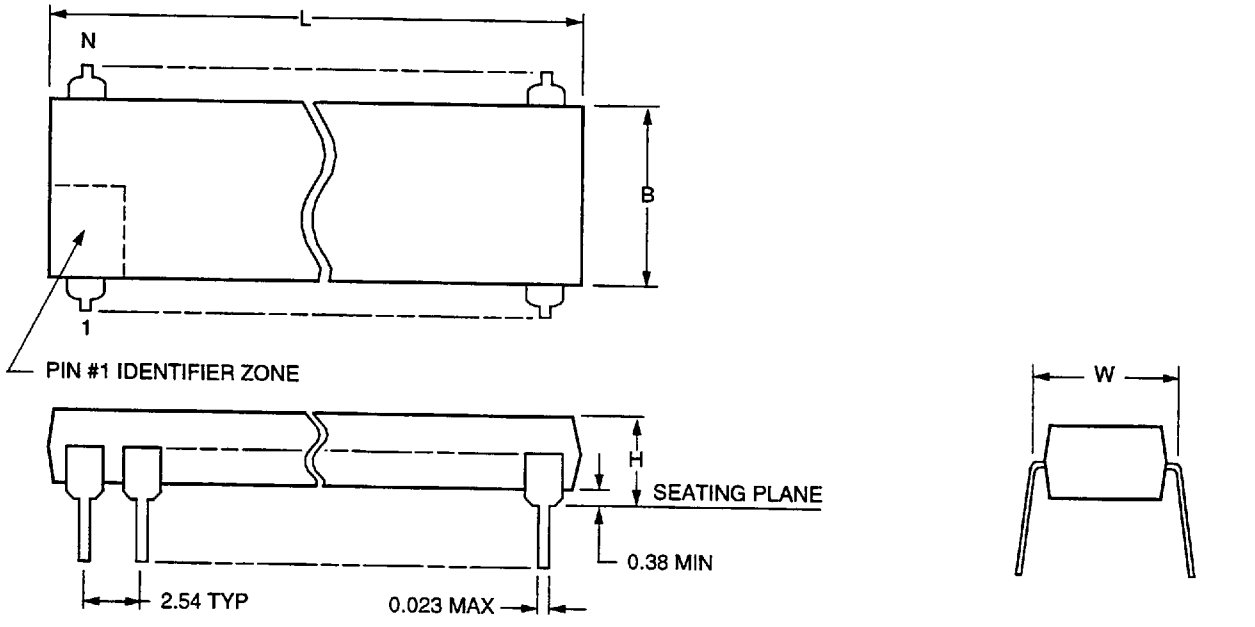


Number of Pins (N)	Package Dimensions (SOJ)			
	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
20	12.95	7.62	8.81	3.18

Outline Diagrams (continued)

20-Pin, Plastic DIP

Dimensions are in millimeters.



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Number of Pins (N)	Package Dimensions (DIP)			
	Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
20	26.42	6.48	7.87	5.08

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
T - 7295 - - - 1EL2	20-Pin, Plastic SOJ	–40 °C to +85 °C	107114464
T - 7295 - - - 1PL2	20-Pin, Plastic DIP	–40 °C to +85 °C	107202186