

SN74ALS166 PARALLEL-LOAD 8-BIT SHIFT REGISTER

SDAS156C – APRIL 1982 – REVISED DECEMBER 1994

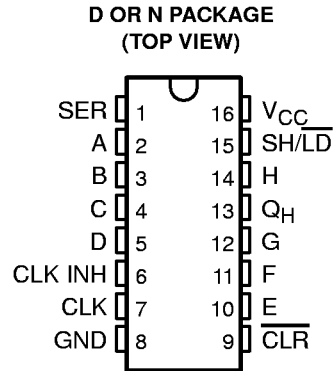
- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs

description

The SN74ALS166 parallel-load 8-bit shift register is compatible with most other TTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clocks (CLK and CLK INH) inputs and an overriding clear ($\overline{\text{CLR}}$) input. The parallel-in or serial-in modes are established by the shift/load ($\text{SH}/\overline{\text{LD}}$) input. When high, $\text{SH}/\overline{\text{LD}}$ enables the serial data (SER) input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data (A–H) inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive-NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running and the register can be stopped on command with the clock input. CLK INH should be changed to the high level only when CLK is high. The buffered $\overline{\text{CLR}}$ overrides all other inputs, including CLK, and sets all flip-flops to zero.

The SN74ALS166 is characterized for operation from 0°C to 70°C.



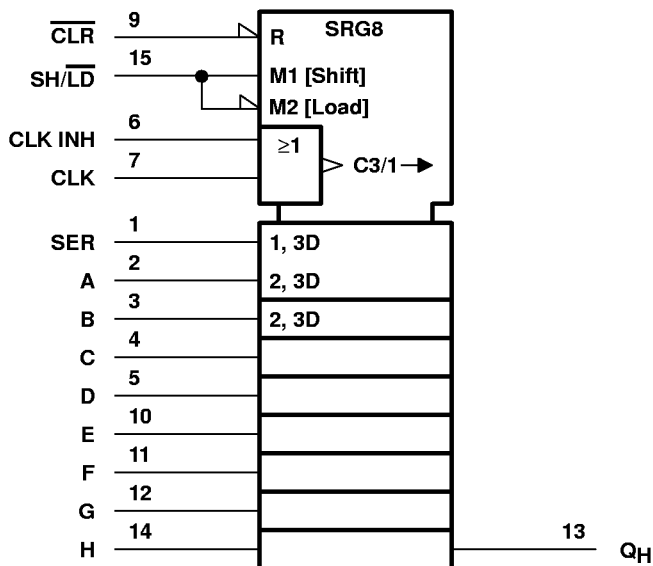
FUNCTION TABLE

INPUTS					PARALLEL A . . . H	INTERNAL OUTPUTS		OUTPUT QH
$\overline{\text{CLR}}$	$\text{SH}/\overline{\text{LD}}$	CLK INH	CLK	SER		QA	QB	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	↑	X	X	QA0	QB0	QH0

SN74ALS166 PARALLEL-LOAD 8-BIT SHIFT REGISTER

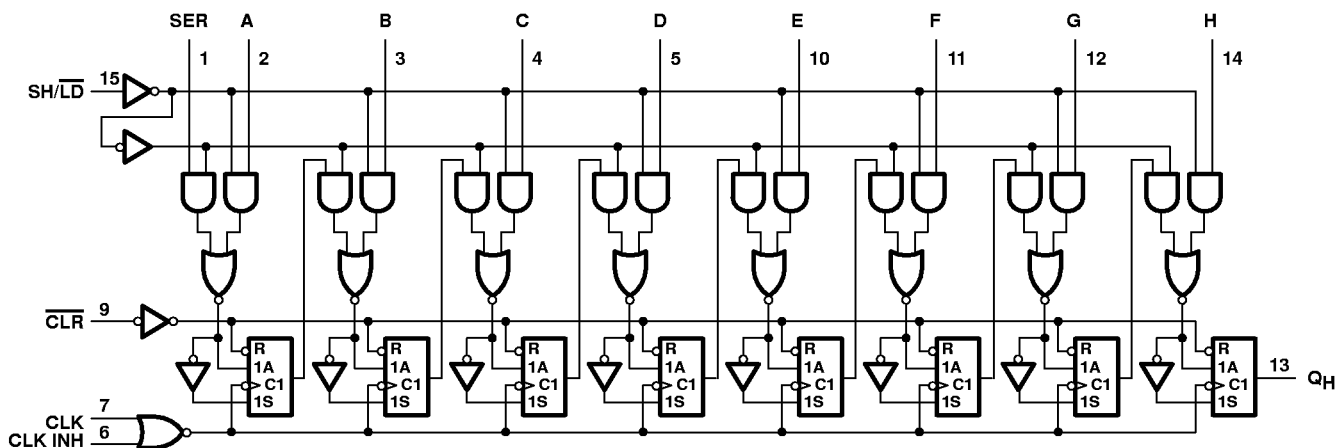
SDAS156C – APRIL 1982 – REVISED DECEMBER 1994

logic symbol†

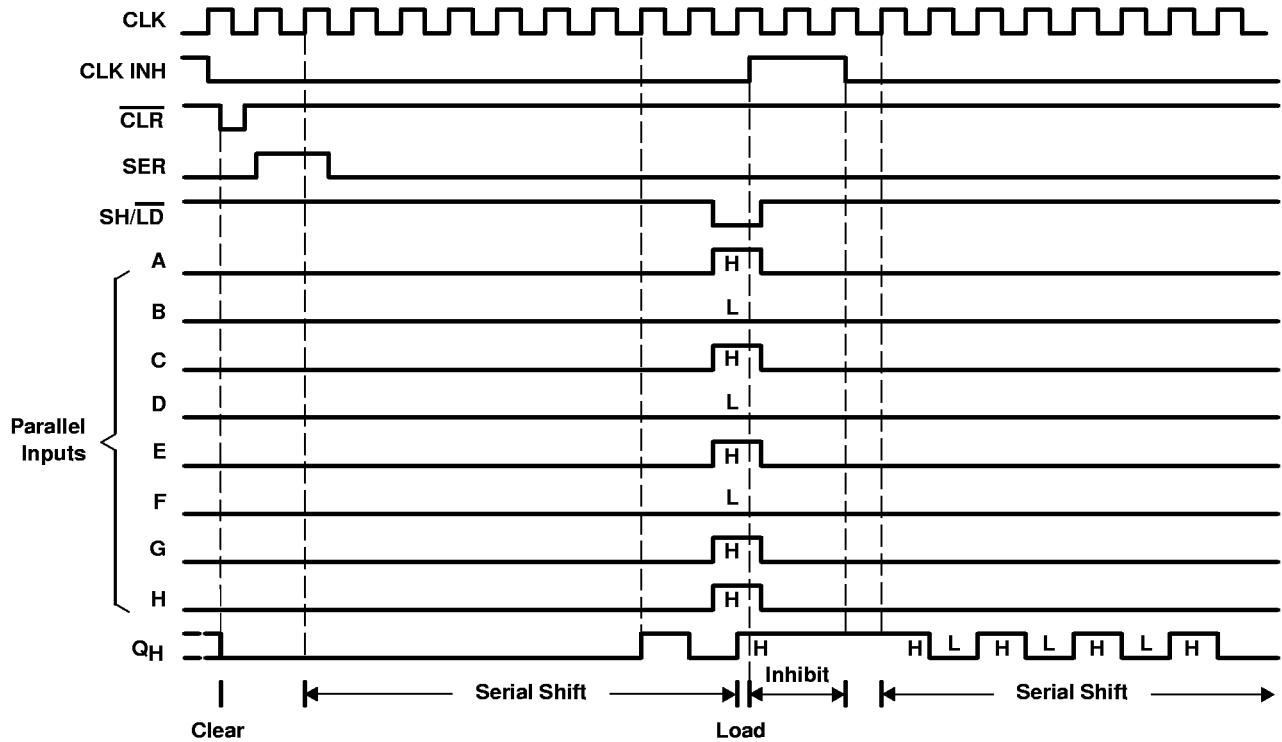


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



typical clear, shift, load, inhibit, and shift sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS166 PARALLEL-LOAD 8-BIT SHIFT REGISTER

SDAS156C – APRIL 1982 – REVISED DECEMBER 1994

recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current			-0.4	mA
I _{OL}	Low-level output current			8	mA
f _{clock}	Clock frequency			45	MHz
t _w	Pulse duration	CLR low	9		ns
		CLK high	10		
		CLK low	10		
t _{su}	Setup time before CLK↑	SH/LD	16		ns
		Data	7		
		CLR inactive	11		
t _h	Hold time, data after CLK↑	3			ns
T _A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA			-1.5	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = -0.4 mA	V _{CC} - 2			V
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4		V
		I _{OL} = 8 mA	0.35	0.5		
I _I	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
I _{IH}	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μA
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1	mA
I _{O‡}	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	mA
I _{CC}	V _{CC} = 5.5 V,	See Note 1		14	24	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: With 4.5 V applied to SER and all other inputs, except the clock, grounded, I_{CC} is measured after a clock transition from 0 V to 4.5 V.

switching characteristics (see Figure 1)

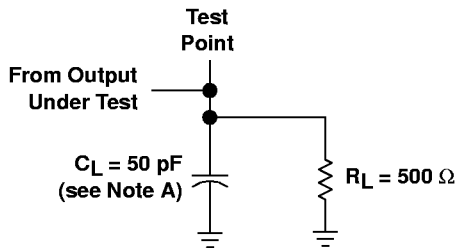
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§			UNIT
			MIN	TYP¶	MAX	
f _{max}			45			MHz
t _{PHL}	CLR	Q _H	4	9	14	ns
t _{PLH}	CLK	Q _H	2	7	12	
t _{PHL}			2	9	13	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

¶ All typical values are at V_{CC} = 5 V, T_A = 25°C.



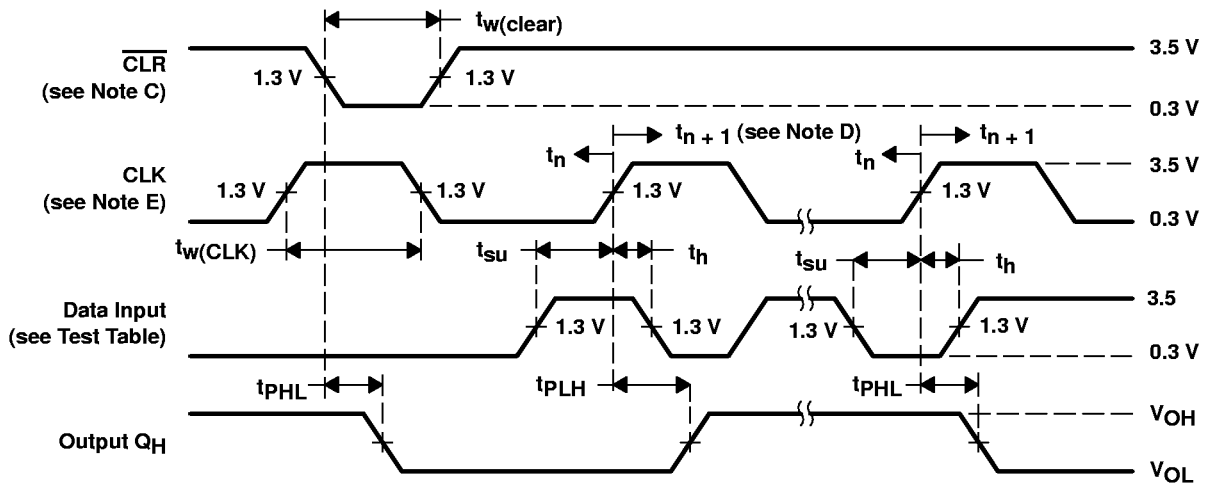
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SH/LD	OUTPUT TESTED (see Note B)
H	0 V	QH at t_{n+1}
Serial Input	4.5 V	QH at t_{n+1}



VOLTAGE WAVEFORMS

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+8} with a functional test.
 - C. A clear pulse is applied prior to each test.
 - D. t_n = bit time before clocking transition, t_{n+1} = bit time after one clocking transition, and t_{n+8} = bit time after eight clocking transitions.
 - E. The clock pulse has the following characteristics: $t_{w(\text{clock})} \leq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(\text{clear})} \leq 20$ ns.
 - F. All pulse generators have the following characteristics: $Z_O \approx 50 \Omega$; $t_r = t_f = 2$ ns. Duty cycle = 50% when testing f_{max} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.