MOTOROLA

Military 54F181

Advance Information

4-Bit Arithmetic Logic Unit

ELECTRICALLY TESTED PER:
MPG54F181

The 54F181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

- Provides 16 Arithmetic Operations Add, Subtract, Compare, Double. Plus Twelve Other Arithmetic Operations
- Provides All 16 Logic Operations of Two Variables Exclusive-OR, Compare, AND, NAND, OR, NOR, Plus Ten Other Logic Operations
- Full Lookahead For High-Speed Arithmetic Operation on Long Words
- 600 or 300 MIL Wide DIP Packages

AVAILABLE AS:

1) JAN: *
2) SMD: *
3) 883C: *

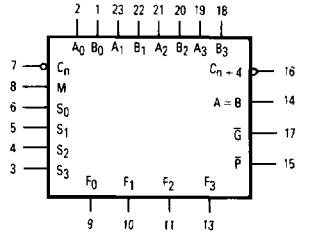
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: J
CERFLAT: K
***Call Factory for latest update**

FUNCTION TABLE

Mode Select Inputs				Active-Low Operands & F_n Outputs		Active-High Operands & F_n Outputs	
S_3	S_2	S_1	S_0	Logic (M=H)	Arithmetic** (M=L) (C_n=L)	Logic (M=H)	Arithmetic** (M=L) (C_n=H)
L	L	L	L	$\overline{A}$	A *minus* 1	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{AB}$	$A+\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{A\overline{B}}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus $(A+B)$	$\overline{A}+B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus $(A+B)$	B	$(A+\overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.
H = HIGH Voltage Level
L = *LOW Voltage Level*

ACTIVE-HIGH OPERANDS



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
B_0	1	1	1	GND
A_0	2	2	2	V_{CC}
S_3	3	3	3	GND
S_2	4	4	4	GND
S_1	5	5	5	GND
S_0	6	6	6	GND
C_n	7	7	7	V_{CC}
M	8	8	8	V_{CC}
F_0	9	9	9	OPEN
F_1	10	10	10	OPEN
F_2	11	11	11	OPEN
GND	12	12	12	GND
F_3	13	13	13	OPEN
A=B	14	14	14	OPEN
P	15	15	15	OPEN
C_{n+4}	16	16	16	OPEN
G	17	17	17	OPEN
B_3	18	18	18	V_{CC}
A_3	19	19	19	V_{CC}
B_2	20	20	20	V_{CC}
A_2	21	21	21	V_{CC}
B_1	22	22	22	V_{CC}
A_1	23	23	23	V_{CC}
V_{CC}	24	24	24	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

5

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL DESCRIPTION

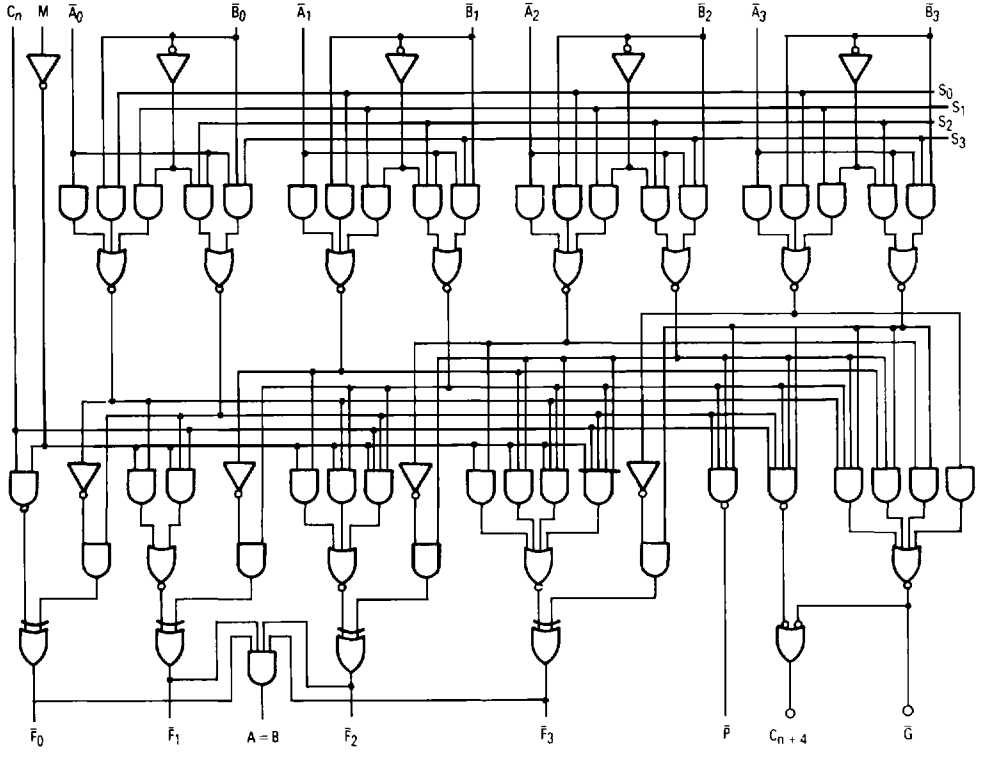
The F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0–S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-HIGH or active-LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple Ripple Carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four F181 devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can be used with the C_{n+4} signal to indicate A>B and A<B.

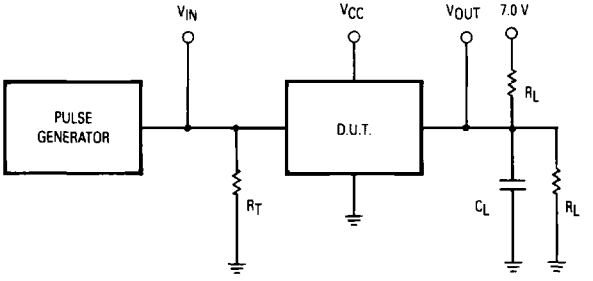
The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow, thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-LOW inputs producing active-LOW outputs or with active-HIGH inputs producing active-HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

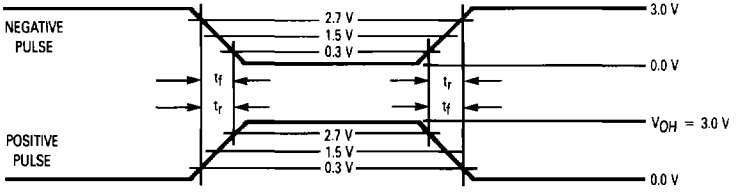
LOGIC DIAGRAM



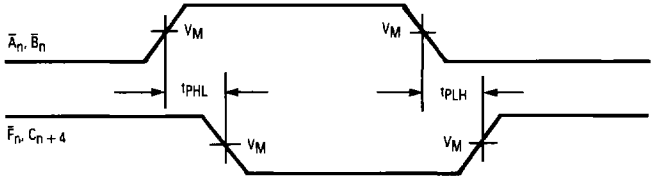
5

TEST CIRCUIT FOR OPEN COLLECTOR





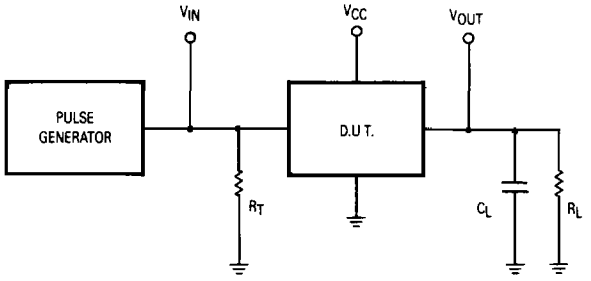
INPUT PULSE

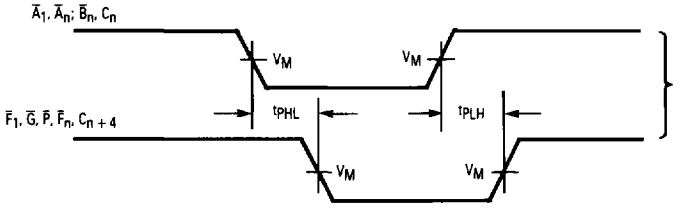


Waveform 1. Propagation Delay For Operands to Carry Output And Outputs.

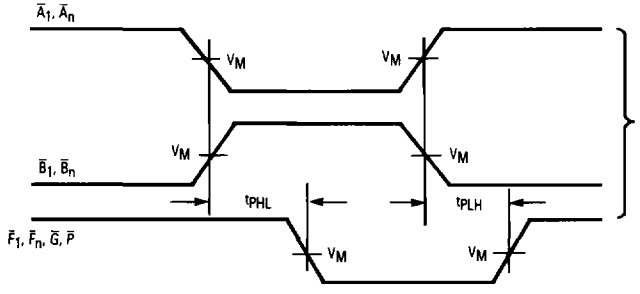
NOTES:
1. Pulse generator has the following characteristics:
   $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, $Z_{out} = R_T \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high $\geq$ 2.0 V, low $\leq$ 0.8 V, or open)
3. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
4. R_L = 499 Ω ± 5.0%.
5. Voltage measurements are to be made with respect to network ground terminal.

TEST CIRCUIT FOR TOTEM-POLE OUTPUTS

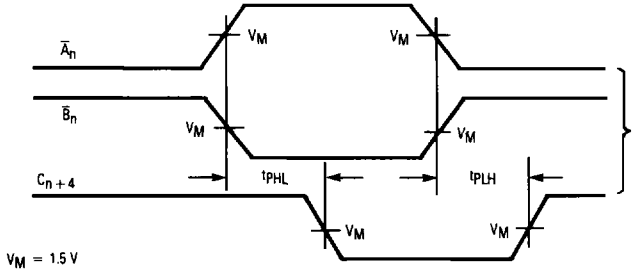




Waveform 2. Propagation Delays For Carry Input To Carry Output, Carry Input To Outputs, And Operands To Carry Generate Operands To Carry Generate And Carry Propagate Outputs.



Waveform 3. Propagation Delay For Operands To Carry Generate And Propagate Outputs, Operands To A = B Output, And Outputs.



Waveform 4. Propagation Delays For Operands To Carry Output.

V_M = 1.5 V

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 2.0 V or 0.8 V (all inputs).
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IN} = 0.8 V or 2.0 V (all inputs).
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = 0 V or 5.5 V.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs = 0 V or 5.5 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V or 0 V all inputs, V_{out} = 0 V.
$I_{IL1(M)}$	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V (M), other inputs = 5.5 V.
$I_{IL2(A, B)}$	Logical "0" Input Current	−0.09	−1.8	−0.09	−1.8	−0.09	−1.8	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V (A, B), other inputs = 5.5 V.
$I_{IL3(S)}$	Logical "0" Input Current	−0.12	−2.4	−0.12	−2.4	−0.12	−2.4	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V (S), other inputs = 5.5 V or 0 V.
$I_{IL4(C_n)}$	Logical "0" Input Current	−0.15	−3.0	−0.15	−3.0	−0.15	−3.0	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V (C_n), other inputs = 0 V or 5.5 V.
I_{CCH}	Power Supply Current Off		65		65		65	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (A − inputs), other inputs = 0 V.
I_{CCL}	Power Supply Current Off		65		65		65	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

5

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	3.0	10	3.0	14.5	3.0	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	3.0	9.0	3.0	14.5	3.0	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	4.0	10	4.0	14	4.0	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	4.0	10.5	3.5	16.5	3.5	16.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	3.5	12	3.5	17	3.5	17	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	5.0	13	5.0	18	5.0	18	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	3.0	7.5	3.0	10.5	3.0	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	2.5	7.0	2.5	10	2.5	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL5}	Propagation Delay /Data-Output C_n to $\overline{F}_n$	3.0	8.5	2.5	12	2.5	12	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH5}	Propagation Delay /Data-Output C_n to $\overline{F}_n$	3.0	8.5	2.5	16	2.5	16	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL6}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	2.5	7.5	2.5	10.5	2.5	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH6}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	2.5	7.5	2.5	10.5	2.5	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL7}	Propagation Delay /Data-Output C_n to C_{n+4}	3.0	8.0	3.0	11.5	3.0	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH7}	Propagation Delay /Data-Output C_n to C_{n+4}	3.0	8.5	3.0	12	3.0	12	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

5

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL8}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	3.0	11	3.0	15.5	3.0	15.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH8}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	3.0	11	3.0	17.5	3.0	17.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL9}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	3.0	10	3.0	15.5	3.0	15.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH9}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	3.5	9.5	3.5	15.5	3.5	15.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL10}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	3.0	12	3.0	17	3.0	17	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH10}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	4.0	12	3.5	17.5	3.5	17.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL11}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	2.5	9.5	2.5	13.5	2.5	13.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH11}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	3.0	9.0	2.5	12	2.5	12	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL12}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	5.0	13	4.0	18	4.0	18	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH12}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	5.0	14	5.0	19.5	5.0	19.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL13}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	3.0	8.5	3.0	12	3.0	12	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH13}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	2.5	8.0	2.5	11	2.5	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL14}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to A = B	5.5	13.5	5.5	21	5.5	21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH14}	Propagation Delay /Data-Output $\overline{A}_n$ or $\overline{B}_n$ to A = B	11	27	8.0	35	8.0	35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

5