

TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S51F, TC75S51FU

Single Operational Amplifier

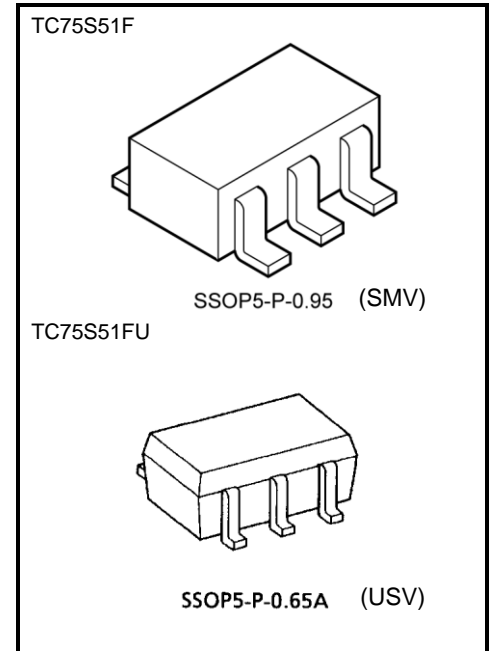
The TC75S51F/TC75S51FU is a CMOS single-operation amplifier which incorporates a phase compensation circuit. It is designed with a low-voltage and low-current power supply; this differentiates this device from general-purpose bipolar op-amps.

Features

- Low-voltage operation : $V_{DD} = \pm 0.75$ to ± 3.5 V or 1.5 to 7 V
- Low-current power supply : $I_{DD} (V_{DD} = 3 \text{ V}) = 60 \mu\text{A}$ (typ.)
- Built-in phase-compensated op-amp, obviating the need for any external device
- Ultra-compact package

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}, V_{SS}	7	V
Differential input voltage	DV_{IN}	± 7	V
Input voltage	V_{IN}	V_{DD} to V_{SS}	V
Power dissipation	P_D	200	mW
Operating temperature	T_{opr}	-40 to 85	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 125	$^\circ\text{C}$



Weight

SSOP5-P-0.95 : 0.014 g (typ.)

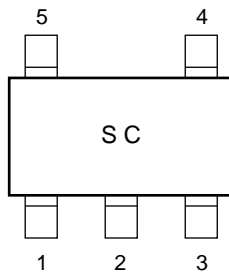
SSOP5-P-0.65A : 0.006 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

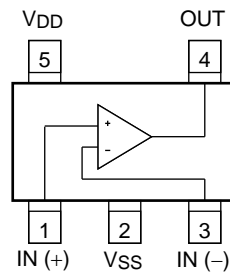
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
1993-07

Marking (top view)



Pin Connection (top view)



Electrical Characteristics

DC Characteristics ($V_{DD} = 3.0\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	—	2	10	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	$R_S = 1\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	0	—	2.5	V
Voltage gain (open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	$R_L \geq 100\text{ k}\Omega$	2.9	—	—	V
	V_{OL}	4	$R_L \geq 100\text{ k}\Omega$	—	—	0.1	
Common mode input signal rejection ratio	$CMRR$	2	$V_{IN} = 0.0\text{ to }2.5\text{ V}$	55	65	—	dB
Supply voltage rejection ratio	$SVRR$	1	$V_{DD} = 1.5\text{ to }7.0\text{ V}$	60	70	—	dB
Supply current	I_{DD}	5	—	—	60	200	μA

DC Characteristics ($V_{DD} = 1.5\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	$R_S = 10\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	—	2	10	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	$R_S = 10\text{ k}\Omega$, $R_F = 100\text{ k}\Omega$	0	—	1.0	V
Voltage gain (open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	$R_L \geq 100\text{ k}\Omega$	1.4	—	—	V
	V_{OL}	4	$R_L \geq 100\text{ k}\Omega$	—	—	0.1	
Supply current	I_{DD}	5	—	—	50	150	μA

Note: For this device, please use a source current of no more than 70 μA .

AC Characteristics ($V_{DD} = 3.0\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

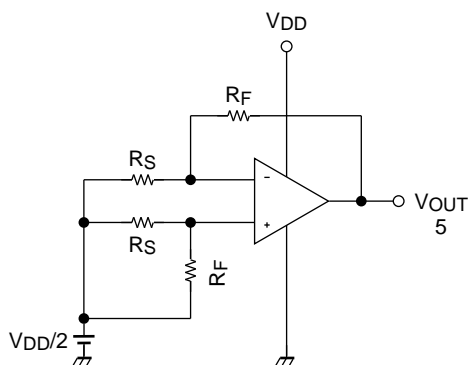
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	$A_V = 0\text{ dB}$	—	0.5	—	$\text{V}/\mu\text{s}$
Unity gain cross frequency	f_T	—	$A_V = 40\text{ dB}$	—	0.6	—	MHz

AC Characteristics ($V_{DD} = 1.5\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	$A_V = 0\text{ dB}$	—	0.3	—	$\text{V}/\mu\text{s}$
Unity gain cross frequency	f_T	—	$A_V = 40\text{ dB}$	—	0.5	—	MHz

Test Circuit

1. SVRR, V_{IO}



- SVRR**
 For each of the two V_{DD} values, measure the V_{OUT} value, as indicated below, and calculate the value of SVRR using the equation shown.

When $V_{DD} = 1.5\text{ V}$, $V_{DD} = V_{DD1}$ and $V_{OUT} = V_{OUT1}$

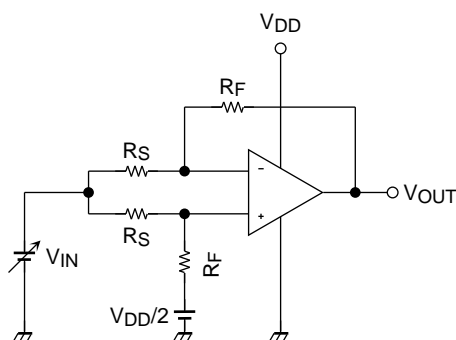
When $V_{DD} = 7.0\text{ V}$, $V_{DD} = V_{DD2}$ and $V_{OUT} = V_{OUT2}$

$$SVRR = 20 \log \left(\left| \frac{V_{OUT1} - V_{OUT2}}{V_{DD1} - V_{DD2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

- V_{IO}**
 Measure the value of V_{OUT} and calculate the value of V_{IO} using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CM_{VIN}



- CMRR**
 Measure the V_{OUT} value, as indicated below, and calculate the value of the CMRR using the equation shown.

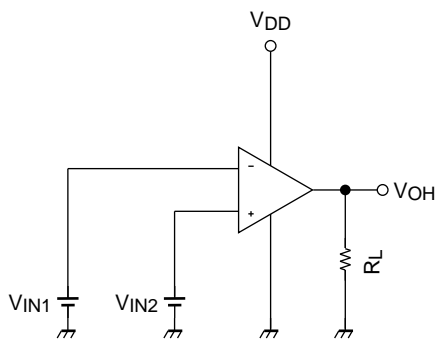
When $V_{IN} = 0.0\text{ V}$, $V_{IN} = V_{IN1}$ and $V_{OUT} = V_{OUT1}$

When $V_{IN} = 2.5\text{ V}$, $V_{IN} = V_{IN2}$ and $V_{OUT} = V_{OUT2}$

$$CMRR = 20 \log \left(\left| \frac{V_{OUT1} - V_{OUT2}}{V_{IN1} - V_{IN2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

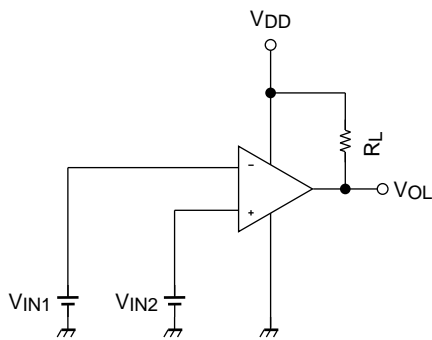
- CM_{VIN}**
 Input range within which the CMRR specification guarantees V_{OUT} value (as varied by the V_{IN} value).

3. VOH



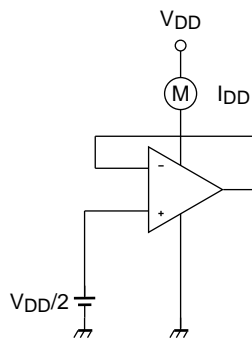
- VOH
 - $V_{IN1} = \frac{V_{DD}}{2} - 0.05 \text{ V}$
 - $V_{IN2} = \frac{V_{DD}}{2} + 0.05 \text{ V}$

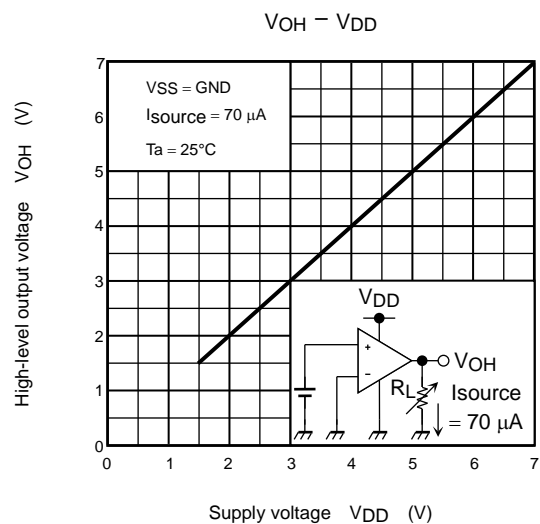
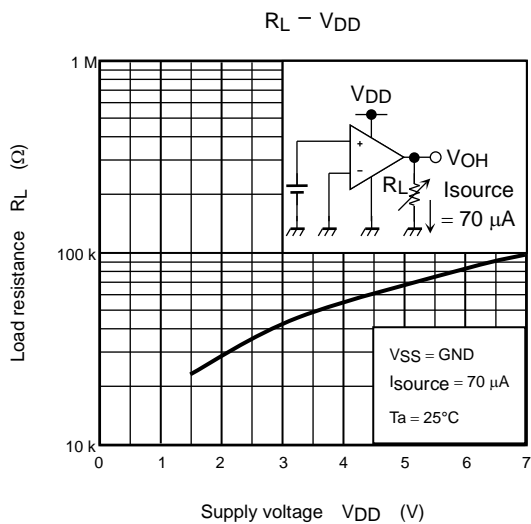
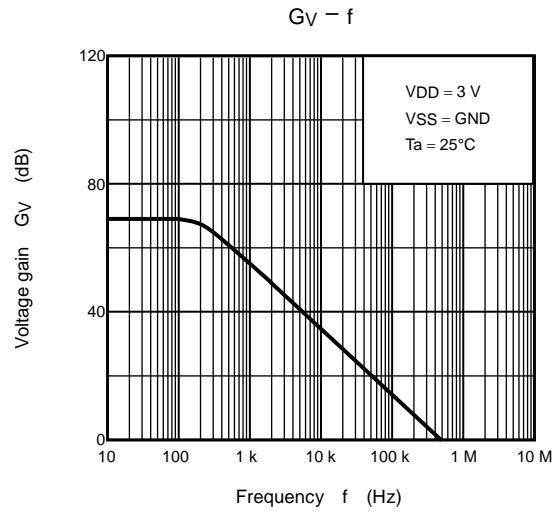
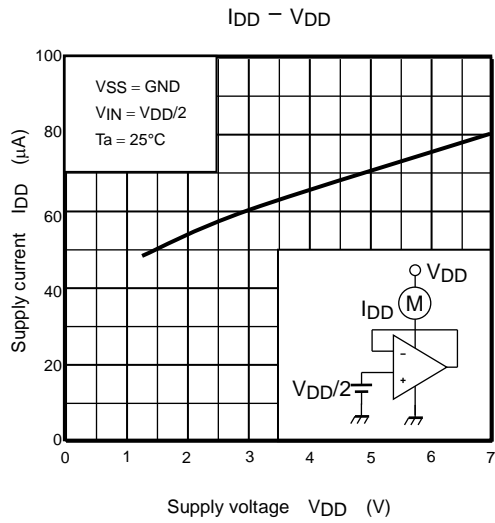
4. VOL



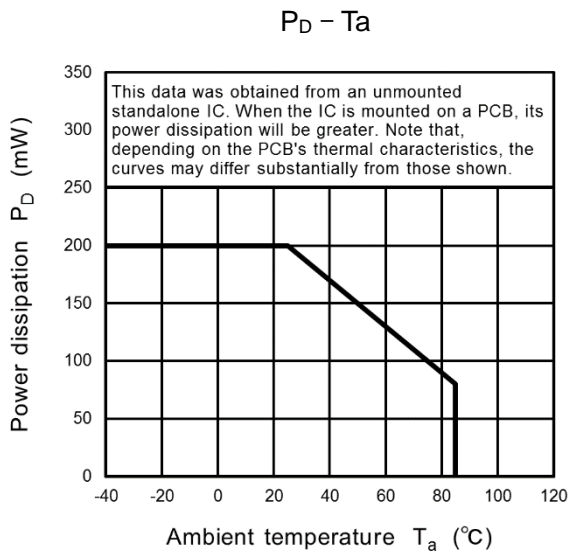
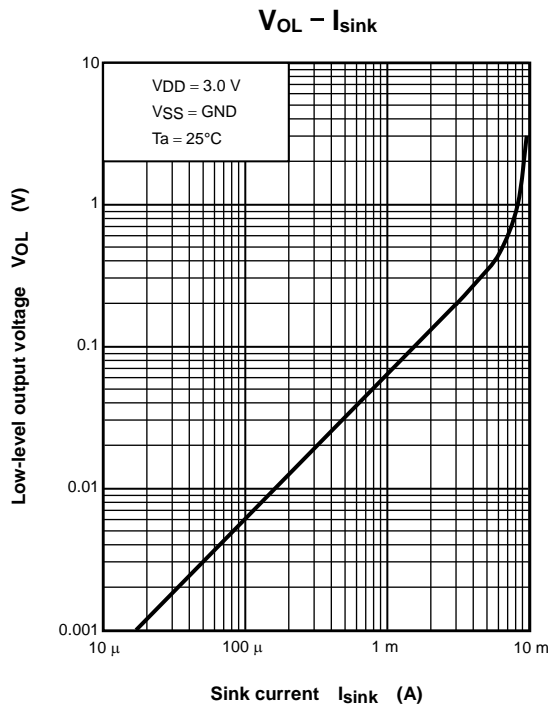
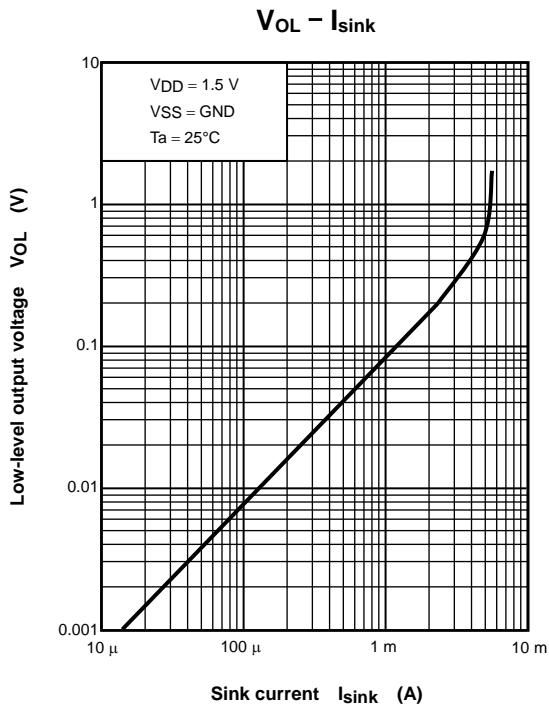
- VOL
 - $V_{IN1} = \frac{V_{DD}}{2} + 0.05 \text{ V}$
 - $V_{IN2} = \frac{V_{DD}}{2} - 0.05 \text{ V}$

5. IDD





The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

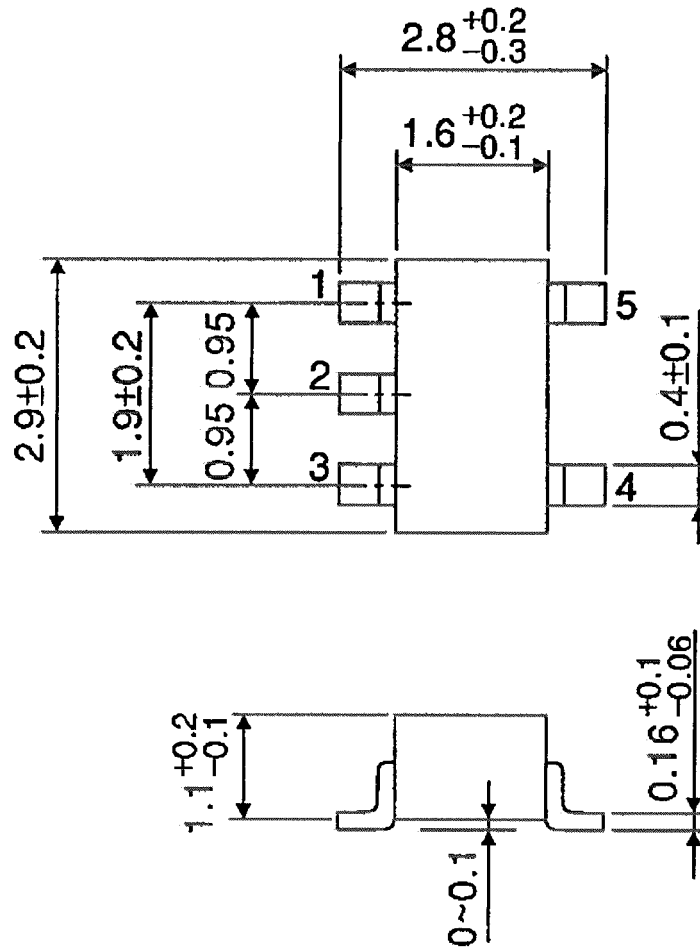


The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

SSOP5-P-0.95

Unit : mm

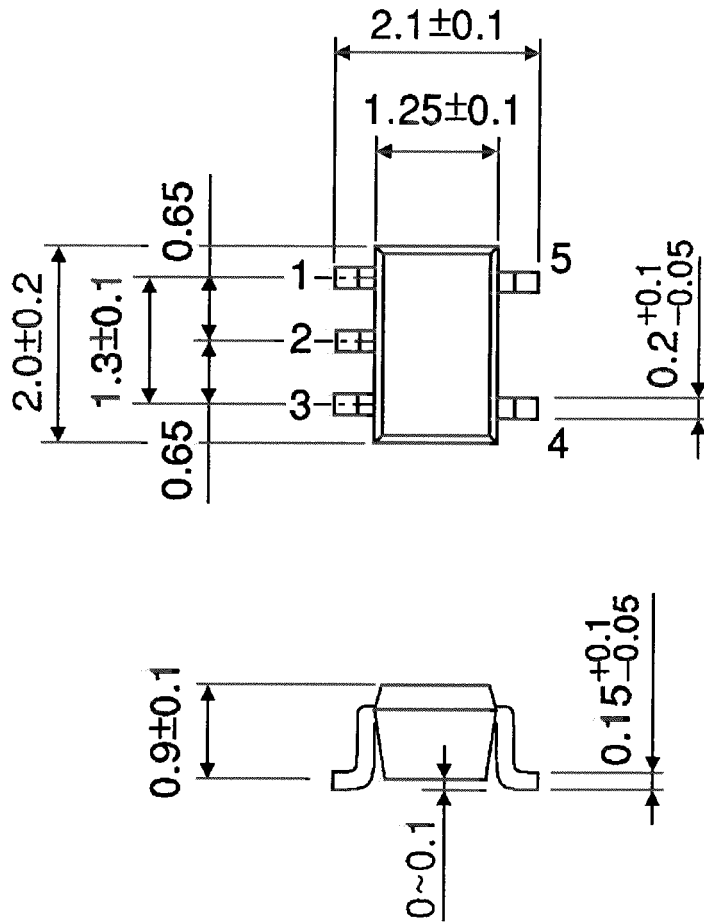


Weight: 0.014 g (typ.)

Package Dimensions

SSOP5-P-0.65A

Unit : mm



Weight: 0.006 g (typ.)

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