

## Philips Components-Signetics

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ECL Products	

# 100255

## Quint ECL-TTL Transceiver

### FEATURES

- Typical propagation delay from ECL input to TTL output: 3.2ns
- Typical propagation delay from TTL input to ECL output: 1.6ns
- Typical ECL supply current ( $-I_{EE}$ ): 105mA
- Typical TTL supply current ( $I_{TTL}$ ): 76mA
- ECL output has three-state capability
- ECL output drives 25 Ohm loads

### DESCRIPTION

The 100255 is a five-bit, inverting, translating transceiver. It allows the exchange of data between a 100K ECL bus and a TTL bus. The A data lines are bidirectional with 100K ECL compatibility and three-state capability. The B data lines are bidirectional with TTL compatibility and three-state capability. The control lines require 100K ECL input levels.

The Direction Control, DIR, selects the data flow path ( $A_n$  to  $B_n$  or  $B_n$  to  $A_n$ ). A Low on the Chip Enable, CE, puts both the  $A_n$  and the  $B_n$  lines into a high imped-

ance state. Each  $A_n$  output can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to  $-2.0V$ ).

The  $GND_1$  line is associated with all the TTL circuitry, the ECL internal logic, and the ECL reference generator.  $GND_2$  services the ECL outputs.

Power may be applied to the  $V_{EE}$  and  $V_{TTL}$  pins in any order.

All unused inputs can be left open due to integrated pull-down resistors.

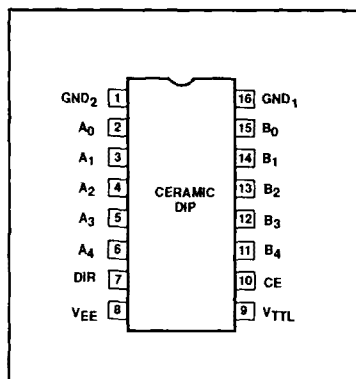
### ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP (300 mils wide)	100255F

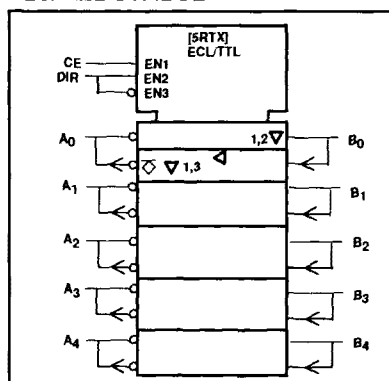
### PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_4$	Bidirectional data lines (100K ECL compatible)
$B_0 - B_4$	Bidirectional data lines (TTL compatible)
DIR	Direction control input (100K ECL compatible)
CE	Chip enable input (100K ECL compatible)

### PIN CONFIGURATION



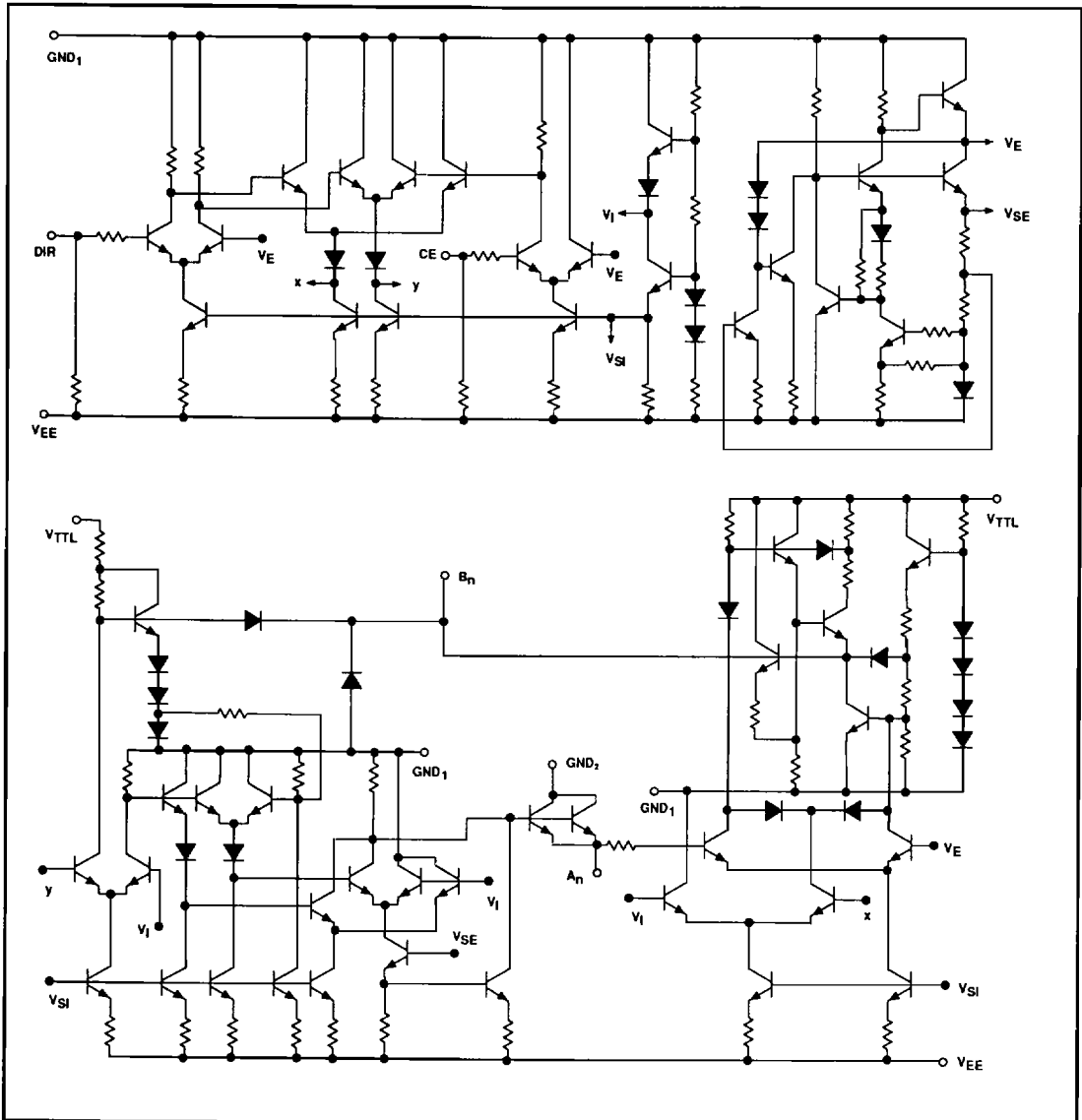
### IEC/IEEE SYMBOL



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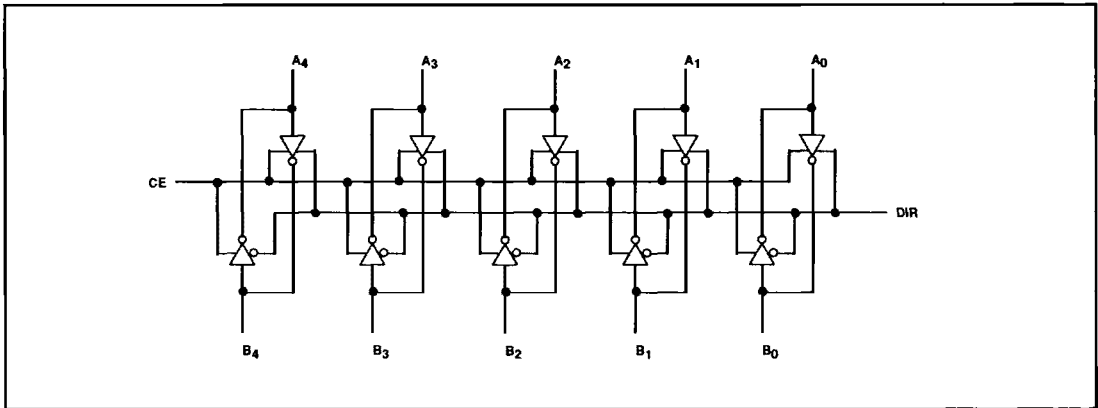
## SIMPLIFIED SCHEMATIC



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## LOGIC DIAGRAM



**NOTE:**

Pins B<sub>0</sub> through B<sub>4</sub> are compatible with TTL. Pins CE, DIR, and A<sub>0</sub> through A<sub>4</sub> are compatible with 100K ECL.

## FUNCTION TABLE

CONTROL		DATA		OPERATING MODE
CE	DIR	A <sub>n</sub>	B <sub>n</sub>	
L	X	Z	Z	A <sub>n</sub> and B <sub>n</sub> in high impedance state
H	H	L	H	Data flows from A <sub>n</sub> to B <sub>n</sub> (ECL-to-TTL translation)
H	L	L	H	Data flows from B <sub>n</sub> to A <sub>n</sub> (TTL-to-ECL translation)

**NOTES:**

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance state

**ABSOLUTE MAXIMUM RATINGS FOR ECL-COMPATIBLE LINES** GND<sub>1</sub> = GND<sub>2</sub> = ground, T<sub>A</sub> = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V <sub>EE</sub>	ECL supply voltage range	-7.0 to +0.5	V
V <sub>IN</sub>	Input voltage (V <sub>IN</sub> should never be more negative than V <sub>EE</sub> )	V <sub>EE</sub> to +0.5	V
I <sub>O</sub>	Output source current (continuous)	-100	mA
T <sub>S</sub>	Storage temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+150	°C

**NOTE:**

Operation beyond the limits set forth in this table may impair the useful life of the device.

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**ABSOLUTE MAXIMUM RATINGS FOR TTL-COMPATIBLE LINES**  $GND_1 = GND_2 = \text{ground}$ ,  $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
$V_{TTL}$	TTL supply voltage range	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to $V_{TTL}$	V
$I_{IN}$	Input current	-30 to +5.0	mA
$V_{OUT}$	Voltage applied to $B_n$ in High state	-0.5 to $V_{TTL}$	V
$T_S$	Storage temperature range	-65 to +150	$^\circ\text{C}$
$T_J$	Maximum junction temperature	+150	$^\circ\text{C}$

**NOTE:**

Operation beyond the limits set forth in this table may impair the useful life of the device.

**DC OPERATING CONDITIONS FOR ECL-COMPATIBLE LINES**

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
$GND_1, GND_2$	Circuit ground		0	0	0	V
$V_{EE}$	ECL supply voltage		-4.8	-4.5	-4.2	V
$V_{EE}$	ECL supply voltage when operating with the 10K or the 10KH ECL family		-5.7			V
$V_{IH}$	High level input voltage	$V_{EE} = -4.2\text{V}$	-1150		-880	mV
		$V_{EE} = -4.5\text{V}$	-1165			
		$V_{EE} = -4.8\text{V}$	-1165			
$V_{IL}$	Low level input voltage	$V_{EE} = -4.2\text{V}$	-1810		-1475	mV
		$V_{EE} = -4.5\text{V}$			-1475	mV
		$V_{EE} = -4.8\text{V}$			-1490	mV
$T_A$	Operating ambient temperature range		0	+25	+85	$^\circ\text{C}$

**NOTE:**

When operating at other than the specified  $V_{EE}$  voltages (-4.2V, -4.5V, -4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

**DC OPERATING CONDITIONS FOR TTL-COMPATIBLE LINES**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
$V_{TTL}$	TTL supply voltage	+4.5	+5.0	+5.5	V
$V_{IH}$	High level input voltage	+2.0			V
$V_{IL}$	Low level input voltage			+0.8	V
$-I_{OH}$	High level output current			2	mA
$I_{OL}$	Low level output current			20	mA
$T_A$	Operating ambient temperature range	0	+25	+85	$^\circ\text{C}$

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## DC ELECTRICAL CHARACTERISTICS FOR ECL-COMPATIBLE LINES

GND<sub>1</sub> = GND<sub>2</sub> = ground, V<sub>EE</sub> = -4.8V to -4.2V, V<sub>TTL</sub> = 4.5V to 5.5V, T<sub>A</sub> = 0°C to +85°C unless otherwise specified<sup>1,3,4</sup>

SYMBOL	PARAMETER	TEST CONDITIONS <sup>2</sup>	LIMITS			UNIT			
			MIN.	TYP.	MAX.				
V <sub>OH</sub>	High level output voltage	B <sub>n</sub> at 0.4V.	V <sub>EE</sub> = -4.2V	-1020		-870	mV		
			V <sub>EE</sub> = -4.5V	-1025	-955	-880	mV		
			V <sub>EE</sub> = -4.8V	-1035		-880	mV		
V <sub>OHT</sub>	High level output threshold voltage	B <sub>n</sub> at 0.8V.	V <sub>EE</sub> = -4.2V	-1030			mV		
			V <sub>EE</sub> = -4.5V	-1035			mV		
			V <sub>EE</sub> = -4.8V	-1045			mV		
V <sub>OLT</sub>	Low level output threshold voltage	B <sub>n</sub> at 2.0V.	V <sub>EE</sub> = -4.2V			-1595	mV		
			V <sub>EE</sub> = -4.5V			-1610	mV		
			V <sub>EE</sub> = -4.8V			-1610	mV		
V <sub>OL</sub>	Low level output voltage	B <sub>n</sub> at 2.4V.	V <sub>EE</sub> = -4.2V	-1810		-1605	mV		
			V <sub>EE</sub> = -4.5V	-1810	-1705	-1620	mV		
			V <sub>EE</sub> = -4.8V	-1830		-1620	mV		
I <sub>IH</sub>	High level input current <sup>5</sup>	DIR, CE	One control input under test at V <sub>IHMAX</sub> , other control input at V <sub>ILMIN</sub> . A <sub>n</sub> and B <sub>n</sub> are open.			350	μA		
		A <sub>n</sub>	One A <sub>n</sub> under test at V <sub>IHMAX</sub> , all other A <sub>n</sub> at V <sub>ILMIN</sub> . CE and DIR at V <sub>IHMAX</sub> .			350	μA		
I <sub>IL</sub>	Low level input current for DIR and CE		One control input under test at V <sub>ILMIN</sub> , other control input at V <sub>IHMAX</sub> . A <sub>n</sub> and B <sub>n</sub> are open.			+0.5	μA		
I <sub>OZ</sub>	Off-state output current <sup>6</sup>		One A <sub>n</sub> under test at -2.1V, all other A <sub>n</sub> open. B <sub>n</sub> , CE and DIR at V <sub>ILMIN</sub> .			-50	50	μA	
-I <sub>EE</sub>	ECL supply current		CE at V <sub>IHMAX</sub> .			60	105	150	mA

## NOTES:

- The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
- Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
- The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
- The device can function down to V<sub>EE</sub> = -5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for extended V<sub>EE</sub> range. For more information, see Chapter 10, section 4.
- For bidirectional lines, this parameter includes output leakage current.
- This parameter includes input reverse leakage current.

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## DC ELECTRICAL CHARACTERISTICS FOR TTL-COMPATIBLE LINES

GND<sub>1</sub> = GND<sub>2</sub> = ground, V<sub>EE</sub> = -4.8V to -4.2V, V<sub>TTL</sub> = 4.5V to 5.5V, T<sub>A</sub> = 0°C to +85°C unless otherwise specified<sup>1,3</sup>

SYMBOL	PARAMETER	TEST CONDITIONS <sup>2</sup>	LIMITS			UNIT
			MIN.	TYP.	MAX.	
V <sub>OH</sub>	High level output voltage	A <sub>n</sub> at V <sub>ILMAX</sub> , DIR and CE at V <sub>IHMAX</sub> , I <sub>OH</sub> = -2.0mA.	2.4			V
V <sub>OL</sub>	Low level output voltage	A <sub>n</sub> at V <sub>IHMIN</sub> , DIR and CE at V <sub>IHMAX</sub> , I <sub>OL</sub> = +20mA.		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage	Apply -18mA to B <sub>n</sub> under test with other B <sub>n</sub> open. CE at V <sub>ILMIN</sub> .	-1.2	-0.73		V
I <sub>I</sub>	Input current at maximum input voltage <sup>4</sup>	B <sub>n</sub> under test at +5.5V, other B <sub>n</sub> at ground. CE at V <sub>ILMIN</sub> . V <sub>TTL</sub> at +5.5V.			1.0	mV
I <sub>IH</sub>	High level input current <sup>4</sup>	B <sub>n</sub> under test at +2.4V, other B <sub>n</sub> at ground. CE at V <sub>IHMAX</sub> . DIR at V <sub>ILMIN</sub> .			40	μA
-I <sub>IL</sub>	Low level input current <sup>4</sup>	B <sub>n</sub> under test at +0.4V, other B <sub>n</sub> at +2.4V. CE at V <sub>IHMAX</sub> . DIR at V <sub>ILMIN</sub> .			1.6	mA
I <sub>OZH</sub>	Off-state output current, High level voltage applied <sup>5</sup>	B <sub>n</sub> at +2.4V. A <sub>n</sub> at V <sub>ILMAX</sub> . CE at V <sub>ILMIN</sub> . DIR at V <sub>IHMAX</sub> .			40	μA
-I <sub>OZL</sub>	Off-state output current, Low level voltage applied <sup>5</sup>	B <sub>n</sub> at +0.4V. A <sub>n</sub> at V <sub>IHMIN</sub> . CE at V <sub>ILMIN</sub> . DIR at V <sub>IHMAX</sub> .			40	μA
-I <sub>OS</sub>	Short circuit output current <sup>6</sup>	A <sub>n</sub> at V <sub>ILMIN</sub> . One B <sub>n</sub> under test at ground. V <sub>TTL</sub> at +5.5V. DIR and CE at V <sub>IHMAX</sub> .	40		130	mA
I <sub>TTLH</sub>	TTL supply current with outputs High	All A <sub>n</sub> at V <sub>ILMIN</sub> . V <sub>TTL</sub> at +5.5V. All B <sub>n</sub> open. DIR and CE at V <sub>IHMAX</sub> .	25	35	44	mA
I <sub>TTL</sub>	TTL supply current with outputs Low	All A <sub>n</sub> at V <sub>IHMAX</sub> . V <sub>TTL</sub> at +5.5V. All B <sub>n</sub> open. CE and DIR at V <sub>IHMAX</sub> .	19	35	44	mA
I <sub>TTLZ</sub>	TTL supply current with outputs in the high impedance state	V <sub>TTL</sub> at +5.5V. All B <sub>n</sub> open. CE at V <sub>ILMIN</sub> .	25	44	48	mA

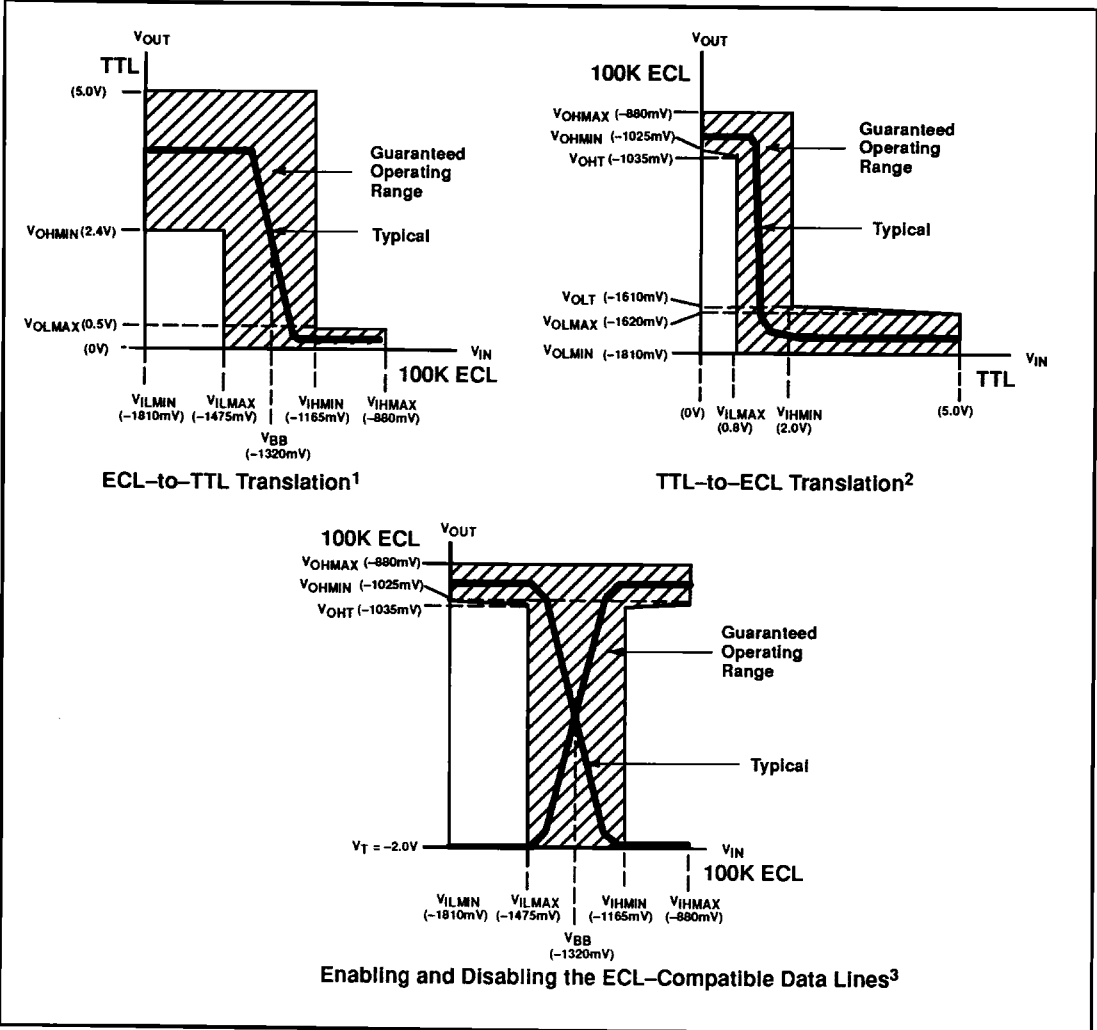
## NOTES:

- The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
- Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
- The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
- This parameter includes output leakage current.
- This parameter includes input reverse leakage current.
- Not more than one output should be shorted at a time. The other outputs should not be loaded. For testing I<sub>OS</sub>, the use of a high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

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## TRANSFER CHARACTERISTICS



**NOTES:**

1.  $V_{IN}$  is applied to  $A_n$  and  $V_{OUT}$  is measured at  $B_n$ .
2.  $V_{IN}$  is applied to  $B_n$  and  $V_{OUT}$  is measured at  $A_n$ .
3.  $V_{IN}$  is applied to DIR or CE and  $V_{OUT}$  is measured at  $A_n$ .

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## AC ELECTRICAL CHARACTERISTICS FOR TTL-TO-ECL DATA FLOW

Ceramic DIP  $GND_1 = GND_2 = \text{ground}$ ,  $V_{EE} = -5.7V$  to  $-4.2V$ ,  $V_{TTL} = 4.5V$  to  $5.5V$ .

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}$ $t_{PHL}$	Propagation delay $B_n$ to $A_n$	Waveform 1	1.00	4.00	1.00	4.00	1.00	4.00	ns
$t_{PZH}$	Output enable time CE, DIR to $A_n$	Waveform 2	4.00	8.00	4.00	8.00	4.00	8.00	ns
$t_{PHZ}$	Output disable time CE, DIR to $A_n$	Waveform 2	1.50	4.00	1.50	4.00	1.50	4.00	ns
$t_{TLH}$ $t_{THL}$	Transition time for $A_n$	Waveform 1	1.00	2.50	1.00	2.50	1.00	2.50	ns

**NOTE:**

For AC test setup information, see AC Testing, Chapter 2, Section 3.

## AC ELECTRICAL CHARACTERISTICS FOR ECL-TO-TTL DATA FLOW

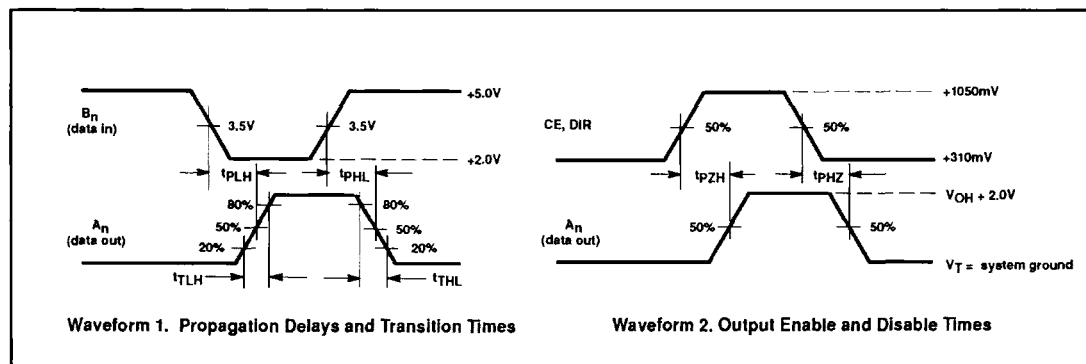
Ceramic DIP  $GND_1 = GND_2 = \text{ground}$ ,  $V_{EE} = -5.7V$  to  $-4.2V$ ,  $V_{TTL} = 4.5V$  to  $5.5V$ .

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}$ $t_{PHL}$	Propagation delay $A_n$ to $B_n$	Waveform 3		4.50		4.50		4.50	ns
$t_{PZH}$ $t_{PZL}$	Output enable time CE, DIR to $B_n$	Waveform 4		7.00		7.00		7.00	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time CE, DIR to $B_n$	Waveform 4		3.00		3.00		3.00	ns
$t_{TLH}$ $t_{THL}$	Transition time for $B_n$	Waveform 3	1.00	3.50	1.00	3.50	1.00	3.50	ns

**NOTE:**

For AC test setup information, see AC Testing, Chapter 2, Section 3.

## AC WAVEFORMS FOR TTL-TO-ECL DATA FLOW



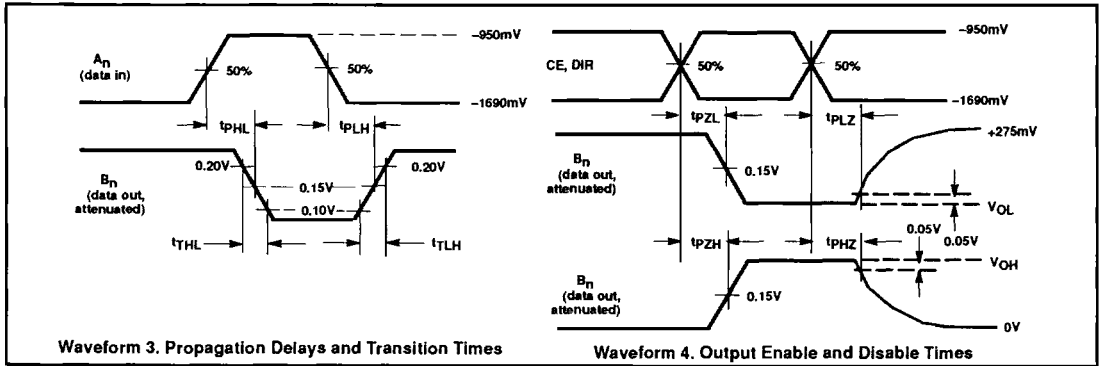
**NOTE:**

All power and signal voltages shifted up 2.0V for AC bench test purposes.

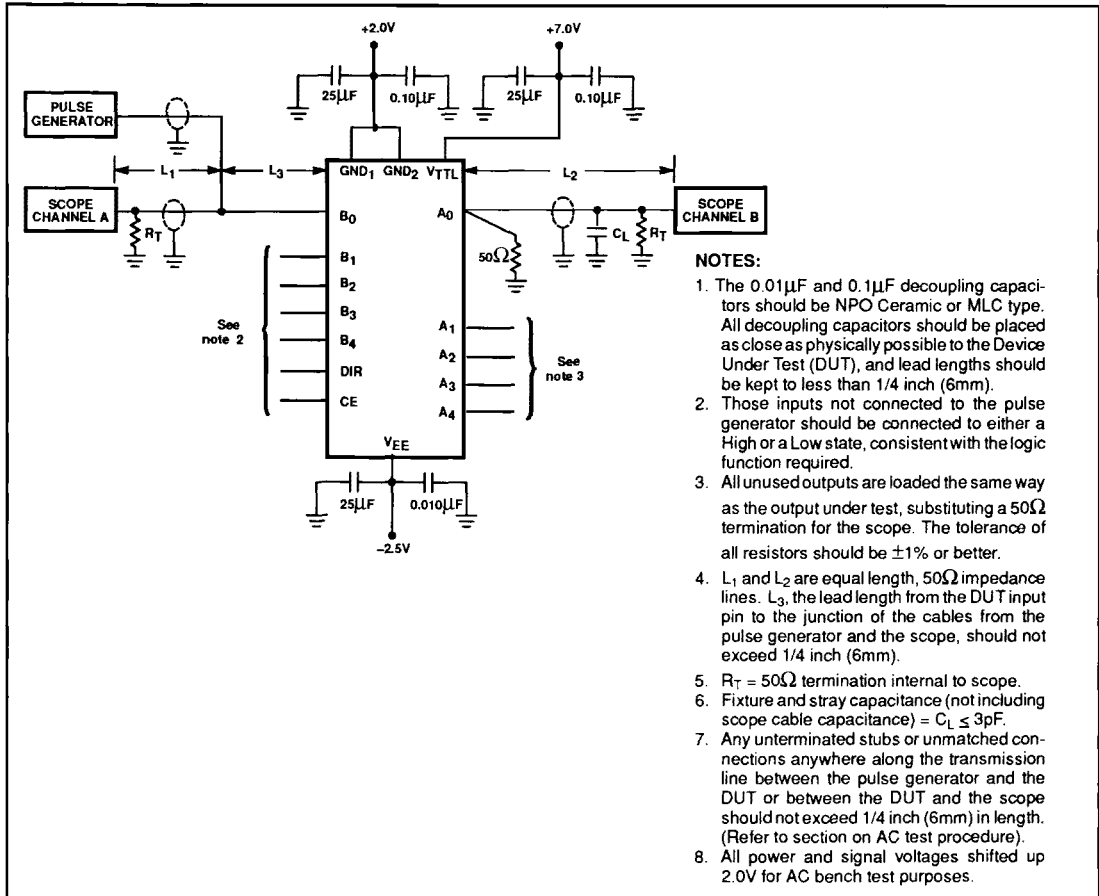
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## AC WAVEFORMS FOR ECL-TO-TTL DATA FLOW



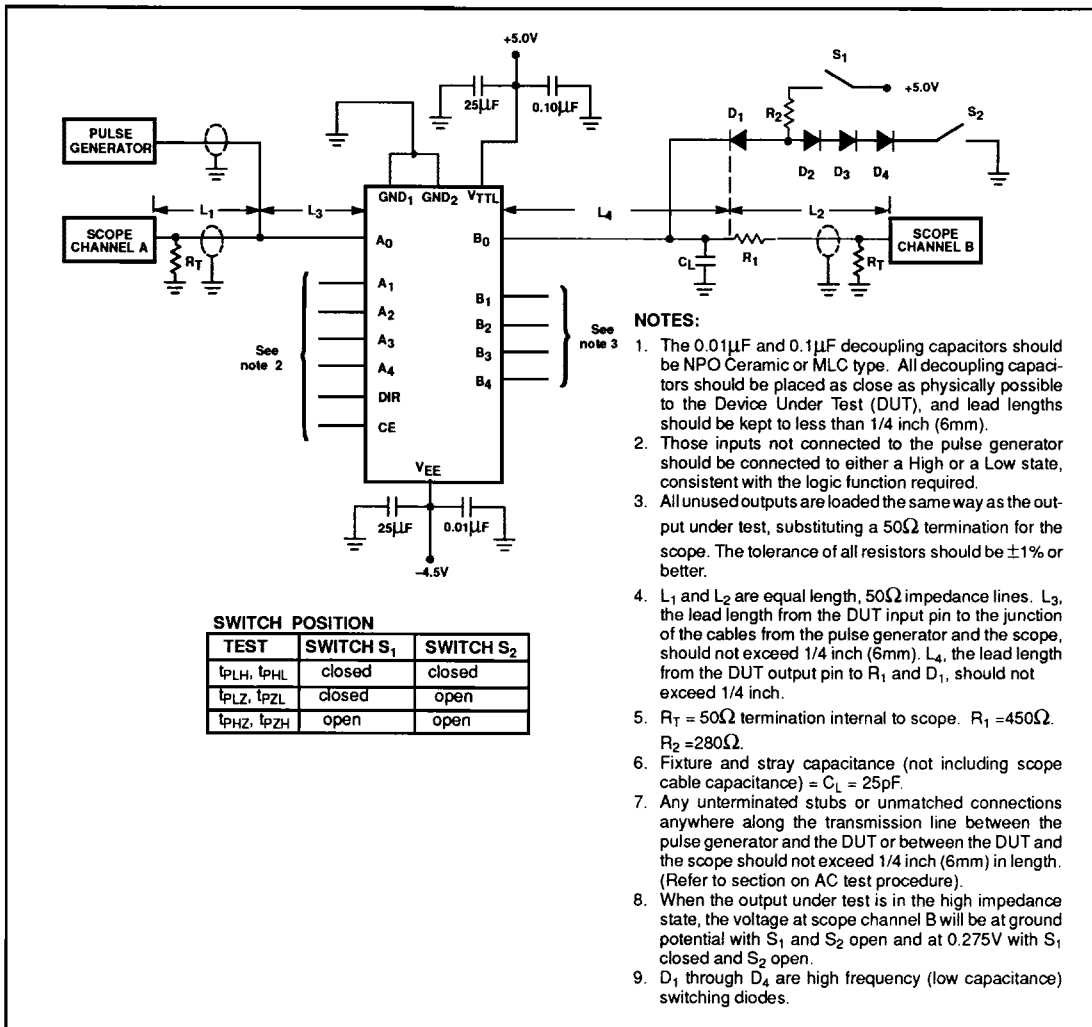
## AC TEST CIRCUIT FOR TTL-TO-ECL DATA FLOW



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## AC TEST CIRCUIT FOR ECL-TO-TTL DATA FLOW



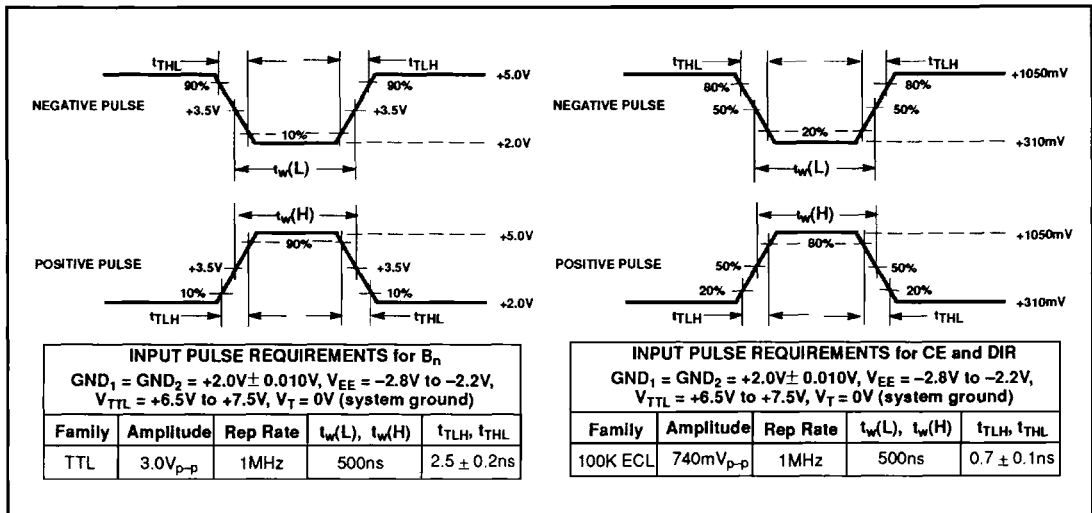
**SWITCH POSITION**

TEST	SWITCH S <sub>1</sub>	SWITCH S <sub>2</sub>
t <sub>PLH</sub> , t <sub>PHL</sub>	closed	closed
t <sub>PZL</sub> , t <sub>PZH</sub>	closed	open
t <sub>PHZ</sub> , t <sub>PZH</sub>	open	open

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## INPUT PULSE DEFINITION FOR TTL-TO-ECL DATA FLOW



**NOTE:**  
 All power and signal voltages shifted up 2.0V for AC bench test purposes.

## INPUT PULSE DEFINITION FOR ECL-TO-TTL DATA FLOW

