Preliminary **32Mx64 Two Bank Unbuffered DDR SDRAM Module**

Features

- 184-Pin Unbuffered 8-Byte Dual In-Line Memory Module
- 32Mx64 Double Data Rate (DDR) SDRAM DIMM (16M x 8 SDRAMs)
- Performance:

		PC1600	PC2100	Units
DIMM $\overline{CAS}$ Latency		2	2.5	
f_{CK}	Clock Frequency	100	133	MHz
t_{CK}	Clock Cycle	10	7.5	ns
f_{DQ}	DQ Burst Frequency	200	266	MHz

- Intended for 100 MHz and 133 MHz applications
- Inputs and outputs are SSTL-2 compatible
- V_{DD} = 2.5Volt ± 0.2, V_{DDQ} = 2.5Volt ± 0.2
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have four internal banks for concurrent operation
- Module has two physical banks
- DRAM D_{LL} aligns DQ and DQS transitions with clock transitions. Also aligns $\overline{QFC}$ transitions with clock during Read cycles
- Differential clock inputs
- Data is read or written on both clock edges
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 2, 2.5
  - Burst Type: Sequential or Interleave
  - Burst Length: 2, 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 12/10/2 Addressing (row/column/bank)
- 15.6 µs Max. Average Periodic Refresh Interval
- Card size: 5.25" x 0.157" x 1.25"
- Gold contacts
- SDRAMs in 66-pin TSOP-II Package
- Serial Presence Detect

Description

IBMB6N32644JGA is an unbuffered 184-Pin Double Data Rate (DDR) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as a two-bank high-speed memory array. The 32Mx64 module is a dual-bank DIMM that uses sixteen 16Mx8 DDR SDRAMs in 400 mil TSOP packages. The DIMM achieves high-speed data transfer rates of up to 266 MHz.

The DIMM is intended for use in applications operating from 100 MHz to 133 MHz clock speeds with data rates of 200 to 266 MHz.

Clock enables CKE0 and/or CKE1 control all devices on the DIMM.

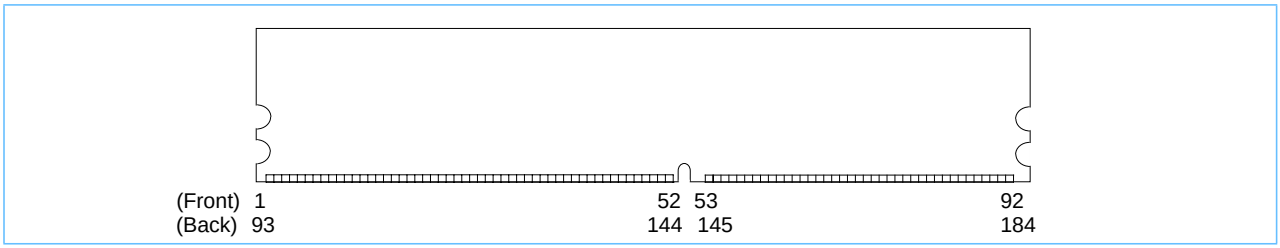
Prior to any access operation, the device $\overline{CAS}$ latency and burst type/length/operation type must be programmed into the DIMM by address inputs A0-A11 and I/O inputs BA0 and BA1 using the mode register set cycle.

These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The last 128 bytes are available to the customer.

All IBM 184 DDR SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25” long space-saving footprint.

Card Outline



Pin Description

CK0, $\overline{CK}$0 CK1,$\overline{CK}$1 CK2, $\overline{CK}$2	Differential Clock Inputs	DQ0 - DQ63	Data Input/Output
CKE0, CKE1	Clock Enables	DQS0-DQS7, DQS9-DQS16	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	V_{DD}	Power (2.5V)
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Supply voltage for DQs (2.5V)
$\overline{WE}$	Write Enable	V_{SS}	Ground
$\overline{S}$0, $\overline{S}$1	Chip Selects	NC	No Connect
A0 - A9, A11	Address Inputs	SCL	Serial Presence Detect Clock Input
A10/AP	Address Input/Autoprecharge	SDA	Serial Presence Detect Data Input/Output
BA0, BA1	SDRAM Bank Address Inputs	SA0-SA2	Serial Presence Detect Address Inputs
V_{REF}	Ref. Voltage for SSTL_2 inputs	V_{DDSPD}	Serial EEPROM positive power supply (2.5 V)

184-Pin DDR SDRAM DIMM Pin Assignments

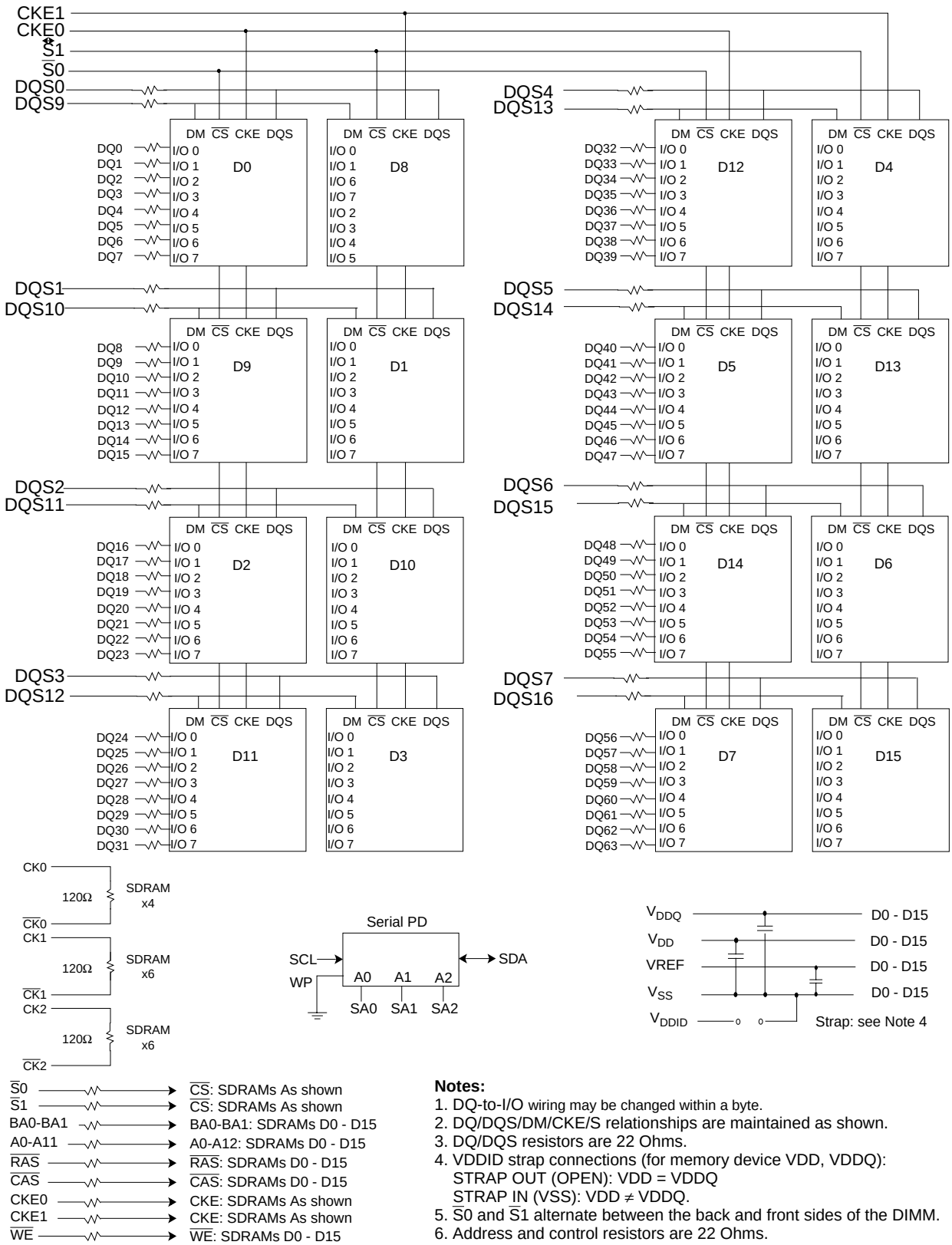
Front Side (left side 1 - 52, right side 53 - 92)		Back Side (left side 93-144, right side 145-184)		Front Side (left side 1 - 52, right side 53 - 92)		Back Side (left side 93 -144, right side 145 -184)	
Pin #	x64 Non-Parity	Pin #	x64 Non-Parity	Pin #	x64 Non-Parity	Pin #	x64 Non-Parity
1	VREF	93	VSS	48	A0	140	NC
2	DQ0	94	DQ4	49	NC	141	A10
3	VSS	95	DQ5	50	VSS	142	NC
4	DQ1	96	VDDQ	51	NC	143	VDDQ
5	DQS0	97	DQS9	52	BA1	144	NC
6	DQ2	98	DQ6	KEY		KEY	
7	VDD	99	DQ7	53	DQ32	145	VSS
8	DQ3	100	VSS	54	VDDQ	146	DQ36
9	NC	101	NC	55	DQ33	147	DQ37
10	$\overline{\text{RESET}}$	102	NC	56	DQS4	148	VDD
11	VSS	103	NC	57	DQ34	149	DQS13
12	DQ8	104	VDDQ	58	VSS	150	DQ38
13	DQ9	105	DQ12	59	BA0	151	DQ39
14	DQS1	106	DQ13	60	DQ35	152	VSS
15	VDDQ	107	DQS10	61	DQ40	153	DQ44
16	CK1	108	VDD	62	VDDQ	154	$\overline{\text{RAS}}$
17	$\overline{\text{CK1}}$	109	DQ14	63	$\overline{\text{WE}}$	155	DQ45
18	VSS	110	DQ15	64	DQ41	156	VDDQ
19	DQ10	111	CKE1	65	$\overline{\text{CAS}}$	157	$\overline{\text{S}}$0
20	DQ11	112	VDDQ	66	VSS	158	$\overline{\text{S}}$1
21	CKE0	113	NC	67	DQS5	159	DQS14
22	VDDQ	114	DQ20	68	DQ42	160	VSS
23	DQ16	115	NC	69	DQ43	161	DQ46
24	DQ17	116	VSS	70	VDD	162	DQ47
25	DQS2	117	DQ21	71	NC	163	NC
26	VSS	118	A11	72	DQ48	164	VDDQ
27	A9	119	DQS11	73	DQ49	165	DQ52
28	DQ18	120	VDD	74	VSS	166	DQ53
29	A7	121	DQ22	75	$\overline{\text{CK2}}$	167	NC
30	VDDQ	122	A8	76	CK2	168	VDD
31	DQ19	123	DQ23	77	VDDQ	169	DQS15
32	A5	124	VSS	78	DQS6	170	DQ54
33	DQ24	125	A6	79	DQ50	171	DQ55
34	VSS	126	DQ28	80	DQ51	172	VDDQ
35	DQ25	127	DQ29	81	VSS	173	NC
36	DQS3	128	VDDQ	82	VDDID	174	DQ60
37	A4	129	DQS12	83	DQ56	175	DQ61
38	VDD	130	A3	84	DQ57	176	VSS
39	DQ26	131	DQ30	85	VDD	177	DQS16
40	DQ27	132	VSS	86	DQS7	178	DQ62
41	A2	133	DQ31	87	DQ58	179	DQ63
42	VSS	134	NC	88	DQ59	180	VDDQ
43	A1	135	NC	89	VSS	181	SA0
44	NC	136	VDDQ	90	NC	182	SA1
45	NC	137	CK0	91	SDA	183	SA2
46	VDD	138	$\overline{\text{CK0}}$	92	SCL	184	VDDSPD
47	NC	139	VSS				

NC = No Connect; NU = Not Useable; DU = Do Not Use

Ordering Information

Part Number	Organization	Speed	SDRAM CAS Latency	Leads	Dimension	Power V_{DD}/V_{DDQ}
IBMB6N32644JGA - 8NT	32Mx64	PC1600	2	Gold	5.25" x 1.25" x 0.157"	2.5 V/2.5 V
IBMB6N32644JGA - 75NT		PC2100	2.5			

x64 Non-Parity DDR Unbuffered SDRAM DIMM Block Diagram (2 Banks, x8 DDR SDRAMs)



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS resistors are 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD ≠ VDDQ.
5. S0 and S1 alternate between the back and front sides of the DIMM.
6. Address and control resistors are 22 Ohms.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK}$0, $\overline{CK}$1, $\overline{CK}$2	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CK low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S}$0, $\overline{S}$1	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0,1	(SSTL)	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11, A10/AP	(SSTL)	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63	(SSTL)	—	Data Input/Output pins.
DQS0 - DQS7 DQS9 - DQS16	(SSTL)	—	Data strobes: Output with read data, input with write data. Edge aligned with read data, centered on write data. Used to capture write data.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
SA0 - 2		—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Serial Presence Detect (Part 1 of 2)

Byte #	Description		SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production		128	80	
1	Total number of bytes in Serial PD Device		256	08	
2	Fundamental Memory Type		SDRAM DDR	07	
3	Number of Row Addresses on Assembly		12	0C	
4	Number of Column Addresses on Assembly		10	0A	
5	Number of Physical Banks on DIMM		2	02	
6-7	Data Width of Assembly		x64	4000	
8	Voltage Interface Level of this Assembly		SSTL 2.5V	04	
9	SDRAM Device Cycle Time at CLX (CL = 2.5)	PC1600	8.0ns	80	
		PC2100	7.5ns	75	
10	SDRAM Device Access Time from Clock at CL = 2.5	PC1600	0.8ns	80	
		PC2100	0.75ns	75	
11	DIMM Configuration Type		Non-parity	00	
12	Refresh Rate/Type		15.625 µs/SR	80	
13	Primary SDRAM Device Width		x8	08	
14	Error Checking SDRAM Device Width		N/A	00	
15	SDRAM Device Attributes: Minimum Clock Delay, Random Column Access		1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported		2, 4, 8	0E	
17	SDRAM Device Attributes: Number of Device Banks		4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latencies supported		2, 2.5	0C	
19	SDRAM Device Attributes: $\overline{CS}$ Latency		0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency		1	02	
21	SDRAM Module Attributes		Unbuffered, Differential Clock	20	
22	SDRAM Device Attributes: General		AP, $V_{DD} \pm 0.2V$	80	
23	Minimum Clock Cycle at CLX-0.5 (CL = 2)	PC1600	10.0ns	A0	
		PC2100	8.0ns	80	
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-0.5 (CL = 2)	PC1600	$\pm$ 0.8ns	80	
		PC2100	$\pm$ 0.75ns	75	
25	Minimum Clock Cycle Time at CLX-1 (CL = 1.5)		N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 1.5)		N/A	00	
27	Minimum Row Precharge Time (t_{RP})		20.0ns	50	
28	Minimum Row Active to Row Active Delay (t_{RRD})		15.0ns	3C	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD})		20.0ns	50	
30	Minimum Active to Precharge Time (t_{RAS})	PC1600	50.0ns	32	
		PC2100	45.0ns	2D	
31	Module Bank Density - 16Mx64		128MB	20	

1. Setup and hold values assume a 1 Volt/ns slew rate.
2. cc = Checksum Data byte, 00-FF (Hex).
3. “MM” = Alphanumeric revision code, A-Z, 0-9.
4. mm = ASCII coded revision code byte “MM”.
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).

Serial Presence Detect (Part 2 of 2)

Byte #	Description		SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
32	Address and Command Setup Time before Clock	PC1600	1.1ns	B0	1
		PC2100	0.9ns	90	
33	Address and Command Hold Time after Clock	PC1600	1.1ns	B0	
		PC2100	0.9ns	90	
34	Data/Data Mask Input Setup Time before Clock	PC1600	0.6ns	60	
		PC2100	0.5ns	50	
35	Data/Data Mask Input Hold Time after Clock	PC1600	0.6ns	60	
		PC2100	0.5ns	50	
36-40	Reserved for VCSDRAM		Undefined	00	
41	Minimum Active/Auto Refresh Time (t_{RC})	PC1600	70	46	
		PC2100	65	41	
42-61	Reserved		Undefined	00	
62	SPD Revision		0	00	
63	Checksum for Bytes 0 - 62		Checksum Data	cc	2
64-71	Manufacturers' JEDEC ID Code		IBM	A400000000000000	
72	Module Manufacturing Location		MM	mm	3, 4
73-90	Module Part Number	PC1600	ASCII 'B6N32644JGA -8NT'	42364E33223634344A4741 2D384E54202020	
		PC2100	ASCII 'B6N32644JGA -75NT'	42364E33223634344A4741 2D37354E542020	
91-92	Module Revision Code		'A' plus ASCII blank	4120	
93-94	Module Manufacturing Date		Year/Week Code	yyww	5, 6
95-98	Module Serial Number		Serial Number	ssssssss	7
99-127	Reserved		Undefined	00	
128-255	Open for Customer Use		Undefined	00	

1. Setup and hold values assume a 1 Volt/ns slew rate.
2. cc = Checksum Data byte, 00-FF (Hex).
3. "MM" = Alphanumeric revision code, A-Z, 0-9.
4. mm = ASCII coded revision code byte "MM".
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).

Absolute Maximum Ratings

Symbol	Parameter		Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}		−0.5 to V_{DDQ}+ 0.5	V
V_{IN}	Voltage on Inputs relative to V_{SS}	SDRAM device	−0.5 to +3.6	V
		Serial PD device	-0.3 to +6.5	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}		−0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}		−0.5 to +3.6	V
V_{DDSPD}	Voltage on V_{DDSPD} supply relative to V_{SS}		−0.3 to +5.5	V
T_A	Operating Temperature (Ambient)		0 to +70	°C
T_{STG}	Storage Temperature (Plastic)		−55 to +150	°C
P_D	Power Dissipation		TBD	W
I_{OUT}	Short Circuit Output Current		50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Max.	Units	Notes
Input Capacitance: CK0, $\overline{CK}$0, CK1, $\overline{CK}$1, CK2, $\overline{CK}$2	C_{I1}	24	pF	1
Input Capacitance: A0-A11, BA0, BA1, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$	C_{I2}	60	pF	1
Input Capacitance: CKE0, CKE1, $\overline{S}$0, $\overline{S}$1	C_{I5}	30	pF	1
Input Capacitance: SA0-SA2, SCL	C_{I4}	9	pF	1
Input/Output Capacitance DQ0-63; DQS0-7, 9-16	C_{IO1}	14	pF	1, 2
Input/Output Capacitance: SDA	C_{IO3}	11	pF	

1. V_{DDQ} = V_{DD} = 2.5V 0.2V, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = $V_{DDQ/2}$, V_{OUT} (Peak to Peak) = 0.2V.
2. DQS inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

Electrical Characteristics and DC Operating Conditions

($0^{\circ}C \leq T_A \leq 70^{\circ}C$; V_{DDQ} = 2.5V ± 0.2V, V_{DD} = + 2.5V ± 0.2V, see AC Characteristics)

Symbol	Parameter		Min	Max	Units	Notes
V_{DD}	Supply Voltage		2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage		2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage I/O Supply Voltage		0	0	V	
V_{REF}	I/O Reference Voltage		1.15	1.35	V	1, 2
V_{TT}	I/O Termination Voltage (System)		V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
V_{DDSPD}	Supply Voltage SPD Supply Voltage		2.3	2.7	V	
$V_{IH(DC)}$	Input High (Logic1) Voltage		V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL(DC)}$	Input Low (Logic0) Voltage		– 0.3	V_{REF} – 0.15	V	1
$V_{IN(DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs		– 0.3	V_{DDQ} + 0.3	V	1
$V_{ID(DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs		0.00	V_{DDQ} + 0.6	V	1, 4
I_I	Input Leakage Current Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	Address and control inputs	– 64	64	µA	1
		DQ0-63; DQS0-7, 9-16	– 10	10		
		CK0, $\overline{CK}$0 CK1, $\overline{CK}$1 CK2, $\overline{CK}$2	– 30	30		
I_{OZ}	Output Leakage Current (DQs are disabled; 0V ≤ V_{out} ≤ V_{DDQ}	DQ0-63; DQS0-7, 9-16	– 10	10	µA	1
		SDA	– 1	1		
I_{OH}	Output High Current (V_{OUT} = V_{DDQ} -0.373V, min V_{REF}, min V_{TT})		– 16.8		mA	1
I_{OL}	Output Low Current (V_{OUT} = 0.373, max V_{REF}, max V_{TT})		16.8		mA	1

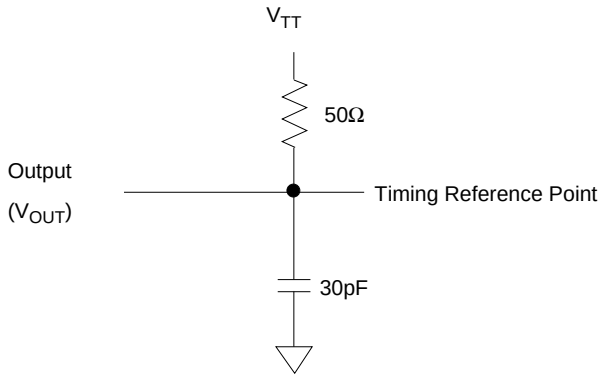
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$ unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuit Diagram



AC Operating Conditions ($0\,^{\circ}C \le T_A \le 70\,^{\circ}C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$, See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage.	V_{REF} + 0.31		V	1, 2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage.		V_{REF} – 0.31	V	1, 2
$V_{ID(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX(AC)}$	Input Differential Pair Cross Point Voltage, CK and $\overline{CK}$ Inputs	(0.5*V_{DDQ}) – 0.2	(0.5*V_{DDQ}) + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents ($0\,^{\circ}C \le T_A \le 70\,^{\circ}C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$, See AC Characteristics)

Symbol	Parameter/Condition	PC1600 t_{CK} = 10ns	PC2100 t_{CK} = 7.5ns	Unit	Notes
I_{DD0}	**Operating Current**: one bank; active / precharge; $t_{RC} = t_{RC\ MIN}$; $t_{CK} = t_{CK\ MIN}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1000	116	mA	1, 2, 5
I_{DD1}	**Operating Current**: one bank; active / read / precharge; Burst = 2; $t_{RC} = t_{RC\ MIN}$; CL = 2.5; $t_{CK} = t_{CK\ MIN}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	1120	1360	mA	1, 2, 5
I_{DD2P}	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; $CKE \le V_{IL\ MAX}$; $t_{CK} = t_{CK\ MIN}$	240	240	mA	1, 2
I_{DD2N}	**Idle Standby Current:** $\overline{CS} \ge V_{IH\ MIN}$; all banks idle; $CKE \ge V_{IH\ MIN}$; $t_{CK} = t_{CK\ MIN}$; address and control inputs changing once per clock cycle	480	560	mA	1, 2
I_{DD3P}	**Active Power-Down Standby Current**: one bank active; power-down mode; $CKE \le V_{IL\ MAX}$; $t_{CK} = t_{CK\ MIN}$	240	240	mA	1, 2
I_{DD3N}	**Active Standby Current**: one bank; active / precharge; $\overline{CS} \ge V_{IH\ MIN}$; $CKE \ge V_{IH\ MIN}$; $t_{RC} = t_{RAS\ MAX}$; $t_{CK} = t_{CK\ MIN}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	800	960	mA	1, 2
I_{DD4R}	**Operating Current:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; $t_{CK} = t_{CK\ MIN}$; I_{OUT} = 0mA	1640	1800	mA	1, 2, 5
I_{DD4W}	**Operating Current**: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2.5; $t_{CK} = t_{CK\ MIN}$	1320	1680	mA	1, 2, 5
I_{DD5}	**Auto-Refresh Current**: $t_{RC} = t_{RFC\ MIN}$	1840	2400	mA	1, 2, 4
	t_{RC} = 15.625 µs	252	252		
I_{DD6}	**Self-Refresh Current**: $CKE \le 0.2V$	32	32	mA	1, 2, 3

1. I_{DD} specifications are tested after the device is properly initialized.
2. Input slew rate = 1V/ns.
3. Enables on-chip refresh and address counters.
4. Current at 15.625 µs is time averaged value of I_{DD5} at $t_{RFC\ MIN}$ and I_{DD2P} over 15.625 µs.
5. One bank in mode shown; second bank in Active Standby.

AC Timing Specifications for DDR SDRAM Devices Used on Module

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter		PC 2100		PC 1600		Unit	Notes
			Min	Max	Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1, 2, 3, 4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1, 2, 3, 4
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	t_{CK}	1, 2, 3, 4
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	t_{CK}	1, 2, 3, 4
t_{CK}	Clock cycle time	CL = 2.5	7.5	12	8	12	ns	1, 2, 3, 4
t_{CK}		CL = 2.0	8	12	10	12	ns	1, 2, 3, 4
t_{DH}	DQ and DM input hold time		0.5		0.6		ns	1, 2, 3, 4, 18, 19
t_{DS}	DQ and DM input setup time		0.5		0.6		ns	1, 2, 3, 4, 18, 19
t_{DIPW}	DQ and DM input pulse width (each input)		1.75		2		ns	1, 2, 3, 4
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1, 2, 3, 4, 5
t_{LZ}	Data-out low-impedance time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1, 2, 3, 4, 5
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)			+ 0.5		+ 0.6	ns	1, 2, 3, 4
t_{DQSQA}	DQS-DQ skew (DQS & all DQ signals)			+ 0.5		+ 0.6	ns	1, 2, 3, 4
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time		t_{CH} or t_{CL}		t_{CH} or t_{CL}		t_{CK}	1, 2, 3, 4
t_{QH}	Data output hold time from DQS		t_{HP}- 0.75ns		t_{HP}- 1.0ns		t_{CK}	1, 2, 3, 4
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	t_{CK}	1, 2, 3, 4
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35		0.35		t_{CK}	1, 2, 3, 4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		t_{CK}	1, 2, 3, 4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		t_{CK}	1, 2, 3, 4
t_{MRD}	Mode register set command cycle time		15		16		ns	1, 2, 3, 4
t_{WPRES}	Write preamble setup time		0		0		ns	1, 2, 3, 4, 7
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	t_{CK}	1, 2, 3, 4, 6
t_{WPRE}	Write preamble		0.25		0.25		t_{CK}	1, 2, 3, 4
t_{IH}	Address and control input hold time (fast slew rate)		0.9		1.1		ns	2, 3, 4, 11, 13, 14
t_{IS}	Address and control input setup time (fast slew rate)		0.9		1.1		ns	2, 3, 4, 11, 13, 14
t_{IH}	Address and control input hold time (slow slew rate)		1.0		1.1		ns	2, 3, 4, 12, 13, 14, 17

AC Timing Specifications for DDR SDRAM Devices Used on Module

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	PC 2100		PC 1600		Unit	Notes
		Min	Max	Min	Max		
t_{IS}	Address and control input setup time (slow slew rate)	1.0		1.1		ns	2, 3, 4, 12, 13, 14, 17
t_{IPW}	Input pulse width	2.2				ns	2, 3, 4, 14
t_{RPRE}	Read preamble	0.9	1.1	0.9	1.1	t_{CK}	1, 2, 3, 4
t_{RPST}	Read postamble	0.40	0.60	0.40	0.60	t_{CK}	1, 2, 3, 4
t_{RAS}	Active to Precharge command	45	120,000	50	120,000	ns	1, 2, 3, 4
t_{RC}	Active to Active/Auto-refresh command period	65		70		ns	1, 2, 3, 4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	75		80		ns	1, 2, 3, 4
t_{RCD}	Active to Read or Write delay	20		20		ns	1, 2, 3, 4
t_{RAP}	Active to Read Command with Autoprecharge	20		20		ns	1, 2, 3, 4
t_{RP}	Precharge command period	20		20		ns	1, 2, 3, 4
t_{RRD}	Active bank A to Active bank B command	15		15		ns	1, 2, 3, 4
t_{WR}	Write recovery time	15		15		ns	1, 2, 3, 4
t_{DAL}	Auto precharge write recovery + precharge time	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}	1, 2, 3, 4, 16
t_{WTR}	Internal write to read command delay	1		1		t_{CK}	1, 2, 3, 4
t_{XSNR}	Exit self-refresh to non-read command	75		80		ns	1, 2, 3, 4
t_{XSRD}	Exit self-refresh to read command	200		200		t_{CK}	1, 2, 3, 4
t_{REFI}	Average Periodic Refresh Interval		15.6		15.6	µs	1, 2, 3, 4, 8
t_{QCS}	$\overline{QFC}$ setup time on Read	0.9	1.1	0.9	1.1	t_{CK}	1, 2, 3, 4, 15
t_{QCH}	$\overline{QFC}$ hold time on Read	0.4	0.6	0.4	0.6	t_{CK}	1, 2, 3, 4, 15
t_{QCSW}	Delay from CK edge of write command to $\overline{QFC}$ low on write		4.0		4.0	ns	1, 2, 3, 4, 9, 15
t_{QCHW}	$\overline{QFC}$ hold time on write	1.25	2.0	1.25	2.0	ns	1, 2, 3, 4, 10, 15

AC Timing Specification Notes

1. Input slew rate = 1V/ns.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on t_{DQSS}.
8. A maximum of eight Auto refresh commands can be posted to any given DDR SDRAM device.
9. $\overline{QFC}$ is enabled as soon as possible after the rising CK edge that registers the Write command.
10. $\overline{QFC}$ is disabled as soon as possible after the last valid DQS edge transitions Low.
11. For command/address input slew rate ≥ 1.0 V/ns. Slew rate is measured between V_{OH}(AC) and V_{OL}(AC).
12. For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns. Slew rate is measured between V_{OH}(AC) and V_{OL}(AC).
13. CK/$\overline{CK}$ slew rates are ≥ 1.0 V/ns.
14. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
15. The specified timing is guaranteed, assuming $\overline{QFC}$ is connected to a test load consisting of 20 pF to ground and a pull up resistor of 150 ohms to V_{ddq}.
16. For each of the terms in parentheses, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time. For example, for PC2100 at CL = 2.5, t_{DAL} = (15ns/7.5ns) + (20ns/7.0ns) = 2 + 3 = 5.

(Notes continue on the following page).

17. An input setup and hold time derating table is used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	Δt_{IS}	Δt_{IH}	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+ 50	0	ps	1, 2
0.3 V/ns	+ 100	0	ps	1, 2

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

18. An input setup and hold time derating table is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	Δt_{DS}	Δt_{DH}	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+ 75	+ 75	ps	1, 2
0.3 V/ns	+ 150	+ 150	ps	1, 2

1. I/O slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

19. An I/O Delta Rise, Fall Derating table is used to increase t_{DS} and t_{DH} in the case where DQ, DM, and DQS slew rates differ.

Delta Rise and Fall Rate	Δt_{DS}	Δt_{DH}	Unit	Note
0.0 ns/V	0	0	ps	1, 2, 3, 4
0.25 ns/V	+ 50	+ 50	ps	1, 2, 3, 4
0.5 ns/V	+ 100	+ 100	ps	1, 2, 3, 4

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: [1/(slew rate 1)] - [1/(slew rate 2)]
   For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns
   Delta rise, fall = (1/0.5) - (1/0.4) [ns/V]
   = -0.5 ns/V
   Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

AC Timing for PC2100 - Applicable Specifications Expressed in Clock Cycles

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter	PC2100 @ CL = 2.5		Units	Notes
		Min	Max		
t_{MRD}	Mode register set command cycle time	2		t_{CK}	1, 2, 3, 4
t_{WPRE}	Write preamble	0.25		t_{CK}	1, 2, 3, 4
t_{RAS}	Active to Precharge command	6	16000	t_{CK}	1, 2, 3, 4
t_{RC}	Active to Active/Auto-refresh command period	9		t_{CK}	1, 2, 3, 4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	10		t_{CK}	1, 2, 3, 4
t_{RCD}	Active to Read or Write delay	3		t_{CK}	1, 2, 3, 4
t_{RAP}	Active to Read Command with Autoprecharge	3		t_{CK}	1, 2, 3, 4
t_{RP}	Precharge command period	3		t_{CK}	1, 2, 3, 4
t_{RRD}	Active bank A to Active bank B command	2		t_{CK}	1, 2, 3, 4
t_{WR}	Write recovery time	2		t_{CK}	1, 2, 3, 4
t_{DAL}	Auto precharge write recovery + precharge time	5		t_{CK}	1, 2, 3, 4, 5
t_{WTR}	Internal write to read command delay	1		t_{CK}	1, 2, 3, 4
t_{XSNR}	Exit self-refresh to non-read command	10		t_{CK}	1, 2, 3, 4
t_{XSRD}	Exit self-refresh to read command	200		t_{CK}	1, 2, 3, 4

1. Input slew rate = 1V/ns.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

Serial Presence Detect EEPROM DC Operating Conditions[1] (V_{DD} = +3.3V ±0.3V)

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply voltage	3	3.6	V
V_{IH}	Input High voltage: Logic 1; all inputs	V_{DD} x 0.7	V_{DD} + 0.5	V
V_{IL}	Input Low voltage: Logic 0; all inputs	-1	V_{DD} x 0.3	V
V_{OL}	Output Low voltage: I_{OUT} = 3mA	—	0.4	V
I_{LI}	Input leakage current: V_{IN} = GND to V_{DD}	—	10	µA
I_{LO}	Output leakage current: V_{OUT} = GND to V_{DD}	—	10	µA
I_{SB}	Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	—	30	µA
I_{CC}	Power supply current: SCL clock frequency = 100 KHz	—	2	mA

1. All voltages referenced to V_{SS}.

Serial Presence Detect EEPROM AC Operating Conditions[1] (V_{DD} = +3.3V ±0.3V)

Symbol	Parameter	Min	Max	Units	Notes
^{t}AA	SCL LOW to SDA data-out valid	0.3	3.5	µs	
^{t}BUF	Time the bus must be free before a new transition can start	4.7		µs	
^{t}DH	Data-out hold time	300		ns	
^{t}F	SDA and SCL fall time		300	ns	
$^{t}HD:DAT$	Data-in hold time	0		µs	
$^{t}HD:STA$	Start condition hold time	4		µs	
$^{t}HIGH$	Clock HIGH period	4		µs	
^{t}I	Noise suppression time constant at SCL, SDA inputs		100	ns	
^{t}LOW	Clock LOW period	4.7		µs	
^{t}R	SDA and SCL rise time		1	µs	
^{t}SCL	SCL clock frequency		100	KHz	
$^{t}SU:DAT$	Data-in setup time	250		ns	
$^{t}SU:STA$	Start condition setup time	4.7		µs	
$^{t}SU:STO$	Stop condition setup time	4.7		µs	
^{t}WRC	WRITE cycle time		10	ms	2

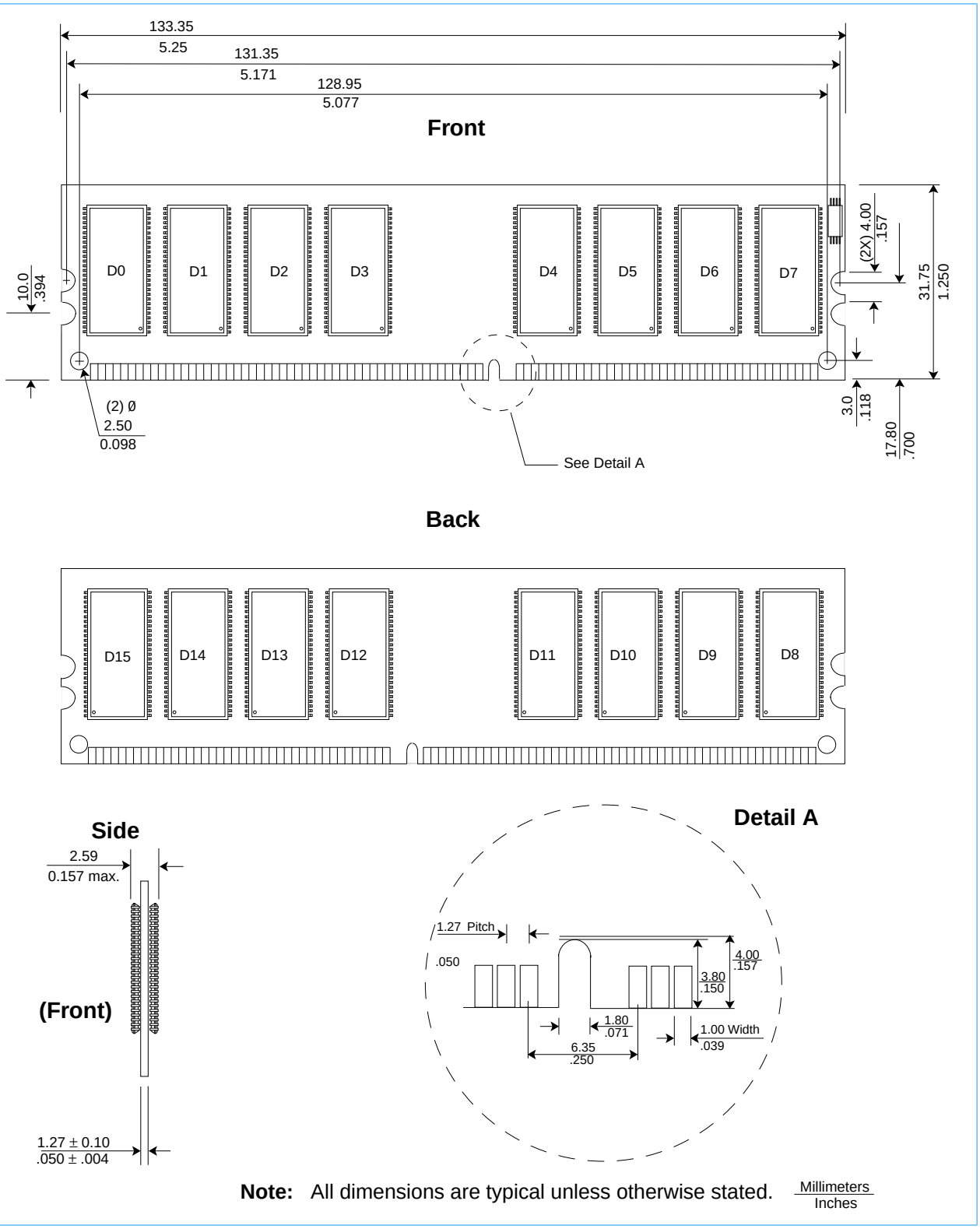
1. All voltages referenced to V_{SS}.
2. The SPD EEPROM Write cycle time (^{t}WRC) is the time from a valid stop condition of a Write sequence to the end of the EEPROM internal erase/program cycle. During the Write cycle, the EEPROM bus interface circuit is disabled, SDA remains High due to pull-up resistor, and the EEPROM does not respond to its slave address.

Functional Description and Timing Diagrams

Refer to IBM 128 Mb Synchronous DDR DRAM datasheet (06K0566.F39350A) for functional description and timing diagrams.

Refer to the IBM Application Notes *DDR Serial Presence Detect on Memory DIMMs and SDRAM Presence Detect Definitions,* for the Serial Presence Detect functional description and timings. All timing information refers to the timings at the SDRAM devices.

Layout Drawing for 32Mx64 2 Bank Unbuffered DIMM



Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Revision Log

Rev	Contents of Modification
12/00	Initial release.

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