

32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ II T2G family

General Description

CYT2B7 is a family of TRAVEO™ T2G microcontrollers targeted at automotive systems such as body control units. CYT2B7 has an Arm® Cortex®-M4 CPU for primary processing, and an Arm® Cortex®-M0+ CPU for peripheral and security processing. These devices contain embedded peripherals supporting Controller Area Network with Flexible Data rate (CAN FD), and Local Interconnect Network (LIN). TRAVEO™ T2G devices are manufactured on an advanced 40-nm process. CYT2B7 incorporates Cypress' low-power flash memory, multiple high-performance analog and digital peripherals, and enables the creation of a secure computing platform.

Features

• Dual CPU subsystem

- 160-MHz (max) 32-bit Arm® Cortex®-M4F CPU with
 - Single-cycle multiply
 - Single-precision floating point unit (FPU)
 - Memory protection unit (MPU)
- 100-MHz (max) 32-bit Arm® Cortex® M0+ CPU with
 - Single-cycle multiply
 - Memory Protection Unit
- Inter-processor communication in hardware
- Three DMA controllers
 - Peripheral DMA controller #0 (P-DMA0) with 89 channels
 - Peripheral DMA controller #1 (P-DMA1) with 33 channels
 - Memory DMA controller #0 (M-DMA0) with 4 channels

• Integrated memories

- 1088 KB of code-flash with an additional 96 KB of work-flash
 - Read-While-Write (RWW) allows updating the code-flash/work-flash while executing from it
 - Single- and dual-bank modes (specifically for Firmware update Over The Air [FOTA])
 - Flash programming through SWD/JTAG interface
- 128 KB of SRAM with selectable retention granularity

• Crypto engine^[1]

- Supports enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM)
- Secure boot and authentication
 - Using digital signature verification
 - Using fast secure boot
- AES: 128-bit blocks, 128-/192-/256-bit keys
- 3DES^[2]: 64-bit blocks, 64-bit key
- Vector unit^[2] supporting asymmetric key cryptography such as Rivest-Shamir-Adleman (RSA) and Elliptic Curve (ECC)
- SHA-1/2/3^[2]: SHA-512, SHA-256, SHA-160 with variable length input data
- CRC^[2]: supports CCITT CRC16 and IEEE-802.3 CRC32
- True random number generator (TRNG) and pseudo random number generator (PRNG)
- Galois/Counter Mode (GCM)

• Functional safety for ASIL-B

- Memory protection unit (MPU)
- Shared memory protection unit (SMPU)
- Peripheral protection unit (PPU)

Notes

1. The Crypto engine features are available on select MPNs.
2. This feature is not available in "eSHE only" parts; for more information, refer to [Ordering information](#).

Features

- Watchdog timer (WDT)
- Multi-counter watchdog timer (MCWDT)
- Low-voltage detector (LVD)
- Brown-out detector (BOD)
- Overvoltage detection (OVD)
- Clock supervisor (CSV)
- Hardware error correction (SECDED ECC) on all safety-critical memories (SRAM, flash)
- **Low-power 2.7-v to 5.5-v operation**
 - Low-power Active, Sleep, Low-power Sleep, DeepSleep, and Hibernate modes for fine-grained power management
 - Configurable options for robust BOD
 - Two threshold levels (2.7 V and 3.0 V) for BOD on V_{DD} and V_{DDA}
 - One threshold level (1.1 V) for BOD on V_{CCD}
- **Wakeup support**
 - Up to two pins to wakeup from Hibernate mode
 - Up to 152 GPIO pins to wakeup from Sleep modes
 - Event Generator, SCB, Watchdog Timer, RTC alarms to wake from DeepSleep modes
- **Clock sources**
 - Internal main oscillator (IMO)
 - Internal low-speed oscillator (ILO)
 - External crystal oscillator (ECO)
 - Watch crystal oscillator (WCO)
 - Phase-locked loop (PLL)
 - Frequency-locked loop (FLL)
- **Communication interfaces**
 - Up to six CAN FD channels
 - Increased data rate (up to 8 Mbps) compared to classic CAN, limited by physical layer topology and transceivers
 - Compliant to ISO 11898-1:2015
 - Supports all the requirements of Bosch CAN FD Specification V1.0 for non-ISO CAN FD
 - ISO 16845:2015 certificate available
 - Up to eight runtime-reconfigurable SCB (serial communication block) channels, each configurable as I²C, SPI, or UART
 - Up to eight independent LIN channels
 - LIN protocol compliant with ISO 17987
- **Timers**
 - Up to 75 16-bit and four 32-bit timer/counter pulse-width modulator (TCPWM) blocks
 - Up to 12 16-bit counters for motor control
 - Up to 63 16-bit counters and four 32-bit counters for regular operations
 - Supports timer, capture, quadrature decoding, pulse-width modulation (PWM), PWM with dead time (PWM_DT), pseudo-random PWM (PWM_PR), and shift-register (SR) modes
 - Up to 11 Event Generation (EVTGEN) timers supporting cyclic wakeup from DeepSleep
 - Events trigger a specific device operation (such as execution of an interrupt handler, a SAR ADC conversion, and so on)
- **Real time clock (RTC)**
 - Year/Month/Date, Day-of-week, Hour:Minute:Second fields
 - 12- and 24-hour formats
 - Automatic leap-year correction

Features

- **I/O**
 - Up to 152 Programmable I/Os
 - Two I/O types
 - GPIO Standard (GPIO_STD)
 - GPIO Enhanced (GPIO_ENH)
- **Regulators**
 - Generates 1.1-V nominal core supply from a 2.7-V to 5.5-V input supply
 - Two types of regulators
 - DeepSleep
 - Core internal
- **Programmable analog**
 - Three SAR A/D converters with up to 67 external channels (64 I/Os + 3 I/Os for motor control)
 - ADC0 supports 24 logical channels, with 24 + 1 physical connections
 - ADC1 supports 32 logical channels, with 32 + 1 physical connections
 - ADC2 supports 8 logical channels, with 8 + 1 physical connections
 - Any external channel can be connected to any logical channel in the respective SAR
 - Each ADC supports 12-bit resolution and sampling rates of up to 1 Msps
 - Each ADC also supports up to six internal analog inputs like
 - Bandgap reference to establish absolute voltage levels
 - Calibrated diode for junction temperature calculations
 - Two AMUXBUS inputs and two direct connections to monitor supply levels
 - Each ADC supports addressing of external multiplexers
 - Each ADC has a sequencer supporting autonomous scanning of configured channels
 - Synchronized sampling of all ADCs for motor-sense applications
- **Smart I/O™**
 - Up to five Smart I/O blocks, which can perform Boolean operations on signals going to and from I/Os
 - Up to 36 I/Os (GPIO_STD) supported
- **Debug interface**
 - JTAG controller and interface compliant to IEEE-1149.1-2001
 - Arm® SWD (Serial Wire Debug) port
 - Supports Arm® Embedded Trace Macrocell (ETM) Trace
 - Data trace using SWD
 - Instruction and data trace using JTAG
- **Compatible with industry-standard tools**
 - GHS/MULTI or IAR EWARM for code development and debugging
- **Packages**
 - 64-LQFP, 10 × 10 × 1.7 mm (max), 0.5-mm lead pitch
 - 80-LQFP, 12 × 12 × 1.7 mm (max), 0.5-mm lead pitch
 - 100-LQFP, 14 × 14 × 1.7 mm (max), 0.5-mm lead pitch
 - 144-LQFP, 20 × 20 × 1.7 mm (max), 0.5-mm lead pitch
 - 176-LQFP, 24 × 24 × 1.7 mm (max), 0.5-mm lead pitch

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1 Features list

Table 1-1 CYT2B7 feature list for all packages

| Features | Packages | | | | |
|---------------------------------------|--|--|--|--|--|
| | 64-LQFP | 80-LQFP | 100-LQFP | 144-LQFP | 176-LQFP |
| CPU | | | | | |
| Core | 32-bit Arm® Cortex®-M4F CPU and 32-bit Arm® Cortex® M0+ CPU | | | | |
| Functional safety | ASIL-B | | | | |
| Operating voltage | 2.7 V to 5.5 V | | | | |
| Core voltage | 1.05 V to 1.15 V | | | | |
| Operating frequency | Arm® Cortex®-M4 160 MHz (max) and Arm® Cortex®-M0+ 100 MHz (max), related by integer frequency ratio (that is, 1:1, 1:2, 1:3, and so on) | | | | |
| MPU, PPU | Supported | | | | |
| FPU | Single precision (32-bit) | | | | |
| DSP-MUL/DIV/MAC | Supported by Arm® Cortex®-M4F CPU | | | | |
| Memory | | | | | |
| Code-flash | 1088 KB (960 KB + 128 KB) | | | | |
| Work-flash | 96 KB (72 KB + 24 KB) | | | | |
| SRAM (configurable for retention) | 128 KB | | | | |
| ROM | 32 KB | | | | |
| Communication Interfaces | | | | | |
| CAN0 (CAN FD: Up to 8 Mbps) | 3 ch | | | | |
| CAN1 (CAN FD: Up to 8 Mbps) | 2 ch | 3 ch | | | |
| CAN RAM | 24 KB per instance (3 ch), 48 KB in total | | | | |
| Serial communication block (SCB/UART) | 7 ch | 8 ch | | | |
| Serial communication block (SCB/I2C) | 6 ch | | 8 ch | | |
| Serial communication block (SCB/SPI) | 3 ch | 6 ch | 8 ch | | |
| LIN0 | 6 ch | 7 ch | | 8 ch | |
| Timers | | | | | |
| RTC | 1 ch | | | | |
| TCPWM (16-bit) (Motor Control) | 12 ch | | | | |
| TCPWM (16-bit) | 63 ch | | | | |
| TCPWM (32-bit) | 4 ch | | | | |
| External Interrupts | 49 | 63 | 78 | 122 | 152 |
| Analog | | | | | |
| 12-bit, 1 Msps SAR ADC | 3 Units (SAR0/24, SAR1/32, SAR2/8 logical channels) | | | | |
| | 27 external channels (SAR0 11 ch, SAR1 9 ch, SAR2 7 ch) | 34 external channels (SAR0 12 ch, SAR1 14 ch, SAR2 8 ch) | 39 external channels (SAR0 14 ch, SAR1 17 ch, SAR2 8 ch) | 54 external channels (SAR0 21 ch, SAR1 25 ch, SAR2 8 ch) | 64 external channels (SAR0 24 ch, SAR1 32 ch, SAR2 8 ch) |
| | 18 ch (6 per ADC) Internal sampling | | | | |

Note

3. Enhanced Secure Hardware Extension (eSHE) and Hardware Security Module (HSM) support are enabled by third-party firmware.

Table 1-1 CYT2B7 feature list for all packages (continued)

| Features | Packages | | | | |
|---|---|-------------------|-------------------|-------------------|-------------------|
| | 64-LQFP | 80-LQFP | 100-LQFP | 144-LQFP | 176-LQFP |
| Motor Control Input | 3 ch (synchronous sampling of one channel on each of the 3 ADCs) | | | | |
| Security | | | | | |
| Flash Security (program/work read protection) | Supported | | | | |
| Flash Chip erase enable | Configurable | | | | |
| eSHE/HSM | By separate firmware ^[3] | | | | |
| System | | | | | |
| DMA Controller | P-DMA0 with 89 channels (16 general purpose), P-DMA1 with 33 channels (8 general purpose), and M-DMA0 with 4 channels | | | | |
| Internal main oscillator | 8 MHz | | | | |
| Internal low-speed oscillator | 32.768 kHz (nominal) | | | | |
| PLL | Input frequency: 3.988 to 33.34 MHz, PLL output frequency: up to 160 MHz | | | | |
| FLL | Input frequency: 0.25 to 80 MHz, FLL output frequency: up to 100 MHz | | | | |
| Watchdog timer and multi-counter watchdog timer | Supported | | | | |
| Clock supervisor | Supported | | | | |
| Cyclic wakeup from DeepSleep | Supported | | | | |
| GPIO_STD | 45 | 59 | 74 | 118 | 148 |
| GPIO_ENH | 4 | | | | |
| Smart I/O (Blocks) | 3 blocks, 9 I/Os | 3 blocks, 14 I/Os | 4 blocks, 20 I/Os | 5 blocks, 29 I/Os | 5 blocks, 36 I/Os |
| Low-voltage detect | Two, 26 selectable levels | | | | |
| Maximum ambient temperature | 105 °C for S-grade and 125 °C for E-grade | | | | |
| Debug interface | SWD/JTAG | | | | |
| Debug trace | Arm® Cortex®-M4 ETB size of 8 KB, Arm® Cortex® M0+ MTB size of 4 KB | | | | |

1.1 Communication peripheral instance list

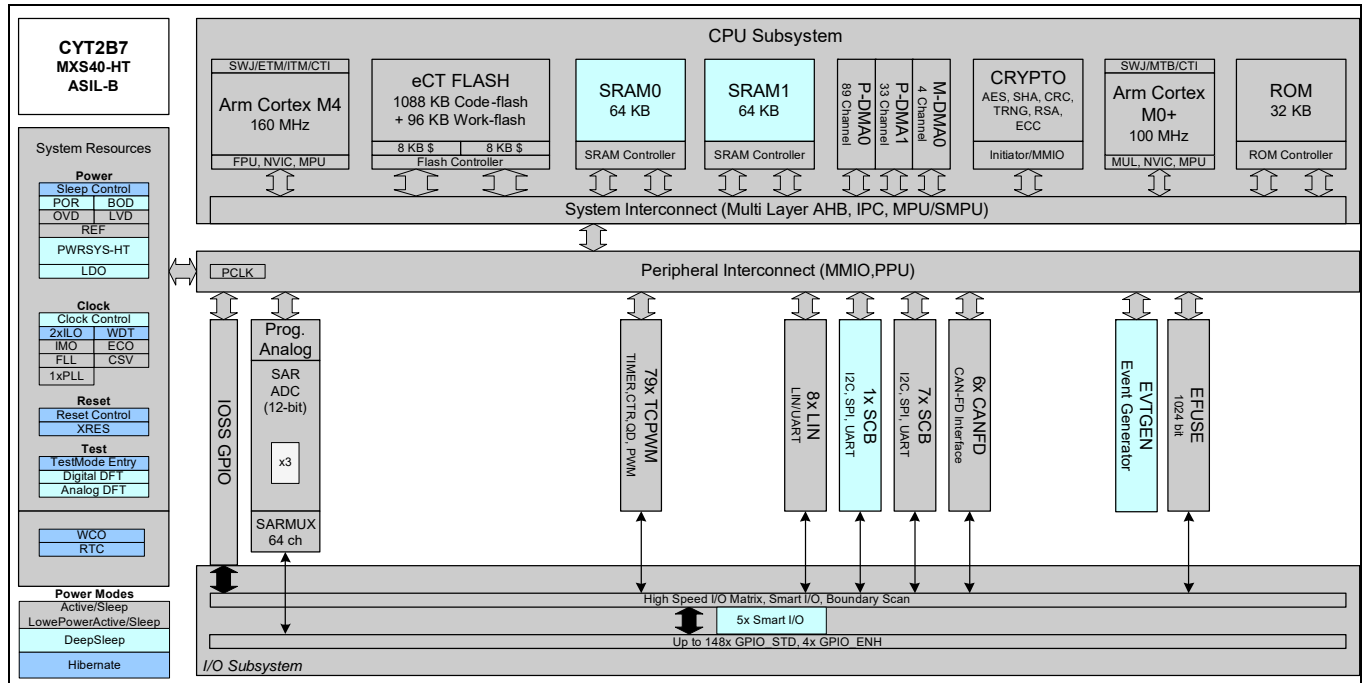
The following table lists the instances supported under each package for communication peripherals, based on the minimum pins needed for the functionality.

Table 1-2 Peripheral instance list

| Module | 64-LQFP | 80-LQFP | 100-LQFP | 144-LQFP | 176-LQFP | Minimum pin functions |
|----------|---------------|-----------------|-----------------|-----------------|-----------------|--------------------------|
| CAN0 | 0/1/2 | 0/1/2 | 0/1/2 | 0/1/2 | 0/1/2 | TX, RX |
| CAN1 | 0/2 | 0/1/2 | 0/1/2 | 0/1/2 | 0/1/2 | TX, RX |
| LIN0 | 0/1/2/3/4/7 | 0/1/2/3/4/6/7 | 0/1/2/3/4/6/7 | 0/1/2/3/4/5/6/7 | 0/1/2/3/4/5/6/7 | TX, RX |
| SCB/UART | 0/1/2/3/4/5/7 | 0/1/2/3/4/5/6/7 | 0/1/2/3/4/5/6/7 | 0/1/2/3/4/5/6/7 | 0/1/2/3/4/5/6/7 | TX, RX |
| SCB/I2C | 0/2/3/4/5/7 | 0/1/3/4/5/7 | 0/1/2/3/4/5/6/7 | 0/1/2/3/4/5/6/7 | 0/1/2/3/4/5/6/7 | SCL, SDA |
| SCB/SPI | 0/3/4 | 0/1/3/4/5/7 | 0/1/2/3/4/5/6/7 | 0/1/2/3/4/5/6/7 | 0/1/2/3/4/5/6/7 | MISO, MOSI, SCK, SELECT0 |

2 Blocks and functionality

Block diagram



The **Block diagram** shows the CYT2B7 architecture, giving a simplified view of the interconnection between subsystems and blocks. CYT2B7 has four major subsystems: CPU, system resources, peripherals, and I/O^[4, 5]. The color-coding shows the lowest power mode where the particular block is still functional.

CYT2B7 provides extensive support for programming, testing, debugging, and tracing of both hardware and firmware.

Debug-on-chip functionality enables in-system debugging using the production device. It does not require special interfaces, debugging pods, simulators, or emulators.

The JTAG interface is fully compatible with industry-standard third-party probes such as I-jet, J-Link, and GHS.

The debug circuits are enabled by default.

CYT2B7 provides a high level of security with robust flash protection and the ability to disable features such as debug.

Additionally, each device interface can be permanently disabled for applications concerned with phishing attacks from a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled.

Notes

- GPIO_STD supporting 2.7 V to 5.5 V V_{DDIO} range.
- GPIO_ENH supporting 2.7 V to 5.5 V V_{DDIO} range with higher currents at lower voltages.

3 Functional description

3.1 CPU subsystem

3.1.1 CPU

The CYT2B7 CPU subsystem contains a 32-bit Arm® Cortex®-M0+ CPU with MPU, and a 32-bit Arm® Cortex®-M4F CPU with MPU, and single-precision FPU. This subsystem also includes P-/M-DMA controllers, a cryptographic accelerator, 1088 KB of code-flash, 96 KB of work-flash, 128 KB of SRAM, and 32 KB of ROM.

The Cortex®-M0+ CPU provides a secure, un-interruptible boot function. This guarantees that, following completion of the boot function, system integrity is valid and privileges are enforced. Shared resources (flash, SRAM, peripherals, and so on) can be accessed through bus arbitration, and exclusive accesses are supported by an inter-processor communication (IPC) mechanism using hardware semaphores.

3.1.2 DMA controllers

CYT2B7 has three DMA controllers: P-DMA0 with 16 general-purpose and 73 dedicated channels, P-DMA1 with 8 general-purpose and 25 dedicated channels, and M-DMA0 with four channels. P-DMA is used for peripheral-to-memory and memory-to-peripheral data transfers and provides low latency for a large number of channels. Each P-DMA controller uses a single data-transfer engine that is shared by the associated channels. General purpose channels have a rich interconnect matrix including P-DMA cross triggering which enables demanding data-transfer scenarios. Dedicated channels have a single triggering input (such as an ADC channel) to handle common transfer needs. M-DMA is used for memory-to-memory data transfers and provides high memory bandwidth for a small number of channels. M-DMA uses a dedicated data-transfer engine for each channel. They support independent accesses to peripherals using the AHB multi-layer bus.

3.1.3 Flash

CYT2B7 has 1088 KB (960 KB with a 32-KB sector size, and 128 KB with an 8-KB sector size) of code-flash with an additional work-flash of up to 96 KB (72 KB with 2-KB sector size, and 24 KB with 128-B sectors size). Work-flash is optimized for reprogramming many more times than code-flash. Code-flash supports Read-While-Write (RWW) operation allowing flash to be updated while the CPU is active. Both the code-flash and work-flash areas support dual-bank operation for over-the-air (OTA) programming.

3.1.4 SRAM

CYT2B7 has 128 KB of SRAM with two independent controllers. The first controller, SRAM0, provides DeepSleep retention in 32-KB increments, while SRAM1 is selectable between fully retained and not retained.

3.1.5 ROM

CYT2B7 has 32-KB ROM that contains boot and configuration routines. This ROM enables secure boot and authentication of user flash to guarantee a secure system.

3.1.6 Cryptography accelerator for security

The cryptography accelerator implements (3)DES block cipher, AES block cipher, SHA hash, cyclic redundancy check, pseudo random number generation, true random number generation, galois/counter mode, and a vector unit to support asymmetric key cryptography such as RSA and ECC.

Depending on the part number, this block is either completely or partially available or not available at all. See [Ordering information](#) for more details.

3.2 System resources

3.2.1 Power system

The power system ensures that the supply voltage levels meet the requirements of each power mode, and provides a full-system reset when these levels are not valid. Internal power-on reset (POR) guarantees full-chip reset during the initial power ramp.

Three Brown-Out Detection (BOD) circuits monitor the external supply voltages (V_{DD} , V_{DDA} , V_{CCD}). The BOD on V_{DD} and V_{CCD} are initially enabled and cannot be disabled. The BOD on V_{DDA} is initially disabled and can be enabled by the user. For the external supplies V_{DD} and V_{DDA} , BOD circuits are software configurable with two settings; a 2.7-V minimum voltage that is robust for all internal signaling and a 3.0-V minimum voltage, which is also robust for all I/O specifications (which are guaranteed at 2.7 V). The BOD on V_{CCD} is provided as a safety measure and is not a robust detector.

Three overvoltage detection (OVD) circuits are provided for monitoring external supplies (V_{DD} , V_{DDA} , V_{CCD}), and overcurrent detection circuits (OCD) for monitoring internal and external regulators. OVD thresholds on V_{DD} and V_{DDA} are configurable with two settings; a 5.0-V and 5.5-V maximum voltage. Two voltage-detection circuits are provided to monitor the external supply voltage (V_{DD}) for falling and rising levels, each configurable for one of the 26 selectable levels.

All BOD, OVD, and OCD circuits on V_{DD} and V_{CCD} generate a reset, because these protect the CPUs and fault logic. The BOD and OVD circuits on V_{DDA} can be configured to generate either a reset, or a fault.

3.2.2 Regulators

CYT2B7 contains two regulators that provide power to the low-voltage core transistors: DeepSleep and core internal. These regulators accept a 2.7–5.5-V V_{DD} supply and provide a low-noise 1.1-V supply to various parts of the device. These regulators are automatically enabled and disabled by hardware and firmware when switching between power modes. The core internal and core external regulators operate in active mode, and provide power to the CPU subsystem and associated peripherals.

3.2.2.1 DeepSleep

The DeepSleep regulator is used to maintain power to a small number of blocks when in DeepSleep mode. These blocks include the ILO and WDT timers, BOD detector, SCB0, SRAM memories, Smart I/O, and other configuration memories. The DeepSleep regulator is enabled when in DeepSleep mode, and the core internal regulator is disabled. It is disabled when XRES_L is asserted (LOW) and when the core internal regulator is disabled.

3.2.2.2 Core internal

The core internal regulator supports load currents up to 150 mA, and is operational during the device start-up (boot process), and in Active/Sleep modes.

3.2.3 Clock system

The CYT2B7 clock system provides clocks to all subsystems that require them, and glitch-free switching between different clock sources. In addition, the clock system ensures that no metastable conditions occur.

The clock system for CYT2B7 consists of the 8-MHz IMO, two ILOs, three watchdog timers, a PLL, an FLL, five clock supervisors (CSV), a 3.988- to 33.34 MHz ECO, and a 32.768-kHz WCO.

The clock system supports two main clock domains: CLK_HF, and CLK_LF.

- CLK_HF are the Active mode clocks. Each can use any of the high frequency clock sources including IMO, EXT_CLK, ECO, FLL, or PLL
- CLK_LF is a DeepSleep domain clock and provides a reference clock for the MCWDT or RTC modules. The reference clock for the CLK_LF domain is either disabled or selectable from ILO0, ILO1, or WCO

Table 3-1 CLK_HF destinations

| Name | Description |
|---------|---|
| CLK_HF0 | CPUSS clocks, PERI, and AHB infrastructure |
| CLK_HF1 | Event Generator, also available in HSIOM as an output |

3.2.3.3 IMO clock source

The IMO is the frequency reference in CYT2B7 when no external reference is available or enabled. The IMO operates at a frequency of around 8 MHz.

3.2.3.4 ILO clock source

An ILO is a low-power oscillator, nominally 32.768 kHz, which generates clocks for a watchdog timer when in DeepSleep mode. There are two ILOs to ensure clock supervisor (CSV) capability in DeepSleep mode. ILO-driven counters can be calibrated to the IMO, WCO, or ECO to improve their accuracy. ILO1 is also used for clock supervision.

3.2.3.5 PLL and FLL

A PLL or FLL may be used to generate high-speed clocks from the IMO, the ECO, or EXT_CLK. The FLL provides a much faster lock than the PLL (5 μ s instead of 35 μ s) in exchange for a small amount ($\pm 2\%$) of frequency error^[6].

3.2.3.6 Clock supervisor (CSV)

Each CSV allows one clock (reference) to supervise the behavior of another clock (monitored). Each CSV has counters for both the monitored and reference clocks. Parameters for each counter determine the frequency of the reference clock as well as the upper and lower frequency limits of the monitored clock. If the frequency range comparator detects a stopped clock or a clock outside the specified frequency range, an abnormal state is signaled and either a reset or an interrupt is generated.

3.2.3.7 EXT_CLK

One of the two GPIO_STD I/Os can be used to provide an external clock input of up to 80 MHz. This clock can be used as the source clock for either the PLL or FLL, or can be used directly by the CLK_HF domain.

3.2.3.8 ECO

The ECO provides high-frequency clocking using an external crystal connected to the ECO_IN and ECO_OUT pins. It supports fundamental mode (non-overtone) quartz crystals, in the range of 3.988 to 33.34 MHz. When used in conjunction with the PLL, it generates CPU and peripheral clocks up to device's maximum frequency. ECO accuracy depends on the selected crystal. If the ECO is disabled, the associated pins can be used for any of the available I/O functions.

3.2.3.9 WCO

The WCO is a low-power, watch-crystal oscillator intended for real-time-clock applications. It requires an external 32.768-kHz crystal connected to the WCO_IN and WCO_OUT pins. The WCO can also be configured as a clock reference for CLK_LF, which is the clock source for the MCWDT and RTC.

3.2.4 Reset

CYT2B7 can be reset from a variety of sources, including software. Reset events are asynchronous and guarantee reversion to a known state. The reset cause (POR, BOD, OVD, overcurrent, XRES_L, WDT, MCWDT, software reset, fault, CSV, Hibernate wakeup, debug) is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES_L pin is available for external reset.

Note

6. Operation of reference-timed peripherals (like a UART) with an FLL-based reference is not recommended due to the allowed frequency error.

3.2.5 Watchdog timers

CYT2B7 has one watchdog timer (WDT) and two multi-counter watchdog timers (MCWDT).

The WDT is a free-running counter clocked only by ILO0, which allows it to be used as a wakeup source from Hibernate. Watchdog operation is possible during all power modes. To prevent a device reset from a WDT timeout, the WDT must be serviced during a configured window. A watchdog reset is recorded in the reset cause register.

An MCWDT is available for each of the CPU cores. These timers provide more capabilities than the WDT, and are only available in Active, Sleep, and DeepSleep modes. These timers have multiple counters that can be used separately or cascaded to trigger interrupts and/or resets. They are clocked from ILO0 or the WCO.

3.2.6 Power modes

CYT2B7 has the following six power modes:

- Active – all peripherals are available
- Low-Power Active (LPACTIVE) – Low-power profile of Active mode where all peripherals and the CPUs are available, but with limited capability
- Sleep – all peripherals except the CPUs are available
- Low-Power Sleep (LPSLEEP) – Low-power profile of Sleep mode where all peripherals except the CPUs are available, but with limited capability
- DeepSleep – only peripherals which work with CLK_LF are available
- Hibernate – the device and I/O states are frozen, the device resets on wakeup

3.3 Peripherals

3.3.1 Peripheral clock dividers

Integer and fractional clock dividers are provided for peripheral and timing purposes.

Table 3-1 Clock dividers

| Divider | Count | Description |
|----------|-------|---|
| div_8 | 32 | Integer divider, 8 bits |
| div_16 | 16 | Integer divider, 16 bits |
| div_24_5 | 8 | Fractional divider, 24.5 bits (24 integer bits, 5 fractional bits) |

3.3.2 Peripheral protection unit

The Peripheral Protection Unit (PPU) controls and monitors unauthorized access from all masters (CPU, P-/M-DMA, Crypto, and any enabled debug interface) to the peripherals. It allows or restricts data transfers on the bus infrastructure. The access rules are enforced based on specific properties of a transfer, such as an address range for the transfer and access attributes (such as read/write, user/privilege, and secure/non-secure).

Note

7. VREF_L prevents IR drops in the VSSIO and VSSA paths from impacting the measurements. VREF_L, when properly connected, reduces or removes the impact of IR drops in the VSSIO and VSSA paths from measurements.

3.3.3 12-bit SAR ADC

CYT2B7 contains three 1-Msps SAR ADCs. These ADCs can be clocked at up to 26.67 MHz and provide a 12-bit result in 26 clock cycles.

The references for all three SAR ADCs come from a dedicated pair of inputs: VREFH and VREFL^[7].

CYT2B7 devices support up to 85 logical ADC channels, and external inputs from up to 67 I/Os. Each ADC also supports six internal connections for diagnostic and monitoring purposes. The number of ADC channels (per ADC and package type) are listed in [Table 1-1](#).

Each ADC has a sequencer, which autonomously cycles through the configured channels (sequencer scan) with zero-switching overhead (that is, the aggregate sampling bandwidth, when clocked at 26.67 MHz, is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is controlled through a state machine or firmware. The sequencer prioritizes trigger requests, enables the appropriate analog channel, controls ADC sampling, initiates ADC data conversion, manages results, and initiates subsequent conversions for repetitive or group conversions without CPU intervention.

Each SAR ADC has an analog multiplexer used to connect the signals to be measured to the ADC. It has 32 GPIO_STD inputs, one special GPIO_STD input for motor-sense, and six additional inputs to measure internal signals such as a band-gap reference, a temperature sensor, and power supplies. The device supports synchronous sampling of one motor-sense channel on each of the three ADCs.

CYT2B7 has one temperature sensor that is shared by all three ADCs. The temperature sensor must only be sampled by one ADC at a time. Software post processing is required to convert the temperature sensor reading into kelvin or Celsius values.

To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmed for each channel. Each ADC also supports range comparison, which allows fast detection of out-of-range values without having to wait for a sequencer scan to complete and for the CPU firmware to evaluate the measurement for out-of-range values.

The ADCs are not usable in DeepSleep and Hibernate modes as they require a high-speed clock. The ADC input reference voltage VREFH range is 2.7 V to V_{DDA} and VREFL is V_{SSA} .

3.3.4 Timer/counter/PWM block (TCPWM)

The TCPWM block consists of 16-bit (75 channels) and 32-bit (four channels) counters with a user-programmable period. Twelve of the 16-bit counters include extra features to support motor control operations. Each TCPWM counter contains a capture register to record the count at the time of an event, a period register (used to either stop or auto-reload the counter when its count is equal to the period register), and compare registers to generate signals that are used as PWM duty-cycle outputs.

Each counter within the TCPWM block supports several functional modes such as timer, capture, quadrature, PWM, PWM with dead-time insertion (PWM_DT, 8-bit), pseudo-random PWM (PWM_PR), and shift-register.

In motor-control applications, the counter within the TCPWM block supports enhanced quadrature mode with features such as asymmetric PWM generation, dead-time insertion (16-bit), and association of different dead times for PWM output signals.

The TCPWM block also provides true and complement outputs, with programmable offset between them, to allow their use as deadband complementary PWM outputs. The TCPWM block also has a kill input (only for the PWM mode) to force outputs to a predetermined state; for example, this may be used in motor-drive systems when an overcurrent state is detected and the PWMs driving the FETs need to be shut off immediately (no time for software intervention).

3.3.5 Serial communication blocks (SCB)

CYT2B7 contains eight serial communication blocks, each configurable to support I²C, UART, or SPI.

3.3.5.10 I²C interface

An SCB can be configured to implement a full I²C master (capable of multi-master arbitration) or slave interface. Each SCB configured for I²C can operate at speeds of up to 1 Mbps (Fast-mode Plus^[8]) and has flexible buffering options to reduce the interrupt overhead and latency of the CPU. In addition, each SCB supports FIFO buffering for receive and transmit data, which, by increasing the time for the CPU to read the data, reduces the need for clock stretching. The I²C interface is compatible with Standard, Fast-mode, and Fast-mode Plus devices as specified in the NXP I²C-bus specification and user manual (UM10204). The I²C-bus I/O is implemented with GPIO in open-drain modes^[9, 10].

3.3.5.11 UART interface

When configured as a UART, each SCB provides a full-featured UART with maximum signalling rate determined by the configured peripheral-clock frequency and over-sampling rate. It supports infrared interface (IrDA) and SmartCard (ISO 7816) protocols, which are minor variants of the UART protocol. It also supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity, number of stop bits, break detect, and frame error are supported. FIFO buffering of transmit and receive data allows greater CPU service latencies to be tolerated.

The LIN protocol is supported by the UART. LIN is based on a single-master multi-slave topology. There is one master node and multiple slave nodes on the LIN bus. The SCB UART supports only LIN slave functionality. Compared to the dedicated LIN blocks, an SCB/UART used for LIN requires a higher level of software interaction and increased CPU load.

3.3.5.12 SPI interface

The SPI configuration supports full Motorola SPI, TI Synchronous Serial Protocol (SSP, essentially adds a start pulse that is used to synchronize SPI-based codecs), and National Microwire (a half-duplex form of SPI). The SPI interface can use the FIFO. The SPI interface operates with up to a 12.5-MHz SPI Clock. SCB also supports EZSPI^[11] mode.

SCB0 supports the following additional features:

- Operable as a slave in DeepSleep mode
- I²C slave EZ (EZI2C^[12]) mode with up to 256-B data buffer for multi-byte communication without CPU intervention
- I²C slave externally-clocked operations
- Command/response mode with a 512-B data buffer for multi-byte communication without CPU intervention

3.3.6 CAN FD

CYT2B7 supports two CAN FD controller blocks, each supporting three CAN FD channels. All CAN FD controllers are compliant with the ISO 11898-1:2015 standard; an ISO 16845:2015 certificate is available. It also implements the time-triggered CAN (TTCAN) protocol specified in ISO 11898-4 (TTCAN protocol levels 1 and 2) completely in hardware.

All functions concerning the handling of messages are implemented by the Rx and Tx handlers. The Rx handler manages message acceptance filtering, transfer of received messages from the CAN core to a message RAM, and provides receive-message status. The Tx handler is responsible for the transfer of transmit messages from the message RAM, to the CAN core, and provides transmit-message status.

Notes

8. I/Os drive level does not support the full bus capacitance in Fast-mode Plus speeds.
9. This is not 100% compliant with the I²C-bus specification; I/Os are not over-voltage tolerant, do not support the 20-mA sink requirement of Fast-mode Plus, and violate the leakage specification when no power is applied.
10. Only Port 0 with the slew rate control enabled meets the minimum fall time requirement.
11. The Easy SPI (EZSPI) protocol is based on the Motorola SPI operating in any mode (0, 1, 2, or 3). It allows communication between master and slave reduces the need for CPU intervention.
12. The Easy I²C (EZI2C) protocol is a unique communication scheme built on top of the I²C protocol by Cypress. It uses a meta protocol around the standard I²C protocol to communicate to an I²C slave using indexed memory transfers. This reduces the need for CPU intervention.

3.3.7 Local Interconnect network (LIN)

CYT2B7 contains up to eight LIN channels. Each channel supports transmission/reception of data following the LIN protocol according to ISO standard 17987. Each LIN channel connects to an external transceiver through a 3-pin interface (including an enable function) and supports master and slave functionality. Each channel also supports classic and enhanced checksum, along with break detection during message reception and wake-up signaling. Break detection, sync field, checksum calculations, and error interrupts are handled in hardware.

3.3.8 One-time-programmable (OTP) eFuse

CYT2B7 contains a 1024-bit OTP eFuse memory that can be used to store and access a unique and unalterable identifier or serial number for each device. eFuses are also used to control the device life-cycle (manufacturing, programming, normal operation, end-of-life, and so on) and the security state. Of the 1024 bits, 192 are available for user purposes.

3.3.9 Event generator

The event generator supports generation of interrupts and triggers in Active mode and interrupts in DeepSleep mode. The event generators are used to trigger a specific device operation (execution of an interrupt handler, a SAR ADC conversion, and so on) and to provide a cyclic wakeup mechanism from DeepSleep mode. They provide CPU-free triggers for device functions, and reduce CPU involvement in triggering device functions, thus reducing overall power consumption and processing overhead.

3.3.10 Trigger multiplexer

CYT2B7 supports connecting various peripherals using trigger signals. Triggers are used to inform a peripheral of the occurrence of an event or change of state. These triggers are used to affect or initiate some action in other peripherals. The trigger multiplexer is used to route triggers from a source peripheral to a destination. Triggers provide active logic functionality and are typically supported in Active mode.

3.4 I/Os

CYT2B7 has up to 152 programmable I/Os.

The I/Os are organized as logical entities called ports, which are a maximum of 8 bits wide. During power-on, and reset, the I/Os are forced to the High-Z state. During the Hibernate mode, I/Os are frozen.

Every I/O can generate an interrupt (if enabled) and each port has an interrupt request (IRQ) and interrupt service routine (ISR) associated with it.

I/O port power source mapping is listed in [Table 3-1](#). The associated supply determines the V_{OH} , V_{OL} , V_{IH} , and V_{IL} levels when configured for CMOS and Automotive thresholds.

Table 3-1 I/O port power source

| Supply | Ports |
|---------|--|
| VDDD | P0, P1, P2, P3, P4, P5, P16, P17, P18, P19, P20, P21, P22, P23 |
| VDDIO_1 | P6, P7, P8, P9 ^[13] |
| VDDIO_2 | P10, P11, P12, P13, P14, P15 |

Note

13. The I/Os in VDDIO_1 domain are referred to the VDDD domain in 64-LQFP package.

3.4.1 Port nomenclature

Px.y describes a particular bit “y” available within an I/O port “x.”

For example, P4.2 reads “port 4, bit 2”.

Each I/O implements the following:

- Programmable drive mode
 - High impedance
 - Resistive pull-up
 - Resistive pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up or pull-down
 - Weak pull-up or pull-down

CYT2B7 has two types of programmable I/Os: GPIO standard and GPIO Enhanced.

- GPIO Standard (GPIO_STD)
 - Supports standard automotive signaling across the 2.7-V to 5.5-V V_{DDIO} range. GPIO Standard I/Os have multiple configurable drive levels, drive modes, and selectable input levels.
- GPIO Enhanced (GPIO_ENH)
 - Supports extended functionality automotive signalling across the 2.7-V to 5.5-V V_{DDIO} range with higher currents at lower voltages (full I²C timing support, slew-rate control).

Both GPIO_STD and GPIO_ENH implement the following:

- Configurable input threshold (CMOS, TTL, or Automotive)
- Hold mode for latching previous state (used for retaining the I/O state in DeepSleep mode)
- Analog input mode (input and output buffers disabled)

3.4.2 Smart I/O

Smart I/O allows Boolean operations on signals going to the I/O from the subsystems of the chip or on signals coming into the chip. CYT2B7 has five Smart I/O blocks. Operation can be synchronous or asynchronous and the blocks operate in all device power modes except for the Hibernate mode.

4 CYT2B7 address map

The CYT2B7 microcontroller supports the memory spaces shown in [Figure 4-1](#).

- 1088KB (960KB + 128KB) of code-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
 - Single-bank mode - 1088KB
 - Dual-bank mode - 544KB per bank
- 96KB (72KB + 24KB) of work-flash, used in the single- or dual-bank mode based on the associated bit in the flash control register
 - Single-bank mode - 96KB
 - Dual-bank mode - 48KB per bank
- 32KB of secure ROM
- 128KB of SRAM (First 2 KB is reserved for internal usage)

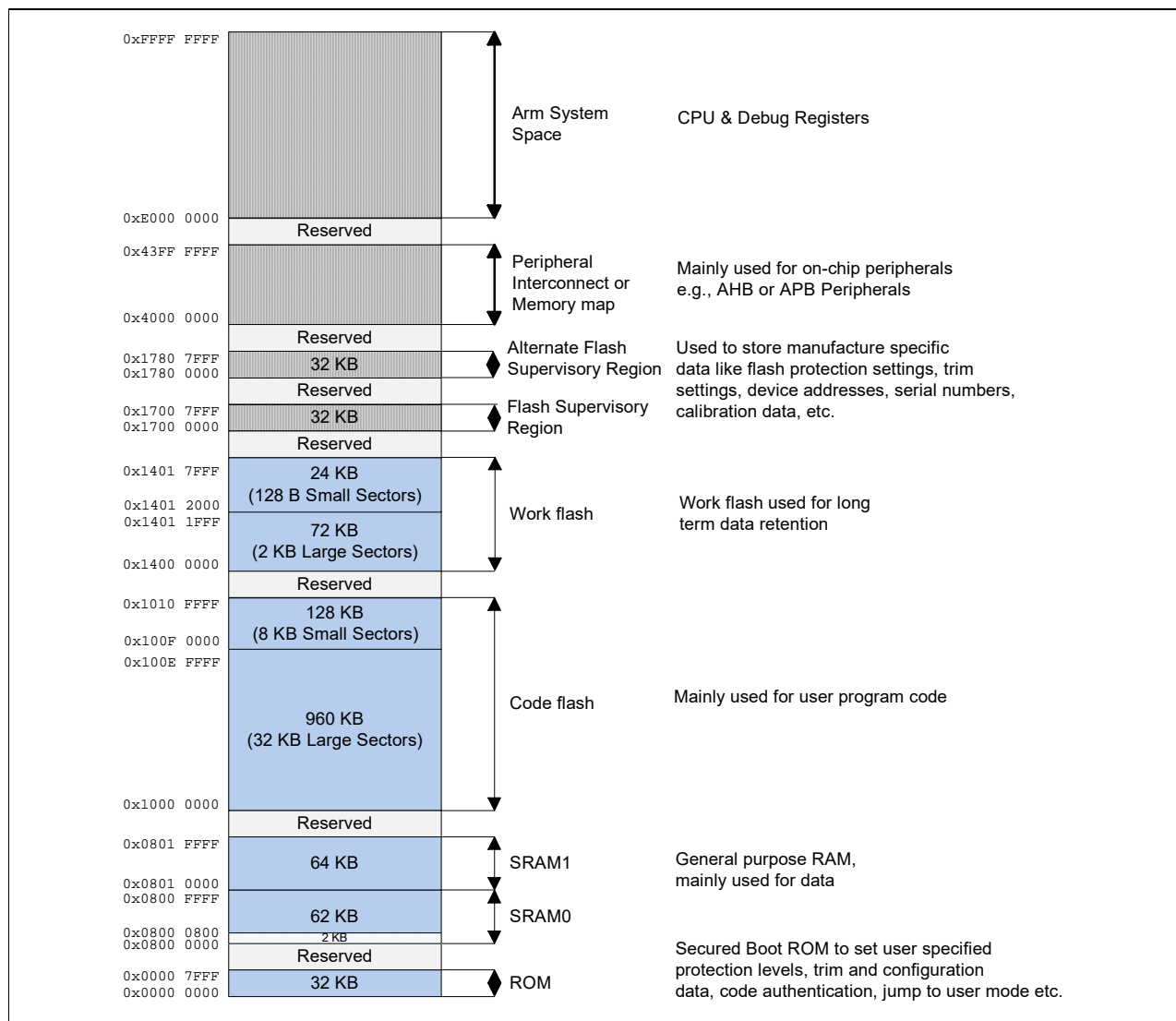


Figure 4-1 CYT2B7 address map^[14, 15]

Notes

14.The size representation is not up to scale.

15.First 2 KB of SRAM is reserved, not available for users. User must keep the power of first 32KB block of SRAM0 in enabled or retained in all Active, LP Active, Sleep, LP Sleep, DeepSleep modes.

5 Flash base address map

Table 5-1 through Table 5-6 give information about the sector mapping of the code- and work-flash regions along with their respective base addresses.

Table 5-1 Code-flash Address Mapping in Single Bank Mode

| Code-flash Size (KB) | Large Sectors (LS) | Small Sectors (SS) | Large Sector Base Address | Small Sector Base Address |
|----------------------|--------------------|--------------------|---------------------------|---------------------------|
| 1088 | 32KB × 30 | 8KB × 16 | 0x1000 0000 | 0x100F 0000 |

Table 5-2 Work-flash Address Mapping in Single Bank Mode

| Work-flash Size (KB) | Large Sectors | Small Sectors | Large Sector Base Address | Small Sector Base Address |
|----------------------|---------------|---------------|---------------------------|---------------------------|
| 96 | 2KB × 36 | 128 B × 192 | 0x1400 0000 | 0x1401 2000 |

Table 5-3 Code-flash Address Mapping in Dual Bank Mode (Mapping A)

| Code-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 1088 | 32KB × 15 | 8KB × 8 | 32KB × 15 | 8KB × 8 | 0x1000 0000 | 0x1007 8000 | 0x1200 0000 | 0x1207 8000 |

Table 5-4 Code-flash Address Mapping in Dual Bank Mode (Mapping B)

| Code-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 1088 | 32KB × 15 | 8KB × 8 | 32KB × 15 | 8KB × 8 | 0x1200 0000 | 0x1207 8000 | 0x1000 0000 | 0x1007 8000 |

Table 5-5 Work-flash Address Mapping in Dual Bank Mode (Mapping A)

| Work-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 96 | 2KB × 18 | 128 B × 96 | 2KB × 18 | 128 B × 96 | 0x1400 0000 | 0x1400 9000 | 0x1500 0000 | 0x1500 9000 |

Table 5-6 Work-flash Address Mapping in Dual Bank Mode (Mapping B)

| Work-flash Size (KB) | First Half LS | First Half SS | Second Half LS | Second Half SS | First Half LS Base Address | First Half SS Base Address | Second Half LS Base Address | Second Half SS Base Address |
|----------------------|---------------|---------------|----------------|----------------|----------------------------|----------------------------|-----------------------------|-----------------------------|
| 96 | 2KB × 18 | 128 B × 96 | 2KB × 18 | 128 B × 96 | 0x1500 0000 | 0x1500 9000 | 0x1400 0000 | 0x1400 9000 |

6 Peripheral I/O map

Table 6-1 CYT2B7 peripheral I/O map

| Section | Description | Base Address | Instances | Instance Size | Group | Slave |
|---------|---|--------------|-------------------|---------------|-------|-------|
| PERI | Peripheral interconnect | 0x4000 0000 | | | 0 | 0 |
| | Peripheral group (0, 1, 2, 3, 5, 6, 9) | 0x4000 4000 | 7 | 0x20 | | |
| | Peripheral trigger group | 0x4000 8000 | 11 | 0x400 | | |
| | Peripheral 1:1 trigger group | 0x4000 C000 | 11 | 0x400 | | |
| PERI_MS | Peripheral interconnect, master interface | 0x4001 0000 | | | 0 | 1 |
| | PERI Programmable PPU | 0x4001 0000 | 6 ^[16] | 0x40 | | |
| | PERI Fixed PPU | 0x4001 0800 | 458 | 0x40 | | |
| Crypto | Cryptography component | 0x4010 0000 | | | 1 | 0 |
| CPUSS | CPU subsystem (CPUSS) | 0x4020 0000 | | | 2 | 0 |
| FAULT | Fault structure subsystem | 0x4021 0000 | | | 2 | 1 |
| | Fault structures | 0x4021 0000 | 4 | 0x100 | | |
| IPC | Inter process communication | 0x4022 0000 | | | 2 | 2 |
| | IPC structures | 0x4022 0000 | 8 | 0x20 | | |
| | IPC interrupt structures | 0x4022 1000 | 8 | 0x20 | | |
| PROT | Protection | 0x4023 0000 | | | 2 | 3 |
| | Shared memory protection unit structures | 0x4023 2000 | 16 | 0x40 | | |
| | Memory protection unit structures | 0x4023 4000 | 16 | 0x400 | | |
| FLASHC | Flash controller | 0x4024 0000 | | | 2 | 4 |
| SRSS | System Resources Subsystem Core Registers | 0x4026 0000 | | | 2 | 5 |
| | Clock Supervision High Frequency | 0x4026 1400 | 3 | 0x10 | | |
| | Clock Supervision Reference Frequency | 0x4026 1710 | 1 | | | |
| | Clock Supervision Low Frequency | 0x4026 1720 | 1 | | | |
| | Clock Supervision Internal Low Frequency | 0x4026 1730 | 1 | | | |
| | Multi Counter WDT | 0x4026 8000 | 2 | 0x100 | | |
| | Free Running WDT | 0x4026 C000 | 1 | | | |
| BACKUP | SRSS Backup Domain/RTC | 0x4027 0000 | | | 2 | 6 |
| | Backup Register | 0x4027 1000 | 4 | 0x04 | | |
| P-DMA | P-DMA0 Controller | 0x4028 0000 | | | 2 | 7 |
| | P-DMA0 channel structures | 0x4028 8000 | 89 | 0x40 | | |
| | P-DMA1 Controller | 0x4029 0000 | | | 2 | 8 |
| | P-DMA1 channel structures | 0x4029 8000 | 33 | 0x40 | | |
| M-DMA | M-DMA0 Controller | 0x402A 0000 | | | 2 | 9 |
| | M-DMA0 channels | 0x402A 1000 | 4 | 0x100 | | |
| eFUSE | eFUSE Customer Data (192 bits) | 0x402C 0868 | 6 | 0x04 | 2 | 10 |

Note

16. These six Programmable PPUs are configured by the Boot ROM and are available for the user based on the access rights. Refer to the device specific TRM to know more about the configuration of these programmable PPUs.

Table 6-1 CYT2B7 peripheral I/O map (continued)

| Section | Description | Base Address | Instances | Instance Size | Group | Slave |
|-----------|---|--------------|-----------|---------------|-------|-------|
| HSIOM | High-Speed I/O Matrix (HSIOM) | 0x4030 0000 | 24 | 0x10 | 3 | 0 |
| GPIO | GPIO port control/configuration | 0x4031 0000 | 24 | 0x80 | 3 | 1 |
| SMARTIO | Programmable I/O configuration | 0x4032 0000 | | | 3 | 2 |
| | SMARTIO port configuration | 0x4032 0C00 | 5 | 0x100 | | |
| TCPWM | Timer/Counter/PWM 0 (TCPWM0) | 0x4038 0000 | | | 3 | 3 |
| | TCPWM0 Group #0 (16-bit) | 0x4038 0000 | 63 | 0x80 | | |
| | TCPWM0 Group #1 (16-bit, Motor control) | 0x4038 8000 | 12 | 0x80 | | |
| | TCPWM0 Group #2 (32-bit) | 0x4039 0000 | 4 | 0x80 | | |
| EVTGEN | Event generator 0 (EVTGEN0) | 0x403F 0000 | | | 3 | 4 |
| | Event generator 0 comparator structures | 0x403F 0800 | 11 | 0x20 | | |
| LIN | Local Interconnect Network 0 (LIN0) | 0x4050 0000 | | | 5 | 0 |
| | LIN0 Channels | 0x4050 8000 | 8 | 0x100 | | |
| TTCANFD | CAN0 controller | 0x4052 0000 | 3 | 0x200 | 5 | 1 |
| | Message RAM CAN0 | 0x4053 0000 | | 0x5FFF | | |
| | CAN1 controller | 0x4054 0000 | 3 | 0x200 | 5 | 2 |
| | Message RAM CAN1 | 0x4055 0000 | | 0x5FFF | | |
| SCB | Serial Communications Block (SPI/UART/I ² C) | 0x4060 0000 | 8 | 0x10000 | 6 | 0-7 |
| PASS0 SAR | Programmable Analog Subsystem (PASS0) | 0x4090 0000 | | | 9 | 0 |
| | SAR0 channel controller | 0x4090 0000 | | | | |
| | SAR1 channel controller | 0x4090 1000 | | | | |
| | SAR2 channel controller | 0x4090 2000 | | | | |
| | SAR0 channel structures | 0x4090 0800 | 24 | 0x40 | | |
| | SAR1 channel structures | 0x4090 1800 | 32 | 0x40 | | |
| | SAR2 channel structures | 0x4090 2800 | 8 | 0x40 | | |

7 CYT2B7 clock diagram

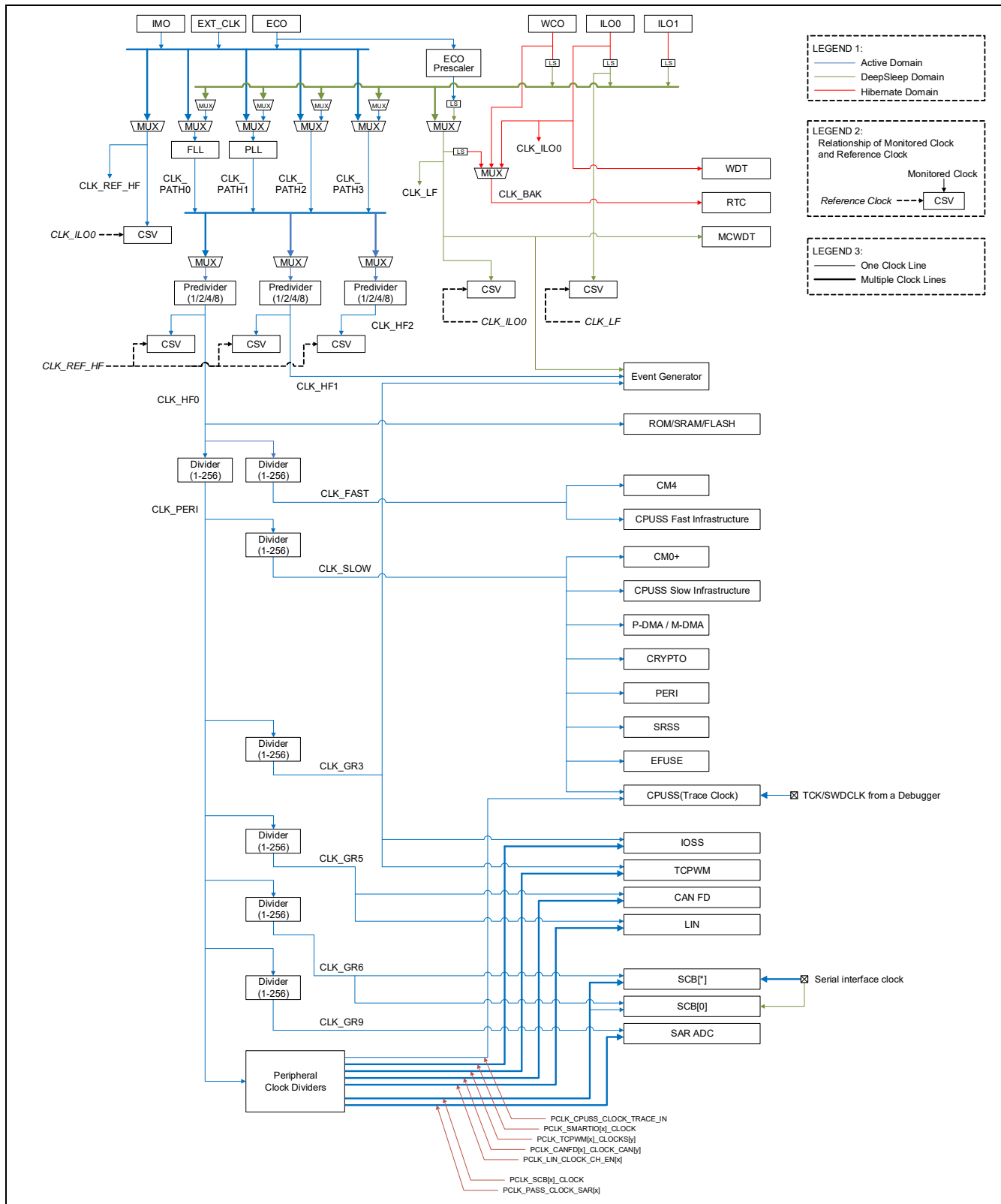


Figure 7-1 CYT2B7 clock diagram

8 CYT2B7 CPU start-up sequence

The start-up sequence is described in the following steps:

1. System Reset (@0x0000 0000)
- 2. CM0+ executes ROM boot (@0x0000 0004)**
 - i. Applies trims
 - ii. Applies Debug Access port (DAP) access restrictions and system protection from eFuse and supervisory flash
 - iii. Authenticates flash boot (only in SECURE life-cycle stage) and transfers control to it
- 3. CM0+ executes flash boot (from Supervisory flash @0x1700 2000)**
 - i. Debug pins are configured as per the SWD/JTAG spec^[17]
 - ii. Sets CM0+ vector offset register (CM0_VTOR part of the Arm® system space) to the beginning of flash (@0x1000 0000)
 - iii. CM0+ branches to its Reset handler
- 4. CM0+ starts execution**
 - i. Moves CM0+ vector table to SRAM (updates CM0+ vector table base)
 - ii. Sets CM4_VECTOR_TABLE_BASE (@0x0000 0200) to the location of CM4 vector table mentioned in flash (specified in CM4 linker definition file)
 - iii. Releases CM4 from reset
 - iv. Continues execution of CM0+ user application
- 5. CM4 executes directly from either code-flash or SRAM**
 - i. CM4 branches to its Reset handler
 - ii. Continues execution of CM4 user application

Note

17. Port configuration of SWD/JTAG pins will be changed from the default GPIO mode to support debugging after the boot process, refer to **Table 11-1** for pin assignments.

9 Pin assignment

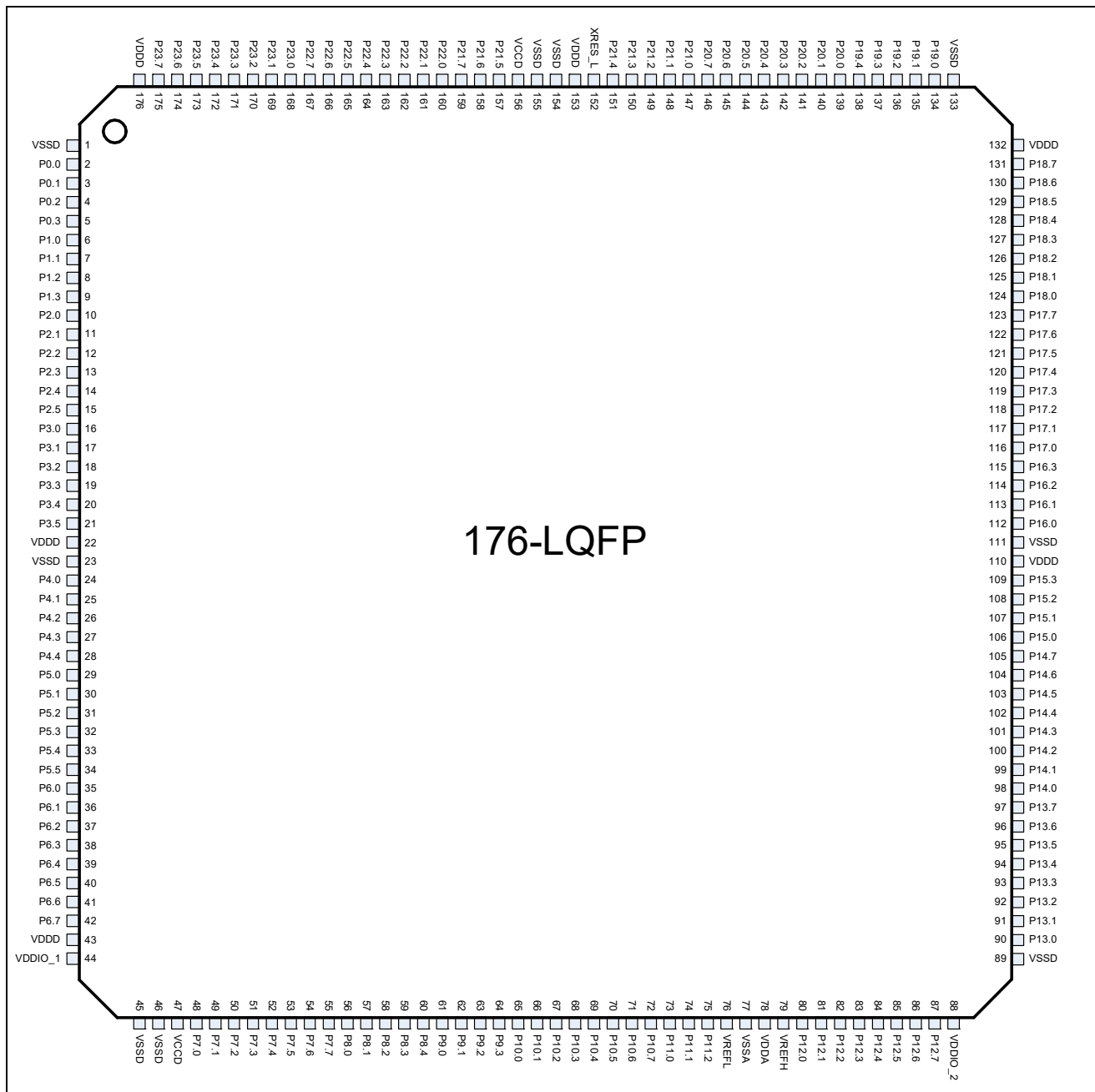


Figure 9-1 176-LQFP pin assignment

32-bit Arm® Cortex® -M4F Microcontroller TRAVEO™ T2G Family CYT2B7



Pin assignment

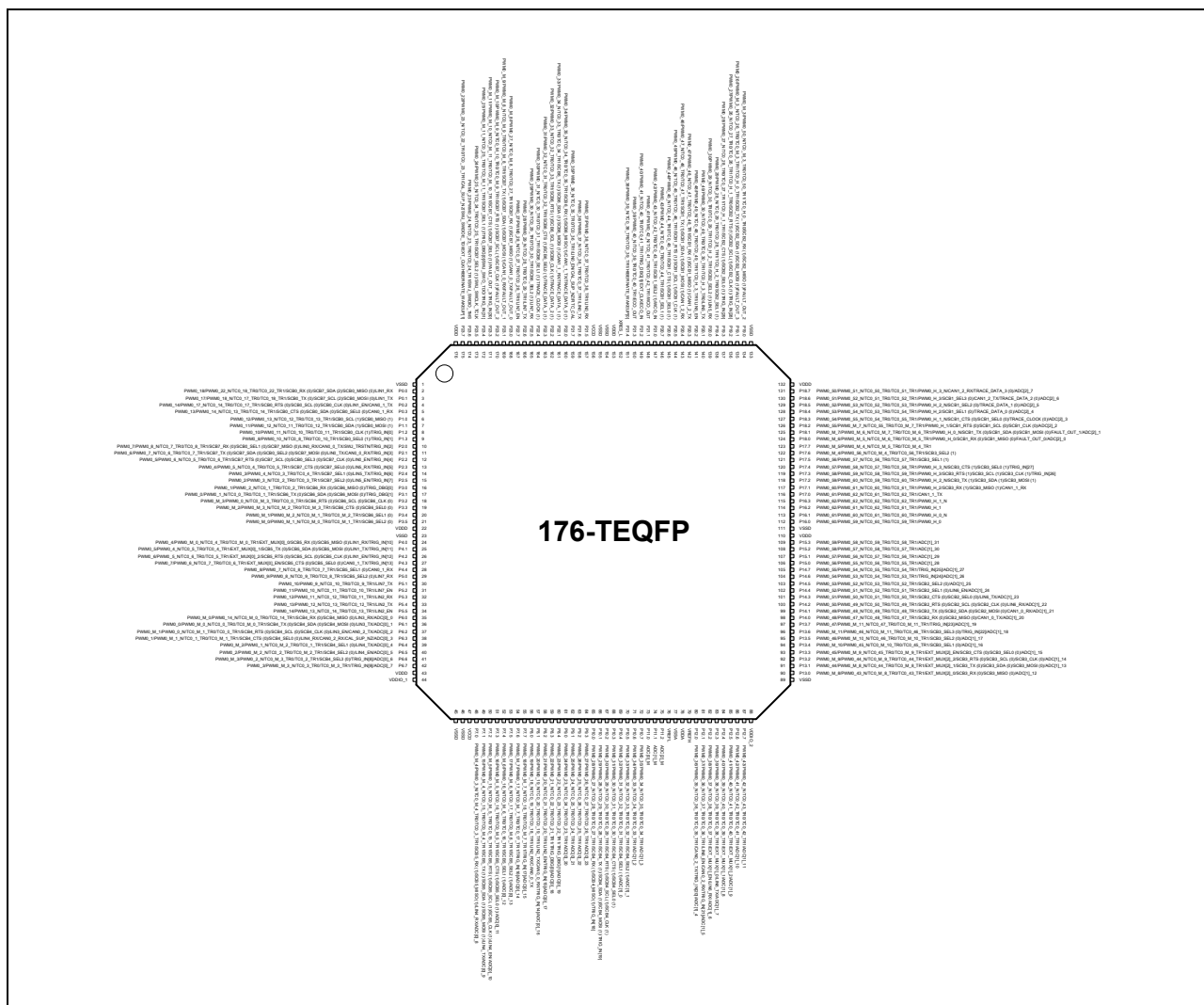


Figure 9-2 176-LQFP pin assignment with alternate functions

32-bit Arm® Cortex® -M4F Microcontroller TRAVEO™ T2G Family CYT2B7



Pin assignment

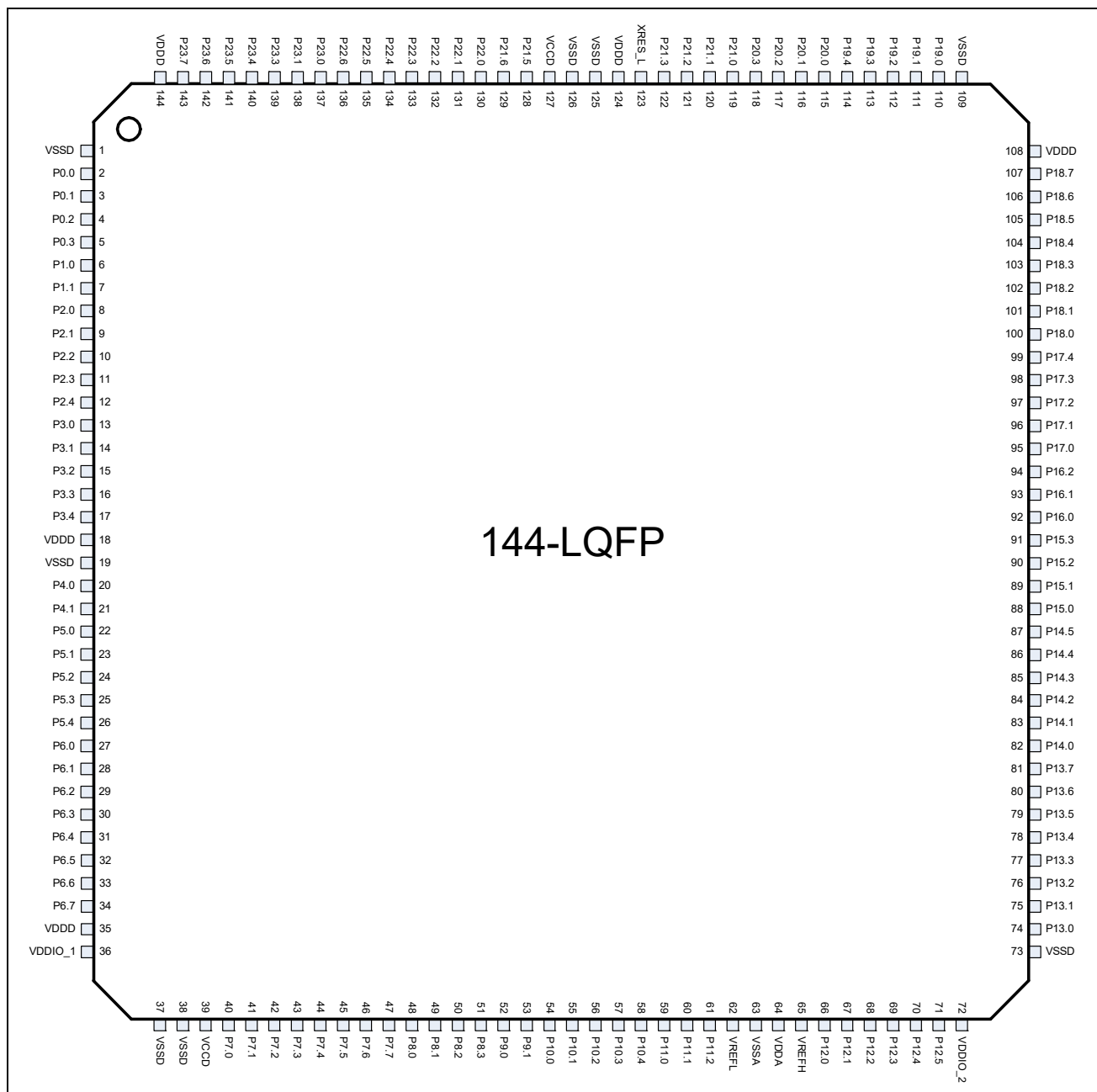


Figure 9-3 144-LQFP pin assignment



Pin assignment

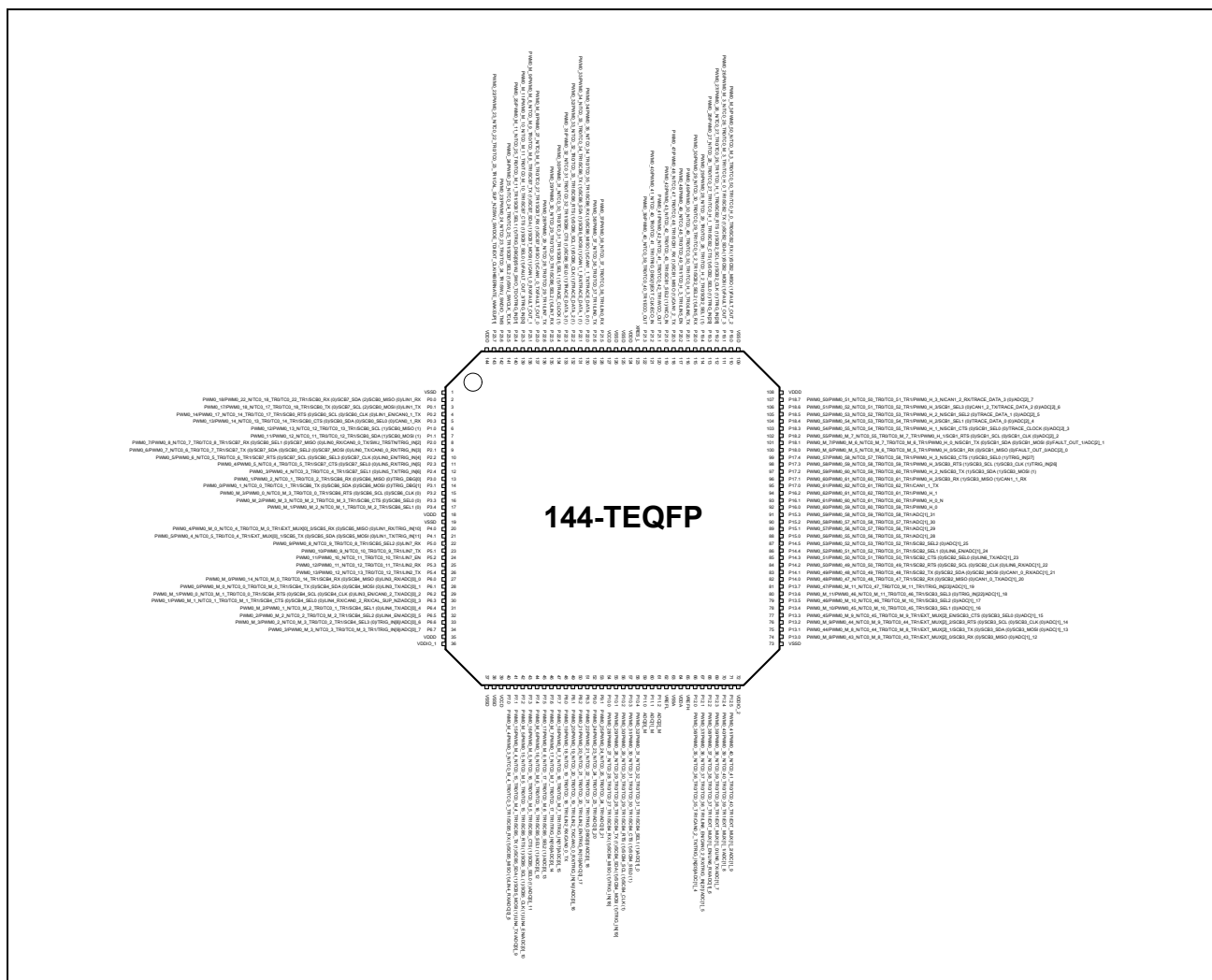


Figure 9-4 144-LQFP pin assignment with alternate functions

Pin assignment

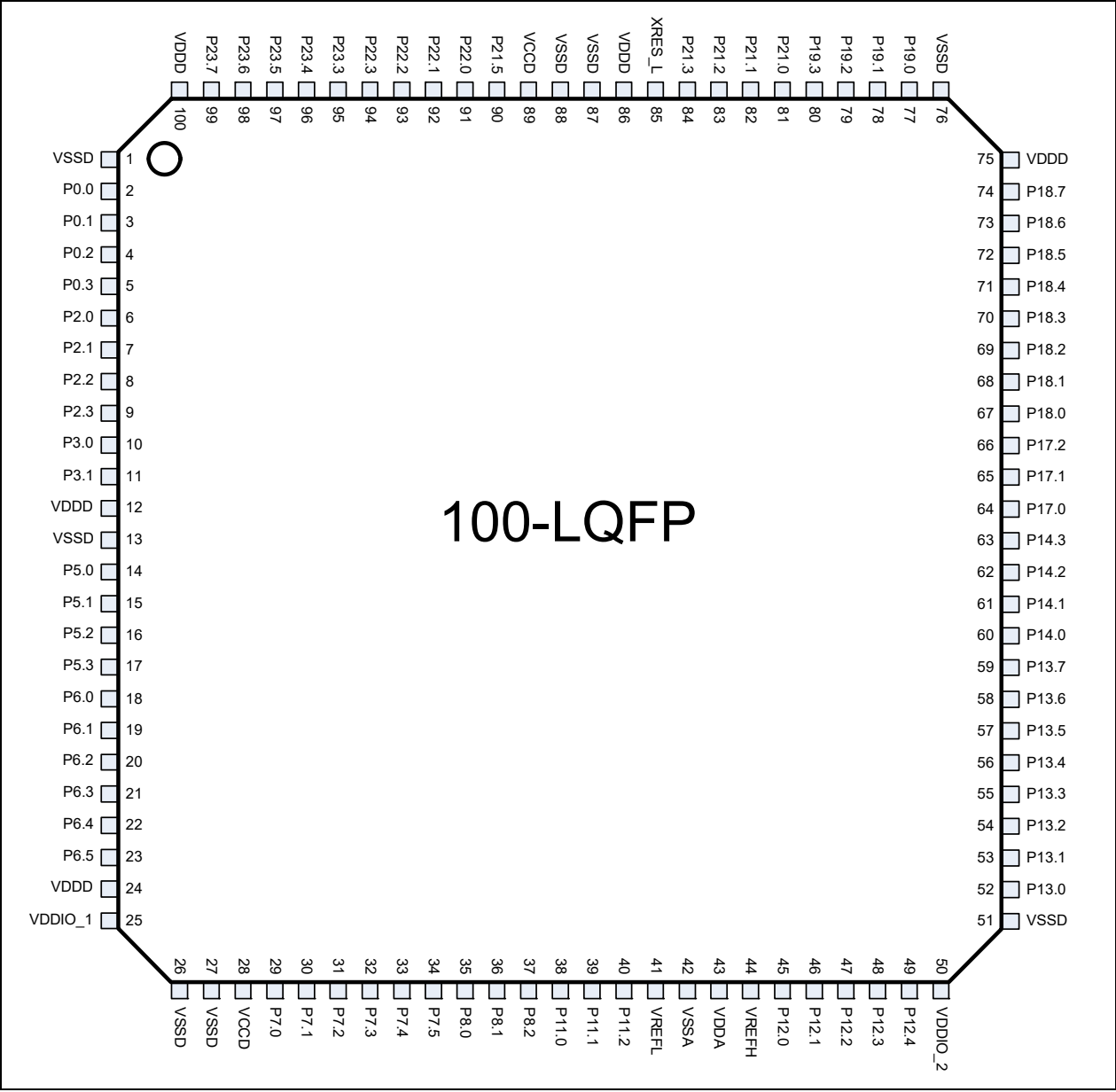


Figure 9-5 100-LQFP pin assignment

32-bit Arm® Cortex® -M4F Microcontroller TRAVEO™ T2G Family CYT2B7



Pin assignment

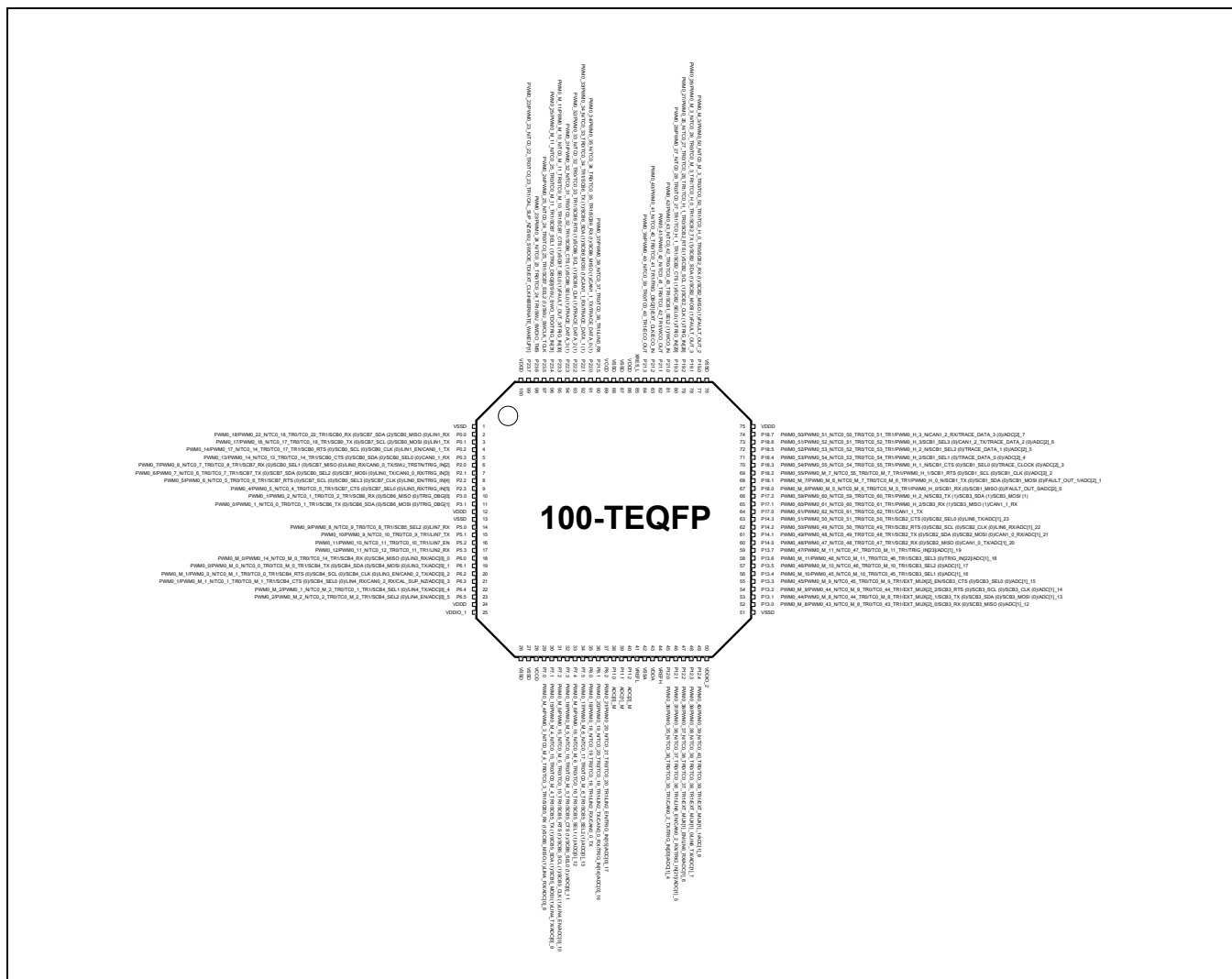


Figure 9-6 100-LQFP pin assignment with alternate functions

Pin assignment

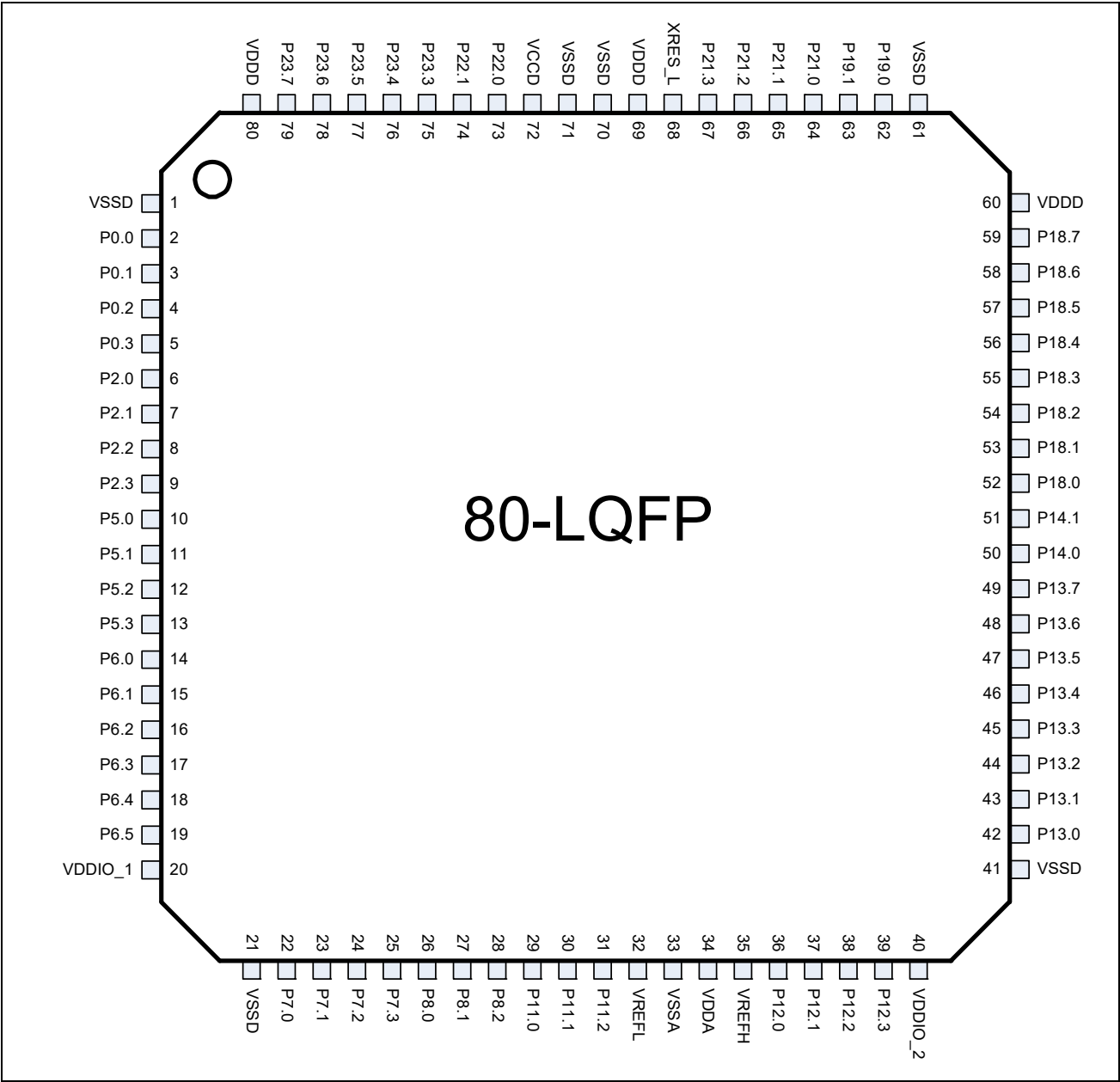


Figure 9-7 80-LQFP pin assignment

Pin assignment

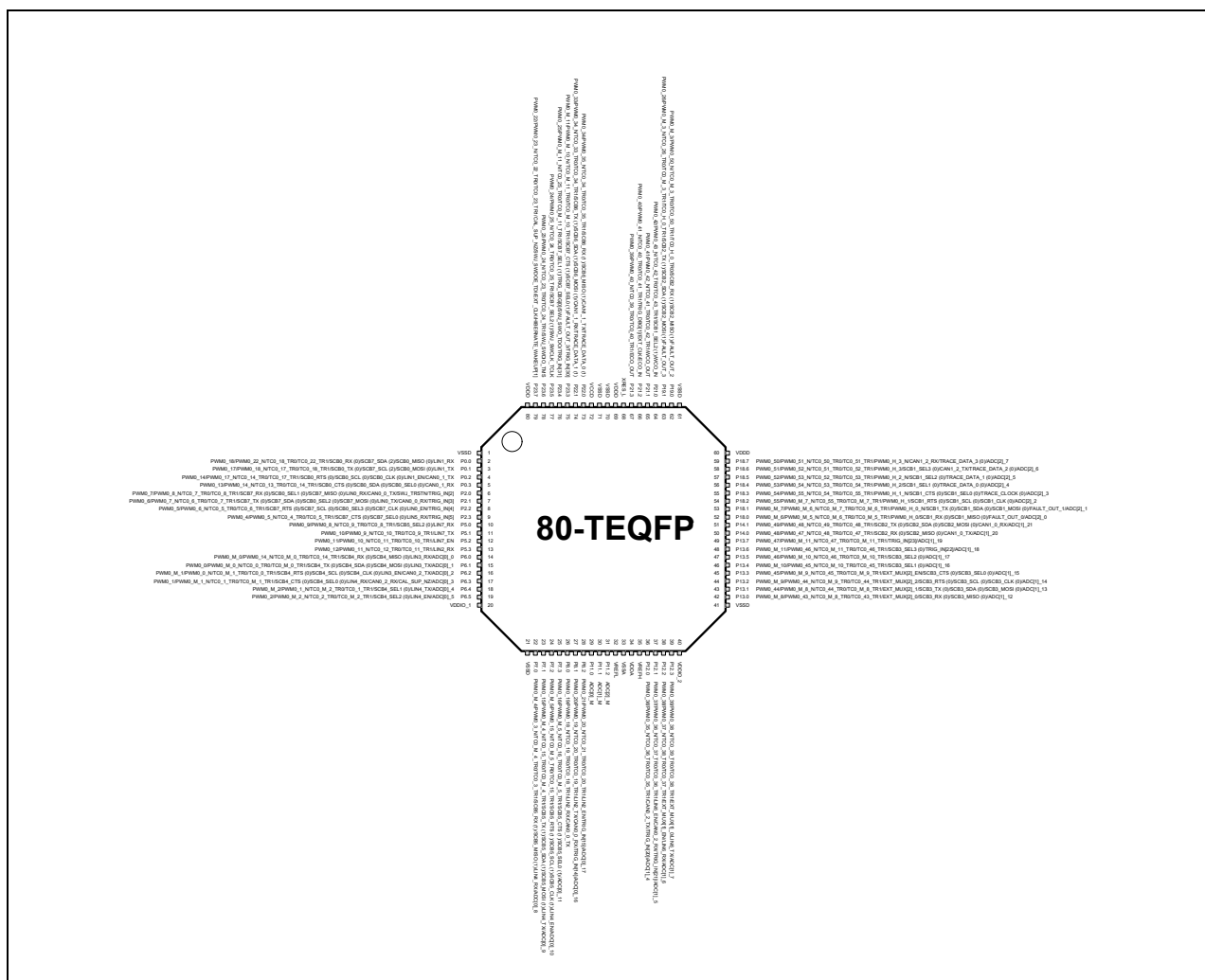


Figure 9-8 80-LQFP pin assignment with alternate functions

Pin assignment

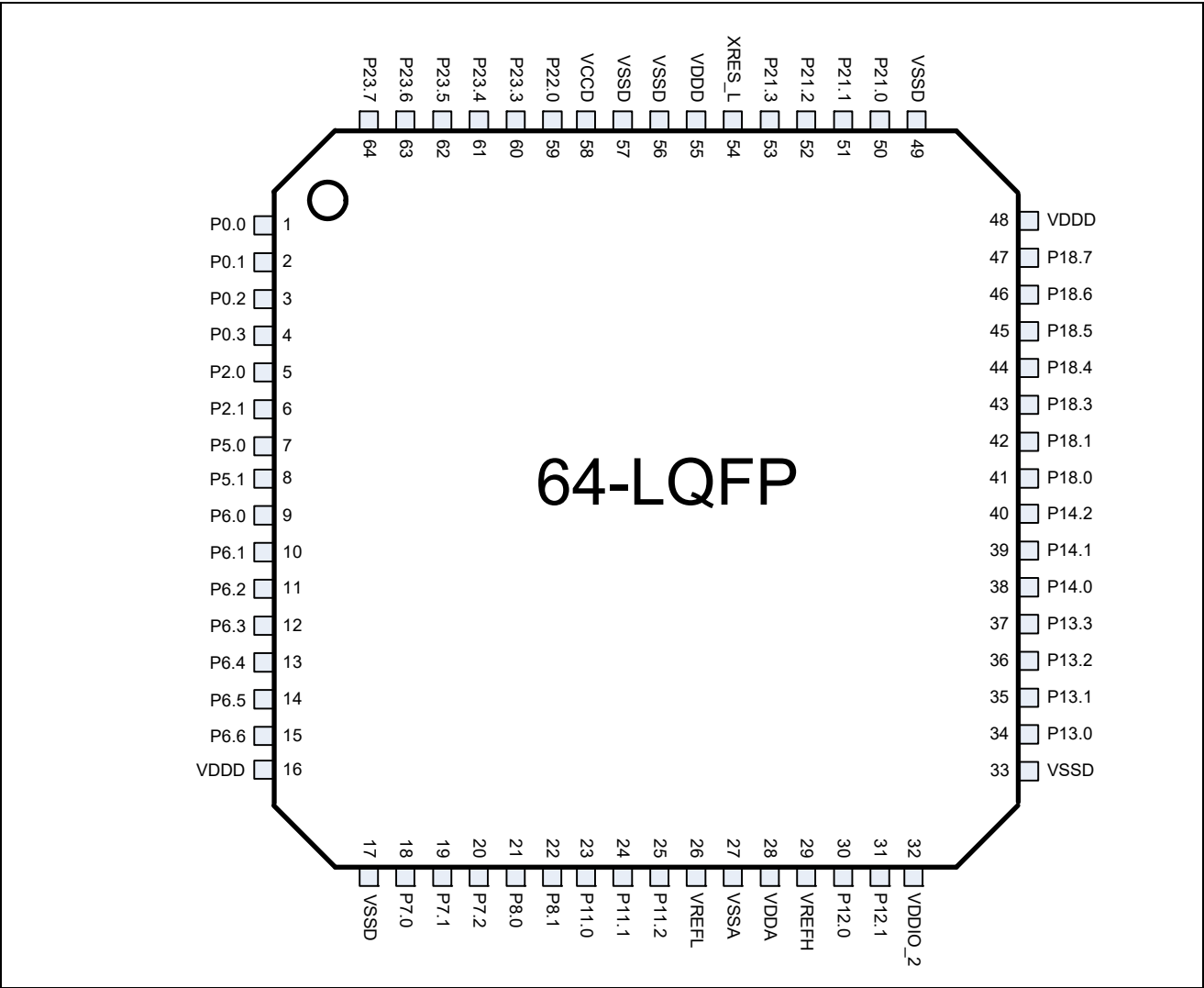


Figure 9-9 64-LQFP pin assignment

10 High-speed I/O matrix connections

Table 10-1 HSIOM connections reference

| Name | Number | Description |
|---------------------|--------|---------------------------|
| HSIOM_SEL_GPIO | 0 | GPIO controls 'out' |
| HSIOM_SEL_GPIO_DSI | 1 | Reserved |
| HSIOM_SEL_DSI_DSI | 2 | |
| HSIOM_SEL_DSI_GPIO | 3 | |
| HSIOM_SEL_AMUXA | 4 | |
| HSIOM_SEL_AMUXB | 5 | |
| HSIOM_SEL_AMUXA_DSI | 6 | |
| HSIOM_SEL_AMUXB_DSI | 7 | |
| HSIOM_SEL_ACT_0 | 8 | Active functionality 0 |
| HSIOM_SEL_ACT_1 | 9 | Active functionality 1 |
| HSIOM_SEL_ACT_2 | 10 | Active functionality 2 |
| HSIOM_SEL_ACT_3 | 11 | Active functionality 3 |
| HSIOM_SEL_DS_0 | 12 | DeepSleep functionality 0 |
| HSIOM_SEL_DS_1 | 13 | DeepSleep functionality 1 |
| HSIOM_SEL_DS_2 | 14 | DeepSleep functionality 2 |
| HSIOM_SEL_DS_3 | 15 | DeepSleep functionality 3 |
| HSIOM_SEL_ACT_4 | 16 | Active functionality 4 |
| HSIOM_SEL_ACT_5 | 17 | Active functionality 5 |
| HSIOM_SEL_ACT_6 | 18 | Active functionality 6 |
| HSIOM_SEL_ACT_7 | 19 | Active functionality 7 |
| HSIOM_SEL_ACT_8 | 20 | Active functionality 8 |
| HSIOM_SEL_ACT_9 | 21 | Active functionality 9 |
| HSIOM_SEL_ACT_10 | 22 | Active functionality 10 |
| HSIOM_SEL_ACT_11 | 23 | Active functionality 11 |
| HSIOM_SEL_ACT_12 | 24 | Active functionality 12 |
| HSIOM_SEL_ACT_13 | 25 | Active functionality 13 |
| HSIOM_SEL_ACT_14 | 26 | Active functionality 14 |
| HSIOM_SEL_ACT_15 | 27 | Active functionality 15 |
| HSIOM_SEL_DS_4 | 28 | DeepSleep functionality 4 |
| HSIOM_SEL_DS_5 | 29 | DeepSleep functionality 5 |
| HSIOM_SEL_DS_6 | 30 | DeepSleep functionality 6 |
| HSIOM_SEL_DS_7 | 31 | DeepSleep functionality 7 |

11 Package pin list and alternate functions

Most pins have alternate functionality, as specified in [Table 11-1](#).

Port 11 has the following additional features,

- Ability to pass full-level analog signals to the SAR without clipping to V_{DD} in cases where $V_{DD} < V_{DDA}$
- Ability to simultaneously capture all three ADC signals with highest priority (ADC[0:2]_M)
- Lower noise, for the most sensitive sensors

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O^[21, 22]

| Name | HCon#0 ^[18] | Package | | | | | | | | | | DeepSleep Mapping ^[20] | | | | Analog | SMARTIO |
|------|------------------------|----------|----------|----------|---------|---------|-----------------------|-----------|-------|---------------|--|-----------------------------------|--|--|--|--------|---------|
| | | 176-LQFP | 144-LQFP | 100-LQFP | 80-LQFP | 64-LQFP | HCon#14 | HCon#29 | | HCon#30 | | | | | | | |
| | | Pin | Pin | Pin | Pin | Pin | DS #0 ^[19] | DS #1 | DS #2 | | | | | | | | |
| P0.0 | GPIO_ENH | 2 | 2 | 2 | 2 | 1 | | | | SCB0_MISO (0) | | | | | | | |
| P0.1 | GPIO_ENH | 3 | 3 | 3 | 3 | 2 | | | | SCB0_MOSI (0) | | | | | | | |
| P0.2 | GPIO_ENH | 4 | 4 | 4 | 4 | 3 | SCB0_SCL (0) | | | SCB0_CLK (0) | | | | | | | |
| P0.3 | GPIO_ENH | 5 | 5 | 5 | 5 | 4 | SCB0_SDA (0) | | | SCB0_SELO (0) | | | | | | | |
| P1.0 | GPIO_STD | 6 | 6 | NA | NA | NA | SCB0_SCL (1) | | | SCB0_MISO (1) | | | | | | | |
| P1.1 | GPIO_STD | 7 | 7 | NA | NA | NA | SCB0_SDA (1) | | | SCB0_MOSI (1) | | | | | | | |
| P1.2 | GPIO_STD | 8 | NA | NA | NA | NA | | | | SCB0_CLK (1) | | | | | | | |
| P1.3 | GPIO_STD | 9 | NA | NA | NA | NA | | | | SCB0_SELO (1) | | | | | | | |
| P2.0 | GPIO_STD | 10 | 8 | 6 | 6 | 5 | | SWJ_TRSTN | | SCB0_SEL1 (0) | | | | | | | |
| P2.1 | GPIO_STD | 11 | 9 | 7 | 7 | 6 | | | | SCB0_SEL2 (0) | | | | | | | |
| P2.2 | GPIO_STD | 12 | 10 | 8 | 8 | NA | | | | SCB0_SEL3 (0) | | | | | | | |
| P2.3 | GPIO_STD | 13 | 11 | 9 | 9 | NA | | | | | | | | | | | |
| P2.4 | GPIO_STD | 14 | 12 | NA | NA | NA | | | | | | | | | | | |
| P2.5 | GPIO_STD | 15 | NA | NA | NA | NA | | | | | | | | | | | |
| P3.0 | GPIO_STD | 16 | 13 | 10 | NA | NA | | | | | | | | | | | |
| P3.1 | GPIO_STD | 17 | 14 | 11 | NA | NA | | | | | | | | | | | |
| P3.2 | GPIO_STD | 18 | 15 | NA | NA | NA | | | | | | | | | | | |

Notes

- HCon refers to High Speed I/O matrix connection reference as per [Table 10-1](#).
- DeepSleep ordering (DS #0, DS #1, DS #2) does not have any impact on choosing any alternate functions; the HSIOM module handles the individual alternate function assignment.
- All port pin functions available in DeepSleep mode are also available in Active mode.
- Refer to [Table 13-2](#) for more information on pin multiplexer abbreviations used.
- For any function marked with an identifier (n), the AC timing is only guaranteed within the respective group "n".

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O^[21, 22] (continued)

| Name | HCon#0 ^[18] | Package | | | | | | | | | | DeepSleep Mapping ^[20] | | | | Analog | SMARTIO |
|------|------------------------|----------|----------|----------|---------|---------|-----------------------|---------|-------|---------|--|-----------------------------------|-----------|--|--|--------|---------|
| | | 176-LQFP | 144-LQFP | 100-LQFP | 80-LQFP | 64-LQFP | HCon#14 | HCon#29 | | HCon#30 | | | | | | | |
| | | Pin | Pin | Pin | Pin | Pin | DS #0 ^[19] | DS #1 | DS #2 | | | | | | | | |
| P3.3 | GPIO_STD | 19 | 16 | NA | NA | NA | NA | NA | | | | | | | | | |
| P3.4 | GPIO_STD | 20 | 17 | NA | NA | NA | NA | NA | | | | | | | | | |
| P3.5 | GPIO_STD | 21 | NA | NA | NA | NA | NA | NA | | | | | | | | | |
| P4.0 | GPIO_STD | 24 | 20 | NA | NA | NA | NA | NA | | | | | | | | | |
| P4.1 | GPIO_STD | 25 | 21 | NA | NA | NA | NA | NA | | | | | | | | | |
| P4.2 | GPIO_STD | 26 | NA | NA | NA | NA | NA | NA | | | | | | | | | |
| P4.3 | GPIO_STD | 27 | NA | NA | NA | NA | NA | NA | | | | | | | | | |
| P4.4 | GPIO_STD | 28 | NA | NA | NA | NA | NA | NA | | | | | | | | | |
| P5.0 | GPIO_STD | 29 | 22 | 14 | 10 | 7 | | | | | | | | | | | |
| P5.1 | GPIO_STD | 30 | 23 | 15 | 11 | 8 | | | | | | | | | | | |
| P5.2 | GPIO_STD | 31 | 24 | 16 | 12 | NA | | | | | | | | | | | |
| P5.3 | GPIO_STD | 32 | 25 | 17 | 13 | NA | | | | | | | | | | | |
| P5.4 | GPIO_STD | 33 | 26 | NA | NA | NA | | | | | | | | | | | |
| P5.5 | GPIO_STD | 34 | NA | NA | NA | NA | | | | | | | | | | | |
| P6.0 | GPIO_STD | 35 | 27 | 18 | 14 | 9 | | | | | | | ADC[0]_0 | | | | |
| P6.1 | GPIO_STD | 36 | 28 | 19 | 15 | 10 | | | | | | | ADC[0]_1 | | | | |
| P6.2 | GPIO_STD | 37 | 29 | 20 | 16 | 11 | | | | | | | ADC[0]_2 | | | | |
| P6.3 | GPIO_STD | 38 | 30 | 21 | 17 | 12 | | | | | | | ADC[0]_3 | | | | |
| P6.4 | GPIO_STD | 39 | 31 | 22 | 18 | 13 | | | | | | | ADC[0]_4 | | | | |
| P6.5 | GPIO_STD | 40 | 32 | 23 | 19 | 14 | | | | | | | ADC[0]_5 | | | | |
| P6.6 | GPIO_STD | 41 | 33 | NA | NA | 15 | | | | | | | ADC[0]_6 | | | | |
| P6.7 | GPIO_STD | 42 | 34 | NA | NA | NA | | | | | | | ADC[0]_7 | | | | |
| P7.0 | GPIO_STD | 48 | 40 | 29 | 22 | 18 | | | | | | | ADC[0]_8 | | | | |
| P7.1 | GPIO_STD | 49 | 41 | 30 | 23 | 19 | | | | | | | ADC[0]_9 | | | | |
| P7.2 | GPIO_STD | 50 | 42 | 31 | 24 | 20 | | | | | | | ADC[0]_10 | | | | |
| P7.3 | GPIO_STD | 51 | 43 | 32 | 25 | NA | | | | | | | ADC[0]_11 | | | | |
| P7.4 | GPIO_STD | 52 | 44 | 33 | NA | NA | | | | | | | ADC[0]_12 | | | | |
| P7.5 | GPIO_STD | 53 | 45 | 34 | NA | NA | | | | | | | ADC[0]_13 | | | | |
| P7.6 | GPIO_STD | 54 | 46 | NA | NA | NA | | | | | | | ADC[0]_14 | | | | |
| P7.7 | GPIO_STD | 55 | 47 | NA | NA | NA | | | | | | | ADC[0]_15 | | | | |
| P8.0 | GPIO_STD | 56 | 48 | 35 | 26 | 21 | | | | | | | | | | | |

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O^[21, 22] (continued)

| Name | HCon#0 ^[18] | DeepSleep Mapping ^[20] | | | | | | | | | | Analog | SMARTIO | | | | |
|-------|------------------------|-----------------------------------|----------|----------|---------|---------|-----------------------|-------|-------|-------|--|-----------|-------------|---------|--|---------|--|
| | | Package | | | | | HCon#14 | | | | | | | HCon#29 | | HCon#30 | |
| | | 176-LQFP | 144-LQFP | 100-LQFP | 80-LQFP | 64-LQFP | DS #0 ^[19] | DS #1 | DS #2 | DS #2 | | | | | | | |
| | I/O Type | Pin | Pin | Pin | Pin | Pin | | | | | | | | | | | |
| P8.1 | GPIO_STD | 57 | 49 | 36 | 27 | 22 | | | | | | ADC[0]_16 | | | | | |
| P8.2 | GPIO_STD | 58 | 50 | 37 | 28 | NA | | | | | | ADC[0]_17 | | | | | |
| P8.3 | GPIO_STD | 59 | 51 | NA | NA | NA | | | | | | ADC[0]_18 | | | | | |
| P8.4 | GPIO_STD | 60 | NA | NA | NA | NA | | | | | | ADC[0]_19 | | | | | |
| P9.0 | GPIO_STD | 61 | 52 | NA | NA | NA | | | | | | ADC[0]_20 | | | | | |
| P9.1 | GPIO_STD | 62 | 53 | NA | NA | NA | | | | | | ADC[0]_21 | | | | | |
| P9.2 | GPIO_STD | 63 | NA | NA | NA | NA | | | | | | ADC[0]_22 | | | | | |
| P9.3 | GPIO_STD | 64 | NA | NA | NA | NA | | | | | | ADC[0]_23 | | | | | |
| P10.0 | GPIO_STD | 65 | 54 | NA | NA | NA | | | | | | | | | | | |
| P10.1 | GPIO_STD | 66 | 55 | NA | NA | NA | | | | | | | | | | | |
| P10.2 | GPIO_STD | 67 | 56 | NA | NA | NA | | | | | | | | | | | |
| P10.3 | GPIO_STD | 68 | 57 | NA | NA | NA | | | | | | | | | | | |
| P10.4 | GPIO_STD | 69 | 58 | NA | NA | NA | | | | | | ADC[1]_0 | | | | | |
| P10.5 | GPIO_STD | 70 | NA | NA | NA | NA | | | | | | ADC[1]_1 | | | | | |
| P10.6 | GPIO_STD | 71 | NA | NA | NA | NA | | | | | | ADC[1]_2 | | | | | |
| P10.7 | GPIO_STD | 72 | NA | NA | NA | NA | | | | | | ADC[1]_3 | | | | | |
| P11.0 | GPIO_STD | 73 | 59 | 38 | 29 | 23 | | | | | | ADC[0]_M | | | | | |
| P11.1 | GPIO_STD | 74 | 60 | 39 | 30 | 24 | | | | | | ADC[1]_M | | | | | |
| P11.2 | GPIO_STD | 75 | 61 | 40 | 31 | 25 | | | | | | ADC[2]_M | | | | | |
| P12.0 | GPIO_STD | 80 | 66 | 45 | 36 | 30 | | | | | | ADC[1]_4 | SMARTIO12_0 | | | | |
| P12.1 | GPIO_STD | 81 | 67 | 46 | 37 | 31 | | | | | | ADC[1]_5 | SMARTIO12_1 | | | | |
| P12.2 | GPIO_STD | 82 | 68 | 47 | 38 | NA | | | | | | ADC[1]_6 | SMARTIO12_2 | | | | |
| P12.3 | GPIO_STD | 83 | 69 | 48 | 39 | NA | | | | | | ADC[1]_7 | SMARTIO12_3 | | | | |
| P12.4 | GPIO_STD | 84 | 70 | 49 | NA | NA | | | | | | ADC[1]_8 | SMARTIO12_4 | | | | |
| P12.5 | GPIO_STD | 85 | 71 | NA | NA | NA | | | | | | ADC[1]_9 | SMARTIO12_5 | | | | |
| P12.6 | GPIO_STD | 86 | NA | NA | NA | NA | | | | | | ADC[1]_10 | SMARTIO12_6 | | | | |
| P12.7 | GPIO_STD | 87 | NA | NA | NA | NA | | | | | | ADC[1]_11 | SMARTIO12_7 | | | | |
| P13.0 | GPIO_STD | 90 | 74 | 52 | 42 | 34 | | | | | | ADC[1]_12 | SMARTIO13_0 | | | | |
| P13.1 | GPIO_STD | 91 | 75 | 53 | 43 | 35 | | | | | | ADC[1]_13 | SMARTIO13_1 | | | | |
| P13.2 | GPIO_STD | 92 | 76 | 54 | 44 | 36 | | | | | | ADC[1]_14 | SMARTIO13_2 | | | | |
| P13.3 | GPIO_STD | 93 | 77 | 55 | 45 | 37 | | | | | | ADC[1]_15 | SMARTIO13_3 | | | | |

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O^[21, 22] (continued)

| Name | HCon#0 ^[18] I/O Type | Package | | | | | | | | | | DeepSleep Mapping ^[20] | | | | Analog | SMARTIO |
|-------|------------------------------------|----------|----------|----------|---------|---------|----------------------------------|------------------|------------------|--|-----------|-----------------------------------|--|--|--|--------|---------|
| | | 176-LQFP | 144-LQFP | 100-LQFP | 80-LQFP | 64-LQFP | HCon#14 DS #0 ^[19] | HCon#29 DS #1 | HCon#30 DS #2 | | | | | | | | |
| | | Pin | Pin | Pin | Pin | Pin | Pin | Pin | Pin | | | | | | | | |
| P13.4 | GPIO_STD | 94 | 78 | 56 | 46 | NA | | | | | ADC[1]_16 | SMARTIO13_4 | | | | | |
| P13.5 | GPIO_STD | 95 | 79 | 57 | 47 | NA | | | | | ADC[1]_17 | SMARTIO13_5 | | | | | |
| P13.6 | GPIO_STD | 96 | 80 | 58 | 48 | NA | | | | | ADC[1]_18 | SMARTIO13_6 | | | | | |
| P13.7 | GPIO_STD | 97 | 81 | 59 | 49 | NA | | | | | ADC[1]_19 | SMARTIO13_7 | | | | | |
| P14.0 | GPIO_STD | 98 | 82 | 60 | 50 | 38 | | | | | ADC[1]_20 | SMARTIO14_0 | | | | | |
| P14.1 | GPIO_STD | 99 | 83 | 61 | 51 | 39 | | | | | ADC[1]_21 | SMARTIO14_1 | | | | | |
| P14.2 | GPIO_STD | 100 | 84 | 62 | NA | 40 | | | | | ADC[1]_22 | SMARTIO14_2 | | | | | |
| P14.3 | GPIO_STD | 101 | 85 | 63 | NA | NA | | | | | ADC[1]_23 | SMARTIO14_3 | | | | | |
| P14.4 | GPIO_STD | 102 | 86 | NA | NA | NA | | | | | ADC[1]_24 | SMARTIO14_4 | | | | | |
| P14.5 | GPIO_STD | 103 | 87 | NA | NA | NA | | | | | ADC[1]_25 | SMARTIO14_5 | | | | | |
| P14.6 | GPIO_STD | 104 | NA | NA | NA | NA | | | | | ADC[1]_26 | SMARTIO14_6 | | | | | |
| P14.7 | GPIO_STD | 105 | NA | NA | NA | NA | | | | | ADC[1]_27 | SMARTIO14_7 | | | | | |
| P15.0 | GPIO_STD | 106 | 88 | NA | NA | NA | | | | | ADC[1]_28 | SMARTIO15_0 | | | | | |
| P15.1 | GPIO_STD | 107 | 89 | NA | NA | NA | | | | | ADC[1]_29 | SMARTIO15_1 | | | | | |
| P15.2 | GPIO_STD | 108 | 90 | NA | NA | NA | | | | | ADC[1]_30 | SMARTIO15_2 | | | | | |
| P15.3 | GPIO_STD | 109 | 91 | NA | NA | NA | | | | | ADC[1]_31 | SMARTIO15_3 | | | | | |
| P16.0 | GPIO_STD | 112 | 92 | NA | NA | NA | | | | | | | | | | | |
| P16.1 | GPIO_STD | 113 | 93 | NA | NA | NA | | | | | | | | | | | |
| P16.2 | GPIO_STD | 114 | 94 | NA | NA | NA | | | | | | | | | | | |
| P16.3 | GPIO_STD | 115 | NA | NA | NA | NA | | | | | | | | | | | |
| P17.0 | GPIO_STD | 116 | 95 | 64 | NA | NA | | | | | | SMARTIO17_0 | | | | | |
| P17.1 | GPIO_STD | 117 | 96 | 65 | NA | NA | | | | | | SMARTIO17_1 | | | | | |
| P17.2 | GPIO_STD | 118 | 97 | 66 | NA | NA | | | | | | SMARTIO17_2 | | | | | |
| P17.3 | GPIO_STD | 119 | 98 | NA | NA | NA | | | | | | SMARTIO17_3 | | | | | |
| P17.4 | GPIO_STD | 120 | 99 | NA | NA | NA | | | | | | SMARTIO17_4 | | | | | |
| P17.5 | GPIO_STD | 121 | NA | NA | NA | NA | | | | | | SMARTIO17_5 | | | | | |
| P17.6 | GPIO_STD | 122 | NA | NA | NA | NA | | | | | | SMARTIO17_6 | | | | | |
| P17.7 | GPIO_STD | 123 | NA | NA | NA | NA | | | | | | SMARTIO17_7 | | | | | |
| P18.0 | GPIO_STD | 124 | 100 | 67 | 52 | 41 | | | | | ADC[2]_0 | | | | | | |
| P18.1 | GPIO_STD | 125 | 101 | 68 | 53 | 42 | | | | | ADC[2]_1 | | | | | | |
| P18.2 | GPIO_STD | 126 | 102 | 69 | 54 | NA | | | | | ADC[2]_2 | | | | | | |

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O^[21, 22] (continued)

| Name | HCon#0 ^[18] I/O Type | Package | | | | | | | | | | DeepSleep Mapping ^[20] | | | | Analog | SMARTIO |
|-----------------------|------------------------------------|----------|----------|----------|---------|---------|-----------------------|---------|---------|--|---------|-----------------------------------|--|-------------------------|--|--------|---------|
| | | 176-LQFP | 144-LQFP | 100-LQFP | 80-LQFP | 64-LQFP | HCon#14 | HCon#29 | HCon#30 | | | | | | | | |
| | | Pin | Pin | Pin | Pin | Pin | DS #0 ^[19] | DS #1 | DS #2 | | | | | | | | |
| P18.3 | GPIO_STD | 127 | 103 | 70 | 55 | 43 | | | | | | | | ADC[2]_3 | | | |
| P18.4 | GPIO_STD | 128 | 104 | 71 | 56 | 44 | | | | | | | | ADC[2]_4 | | | |
| P18.5 | GPIO_STD | 129 | 105 | 72 | 57 | 45 | | | | | | | | ADC[2]_5 | | | |
| P18.6 | GPIO_STD | 130 | 106 | 73 | 58 | 46 | | | | | | | | ADC[2]_6 | | | |
| P18.7 | GPIO_STD | 131 | 107 | 74 | 59 | 47 | | | | | | | | ADC[2]_7 | | | |
| P19.0 | GPIO_STD | 134 | 110 | 77 | 62 | NA | | | | | | | | | | | |
| P19.1 | GPIO_STD | 135 | 111 | 78 | 63 | NA | | | | | | | | | | | |
| P19.2 | GPIO_STD | 136 | 112 | 79 | NA | NA | | | | | | | | | | | |
| P19.3 | GPIO_STD | 137 | 113 | 80 | NA | NA | | | | | | | | | | | |
| P19.4 | GPIO_STD | 138 | 114 | NA | NA | NA | | | | | | | | | | | |
| P20.0 | GPIO_STD | 139 | 115 | NA | NA | NA | | | | | | | | | | | |
| P20.1 | GPIO_STD | 140 | 116 | NA | NA | NA | | | | | | | | | | | |
| P20.2 | GPIO_STD | 141 | 117 | NA | NA | NA | | | | | | | | | | | |
| P20.3 | GPIO_STD | 142 | 118 | NA | NA | NA | | | | | | | | | | | |
| P20.4 | GPIO_STD | 143 | NA | NA | NA | NA | | | | | | | | | | | |
| P20.5 | GPIO_STD | 144 | NA | NA | NA | NA | | | | | | | | | | | |
| P20.6 | GPIO_STD | 145 | NA | NA | NA | NA | | | | | | | | | | | |
| P20.7 | GPIO_STD | 146 | NA | NA | NA | NA | | | | | | | | | | | |
| P21.0 | GPIO_STD | 147 | 119 | 81 | 64 | 50 | | | | | | | | WCO_IN ^[23] | | | |
| P21.1 | GPIO_STD | 148 | 120 | 82 | 65 | 51 | | | | | | | | WCO_OUT ^[23] | | | |
| P21.2 | GPIO_STD | 149 | 121 | 83 | 66 | 52 | | | | | | | | ECO_IN ^[23] | | | |
| P21.3 | GPIO_STD | 150 | 122 | 84 | 67 | 53 | | | | | | | | ECO_OUT ^[23] | | | |
| P21.4 ^[24] | GPIO_STD | 151 | NA | NA | NA | NA | | | | | | | | HIBERNATE_WAKEUP[0] | | | |
| P21.5 | GPIO_STD | 157 | 128 | 90 | NA | NA | | | | | | | | | | | |
| P21.6 | GPIO_STD | 158 | 129 | NA | NA | NA | | | | | | | | | | | |
| P21.7 | GPIO_STD | 159 | NA | NA | NA | NA | | | | | RTC_CAL | | | | | | |
| P22.0 | GPIO_STD | 160 | 130 | 91 | 73 | 59 | | | | | | | | | | | |
| P22.1 | GPIO_STD | 161 | 131 | 92 | 74 | NA | | | | | | | | | | | |
| P22.2 | GPIO_STD | 162 | 132 | 93 | NA | NA | | | | | | | | | | | |
| P22.3 | GPIO_STD | 163 | 133 | 94 | NA | NA | | | | | | | | | | | |
| P22.4 | GPIO_STD | 164 | 134 | NA | NA | NA | | | | | | | | | | | |

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O^[21, 22] (continued)

| Name | HCon#0 ^[18] I/O Type | Package | | | | | | DeepSleep Mapping ^[20] | | | | Analog | SMARTIO |
|-------|------------------------------------|----------|----------|----------|---------|---------|-----------------------|-----------------------------------|---------|--|---------------------|--------|---------|
| | | 176-LQFP | 144-LQFP | 100-LQFP | 80-LQFP | 64-LQFP | HCon#14 | HCon#29 | HCon#30 | | | | |
| | | Pin | Pin | Pin | Pin | Pin | DS #0 ^[19] | DS #1 | DS #2 | | | | |
| P22.5 | GPIO_STD | 165 | 135 | NA | NA | NA | | | | | | | |
| P22.6 | GPIO_STD | 166 | 136 | NA | NA | NA | | | | | | | |
| P22.7 | GPIO_STD | 167 | NA | NA | NA | NA | | | | | | | |
| P23.0 | GPIO_STD | 168 | 137 | NA | NA | NA | | | | | | | |
| P23.1 | GPIO_STD | 169 | 138 | NA | NA | NA | | | | | | | |
| P23.2 | GPIO_STD | 170 | NA | NA | NA | NA | | | | | | | |
| P23.3 | GPIO_STD | 171 | 139 | 95 | 75 | 60 | | | | | | | |
| P23.4 | GPIO_STD | 172 | 140 | 96 | 76 | 61 | | SWJ_SWO_TDO | | | | | |
| P23.5 | GPIO_STD | 173 | 141 | 97 | 77 | 62 | | SWJ_SWCLK_TCLK | | | | | |
| P23.6 | GPIO_STD | 174 | 142 | 98 | 78 | 63 | | SWJ_SWDIO_TMS | | | | | |
| P23.7 | GPIO_STD | 175 | 143 | 99 | 79 | 64 | | SWJ_SWDOE_TDI | | | HIBERNATE_WAKEUP[1] | | |

Notes

23. I/O pins that support an oscillator function (WCO or ECO) must be configured for high-impedance if the oscillator is enabled.
24. This I/O has increased leakage to ground when the V_{DD} supply is below the POR threshold.

Power pin assignments

12 Power pin assignments

Table 12-1 Power pin assignments

| Name | Package | | | | | Remarks |
|----------------------|--------------------|-----------------------|-------------------------------|----------------------------------|---------------------------------------|---|
| | 64-LQFP | 80-LQFP | 100-LQFP | 144-LQFP | 176-LQFP | |
| VDDD | 55, 48, 16 | 80, 69, 60 | 100, 86, 75, 24, 12 | 144, 124, 108, 35, 18 | 176, 153, 132, 110, 43, 22 | Main digital supply |
| VSSD | 57, 56, 49, 33, 17 | 71, 70, 61, 41, 21, 1 | 88, 87, 76, 51, 27, 26, 13, 1 | 126, 125, 109, 73, 38, 37, 19, 1 | 155, 154, 133, 111, 89, 46, 45, 23, 1 | Main digital ground |
| VDDIO_1 | NA | 20 | 25 | 36 | 44 | I/O supply for analog I/Os (except analog I/Os on V _{DDA}) |
| VDDIO_2 | 32 | 40 | 50 | 72 | 88 | I/O supply for analog I/Os (except analog I/Os on V _{DDA}), P11 |
| VCCD ^[25] | 58 | 72 | 89, 28 | 127, 39 | 156, 47 | Main regulated supply. Driven by LDO regulator (either internal LDO or external LDO/PMIC) |
| VREFH | 29 | 35 | 44 | 65 | 79 | High reference voltage for SAR ADCs |
| VREFL | 26 | 32 | 41 | 62 | 76 | Low reference voltage for SAR ADCs |
| VDDA | 28 | 34 | 43 | 64 | 78 | Main analog supply for SAR ADCs |
| VSSA | 27 | 33 | 42 | 63 | 77 | Main analog ground |
| XRES_L | 54 | 68 | 85 | 123 | 152 | Active LOW external reset input |

Note

25. The V_{CCD} pins must be connected together to ensure a low-impedance connection. (see the requirement in **Figure 26-2**)

13 Alternate function pin assignments

Table 13-1 Alternate pin functions in Active Mode^[28, 29]

| Active Mapping | | | | | | | | | | | | | |
|----------------|---|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|--|
| Name | HCon#8 ^[26] ACT#0 ^[27] | HCon#9 ACT#1 | HCon#10 ACT#2 | HCon#11 ACT#3 | HCon#16 ACT#4 | HCon#17 ACT#5 | HCon#18 ACT#6 | HCon#19 ACT#7 | HCon#20 ACT#8 | HCon#21 ACT#9 | HCon#26 ACT#14 | HCon#27 ACT#15 | |
| P0.0 | PWM0_18 | PWM0_22_N | TC0_18_TR0 | TC0_22_TR1 | | SCB0_RX (0) | SCB7_SDA (2) | | LIN1_RX | | | | |
| P0.1 | PWM0_17 | PWM0_18_N | TC0_17_TR0 | TC0_18_TR1 | | SCB0_TX (0) | SCB7_SCL (2) | | LIN1_TX | | | | |
| P0.2 | PWM0_14 | PWM0_17_N | TC0_14_TR0 | TC0_17_TR1 | | SCB0_RTS (0) | | | LIN1_EN | CAN0_1_TX | | | |
| P0.3 | PWM0_13 | PWM0_14_N | TC0_13_TR0 | TC0_14_TR1 | | SCB0_CTS (0) | | | | CAN0_1_RX | | | |
| P1.0 | PWM0_12 | PWM0_13_N | TC0_12_TR0 | TC0_13_TR1 | | | | | | | | | |
| P1.1 | PWM0_11 | PWM0_12_N | TC0_11_TR0 | TC0_12_TR1 | | | | | | | | | |
| P1.2 | PWM0_10 | PWM0_11_N | TC0_10_TR0 | TC0_11_TR1 | | | | | | | TRIG_IN[0] | | |
| P1.3 | PWM0_8 | PWM0_10_N | TC0_8_TR0 | TC0_10_TR1 | | | | | | | TRIG_IN[1] | | |
| P2.0 | PWM0_7 | PWM0_8_N | TC0_7_TR0 | TC0_8_TR1 | | SCB7_RX (0) | | SCB7_MISO (0) | LIN0_RX | CAN0_0_TX | TRIG_IN[2] | | |
| P2.1 | PWM0_6 | PWM0_7_N | TC0_6_TR0 | TC0_7_TR1 | | SCB7_TX (0) | SCB7_SDA (0) | SCB7_MOSI (0) | LIN0_TX | CAN0_0_RX | TRIG_IN[3] | | |
| P2.2 | PWM0_5 | PWM0_6_N | TC0_5_TR0 | TC0_6_TR1 | | SCB7_RTS (0) | SCB7_SCL (0) | SCB7_CLK (0) | LIN0_EN | | TRIG_IN[4] | | |
| P2.3 | PWM0_4 | PWM0_5_N | TC0_4_TR0 | TC0_5_TR1 | | SCB7_CTS (0) | | SCB7_SEL0 (0) | LIN5_RX | | TRIG_IN[5] | | |
| P2.4 | PWM0_3 | PWM0_4_N | TC0_3_TR0 | TC0_4_TR1 | | | | SCB7_SEL1 (0) | LIN5_TX | | TRIG_IN[6] | | |
| P2.5 | PWM0_2 | PWM0_3_N | TC0_2_TR0 | TC0_3_TR1 | | | | SCB7_SEL2 (0) | LIN5_EN | | TRIG_IN[7] | | |
| P3.0 | PWM0_1 | PWM0_2_N | TC0_1_TR0 | TC0_2_TR1 | | SCB6_RX (0) | | SCB6_MISO (0) | | | | TRIG_DBG[0] | |
| P3.1 | PWM0_0 | PWM0_1_N | TC0_0_TR0 | TC0_1_TR1 | | SCB6_TX (0) | SCB6_SDA (0) | SCB6_MOSI (0) | | | | TRIG_DBG[1] | |
| P3.2 | PWM0_M_3 | PWM0_0_N | TC0_M_3_TR0 | TC0_0_TR1 | | SCB6_RTS (0) | SCB6_SCL (0) | SCB6_CLK (0) | | | | | |
| P3.3 | PWM0_M_2 | PWM0_M_3_N | TC0_M_2_TR0 | TC0_M_3_TR1 | | SCB6_CTS (0) | | SCB6_SEL0 (0) | | | | | |
| P3.4 | PWM0_M_1 | PWM0_M_2_N | TC0_M_1_TR0 | TC0_M_2_TR1 | | | | SCB6_SEL1 (0) | | | | | |
| P3.5 | PWM0_M_0 | PWM0_M_1_N | TC0_M_0_TR0 | TC0_M_1_TR1 | | | | SCB6_SEL2 (0) | | | | | |
| P4.0 | PWM0_4 | PWM0_M_0_N | TC0_4_TR0 | TC0_M_0_TR1 | EXT_MUX[0]_0 | SCB5_RX (0) | | SCB5_MISO (0) | LIN1_RX | | TRIG_IN[10] | | |
| P4.1 | PWM0_5 | PWM0_4_N | TC0_5_TR0 | TC0_4_TR1 | EXT_MUX[0]_1 | SCB5_TX (0) | SCB5_SDA (0) | SCB5_MOSI (0) | LIN1_TX | | TRIG_IN[11] | | |
| P4.2 | PWM0_6 | PWM0_5_N | TC0_6_TR0 | TC0_5_TR1 | EXT_MUX[0]_2 | SCB5_RTS (0) | SCB5_SCL (0) | SCB5_CLK (0) | LIN1_EN | | TRIG_IN[12] | | |
| P4.3 | PWM0_7 | PWM0_6_N | TC0_7_TR0 | TC0_6_TR1 | EXT_MUX[0]_EN | SCB5_CTS (0) | | SCB5_SEL0 (0) | | CAN0_1_TX | TRIG_IN[13] | | |

Notes

- 26.High Speed I/O matrix connection (HCon) reference as per [Table 10-1](#).
- 27.Active Mode ordering (ACT#0, ACT#1, and so on) does not have any impact on configuring alternate functions; the HSIOM module handles the alternate function assignments.
- 28.Refer to [Table 13-2](#) for more information on pin multiplexer abbreviations used.
- 29.For any function marked with an identifier (n), the AC timing is only guaranteed within the respective group "n".

Alternate function pin assignments

Table 13-1 Alternate pin functions in Active Mode^[28, 29]

| Active Mapping | | | | | | | | | | | | |
|----------------|---|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|
| Name | HCon#8 ^[26] ACT#0 ^[27] | HCon#9 ACT#1 | HCon#10 ACT#2 | HCon#11 ACT#3 | HCon#16 ACT#4 | HCon#17 ACT#5 | HCon#18 ACT#6 | HCon#19 ACT#7 | HCon#20 ACT#8 | HCon#21 ACT#9 | HCon#26 ACT#14 | HCon#27 ACT#15 |
| P4.4 | PWM0_8 | PWM0_7_N | TC0_8_TR0 | TC0_7_TR1 | | | | SCB5_SEL1 (0) | | CAN0_1_RX | | |
| P5.0 | PWM0_9 | PWM0_8_N | TC0_9_TR0 | TC0_8_TR1 | | | | SCB5_SEL2 (0) | LIN7_RX | | | |
| P5.1 | PWM0_10 | PWM0_9_N | TC0_10_TR0 | TC0_9_TR1 | | | | | LIN7_TX | | | |
| P5.2 | PWM0_11 | PWM0_10_N | TC0_11_TR0 | TC0_10_TR1 | | | | | LIN7_EN | | | |
| P5.3 | PWM0_12 | PWM0_11_N | TC0_12_TR0 | TC0_11_TR1 | | | | | LIN2_RX | | | |
| P5.4 | PWM0_13 | PWM0_12_N | TC0_13_TR0 | TC0_12_TR1 | | | | | LIN2_TX | | | |
| P5.5 | PWM0_14 | PWM0_13_N | TC0_14_TR0 | TC0_13_TR1 | | | | | LIN2_EN | | | |
| P6.0 | PWM0_M_0 | PWM0_14_N | TC0_M_0_TR0 | TC0_14_TR1 | | SCB4_RX (0) | | SCB4_MISO (0) | LIN3_RX | | | |
| P6.1 | PWM0_0 | PWM0_M_0_N | TC0_0_TR0 | TC0_M_0_TR1 | | SCB4_TX (0) | SCB4_SDA (0) | SCB4_MOSI (0) | LIN3_TX | | | |
| P6.2 | PWM0_M_1 | PWM0_0_N | TC0_M_1_TR0 | TC0_0_TR1 | | SCB4_RTS (0) | SCB4_SCL (0) | SCB4_CLK (0) | LIN3_EN | CAN0_2_TX | | |
| P6.3 | PWM0_1 | PWM0_M_1_N | TC0_1_TR0 | TC0_M_1_TR1 | | SCB4_CTS (0) | | SCB4_SELO (0) | LIN4_RX | CAN0_2_RX | | CAL_SUP_NZ |
| P6.4 | PWM0_M_2 | PWM0_1_N | TC0_M_2_TR0 | TC0_1_TR1 | | | | SCB4_SEL1 (0) | LIN4_TX | | | |
| P6.5 | PWM0_2 | PWM0_M_2_N | TC0_2_TR0 | TC0_M_2_TR1 | | | | SCB4_SEL2 (0) | LIN4_EN | | | |
| P6.6 | PWM0_M_3 | PWM0_2_N | TC0_M_3_TR0 | TC0_2_TR1 | | | | SCB4_SEL3 (0) | | TRIG_IN[8] | | |
| P6.7 | PWM0_3 | PWM0_M_3_N | TC0_3_TR0 | TC0_M_3_TR1 | | | | | | TRIG_IN[9] | | |
| P7.0 | PWM0_M_4 | PWM0_3_N | TC0_M_4_TR0 | TC0_3_TR1 | | SCB5_RX (1) | | SCB5_MISO (1) | LIN4_RX | | | |
| P7.1 | PWM0_15 | PWM0_M_4_N | TC0_15_TR0 | TC0_M_4_TR1 | | SCB5_TX (1) | SCB5_SDA (1) | SCB5_MOSI (1) | LIN4_TX | | | |
| P7.2 | PWM0_M_5 | PWM0_15_N | TC0_M_5_TR0 | TC0_15_TR1 | | SCB5_RTS (1) | SCB5_SCL (1) | SCB5_CLK (1) | LIN4_EN | | | |
| P7.3 | PWM0_16 | PWM0_M_5_N | TC0_16_TR0 | TC0_M_5_TR1 | | SCB5_CTS (1) | | SCB5_SELO (1) | | | | |
| P7.4 | PWM0_M_6 | PWM0_16_N | TC0_M_6_TR0 | TC0_16_TR1 | | | | SCB5_SEL1 (1) | | | | |
| P7.5 | PWM0_17 | PWM0_M_6_N | TC0_17_TR0 | TC0_M_6_TR1 | | | | SCB5_SEL2 (1) | | | | |
| P7.6 | PWM0_M_7 | PWM0_17_N | TC0_M_7_TR0 | TC0_17_TR1 | | | | | | TRIG_IN[16] | | |
| P7.7 | PWM0_18 | PWM0_M_7_N | TC0_18_TR0 | TC0_M_7_TR1 | | | | | | TRIG_IN[17] | | |
| P8.0 | PWM0_19 | PWM0_18_N | TC0_19_TR0 | TC0_18_TR1 | | | | | LIN2_RX | CAN0_0_TX | | |
| P8.1 | PWM0_20 | PWM0_19_N | TC0_20_TR0 | TC0_19_TR1 | | | | | LIN2_TX | CAN0_0_RX | TRIG_IN[14] | |
| P8.2 | PWM0_21 | PWM0_20_N | TC0_21_TR0 | TC0_20_TR1 | | | | | LIN2_EN | TRIG_IN[15] | | |
| P8.3 | PWM0_22 | PWM0_21_N | TC0_22_TR0 | TC0_21_TR1 | | | | | | | TRIG_DBG[0] | |
| P8.4 | PWM0_23 | PWM0_22_N | TC0_23_TR0 | TC0_22_TR1 | | | | | | | TRIG_DBG[1] | |
| P9.0 | PWM0_24 | PWM0_23_N | TC0_24_TR0 | TC0_23_TR1 | | | | | | | | |
| P9.1 | PWM0_25 | PWM0_24_N | TC0_25_TR0 | TC0_24_TR1 | | | | | | | | |
| P9.2 | PWM0_26 | PWM0_25_N | TC0_26_TR0 | TC0_25_TR1 | | | | | | | | |

Alternate function pin assignments

Table 13-1 Alternate pin functions in Active Mode^[28, 29]

| Active Mapping | | | | | | | | | | | | |
|----------------|---|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|
| Name | HCon#8 ^[26] ACT#0 ^[27] | HCon#9 ACT#1 | HCon#10 ACT#2 | HCon#11 ACT#3 | HCon#16 ACT#4 | HCon#17 ACT#5 | HCon#18 ACT#6 | HCon#19 ACT#7 | HCon#20 ACT#8 | HCon#21 ACT#9 | HCon#26 ACT#14 | HCon#27 ACT#15 |
| P9.3 | PWM0_27 | PWM0_26_N | TC0_27_TR0 | TC0_26_TR1 | | | | | | | | |
| P10.0 | PWM0_28 | PWM0_27_N | TC0_28_TR0 | TC0_27_TR1 | | SCB4_RX (1) | | SCB4_MISO (1) | | | TRIG_IN[18] | |
| P10.1 | PWM0_29 | PWM0_28_N | TC0_29_TR0 | TC0_28_TR1 | | SCB4_TX (1) | SCB4_SDA (1) | SCB4_MOSI (1) | | | TRIG_IN[19] | |
| P10.2 | PWM0_30 | PWM0_29_N | TC0_30_TR0 | TC0_29_TR1 | | SCB4_RTS (1) | SCB4_SCL (1) | SCB4_CLK (1) | | | | |
| P10.3 | PWM0_31 | PWM0_30_N | TC0_31_TR0 | TC0_30_TR1 | | SCB4_CTS (1) | | SCB4_SELO (1) | | | | |
| P10.4 | PWM0_32 | PWM0_31_N | TC0_32_TR0 | TC0_31_TR1 | | | | SCB4_SEL1 (1) | | | | |
| P10.5 | PWM0_33 | PWM0_32_N | TC0_33_TR0 | TC0_32_TR1 | | | | SCB4_SEL2 (1) | | | | |
| P10.6 | PWM0_34 | PWM0_33_N | TC0_34_TR0 | TC0_33_TR1 | | | | | | | | |
| P10.7 | PWM0_35 | PWM0_34_N | TC0_35_TR0 | TC0_34_TR1 | | | | | | | | |
| P11.0 | | | | | | | | | | | | |
| P11.1 | | | | | | | | | | | | |
| P11.2 | | | | | | | | | | | | |
| P12.0 | PWM0_36 | PWM0_35_N | TC0_36_TR0 | TC0_35_TR1 | | | | | | CAN0_2_TX | TRIG_IN[20] | |
| P12.1 | PWM0_37 | PWM0_36_N | TC0_37_TR0 | TC0_36_TR1 | | | | | LIN6_EN | CAN0_2_RX | TRIG_IN[21] | |
| P12.2 | PWM0_38 | PWM0_37_N | TC0_38_TR0 | TC0_37_TR1 | EXT_MUX[1]_EN | | | | LIN6_RX | | | |
| P12.3 | PWM0_39 | PWM0_38_N | TC0_39_TR0 | TC0_38_TR1 | EXT_MUX[1]_0 | | | | LIN6_TX | | | |
| P12.4 | PWM0_40 | PWM0_39_N | TC0_40_TR0 | TC0_39_TR1 | EXT_MUX[1]_1 | | | | | | | |
| P12.5 | PWM0_41 | PWM0_40_N | TC0_41_TR0 | TC0_40_TR1 | EXT_MUX[1]_2 | | | | | | | |
| P12.6 | PWM0_42 | PWM0_41_N | TC0_42_TR0 | TC0_41_TR1 | | | | | | | | |
| P12.7 | PWM0_43 | PWM0_42_N | TC0_43_TR0 | TC0_42_TR1 | | | | | | | | |
| P13.0 | PWM0_M_8 | PWM0_43_N | TC0_M_8_TR0 | TC0_43_TR1 | EXT_MUX[2]_0 | SCB3_RX (0) | | SCB3_MISO (0) | | | | |
| P13.1 | PWM0_44 | PWM0_M_8_N | TC0_44_TR0 | TC0_M_8_TR1 | EXT_MUX[2]_1 | SCB3_TX (0) | SCB3_SDA (0) | SCB3_MOSI (0) | | | | |
| P13.2 | PWM0_M_9 | PWM0_44_N | TC0_M_9_TR0 | TC0_44_TR1 | EXT_MUX[2]_2 | SCB3_RTS (0) | SCB3_SCL (0) | SCB3_CLK (0) | | | | |
| P13.3 | PWM0_45 | PWM0_M_9_N | TC0_45_TR0 | TC0_M_9_TR1 | EXT_MUX[2]_EN | SCB3_CTS (0) | | SCB3_SELO (0) | | | | |
| P13.4 | PWM0_M_10 | PWM0_45_N | TC0_M_10_TR0 | TC0_45_TR1 | | | | SCB3_SEL1 (0) | | | | |
| P13.5 | PWM0_46 | PWM0_M_10_N | TC0_46_TR0 | TC0_M_10_TR1 | | | | SCB3_SEL2 (0) | | | | |
| P13.6 | PWM0_M_11 | PWM0_46_N | TC0_M_11_TR0 | TC0_46_TR1 | | | | SCB3_SEL3 (0) | | | TRIG_IN[22] | |
| P13.7 | PWM0_47 | PWM0_M_11_N | TC0_47_TR0 | TC0_M_11_TR1 | | | | | | | TRIG_IN[23] | |
| P14.0 | PWM0_48 | PWM0_47_N | TC0_48_TR0 | TC0_47_TR1 | | SCB2_RX (0) | | SCB2_MISO (0) | | CAN1_0_TX | | |
| P14.1 | PWM0_49 | PWM0_48_N | TC0_49_TR0 | TC0_48_TR1 | | SCB2_TX (0) | SCB2_SDA (0) | SCB2_MOSI (0) | | CAN1_0_RX | | |
| P14.2 | PWM0_50 | PWM0_49_N | TC0_50_TR0 | TC0_49_TR1 | | SCB2_RTS (0) | SCB2_SCL (0) | SCB2_CLK (0) | LIN6_RX | | | |

Alternate function pin assignments

Table 13-1 Alternate pin functions in Active Mode^[28, 29]

| Active Mapping | | | | | | | | | | | | |
|----------------|------------------------|------------|-------------|-------------|-------------|--------------|--------------|---------------|---------|-----------|-------------|------------------|
| Name | HCon#8 ^[26] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#26 | HCon#27 |
| | ACT#0 ^[27] | ACT#1 | ACT#2 | ACT#3 | ACT#4 | ACT#5 | ACT#6 | ACT#7 | ACT#8 | ACT#9 | ACT#14 | ACT#15 |
| P14.3 | PWM0_51 | PWM0_50_N | TC0_51_TR0 | TC0_50_TR1 | | SCB2_CTS (0) | | SCB2_SELO (0) | LIN6_TX | | | |
| P14.4 | PWM0_52 | PWM0_51_N | TC0_52_TR0 | TC0_51_TR1 | | | | SCB2_SEL1 (0) | LIN6_EN | | | |
| P14.5 | PWM0_53 | PWM0_52_N | TC0_53_TR0 | TC0_52_TR1 | | | | SCB2_SEL2 (0) | | | | |
| P14.6 | PWM0_54 | PWM0_53_N | TC0_54_TR0 | TC0_53_TR1 | | | | | | | TRIG_IN[24] | |
| P14.7 | PWM0_55 | PWM0_54_N | TC0_55_TR0 | TC0_54_TR1 | | | | | | | TRIG_IN[25] | |
| P15.0 | PWM0_56 | PWM0_55_N | TC0_56_TR0 | TC0_55_TR1 | | | | | | | | |
| P15.1 | PWM0_57 | PWM0_56_N | TC0_57_TR0 | TC0_56_TR1 | | | | | | | | |
| P15.2 | PWM0_58 | PWM0_57_N | TC0_58_TR0 | TC0_57_TR1 | | | | | | | | |
| P15.3 | PWM0_59 | PWM0_58_N | TC0_59_TR0 | TC0_58_TR1 | | | | | | | | |
| P16.0 | PWM0_60 | PWM0_59_N | TC0_60_TR0 | TC0_59_TR1 | PWM0_H_0 | | | | | | | |
| P16.1 | PWM0_61 | PWM0_60_N | TC0_61_TR0 | TC0_60_TR1 | PWM0_H_0_N | | | | | | | |
| P16.2 | PWM0_62 | PWM0_61_N | TC0_62_TR0 | TC0_61_TR1 | PWM0_H_1 | | | | | | | |
| P16.3 | PWM0_62 | PWM0_62_N | TC0_62_TR0 | TC0_62_TR1 | PWM0_H_1_N | | | | | | | |
| P17.0 | PWM0_61 | PWM0_62_N | TC0_61_TR0 | TC0_62_TR1 | | | | | | CAN1_1_TX | | |
| P17.1 | PWM0_60 | PWM0_61_N | TC0_60_TR0 | TC0_61_TR1 | PWM0_H_2 | SCB3_RX (1) | | SCB3_MISO (1) | | CAN1_1_RX | | |
| P17.2 | PWM0_59 | PWM0_60_N | TC0_59_TR0 | TC0_60_TR1 | PWM0_H_2_N | SCB3_TX (1) | SCB3_SDA (1) | SCB3_MOSI (1) | | | | |
| P17.3 | PWM0_58 | PWM0_59_N | TC0_58_TR0 | TC0_59_TR1 | PWM0_H_3 | SCB3_RTS (1) | SCB3_SCL (1) | SCB3_CLK (1) | | | TRIG_IN[26] | |
| P17.4 | PWM0_57 | PWM0_58_N | TC0_57_TR0 | TC0_58_TR1 | PWM0_H_3_N | SCB3_CTS (1) | | SCB3_SELO (1) | | | TRIG_IN[27] | |
| P17.5 | PWM0_56 | PWM0_57_N | TC0_56_TR0 | TC0_57_TR1 | | | | SCB3_SEL1 (1) | | | | |
| P17.6 | PWM0_M_4 | PWM0_56_N | TC0_M_4_TR0 | TC0_56_TR1 | | | | SCB3_SEL2 (1) | | | | |
| P17.7 | PWM0_M_5 | PWM0_M_4_N | TC0_M_5_TR0 | TC0_M_4_TR1 | | | | | | | | |
| P18.0 | PWM0_M_6 | PWM0_M_5_N | TC0_M_6_TR0 | TC0_M_5_TR1 | PWM0_H_0 | SCB1_RX (0) | | SCB1_MISO (0) | | | | FAULT_OUT_0 |
| P18.1 | PWM0_M_7 | PWM0_M_6_N | TC0_M_7_TR0 | TC0_M_6_TR1 | PWM0_H_0_N | SCB1_TX (0) | SCB1_SDA (0) | SCB1_MOSI (0) | | | | FAULT_OUT_1 |
| P18.2 | PWM0_55 | PWM0_M_7_N | TC0_55_TR0 | TC0_M_7_TR1 | PWM0_H_1 | SCB1_RTS (0) | SCB1_SCL (0) | SCB1_CLK (0) | | | | |
| P18.3 | PWM0_54 | PWM0_55_N | TC0_54_TR0 | TC0_55_TR1 | PWM0_H_1_N | SCB1_CTS (0) | | SCB1_SELO (0) | | | | TRACE_CLOCK (0) |
| P18.4 | PWM0_53 | PWM0_54_N | TC0_53_TR0 | TC0_54_TR1 | PWM0_H_2 | | | SCB1_SEL1 (0) | | | | TRACE_DATA_0 (0) |
| P18.5 | PWM0_52 | PWM0_53_N | TC0_52_TR0 | TC0_53_TR1 | PWM0_H_2_N | | | SCB1_SEL2 (0) | | | | TRACE_DATA_1 (0) |
| P18.6 | PWM0_51 | PWM0_52_N | TC0_51_TR0 | TC0_52_TR1 | PWM0_H_3 | | | SCB1_SEL3 (0) | | CAN1_2_TX | | TRACE_DATA_2 (0) |
| P18.7 | PWM0_50 | PWM0_51_N | TC0_50_TR0 | TC0_51_TR1 | PWM0_H_3_N | | | | | CAN1_2_RX | | TRACE_DATA_3 (0) |
| P19.0 | PWM0_M_3 | PWM0_50_N | TC0_M_3_TR0 | TC0_50_TR1 | TC0_H_0_TR0 | SCB2_RX (1) | | SCB2_MISO (1) | | | | FAULT_OUT_2 |
| P19.1 | PWM0_26 | PWM0_M_3_N | TC0_26_TR0 | TC0_M_3_TR1 | TC0_H_0_TR1 | SCB2_TX (1) | SCB2_SDA (1) | SCB2_MOSI (1) | | | | FAULT_OUT_3 |

Alternate function pin assignments

Table 13-1 Alternate pin functions in Active Mode^[28, 29]

| Active Mapping | | | | | | | | | | | | |
|----------------|---|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|
| Name | HCon#8 ^[26] ACT#0 ^[27] | HCon#9 ACT#1 | HCon#10 ACT#2 | HCon#11 ACT#3 | HCon#16 ACT#4 | HCon#17 ACT#5 | HCon#18 ACT#6 | HCon#19 ACT#7 | HCon#20 ACT#8 | HCon#21 ACT#9 | HCon#26 ACT#14 | HCon#27 ACT#15 |
| P19.2 | PWM0_27 | PWM0_26_N | TC0_27_TR0 | TC0_26_TR1 | TC0_H_1_TR0 | SCB2_RTS (1) | SCB2_SCL (1) | SCB2_CLK (1) | | | TRIG_IN[28] | |
| P19.3 | PWM0_28 | PWM0_27_N | TC0_28_TR0 | TC0_27_TR1 | TC0_H_1_TR1 | SCB2_CTS (1) | | SCB2_SEL0 (1) | | | TRIG_IN[29] | |
| P19.4 | PWM0_29 | PWM0_28_N | TC0_29_TR0 | TC0_28_TR1 | TC0_H_2_TR0 | | | SCB2_SEL1 (1) | | | | |
| P20.0 | PWM0_30 | PWM0_29_N | TC0_30_TR0 | TC0_29_TR1 | TC0_H_2_TR1 | | | SCB2_SEL2 (1) | LIN5_RX | | | |
| P20.1 | PWM0_49 | PWM0_30_N | TC0_49_TR0 | TC0_30_TR1 | TC0_H_3_TR0 | | | | LIN5_TX | | | |
| P20.2 | PWM0_48 | PWM0_49_N | TC0_48_TR0 | TC0_49_TR1 | TC0_H_3_TR1 | | | | LIN5_EN | | | |
| P20.3 | PWM0_47 | PWM0_48_N | TC0_47_TR0 | TC0_48_TR1 | | SCB1_RX (1) | | SCB1_MISO (1) | | CAN1_2_TX | | |
| P20.4 | PWM0_46 | PWM0_47_N | TC0_46_TR0 | TC0_47_TR1 | | SCB1_TX (1) | SCB1_SDA (1) | SCB1_MOSI (1) | | CAN1_2_RX | | |
| P20.5 | PWM0_45 | PWM0_46_N | TC0_45_TR0 | TC0_46_TR1 | | SCB1_RTS (1) | SCB1_SCL (1) | SCB1_CLK (1) | | | | |
| P20.6 | PWM0_44 | PWM0_45_N | TC0_44_TR0 | TC0_45_TR1 | | SCB1_CTS (1) | | SCB1_SEL0 (1) | | | | |
| P20.7 | PWM0_43 | PWM0_44_N | TC0_43_TR0 | TC0_44_TR1 | | | | SCB1_SEL1 (1) | | | | |
| P21.0 | PWM0_42 | PWM0_43_N | TC0_42_TR0 | TC0_43_TR1 | | | | SCB1_SEL2 (1) | | | | |
| P21.1 | PWM0_41 | PWM0_42_N | TC0_41_TR0 | TC0_42_TR1 | | | | | | | | |
| P21.2 | PWM0_40 | PWM0_41_N | TC0_40_TR0 | TC0_41_TR1 | | | | | | | EXT_CLK | TRIG_DBG[1] |
| P21.3 | PWM0_39 | PWM0_40_N | TC0_39_TR0 | TC0_40_TR1 | | | | | | | | |
| P21.4 | PWM0_38 | PWM0_39_N | TC0_38_TR0 | TC0_39_TR1 | | | | | | | | |
| P21.5 | PWM0_37 | PWM0_38_N | TC0_37_TR0 | TC0_38_TR1 | | | | | LIN0_RX | | | |
| P21.6 | PWM0_36 | PWM0_37_N | TC0_36_TR0 | TC0_37_TR1 | | | | | LIN0_TX | | | |
| P21.7 | PWM0_35 | PWM0_36_N | TC0_35_TR0 | TC0_36_TR1 | | | | | LIN0_EN | | | CAL_SUP_NZ |
| P22.0 | PWM0_34 | PWM0_35_N | TC0_34_TR0 | TC0_35_TR1 | | SCB6_RX (1) | | SCB6_MISO (1) | | CAN1_1_TX | | TRACE_DATA_0 (1) |
| P22.1 | PWM0_33 | PWM0_34_N | TC0_33_TR0 | TC0_34_TR1 | | SCB6_TX (1) | SCB6_SDA (1) | SCB6_MOSI (1) | | CAN1_1_RX | | TRACE_DATA_1 (1) |
| P22.2 | PWM0_32 | PWM0_33_N | TC0_32_TR0 | TC0_33_TR1 | | SCB6_RTS (1) | SCB6_SCL (1) | SCB6_CLK (1) | | | | TRACE_DATA_2 (1) |
| P22.3 | PWM0_31 | PWM0_32_N | TC0_31_TR0 | TC0_32_TR1 | | SCB6_CTS (1) | | SCB6_SEL0 (1) | | | | TRACE_DATA_3 (1) |
| P22.4 | PWM0_30 | PWM0_31_N | TC0_30_TR0 | TC0_31_TR1 | | | | SCB6_SEL1 (1) | | | | TRACE_CLOCK (1) |
| P22.5 | PWM0_29 | PWM0_30_N | TC0_29_TR0 | TC0_30_TR1 | | | | SCB6_SEL2 (1) | LIN7_RX | | | |
| P22.6 | PWM0_28 | PWM0_29_N | TC0_28_TR0 | TC0_29_TR1 | | | | | LIN7_TX | | | |
| P22.7 | PWM0_27 | PWM0_28_N | TC0_27_TR0 | TC0_28_TR1 | | | | | LIN7_EN | | | |
| P23.0 | PWM0_M_8 | PWM0_27_N | TC0_M_8_TR0 | TC0_27_TR1 | | SCB7_RX (1) | | SCB7_MISO (1) | | CAN1_0_TX | | FAULT_OUT_0 |
| P23.1 | PWM0_M_9 | PWM0_M_8_N | TC0_M_9_TR0 | TC0_M_8_TR1 | | SCB7_TX (1) | SCB7_SDA (1) | SCB7_MOSI (1) | | CAN1_0_RX | | FAULT_OUT_1 |
| P23.2 | PWM0_M_10 | PWM0_M_9_N | TC0_M_10_TR0 | TC0_M_9_TR1 | | SCB7_RTS (1) | SCB7_SCL (1) | SCB7_CLK (1) | | | | FAULT_OUT_2 |
| P23.3 | PWM0_M_11 | PWM0_M_10_N | TC0_M_11_TR0 | TC0_M_10_TR1 | | SCB7_CTS (1) | | SCB7_SEL0 (1) | | | TRIG_IN[30] | FAULT_OUT_3 |

Alternate function pin assignments

Table 13-1 Alternate pin functions in Active Mode^[28, 29]

| Name | Active Mapping | | | | | | | | | | | |
|-------|------------------------|-------------|------------|--------------|---------|---------|---------|---------------|---------|---------|-------------|-------------|
| | HCon#8 ^[26] | HCon#9 | HCon#10 | HCon#11 | HCon#16 | HCon#17 | HCon#18 | HCon#19 | HCon#20 | HCon#21 | HCon#26 | HCon#27 |
| | ACT#0 ^[27] | ACT#1 | ACT#2 | ACT#3 | ACT#4 | ACT#5 | ACT#6 | ACT#7 | ACT#8 | ACT#9 | ACT#14 | ACT#15 |
| | | | | | | | | | | | | |
| P23.4 | PWM0_25 | PWM0_M_11_N | TC0_25_TR0 | TC0_M_11_TR1 | | | | SCB7_SEL1 (1) | | | TRIG_IN[31] | TRIG_DBG[0] |
| P23.5 | PWM0_24 | PWM0_25_N | TC0_24_TR0 | TC0_25_TR1 | | | | SCB7_SEL2 (1) | | | | |
| P23.6 | PWM0_23 | PWM0_24_N | TC0_23_TR0 | TC0_24_TR1 | | | | | | | | |
| P23.7 | PWM0_22 | PWM0_23_N | TC0_22_TR0 | TC0_23_TR1 | | | | | | | EXT_CLK | CAL_SUP_NZ |

Table 13-2 Pin mux descriptions

| Sl. No. | Pin | Module | Description |
|---------|----------------|----------|---|
| 1 | PWMx_y | TCPWM | TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number |
| 2 | PWMx_y_N | TCPWM | TCPWM 16-bit PWM (no motor control), PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number |
| 3 | PWMx_M_y | TCPWM | TCPWM 16-bit PWM with motor control line out, x-TCPWM block, y-counter number |
| 4 | PWMx_M_y_N | TCPWM | TCPWM 16-bit PWM with motor control complementary line out (N), x-TCPWM block, y-counter number |
| 5 | PWMx_H_y | TCPWM | TCPWM 32-bit PWM, PWM_DT and PWM_PR line out, x-TCPWM block, y-counter number |
| 6 | PWMx_H_y_N | TCPWM | TCPWM 32-bit PWM, PWM_DT and PWM_PR complementary line out (N), x-TCPWM block, y-counter number |
| 7 | TCx_y_TRz | TCPWM | TCPWM 16-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number |
| 8 | TCx_M_y_TRz | TCPWM | TCPWM 16-bit dedicated counter input triggers with motor control, x-TCPWM block, y-counter number, z-trigger number |
| 9 | TCx_H_y_TRz | TCPWM | TCPWM 32-bit dedicated counter input triggers, x-TCPWM block, y-counter number, z-trigger number |
| 10 | SCBx_RX | SCB | UART Receive, x-SCB block |
| 11 | SCBx_TX | SCB | UART Transmit, x-SCB block |
| 12 | SCBx_RTS | SCB | UART Request to Send (Handshake), x-SCB block |
| 13 | SCBx_CTS | SCB | UART Clear to Send (Handshake), x-SCB block |
| 14 | SCBx_SDA | SCB | I2C Data line, x-SCB block |
| 15 | SCBx_SCL | SCB | I2C Clock line, x-SCB block |
| 16 | SCBx_MISO | SCB | SPI Master Input Slave Output, x-SCB block |
| 17 | SCBx_MOSI | SCB | SPI Master Output Slave Input, x-SCB block |
| 18 | SCBx_CLK | SCB | SPI Serial Clock, x-SCB block |
| 19 | SCBx_SELy | SCB | SPI Slave Select, x-SCB block, y-select line |
| 20 | LINx_RX | LIN | LIN Receive line, x-LIN block |
| 21 | LINx_TX | LIN | LIN Transmit line, x-LIN block |
| 22 | LINx_EN | LIN | LIN Enable line, x-LIN block |
| 23 | CANx_y_TX | CANFD | CAN Transmit line, x-CAN block, y-channel number |
| 24 | CANx_y_RX | CANFD | CAN Receive line, x-CAN block, y-channel number |
| 25 | CAL_SUP_NZ | CPUSS | ETAS Calibration support line |
| 26 | FAULT_OUT_x | SRSS | Fault output line x-0 to 3 |
| 27 | TRACE_DATA_x | SRSS | Trace dataout line x-0 to 3 |
| 28 | TRACE_CLOCK | SRSS | Trace clock line |
| 29 | RTC_CAL | SRSS RTC | RTC calibration clock input |
| 30 | SWJ_TRSTN | SRSS | JTAG Test reset line (Active low) |
| 31 | SWJ_SWO_TDO | SRSS | JTAG Test data output/SWO (Serial Wire Output) |
| 32 | SWJ_SWCLK_TCLK | SRSS | JTAG Test clock/SWD clock (Serial Wire Clock) |

Table 13-2 Pin mux descriptions *(continued)*

| Sl. No. | Pin | Module | Description |
|---------|----------------------|----------|--|
| 33 | SWJ_SWDIO_TMS | SRSS | JTAG Test mode select/SWD data (Serial Wire Data Input/Output) |
| 34 | SWJ_SWDOE_TDI | SRSS | JTAG Test data input |
| 35 | HIBER-NATE_WAKEUP[x] | SRSS | Hibernate wakeup line x-0 to 1 |
| 36 | ADC[x]_y | PASS SAR | SAR, channel, x-SAR number, y-channel number |
| 37 | ADC[x]_M | PASS SAR | SAR motor control input, x-SAR number |
| 38 | EXT_MUX[x]_y | PASS SAR | External SAR MUX inputs, x-MUX number, y-MUX input 0 to 2 |
| 39 | EXT_MUX[x]_EN | PASS SAR | External SAR MUX enable line |

14 Interrupts and wake-up assignments

Table 14-1 Peripheral interrupt assignments and wake-up sources

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|--|
| 0 | cpuss_interrupts_ipc_0_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #0 |
| 1 | cpuss_interrupts_ipc_1_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #1 |
| 2 | cpuss_interrupts_ipc_2_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #2 |
| 3 | cpuss_interrupts_ipc_3_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #3 |
| 4 | cpuss_interrupts_ipc_4_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #4 |
| 5 | cpuss_interrupts_ipc_5_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #5 |
| 6 | cpuss_interrupts_ipc_6_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #6 |
| 7 | cpuss_interrupts_ipc_7_IRQn | DeepSleep | CPUSS Inter Process Communication Interrupt #7 |
| 8 | cpuss_interrupts_fault_0_IRQn | DeepSleep | CPUSS Fault Structure #0 Interrupt |
| 9 | cpuss_interrupts_fault_1_IRQn | DeepSleep | CPUSS Fault Structure #1 Interrupt |
| 10 | cpuss_interrupts_fault_2_IRQn | DeepSleep | CPUSS Fault Structure #2 Interrupt |
| 11 | cpuss_interrupts_fault_3_IRQn | DeepSleep | CPUSS Fault Structure #3 Interrupt |
| 12 | srss_interrupt_backup_IRQn | DeepSleep | BACKUP domain Interrupt |
| 13 | srss_interrupt_mcwdt_0_IRQn | DeepSleep | Multi Counter Watchdog Timer #0 interrupt |
| 14 | srss_interrupt_mcwdt_1_IRQn | DeepSleep | Multi Counter Watchdog Timer #1 interrupt |
| 15 | srss_interrupt_wdt_IRQn | DeepSleep | Hardware Watchdog Timer interrupt |
| 16 | srss_interrupt_IRQn | DeepSleep | Other combined Interrupts for SRSS (LVD, CLKCAL) |
| 17 | scb_0_interrupt_IRQn | DeepSleep | SCB0 interrupt (DeepSleep capable) |
| 18 | evtgen_0_interrupt_dpslp_IRQn | DeepSleep | Event gen DeepSleep domain interrupt |
| 19 | ioss_interrupt_vdd_IRQn | DeepSleep | I/O Supply (V _{DDIO} , V _{DDA} , V _{DDD}) state change Interrupt |
| 20 | ioss_interrupt_gpio_IRQn | DeepSleep | Consolidated Interrupt for GPIO_STD and GPIO_ENH, All Ports |
| 21 | ioss_interrupts_gpio_0_IRQn | DeepSleep | GPIO_ENH Port #0 Interrupt |
| 22 | ioss_interrupts_gpio_1_IRQn | DeepSleep | GPIO_STD Port #1 Interrupt |
| 23 | ioss_interrupts_gpio_2_IRQn | DeepSleep | GPIO_STD Port #2 Interrupt |
| 24 | ioss_interrupts_gpio_3_IRQn | DeepSleep | GPIO_STD Port #3 Interrupt |
| 25 | ioss_interrupts_gpio_4_IRQn | DeepSleep | GPIO_STD Port #4 Interrupt |
| 26 | ioss_interrupts_gpio_5_IRQn | DeepSleep | GPIO_STD Port #5 Interrupt |
| 27 | ioss_interrupts_gpio_6_IRQn | DeepSleep | GPIO_STD Port #6 Interrupt |
| 28 | ioss_interrupts_gpio_7_IRQn | DeepSleep | GPIO_STD Port #7 Interrupt |
| 29 | ioss_interrupts_gpio_8_IRQn | DeepSleep | GPIO_STD Port #8 Interrupt |
| 30 | ioss_interrupts_gpio_9_IRQn | DeepSleep | GPIO_STD Port #9 Interrupt |
| 31 | ioss_interrupts_gpio_10_IRQn | DeepSleep | GPIO_STD Port #10 Interrupt |
| 32 | ioss_interrupts_gpio_11_IRQn | DeepSleep | GPIO_STD Port #11 Interrupt |
| 33 | ioss_interrupts_gpio_12_IRQn | DeepSleep | GPIO_STD Port #12 Interrupt |
| 34 | ioss_interrupts_gpio_13_IRQn | DeepSleep | GPIO_STD Port #13 Interrupt |
| 35 | ioss_interrupts_gpio_14_IRQn | DeepSleep | GPIO_STD Port #14 Interrupt |
| 36 | ioss_interrupts_gpio_15_IRQn | DeepSleep | GPIO_STD Port #15 Interrupt |

Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|---------------------------------|------------|--|
| 37 | ioss_interrupts_gpio_16_IRQn | DeepSleep | GPIO_STD Port #16 Interrupt |
| 38 | ioss_interrupts_gpio_17_IRQn | DeepSleep | GPIO_STD Port #17 Interrupt |
| 39 | ioss_interrupts_gpio_18_IRQn | DeepSleep | GPIO_STD Port #18 Interrupt |
| 40 | ioss_interrupts_gpio_19_IRQn | DeepSleep | GPIO_STD Port #19 Interrupt |
| 41 | ioss_interrupts_gpio_20_IRQn | DeepSleep | GPIO_STD Port #20 Interrupt |
| 42 | ioss_interrupts_gpio_21_IRQn | DeepSleep | GPIO_STD Port #21 Interrupt |
| 43 | ioss_interrupts_gpio_22_IRQn | DeepSleep | GPIO_STD Port #22 Interrupt |
| 44 | ioss_interrupts_gpio_23_IRQn | DeepSleep | GPIO_STD Port #23 Interrupt |
| 45 | cpuss_interrupt_crypto_IRQn | Active | Crypto Accelerator Interrupt |
| 46 | cpuss_interrupt_fm_IRQn | Active | FLASH Macro Interrupt |
| 47 | cpuss_interrupts_cm4_fp_IRQn | Active | CM4 Floating Point operation fault |
| 48 | cpuss_interrupts_cm0_cti_0_IRQn | Active | CM0+ CTI (Cross Trigger Interface) #0 |
| 49 | cpuss_interrupts_cm0_cti_1_IRQn | Active | CM0+ CTI #1 |
| 50 | cpuss_interrupts_cm4_cti_0_IRQn | Active | CM4 CTI #0 |
| 51 | cpuss_interrupts_cm4_cti_1_IRQn | Active | CM4 CTI #1 |
| 52 | evtgen_0_interrupt_IRQn | Active | Event gen Active domain interrupt |
| 53 | canfd_0_interrupt0_IRQn | Active | CAN0, Consolidated Interrupt #0 for all three channels |
| 54 | canfd_0_interrupt1_IRQn | Active | CAN0, Consolidated Interrupt #1 for all three channels |
| 55 | canfd_1_interrupt0_IRQn | Active | CAN1, Consolidated Interrupt #0 for all three channels |
| 56 | canfd_1_interrupt1_IRQn | Active | CAN1, Consolidated Interrupt #1 for all three channels |
| 57 | canfd_0_interrupts0_0_IRQn | Active | CAN0, Interrupt #0, Channel #0 |
| 58 | canfd_0_interrupts0_1_IRQn | Active | CAN0, Interrupt #0, Channel #1 |
| 59 | canfd_0_interrupts0_2_IRQn | Active | CAN0, Interrupt #0, Channel #2 |
| 60 | canfd_0_interrupts1_0_IRQn | Active | CAN0, Interrupt #1, Channel #0 |
| 61 | canfd_0_interrupts1_1_IRQn | Active | CAN0, Interrupt #1, Channel #1 |
| 62 | canfd_0_interrupts1_2_IRQn | Active | CAN0, Interrupt #1, Channel #2 |
| 63 | canfd_1_interrupts0_0_IRQn | Active | CAN1, Interrupt #0, Channel #0 |
| 64 | canfd_1_interrupts0_1_IRQn | Active | CAN1, Interrupt #0, Channel #1 |
| 65 | canfd_1_interrupts0_2_IRQn | Active | CAN1, Interrupt #0, Channel #2 |
| 66 | canfd_1_interrupts1_0_IRQn | Active | CAN1, Interrupt #1, Channel #0 |
| 67 | canfd_1_interrupts1_1_IRQn | Active | CAN1, Interrupt #1, Channel #1 |
| 68 | canfd_1_interrupts1_2_IRQn | Active | CAN1, Interrupt #1, Channel #2 |
| 69 | lin_0_interrupts_0_IRQn | Active | LIN0, Channel #0 Interrupt |
| 70 | lin_0_interrupts_1_IRQn | Active | LIN0, Channel #1 Interrupt |
| 71 | lin_0_interrupts_2_IRQn | Active | LIN0, Channel #2 Interrupt |
| 72 | lin_0_interrupts_3_IRQn | Active | LIN0, Channel #3 Interrupt |
| 73 | lin_0_interrupts_4_IRQn | Active | LIN0, Channel #4 Interrupt |
| 74 | lin_0_interrupts_5_IRQn | Active | LIN0, Channel #5 Interrupt |

Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|-------------------------------------|
| 75 | lin_0_interrupts_6_IRQn | Active | LIN0, Channel #6 Interrupt |
| 76 | lin_0_interrupts_7_IRQn | Active | LIN0, Channel #7 Interrupt |
| 77 | scb_1_interrupt_IRQn | Active | SCB1 Interrupt |
| 78 | scb_2_interrupt_IRQn | Active | SCB2 Interrupt |
| 79 | scb_3_interrupt_IRQn | Active | SCB3 Interrupt |
| 80 | scb_4_interrupt_IRQn | Active | SCB4 Interrupt |
| 81 | scb_5_interrupt_IRQn | Active | SCB5 Interrupt |
| 82 | scb_6_interrupt_IRQn | Active | SCB6 Interrupt |
| 83 | scb_7_interrupt_IRQn | Active | SCB7 Interrupt |
| 84 | pass_0_interrupts_sar_0_IRQn | Active | SAR0, Logical Channel #0 Interrupt |
| 85 | pass_0_interrupts_sar_1_IRQn | Active | SAR0, Logical Channel #1 Interrupt |
| 86 | pass_0_interrupts_sar_2_IRQn | Active | SAR0, Logical Channel #2 Interrupt |
| 87 | pass_0_interrupts_sar_3_IRQn | Active | SAR0, Logical Channel #3 Interrupt |
| 88 | pass_0_interrupts_sar_4_IRQn | Active | SAR0, Logical Channel #4 Interrupt |
| 89 | pass_0_interrupts_sar_5_IRQn | Active | SAR0, Logical Channel #5 Interrupt |
| 90 | pass_0_interrupts_sar_6_IRQn | Active | SAR0, Logical Channel #6 Interrupt |
| 91 | pass_0_interrupts_sar_7_IRQn | Active | SAR0, Logical Channel #7 Interrupt |
| 92 | pass_0_interrupts_sar_8_IRQn | Active | SAR0, Logical Channel #8 Interrupt |
| 93 | pass_0_interrupts_sar_9_IRQn | Active | SAR0, Logical Channel #9 Interrupt |
| 94 | pass_0_interrupts_sar_10_IRQn | Active | SAR0, Logical Channel #10 Interrupt |
| 95 | pass_0_interrupts_sar_11_IRQn | Active | SAR0, Logical Channel #11 Interrupt |
| 96 | pass_0_interrupts_sar_12_IRQn | Active | SAR0, Logical Channel #12 Interrupt |
| 97 | pass_0_interrupts_sar_13_IRQn | Active | SAR0, Logical Channel #13 Interrupt |
| 98 | pass_0_interrupts_sar_14_IRQn | Active | SAR0, Logical Channel #14 Interrupt |
| 99 | pass_0_interrupts_sar_15_IRQn | Active | SAR0, Logical Channel #15 Interrupt |
| 100 | pass_0_interrupts_sar_16_IRQn | Active | SAR0, Logical Channel #16 Interrupt |
| 101 | pass_0_interrupts_sar_17_IRQn | Active | SAR0, Logical Channel #17 Interrupt |
| 102 | pass_0_interrupts_sar_18_IRQn | Active | SAR0, Logical Channel #18 Interrupt |
| 103 | pass_0_interrupts_sar_19_IRQn | Active | SAR0, Logical Channel #19 Interrupt |
| 104 | pass_0_interrupts_sar_20_IRQn | Active | SAR0, Logical Channel #20 Interrupt |
| 105 | pass_0_interrupts_sar_21_IRQn | Active | SAR0, Logical Channel #21 Interrupt |
| 106 | pass_0_interrupts_sar_22_IRQn | Active | SAR0, Logical Channel #22 Interrupt |
| 107 | pass_0_interrupts_sar_23_IRQn | Active | SAR0, Logical Channel #23 Interrupt |
| 108 | pass_0_interrupts_sar_32_IRQn | Active | SAR1, Logical Channel #0 Interrupt |
| 109 | pass_0_interrupts_sar_33_IRQn | Active | SAR1, Logical Channel #1 Interrupt |
| 110 | pass_0_interrupts_sar_34_IRQn | Active | SAR1, Logical Channel #2 Interrupt |
| 111 | pass_0_interrupts_sar_35_IRQn | Active | SAR1, Logical Channel #3 Interrupt |
| 112 | pass_0_interrupts_sar_36_IRQn | Active | SAR1, Logical Channel #4 Interrupt |
| 113 | pass_0_interrupts_sar_37_IRQn | Active | SAR1, Logical Channel #5 Interrupt |
| 114 | pass_0_interrupts_sar_38_IRQn | Active | SAR1, Logical Channel #6 Interrupt |
| 115 | pass_0_interrupts_sar_39_IRQn | Active | SAR1, Logical Channel #7 Interrupt |

Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|-------------------------------|------------|-------------------------------------|
| 116 | pass_0_interrupts_sar_40_IRQn | Active | SAR1, Logical Channel #8 Interrupt |
| 117 | pass_0_interrupts_sar_41_IRQn | Active | SAR1, Logical Channel #9 Interrupt |
| 118 | pass_0_interrupts_sar_42_IRQn | Active | SAR1, Logical Channel #10 Interrupt |
| 119 | pass_0_interrupts_sar_43_IRQn | Active | SAR1, Logical Channel #11 Interrupt |
| 120 | pass_0_interrupts_sar_44_IRQn | Active | SAR1, Logical Channel #12 Interrupt |
| 121 | pass_0_interrupts_sar_45_IRQn | Active | SAR1, Logical Channel #13 Interrupt |
| 122 | pass_0_interrupts_sar_46_IRQn | Active | SAR1, Logical Channel #14 Interrupt |
| 123 | pass_0_interrupts_sar_47_IRQn | Active | SAR1, Logical Channel #15 Interrupt |
| 124 | pass_0_interrupts_sar_48_IRQn | Active | SAR1, Logical Channel #16 Interrupt |
| 125 | pass_0_interrupts_sar_49_IRQn | Active | SAR1, Logical Channel #17 Interrupt |
| 126 | pass_0_interrupts_sar_50_IRQn | Active | SAR1, Logical Channel #18 Interrupt |
| 127 | pass_0_interrupts_sar_51_IRQn | Active | SAR1, Logical Channel #19 Interrupt |
| 128 | pass_0_interrupts_sar_52_IRQn | Active | SAR1, Logical Channel #20 Interrupt |
| 129 | pass_0_interrupts_sar_53_IRQn | Active | SAR1, Logical Channel #21 Interrupt |
| 130 | pass_0_interrupts_sar_54_IRQn | Active | SAR1, Logical Channel #22 Interrupt |
| 131 | pass_0_interrupts_sar_55_IRQn | Active | SAR1, Logical Channel #23 Interrupt |
| 132 | pass_0_interrupts_sar_56_IRQn | Active | SAR1, Logical Channel #24 Interrupt |
| 133 | pass_0_interrupts_sar_57_IRQn | Active | SAR1, Logical Channel #25 Interrupt |
| 134 | pass_0_interrupts_sar_58_IRQn | Active | SAR1, Logical Channel #26 Interrupt |
| 135 | pass_0_interrupts_sar_59_IRQn | Active | SAR1, Logical Channel #27 Interrupt |
| 136 | pass_0_interrupts_sar_60_IRQn | Active | SAR1, Logical Channel #28 Interrupt |
| 137 | pass_0_interrupts_sar_61_IRQn | Active | SAR1, Logical Channel #29 Interrupt |
| 138 | pass_0_interrupts_sar_62_IRQn | Active | SAR1, Logical Channel #30 Interrupt |
| 139 | pass_0_interrupts_sar_63_IRQn | Active | SAR1, Logical Channel #31 Interrupt |
| 140 | pass_0_interrupts_sar_64_IRQn | Active | SAR2, Logical Channel #0 Interrupt |
| 141 | pass_0_interrupts_sar_65_IRQn | Active | SAR2, Logical Channel #1 Interrupt |
| 142 | pass_0_interrupts_sar_66_IRQn | Active | SAR2, Logical Channel #2 Interrupt |
| 143 | pass_0_interrupts_sar_67_IRQn | Active | SAR2, Logical Channel #3 Interrupt |
| 144 | pass_0_interrupts_sar_68_IRQn | Active | SAR2, Logical Channel #4 Interrupt |
| 145 | pass_0_interrupts_sar_69_IRQn | Active | SAR2, Logical Channel #5 Interrupt |
| 146 | pass_0_interrupts_sar_70_IRQn | Active | SAR2, Logical Channel #6 Interrupt |
| 147 | pass_0_interrupts_sar_71_IRQn | Active | SAR2, Logical Channel #7 Interrupt |
| 148 | cpuss_interrupts_dmac_0_IRQn | Active | CPUSS M-DMA0, Channel #0 Interrupt |
| 149 | cpuss_interrupts_dmac_1_IRQn | Active | CPUSS M-DMA0, Channel #1 Interrupt |
| 150 | cpuss_interrupts_dmac_2_IRQn | Active | CPUSS M-DMA0, Channel #2 Interrupt |
| 151 | cpuss_interrupts_dmac_3_IRQn | Active | CPUSS M-DMA0, Channel #3 Interrupt |
| 152 | cpuss_interrupts_dw0_0_IRQn | Active | CPUSS P-DMA0, Channel #0 Interrupt |
| 153 | cpuss_interrupts_dw0_1_IRQn | Active | CPUSS P-DMA0, Channel #1 Interrupt |
| 154 | cpuss_interrupts_dw0_2_IRQn | Active | CPUSS P-DMA0, Channel #2 Interrupt |
| 155 | cpuss_interrupts_dw0_3_IRQn | Active | CPUSS P-DMA0, Channel #3 Interrupt |
| 156 | cpuss_interrupts_dw0_4_IRQn | Active | CPUSS P-DMA0, Channel #4 Interrupt |

Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|------------------------------|------------|-------------------------------------|
| 157 | cpuss_interrupts_dw0_5_IRQn | Active | CPUSS P-DMA0, Channel #5 Interrupt |
| 158 | cpuss_interrupts_dw0_6_IRQn | Active | CPUSS P-DMA0, Channel #6 Interrupt |
| 159 | cpuss_interrupts_dw0_7_IRQn | Active | CPUSS P-DMA0, Channel #7 Interrupt |
| 160 | cpuss_interrupts_dw0_8_IRQn | Active | CPUSS P-DMA0, Channel #8 Interrupt |
| 161 | cpuss_interrupts_dw0_9_IRQn | Active | CPUSS P-DMA0, Channel #9 Interrupt |
| 162 | cpuss_interrupts_dw0_10_IRQn | Active | CPUSS P-DMA0, Channel #10 Interrupt |
| 163 | cpuss_interrupts_dw0_11_IRQn | Active | CPUSS P-DMA0, Channel #11 Interrupt |
| 164 | cpuss_interrupts_dw0_12_IRQn | Active | CPUSS P-DMA0, Channel #12 Interrupt |
| 165 | cpuss_interrupts_dw0_13_IRQn | Active | CPUSS P-DMA0, Channel #13 Interrupt |
| 166 | cpuss_interrupts_dw0_14_IRQn | Active | CPUSS P-DMA0, Channel #14 Interrupt |
| 167 | cpuss_interrupts_dw0_15_IRQn | Active | CPUSS P-DMA0, Channel #15 Interrupt |
| 168 | cpuss_interrupts_dw0_16_IRQn | Active | CPUSS P-DMA0, Channel #16 Interrupt |
| 169 | cpuss_interrupts_dw0_17_IRQn | Active | CPUSS P-DMA0, Channel #17 Interrupt |
| 170 | cpuss_interrupts_dw0_18_IRQn | Active | CPUSS P-DMA0, Channel #18 Interrupt |
| 171 | cpuss_interrupts_dw0_19_IRQn | Active | CPUSS P-DMA0, Channel #19 Interrupt |
| 172 | cpuss_interrupts_dw0_20_IRQn | Active | CPUSS P-DMA0, Channel #20 Interrupt |
| 173 | cpuss_interrupts_dw0_21_IRQn | Active | CPUSS P-DMA0, Channel #21 Interrupt |
| 174 | cpuss_interrupts_dw0_22_IRQn | Active | CPUSS P-DMA0, Channel #22 Interrupt |
| 175 | cpuss_interrupts_dw0_23_IRQn | Active | CPUSS P-DMA0, Channel #23 Interrupt |
| 176 | cpuss_interrupts_dw0_24_IRQn | Active | CPUSS P-DMA0, Channel #24 Interrupt |
| 177 | cpuss_interrupts_dw0_25_IRQn | Active | CPUSS P-DMA0, Channel #25 Interrupt |
| 178 | cpuss_interrupts_dw0_26_IRQn | Active | CPUSS P-DMA0, Channel #26 Interrupt |
| 179 | cpuss_interrupts_dw0_27_IRQn | Active | CPUSS P-DMA0, Channel #27 Interrupt |
| 180 | cpuss_interrupts_dw0_28_IRQn | Active | CPUSS P-DMA0, Channel #28 Interrupt |
| 181 | cpuss_interrupts_dw0_29_IRQn | Active | CPUSS P-DMA0, Channel #29 Interrupt |
| 182 | cpuss_interrupts_dw0_30_IRQn | Active | CPUSS P-DMA0, Channel #30 Interrupt |
| 183 | cpuss_interrupts_dw0_31_IRQn | Active | CPUSS P-DMA0, Channel #31 Interrupt |
| 184 | cpuss_interrupts_dw0_32_IRQn | Active | CPUSS P-DMA0, Channel #32 Interrupt |
| 185 | cpuss_interrupts_dw0_33_IRQn | Active | CPUSS P-DMA0, Channel #33 Interrupt |
| 186 | cpuss_interrupts_dw0_34_IRQn | Active | CPUSS P-DMA0, Channel #34 Interrupt |
| 187 | cpuss_interrupts_dw0_35_IRQn | Active | CPUSS P-DMA0, Channel #35 Interrupt |
| 188 | cpuss_interrupts_dw0_36_IRQn | Active | CPUSS P-DMA0, Channel #36 Interrupt |
| 189 | cpuss_interrupts_dw0_37_IRQn | Active | CPUSS P-DMA0, Channel #37 Interrupt |
| 190 | cpuss_interrupts_dw0_38_IRQn | Active | CPUSS P-DMA0, Channel #38 Interrupt |
| 191 | cpuss_interrupts_dw0_39_IRQn | Active | CPUSS P-DMA0, Channel #39 Interrupt |
| 192 | cpuss_interrupts_dw0_40_IRQn | Active | CPUSS P-DMA0, Channel #40 Interrupt |
| 193 | cpuss_interrupts_dw0_41_IRQn | Active | CPUSS P-DMA0, Channel #41 Interrupt |
| 194 | cpuss_interrupts_dw0_42_IRQn | Active | CPUSS P-DMA0, Channel #42 Interrupt |
| 195 | cpuss_interrupts_dw0_43_IRQn | Active | CPUSS P-DMA0, Channel #43 Interrupt |
| 196 | cpuss_interrupts_dw0_44_IRQn | Active | CPUSS P-DMA0, Channel #44 Interrupt |
| 197 | cpuss_interrupts_dw0_45_IRQn | Active | CPUSS P-DMA0, Channel #45 Interrupt |

Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|------------------------------|------------|-------------------------------------|
| 198 | cpuss_interrupts_dw0_46_IRQn | Active | CPUSS P-DMA0, Channel #46 Interrupt |
| 199 | cpuss_interrupts_dw0_47_IRQn | Active | CPUSS P-DMA0, Channel #47 Interrupt |
| 200 | cpuss_interrupts_dw0_48_IRQn | Active | CPUSS P-DMA0, Channel #48 Interrupt |
| 201 | cpuss_interrupts_dw0_49_IRQn | Active | CPUSS P-DMA0, Channel #49 Interrupt |
| 202 | cpuss_interrupts_dw0_50_IRQn | Active | CPUSS P-DMA0, Channel #50 Interrupt |
| 203 | cpuss_interrupts_dw0_51_IRQn | Active | CPUSS P-DMA0, Channel #51 Interrupt |
| 204 | cpuss_interrupts_dw0_52_IRQn | Active | CPUSS P-DMA0, Channel #52 Interrupt |
| 205 | cpuss_interrupts_dw0_53_IRQn | Active | CPUSS P-DMA0, Channel #53 Interrupt |
| 206 | cpuss_interrupts_dw0_54_IRQn | Active | CPUSS P-DMA0, Channel #54 Interrupt |
| 207 | cpuss_interrupts_dw0_55_IRQn | Active | CPUSS P-DMA0, Channel #55 Interrupt |
| 208 | cpuss_interrupts_dw0_56_IRQn | Active | CPUSS P-DMA0, Channel #56 Interrupt |
| 209 | cpuss_interrupts_dw0_57_IRQn | Active | CPUSS P-DMA0, Channel #57 Interrupt |
| 210 | cpuss_interrupts_dw0_58_IRQn | Active | CPUSS P-DMA0, Channel #58 Interrupt |
| 211 | cpuss_interrupts_dw0_59_IRQn | Active | CPUSS P-DMA0, Channel #59 Interrupt |
| 212 | cpuss_interrupts_dw0_60_IRQn | Active | CPUSS P-DMA0, Channel #60 Interrupt |
| 213 | cpuss_interrupts_dw0_61_IRQn | Active | CPUSS P-DMA0, Channel #61 Interrupt |
| 214 | cpuss_interrupts_dw0_62_IRQn | Active | CPUSS P-DMA0, Channel #62 Interrupt |
| 215 | cpuss_interrupts_dw0_63_IRQn | Active | CPUSS P-DMA0, Channel #63 Interrupt |
| 216 | cpuss_interrupts_dw0_64_IRQn | Active | CPUSS P-DMA0, Channel #64 Interrupt |
| 217 | cpuss_interrupts_dw0_65_IRQn | Active | CPUSS P-DMA0, Channel #65 Interrupt |
| 218 | cpuss_interrupts_dw0_66_IRQn | Active | CPUSS P-DMA0, Channel #66 Interrupt |
| 219 | cpuss_interrupts_dw0_67_IRQn | Active | CPUSS P-DMA0, Channel #67 Interrupt |
| 220 | cpuss_interrupts_dw0_68_IRQn | Active | CPUSS P-DMA0, Channel #68 Interrupt |
| 221 | cpuss_interrupts_dw0_69_IRQn | Active | CPUSS P-DMA0, Channel #69 Interrupt |
| 222 | cpuss_interrupts_dw0_70_IRQn | Active | CPUSS P-DMA0, Channel #70 Interrupt |
| 223 | cpuss_interrupts_dw0_71_IRQn | Active | CPUSS P-DMA0, Channel #71 Interrupt |
| 224 | cpuss_interrupts_dw0_72_IRQn | Active | CPUSS P-DMA0, Channel #72 Interrupt |
| 225 | cpuss_interrupts_dw0_73_IRQn | Active | CPUSS P-DMA0, Channel #73 Interrupt |
| 226 | cpuss_interrupts_dw0_74_IRQn | Active | CPUSS P-DMA0, Channel #74 Interrupt |
| 227 | cpuss_interrupts_dw0_75_IRQn | Active | CPUSS P-DMA0, Channel #75 Interrupt |
| 228 | cpuss_interrupts_dw0_76_IRQn | Active | CPUSS P-DMA0, Channel #76 Interrupt |
| 229 | cpuss_interrupts_dw0_77_IRQn | Active | CPUSS P-DMA0, Channel #77 Interrupt |
| 230 | cpuss_interrupts_dw0_78_IRQn | Active | CPUSS P-DMA0, Channel #78 Interrupt |
| 231 | cpuss_interrupts_dw0_79_IRQn | Active | CPUSS P-DMA0, Channel #79 Interrupt |
| 232 | cpuss_interrupts_dw0_80_IRQn | Active | CPUSS P-DMA0, Channel #80 Interrupt |
| 233 | cpuss_interrupts_dw0_81_IRQn | Active | CPUSS P-DMA0, Channel #81 Interrupt |
| 234 | cpuss_interrupts_dw0_82_IRQn | Active | CPUSS P-DMA0, Channel #82 Interrupt |
| 235 | cpuss_interrupts_dw0_83_IRQn | Active | CPUSS P-DMA0, Channel #83 Interrupt |
| 236 | cpuss_interrupts_dw0_84_IRQn | Active | CPUSS P-DMA0, Channel #84 Interrupt |
| 237 | cpuss_interrupts_dw0_85_IRQn | Active | CPUSS P-DMA0, Channel #85 Interrupt |
| 238 | cpuss_interrupts_dw0_86_IRQn | Active | CPUSS P-DMA0, Channel #86 Interrupt |

Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|------------------------------|------------|---------------------------------------|
| 239 | cpuss_interrupts_dw0_87_IRQn | Active | CPUSS P-DMA0, Channel #87 Interrupt |
| 240 | cpuss_interrupts_dw0_88_IRQn | Active | CPUSS P-DMA0, Channel #88 Interrupt |
| 241 | cpuss_interrupts_dw1_0_IRQn | Active | CPUSS P-DMA1, Channel #0 Interrupt |
| 242 | cpuss_interrupts_dw1_1_IRQn | Active | CPUSS P-DMA1, Channel #1 Interrupt |
| 243 | cpuss_interrupts_dw1_2_IRQn | Active | CPUSS P-DMA1, Channel #2 Interrupt |
| 244 | cpuss_interrupts_dw1_3_IRQn | Active | CPUSS P-DMA1, Channel #3 Interrupt |
| 245 | cpuss_interrupts_dw1_4_IRQn | Active | CPUSS P-DMA1, Channel #4 Interrupt |
| 246 | cpuss_interrupts_dw1_5_IRQn | Active | CPUSS P-DMA1, Channel #5 Interrupt |
| 247 | cpuss_interrupts_dw1_6_IRQn | Active | CPUSS P-DMA1, Channel #6 Interrupt |
| 248 | cpuss_interrupts_dw1_7_IRQn | Active | CPUSS P-DMA1, Channel #7 Interrupt |
| 249 | cpuss_interrupts_dw1_8_IRQn | Active | CPUSS P-DMA1, Channel #8 Interrupt |
| 250 | cpuss_interrupts_dw1_9_IRQn | Active | CPUSS P-DMA1, Channel #9 Interrupt |
| 251 | cpuss_interrupts_dw1_10_IRQn | Active | CPUSS P-DMA1, Channel #10 Interrupt |
| 252 | cpuss_interrupts_dw1_11_IRQn | Active | CPUSS P-DMA1, Channel #11 Interrupt |
| 253 | cpuss_interrupts_dw1_12_IRQn | Active | CPUSS P-DMA1, Channel #12 Interrupt |
| 254 | cpuss_interrupts_dw1_13_IRQn | Active | CPUSS P-DMA1, Channel #13 Interrupt |
| 255 | cpuss_interrupts_dw1_14_IRQn | Active | CPUSS P-DMA1, Channel #14 Interrupt |
| 256 | cpuss_interrupts_dw1_15_IRQn | Active | CPUSS P-DMA1, Channel #15 Interrupt |
| 257 | cpuss_interrupts_dw1_16_IRQn | Active | CPUSS P-DMA1, Channel #16 Interrupt |
| 258 | cpuss_interrupts_dw1_17_IRQn | Active | CPUSS P-DMA1, Channel #17 Interrupt |
| 259 | cpuss_interrupts_dw1_18_IRQn | Active | CPUSS P-DMA1, Channel #18 Interrupt |
| 260 | cpuss_interrupts_dw1_19_IRQn | Active | CPUSS P-DMA1, Channel #19 Interrupt |
| 261 | cpuss_interrupts_dw1_20_IRQn | Active | CPUSS P-DMA1, Channel #20 Interrupt |
| 262 | cpuss_interrupts_dw1_21_IRQn | Active | CPUSS P-DMA1, Channel #21 Interrupt |
| 263 | cpuss_interrupts_dw1_22_IRQn | Active | CPUSS P-DMA1, Channel #22 Interrupt |
| 264 | cpuss_interrupts_dw1_23_IRQn | Active | CPUSS P-DMA1, Channel #23 Interrupt |
| 265 | cpuss_interrupts_dw1_24_IRQn | Active | CPUSS P-DMA1, Channel #24 Interrupt |
| 266 | cpuss_interrupts_dw1_25_IRQn | Active | CPUSS P-DMA1, Channel #25 Interrupt |
| 267 | cpuss_interrupts_dw1_26_IRQn | Active | CPUSS P-DMA1, Channel #26 Interrupt |
| 268 | cpuss_interrupts_dw1_27_IRQn | Active | CPUSS P-DMA1, Channel #27 Interrupt |
| 269 | cpuss_interrupts_dw1_28_IRQn | Active | CPUSS P-DMA1, Channel #28 Interrupt |
| 270 | cpuss_interrupts_dw1_29_IRQn | Active | CPUSS P-DMA1, Channel #29 Interrupt |
| 271 | cpuss_interrupts_dw1_30_IRQn | Active | CPUSS P-DMA1, Channel #30 Interrupt |
| 272 | cpuss_interrupts_dw1_31_IRQn | Active | CPUSS P-DMA1, Channel #31 Interrupt |
| 273 | cpuss_interrupts_dw1_32_IRQn | Active | CPUSS P-DMA1, Channel #32 Interrupt |
| 274 | tcpwm_0_interrupts_0_IRQn | Active | TCPWM0 Group #0, Counter #0 Interrupt |
| 275 | tcpwm_0_interrupts_1_IRQn | Active | TCPWM0 Group #0, Counter #1 Interrupt |
| 276 | tcpwm_0_interrupts_2_IRQn | Active | TCPWM0 Group #0, Counter #2 Interrupt |
| 277 | tcpwm_0_interrupts_3_IRQn | Active | TCPWM0 Group #0, Counter #3 Interrupt |
| 278 | tcpwm_0_interrupts_4_IRQn | Active | TCPWM0 Group #0, Counter #4 Interrupt |
| 279 | tcpwm_0_interrupts_5_IRQn | Active | TCPWM0 Group #0, Counter #5 Interrupt |

Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|----------------------------|------------|--|
| 280 | tcpwm_0_interrupts_6_IRQn | Active | TCPWM0 Group #0, Counter #6 Interrupt |
| 281 | tcpwm_0_interrupts_7_IRQn | Active | TCPWM0 Group #0, Counter #7 Interrupt |
| 282 | tcpwm_0_interrupts_8_IRQn | Active | TCPWM0 Group #0, Counter #8 Interrupt |
| 283 | tcpwm_0_interrupts_9_IRQn | Active | TCPWM0 Group #0, Counter #9 Interrupt |
| 284 | tcpwm_0_interrupts_10_IRQn | Active | TCPWM0 Group #0, Counter #10 Interrupt |
| 285 | tcpwm_0_interrupts_11_IRQn | Active | TCPWM0 Group #0, Counter #11 Interrupt |
| 286 | tcpwm_0_interrupts_12_IRQn | Active | TCPWM0 Group #0, Counter #12 Interrupt |
| 287 | tcpwm_0_interrupts_13_IRQn | Active | TCPWM0 Group #0, Counter #13 Interrupt |
| 288 | tcpwm_0_interrupts_14_IRQn | Active | TCPWM0 Group #0, Counter #14 Interrupt |
| 289 | tcpwm_0_interrupts_15_IRQn | Active | TCPWM0 Group #0, Counter #15 Interrupt |
| 290 | tcpwm_0_interrupts_16_IRQn | Active | TCPWM0 Group #0, Counter #16 Interrupt |
| 291 | tcpwm_0_interrupts_17_IRQn | Active | TCPWM0 Group #0, Counter #17 Interrupt |
| 292 | tcpwm_0_interrupts_18_IRQn | Active | TCPWM0 Group #0, Counter #18 Interrupt |
| 293 | tcpwm_0_interrupts_19_IRQn | Active | TCPWM0 Group #0, Counter #19 Interrupt |
| 294 | tcpwm_0_interrupts_20_IRQn | Active | TCPWM0 Group #0, Counter #20 Interrupt |
| 295 | tcpwm_0_interrupts_21_IRQn | Active | TCPWM0 Group #0, Counter #21 Interrupt |
| 296 | tcpwm_0_interrupts_22_IRQn | Active | TCPWM0 Group #0, Counter #22 Interrupt |
| 297 | tcpwm_0_interrupts_23_IRQn | Active | TCPWM0 Group #0, Counter #23 Interrupt |
| 298 | tcpwm_0_interrupts_24_IRQn | Active | TCPWM0 Group #0, Counter #24 Interrupt |
| 299 | tcpwm_0_interrupts_25_IRQn | Active | TCPWM0 Group #0, Counter #25 Interrupt |
| 300 | tcpwm_0_interrupts_26_IRQn | Active | TCPWM0 Group #0, Counter #26 Interrupt |
| 301 | tcpwm_0_interrupts_27_IRQn | Active | TCPWM0 Group #0, Counter #27 Interrupt |
| 302 | tcpwm_0_interrupts_28_IRQn | Active | TCPWM0 Group #0, Counter #28 Interrupt |
| 303 | tcpwm_0_interrupts_29_IRQn | Active | TCPWM0 Group #0, Counter #29 Interrupt |
| 304 | tcpwm_0_interrupts_30_IRQn | Active | TCPWM0 Group #0, Counter #30 Interrupt |
| 305 | tcpwm_0_interrupts_31_IRQn | Active | TCPWM0 Group #0, Counter #31 Interrupt |
| 306 | tcpwm_0_interrupts_32_IRQn | Active | TCPWM0 Group #0, Counter #32 Interrupt |
| 307 | tcpwm_0_interrupts_33_IRQn | Active | TCPWM0 Group #0, Counter #33 Interrupt |
| 308 | tcpwm_0_interrupts_34_IRQn | Active | TCPWM0 Group #0, Counter #34 Interrupt |
| 309 | tcpwm_0_interrupts_35_IRQn | Active | TCPWM0 Group #0, Counter #35 Interrupt |
| 310 | tcpwm_0_interrupts_36_IRQn | Active | TCPWM0 Group #0, Counter #36 Interrupt |
| 311 | tcpwm_0_interrupts_37_IRQn | Active | TCPWM0 Group #0, Counter #37 Interrupt |
| 312 | tcpwm_0_interrupts_38_IRQn | Active | TCPWM0 Group #0, Counter #38 Interrupt |
| 313 | tcpwm_0_interrupts_39_IRQn | Active | TCPWM0 Group #0, Counter #39 Interrupt |
| 314 | tcpwm_0_interrupts_40_IRQn | Active | TCPWM0 Group #0, Counter #40 Interrupt |
| 315 | tcpwm_0_interrupts_41_IRQn | Active | TCPWM0 Group #0, Counter #41 Interrupt |
| 316 | tcpwm_0_interrupts_42_IRQn | Active | TCPWM0 Group #0, Counter #42 Interrupt |
| 317 | tcpwm_0_interrupts_43_IRQn | Active | TCPWM0 Group #0, Counter #43 Interrupt |
| 318 | tcpwm_0_interrupts_44_IRQn | Active | TCPWM0 Group #0, Counter #44 Interrupt |
| 319 | tcpwm_0_interrupts_45_IRQn | Active | TCPWM0 Group #0, Counter #45 Interrupt |
| 320 | tcpwm_0_interrupts_46_IRQn | Active | TCPWM0 Group #0, Counter #46 Interrupt |

Table 14-1 Peripheral interrupt assignments and wake-up sources (continued)

| Interrupt | Source | Power Mode | Description |
|-----------|-----------------------------|------------|--|
| 321 | tcpwm_0_interrupts_47_IRQn | Active | TCPWM0 Group #0, Counter #47 Interrupt |
| 322 | tcpwm_0_interrupts_48_IRQn | Active | TCPWM0 Group #0, Counter #48 Interrupt |
| 323 | tcpwm_0_interrupts_49_IRQn | Active | TCPWM0 Group #0, Counter #49 Interrupt |
| 324 | tcpwm_0_interrupts_50_IRQn | Active | TCPWM0 Group #0, Counter #50 Interrupt |
| 325 | tcpwm_0_interrupts_51_IRQn | Active | TCPWM0 Group #0, Counter #51 Interrupt |
| 326 | tcpwm_0_interrupts_52_IRQn | Active | TCPWM0 Group #0, Counter #52 Interrupt |
| 327 | tcpwm_0_interrupts_53_IRQn | Active | TCPWM0 Group #0, Counter #53 Interrupt |
| 328 | tcpwm_0_interrupts_54_IRQn | Active | TCPWM0 Group #0, Counter #54 Interrupt |
| 329 | tcpwm_0_interrupts_55_IRQn | Active | TCPWM0 Group #0, Counter #55 Interrupt |
| 330 | tcpwm_0_interrupts_56_IRQn | Active | TCPWM0 Group #0, Counter #56 Interrupt |
| 331 | tcpwm_0_interrupts_57_IRQn | Active | TCPWM0 Group #0, Counter #57 Interrupt |
| 332 | tcpwm_0_interrupts_58_IRQn | Active | TCPWM0 Group #0, Counter #58 Interrupt |
| 333 | tcpwm_0_interrupts_59_IRQn | Active | TCPWM0 Group #0, Counter #59 Interrupt |
| 334 | tcpwm_0_interrupts_60_IRQn | Active | TCPWM0 Group #0, Counter #60 Interrupt |
| 335 | tcpwm_0_interrupts_61_IRQn | Active | TCPWM0 Group #0, Counter #61 Interrupt |
| 336 | tcpwm_0_interrupts_62_IRQn | Active | TCPWM0 Group #0, Counter #62 Interrupt |
| 337 | tcpwm_0_interrupts_256_IRQn | Active | TCPWM0 Group #1, Counter #0 Interrupt |
| 338 | tcpwm_0_interrupts_257_IRQn | Active | TCPWM0 Group #1, Counter #1 Interrupt |
| 339 | tcpwm_0_interrupts_258_IRQn | Active | TCPWM0 Group #1, Counter #2 Interrupt |
| 340 | tcpwm_0_interrupts_259_IRQn | Active | TCPWM0 Group #1, Counter #3 Interrupt |
| 341 | tcpwm_0_interrupts_260_IRQn | Active | TCPWM0 Group #1, Counter #4 Interrupt |
| 342 | tcpwm_0_interrupts_261_IRQn | Active | TCPWM0 Group #1, Counter #5 Interrupt |
| 343 | tcpwm_0_interrupts_262_IRQn | Active | TCPWM0 Group #1, Counter #6 Interrupt |
| 344 | tcpwm_0_interrupts_263_IRQn | Active | TCPWM0 Group #1, Counter #7 Interrupt |
| 345 | tcpwm_0_interrupts_264_IRQn | Active | TCPWM0 Group #1, Counter #8 Interrupt |
| 346 | tcpwm_0_interrupts_265_IRQn | Active | TCPWM0 Group #1, Counter #9 Interrupt |
| 347 | tcpwm_0_interrupts_266_IRQn | Active | TCPWM0 Group #1, Counter #10 Interrupt |
| 348 | tcpwm_0_interrupts_267_IRQn | Active | TCPWM0 Group #1, Counter #11 Interrupt |
| 349 | tcpwm_0_interrupts_512_IRQn | Active | TCPWM0 Group #2, Counter #0 Interrupt |
| 350 | tcpwm_0_interrupts_513_IRQn | Active | TCPWM0 Group #2, Counter #1 Interrupt |
| 351 | tcpwm_0_interrupts_514_IRQn | Active | TCPWM0 Group #2, Counter #2 Interrupt |
| 352 | tcpwm_0_interrupts_515_IRQn | Active | TCPWM0 Group #2, Counter #3 Interrupt |

15 Core interrupt types

Table 15-1 Core interrupt types

| Interrupt | Source | Power Mode | Description |
|-----------|---------------------------------|------------|--------------------------------|
| 0 | CPUIntIdx0_IRQn ^[30] | DeepSleep | CPU User Interrupt #0 |
| 1 | CPUIntIdx1_IRQn ^[30] | DeepSleep | CPU User Interrupt #1 |
| 2 | CPUIntIdx2_IRQn | DeepSleep | CPU User Interrupt #2 |
| 3 | CPUIntIdx3_IRQn | DeepSleep | CPU User Interrupt #3 |
| 4 | CPUIntIdx4_IRQn | DeepSleep | CPU User Interrupt #4 |
| 5 | CPUIntIdx5_IRQn | DeepSleep | CPU User Interrupt #5 |
| 6 | CPUIntIdx6_IRQn | DeepSleep | CPU User Interrupt #6 |
| 7 | CPUIntIdx7_IRQn | DeepSleep | CPU User Interrupt #7 |
| 8 | Internal0_IRQn | Active | Internal Software Interrupt #0 |
| 9 | Internal1_IRQn | Active | Internal Software Interrupt #1 |
| 10 | Internal2_IRQn | Active | Internal Software Interrupt #2 |
| 11 | Internal3_IRQn | Active | Internal Software Interrupt #3 |
| 12 | Internal4_IRQn | Active | Internal Software Interrupt #4 |
| 13 | Internal5_IRQn | Active | Internal Software Interrupt #5 |
| 14 | Internal6_IRQn | Active | Internal Software Interrupt #6 |
| 15 | Internal7_IRQn | Active | Internal Software Interrupt #7 |

Note

30. User interrupt cannot be used for CM0+ application, as it is used internally by system calls. Note, this does not impact CM4 application.

16 Trigger multiplexer

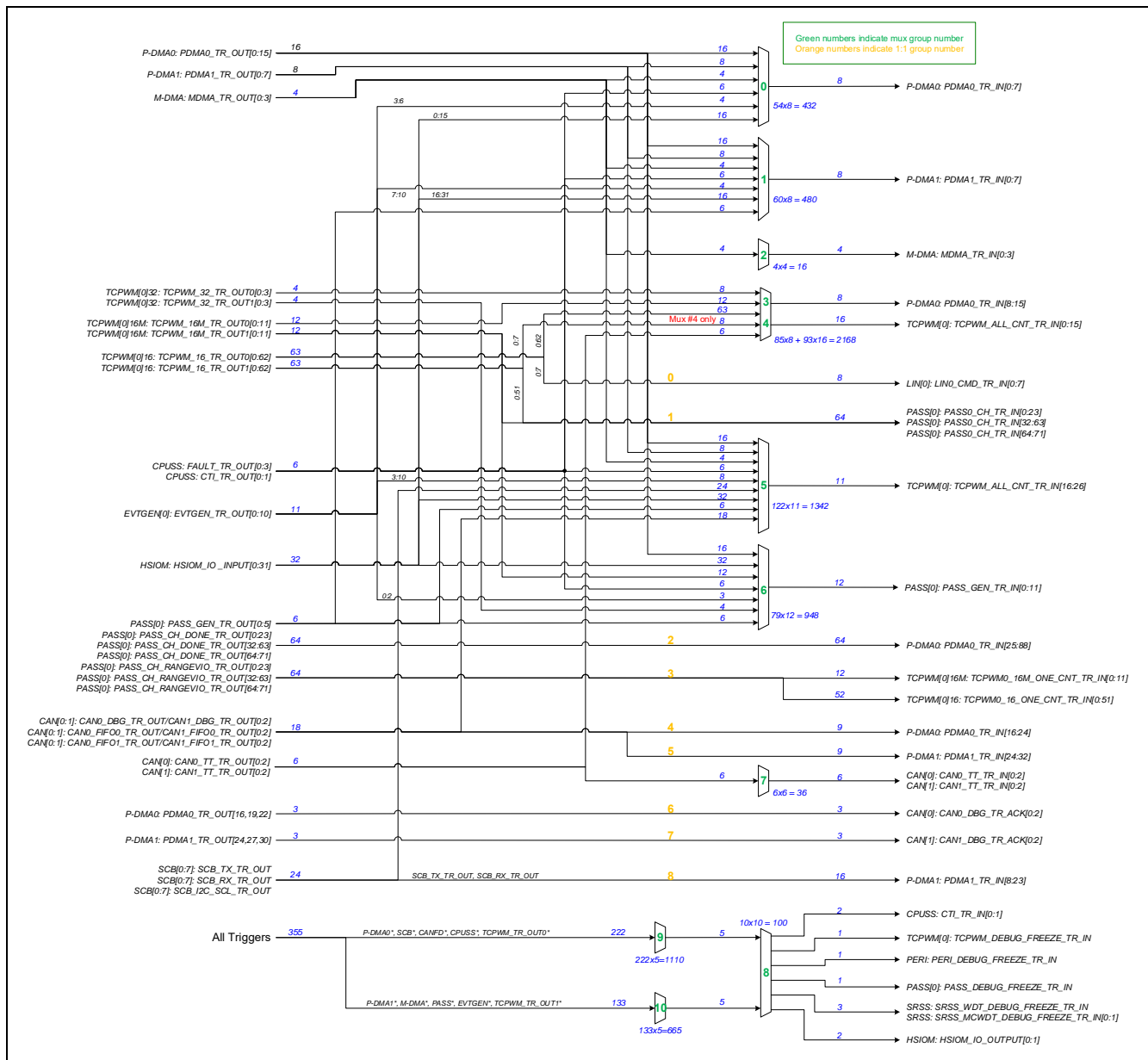


Figure 16-1 Trigger multiplexer^[31]

Note

31. The diagram shows only the TRIG_LABEL, final trigger formation is based on the formula $\text{TRIG_}\{\text{PREFIX(IN/OUT)}\}_{}_{\{\text{MUX_x}\}}_{}_{\{\text{TRIG_LABEL}\}}$ / $\text{TRIG_}\{\text{PREFIX(IN_1TO1/OUT_1TO1)}\}_{}_{\{\text{x}\}}_{}_{\{\text{TRIG_LABEL}\}}$ and Table 17-1, Table 18-1, and Table 19-1.

17 Triggers group inputs

Table 17-1 Trigger inputs

| Input | Trigger Label (TRIG_LABEL) | Description |
|---|----------------------------|---|
| MUX Group 0: PDMA0_TR (P-DMA0_0_15 trigger multiplexer) | | |
| 1:16 ^[32] | PDMA0_TR_OUT[0:15] | Allow P-DMA0 to chain to itself, useful for triggering once per row for 2D transfer |
| 17:24 | PDMA1_TR_OUT[0:7] | Cross connections from P-DMA1 to P-DMA0, Channels 0-7 are used |
| 25:28 | MDMA_TR_OUT[0:3] | Cross connections from M-DMA0 to P-DMA0 |
| 29:32 | FAULT_TR_OUT[0:3] | Allow faults to initiate data transfer for debug purposes |
| 33:34 | CTI_TR_OUT[0:1] | Trace events |
| 35:38 | EVTGEN_TR_OUT[3:6] | EVTGEN triggers |
| 39:54 | HSIOM_IO_INPUT[0:15] | I/O inputs |
| MUX Group 1: PDMA1_TR (P-DMA1 trigger multiplexer) | | |
| 1:16 | PDMA0_TR_OUT[0:15] | Allow P-DMA0 to trigger P-DMA1 |
| 17:24 | PDMA1_TR_OUT[0:7] | Allow P-DMA1 to chain to itself, useful for triggering once per row for 2D transfer |
| 25:28 | MDMA_TR_OUT[0:3] | Allow M-DMA0 to trigger P-DMA0 |
| 29:32 | FAULT_TR_OUT[0:3] | Allow faults to initiate data transfer for debug purposes |
| 33:34 | CTI_TR_OUT[0:1] | Trace events |
| 35:38 | EVTGEN_TR_OUT[7:10] | EVTGEN triggers |
| 39:54 | HSIOM_IO_INPUT[16:31] | I/O inputs |
| 55:60 | PASS_GEN_TR_OUT[0:5] | PASS SAR events |
| MUX Group 2: MDMA (M-DMA0 trigger multiplexer) | | |
| 1:4 | MDMA_TR_OUT[0:3] | Allow M-DMA0 to trigger itself |
| MUX Group 3: TCPWM_TO_PDMA0 (TCPWM0 to P-DMA0 trigger multiplexer) | | |
| 1:4 | TCPWM_32_TR_OUT0[0:3] | 32-bit TCPWM0 counters |
| 5:16 | TCPWM_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM0 counters |
| 17:79 | TCPWM_16_TR_OUT0[0:62] | 16-bit TCPWM0 counters |
| 80:82 | CAN0_TT_TR_OUT[0:2] | CAN0 TT Sync Outputs |
| 83:85 | CAN1_TT_TR_OUT[0:2] | CAN1 TT Sync Outputs |
| MUX Group 4: TCPWM_OUT (TCPWM0 loop back multiplexer) | | |
| 1:4 | TCPWM_32_TR_OUT0[0:3] | 32-bit TCPWM0 counters |
| 5:16 | TCPWM_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM0 counters |
| 17:79 | TCPWM_16_TR_OUT0[0:62] | 16-bit TCPWM0 counters |
| 80:87 | TCPWM_16_TR_OUT1[0:7] | Allows feedback of two signals from same counters |
| 88:90 | CAN0_TT_TR_OUT[0:2] | CAN0 TT Sync Outputs |
| 91:93 | CAN1_TT_TR_OUT[0:2] | CAN1 TT Sync Outputs |
| MUX Group 5: TCPWM_IN (TCPWM0 Trigger Multiplexer) | | |
| 1:16 | PDMA0_TR_OUT[0:15] | General purpose P-DMA0 triggers |
| 17:24 | PDMA1_TR_OUT[0:7] | General purpose P-DMA1 triggers |
| 25:28 | MDMA_TR_OUT[0:3] | M-DMA0 triggers |

Note

32: "a:b" depicts a range starting from 'a' through 'b'.

Triggers group inputs

Table 17-1 Trigger inputs (continued)

| Input | Trigger Label (TRIG_LABEL) | Description |
|---------|----------------------------|-------------------------------|
| 29:30 | CTI_TR_OUT[0:1] | Trace events |
| 31:34 | FAULT_TR_OUT[0:3] | Fault events |
| 35:40 | PASS_GEN_TR_OUT[0:5] | PASS SAR events |
| 41:72 | HSIOM_IO_INPUT[0:31] | I/O inputs |
| 73 | SCB_TX_TR_OUT[0] | SCB0 TX trigger |
| 74 | SCB_RX_TR_OUT[0] | SCB0 RX trigger |
| 75 | SCB_I2C_SCL_TR_OUT[0] | SCB0 I ² C trigger |
| 76 | SCB_TX_TR_OUT[1] | SCB1 TX trigger |
| 77 | SCB_RX_TR_OUT[1] | SCB1 RX trigger |
| 78 | SCB_I2C_SCL_TR_OUT[1] | SCB1 I ² C trigger |
| 79 | SCB_TX_TR_OUT[2] | SCB2 TX trigger |
| 80 | SCB_RX_TR_OUT[2] | SCB2 RX trigger |
| 81 | SCB_I2C_SCL_TR_OUT[2] | SCB2 I ² C trigger |
| 82 | SCB_TX_TR_OUT[3] | SCB3 TX trigger |
| 83 | SCB_RX_TR_OUT[3] | SCB3 RX trigger |
| 84 | SCB_I2C_SCL_TR_OUT[3] | SCB3 I ² C trigger |
| 85 | SCB_TX_TR_OUT[4] | SCB4 TX trigger |
| 86 | SCB_RX_TR_OUT[4] | SCB4 RX trigger |
| 87 | SCB_I2C_SCL_TR_OUT[4] | SCB4 I ² C trigger |
| 88 | SCB_TX_TR_OUT[5] | SCB5 TX trigger |
| 89 | SCB_RX_TR_OUT[5] | SCB5 RX trigger |
| 90 | SCB_I2C_SCL_TR_OUT[5] | SCB5 I ² C trigger |
| 91 | SCB_TX_TR_OUT[6] | SCB6 TX trigger |
| 92 | SCB_RX_TR_OUT[6] | SCB6 RX trigger |
| 93 | SCB_I2C_SCL_TR_OUT[6] | SCB6 I ² C trigger |
| 94 | SCB_TX_TR_OUT[7] | SCB7 TX trigger |
| 95 | SCB_RX_TR_OUT[7] | SCB7 RX trigger |
| 96 | SCB_I2C_SCL_TR_OUT[7] | SCB7 I ² C trigger |
| 97:99 | CAN0_DBG_TR_OUT[0:2] | CAN0 M-DMA0 events |
| 100:102 | CAN0_FIFO0_TR_OUT[0:2] | CAN0 FIFO0 events |
| 103:105 | CAN0_FIFO1_TR_OUT[0:2] | CAN0 FIFO1 events |
| 106:108 | CAN1_DBG_TR_OUT[0:2] | CAN1 M-DMA0 events |
| 109:111 | CAN1_FIFO0_TR_OUT[0:2] | CAN1 FIFO0 events |
| 112:114 | CAN1_FIFO1_TR_OUT[0:2] | CAN1 FIFO1 events |
| 115:122 | EVTGEN_TR_OUT[3:10] | EVTGEN triggers |

MUX Group 6: PASS (PASS SAR trigger multiplexer)

| | | |
|-------|----------------------|---------------------------------|
| 1:16 | PDMA0_TR_OUT[0:15] | General purpose P-DMA0 triggers |
| 17:18 | CTI_TR_OUT[0:1] | Trace events |
| 19:22 | FAULT_TR_OUT[0:3] | Fault events |
| 23:25 | EVTGEN_TR_OUT[0:2] | EVTGEN triggers |
| 26:31 | PASS_GEN_TR_OUT[0:5] | PASS SAR done signals |

Triggers group inputs

Table 17-1 Trigger inputs (continued)

| Input | Trigger Label (TRIG_LABEL) | Description |
|---|----------------------------|--|
| 32:63 | HSIOM_IO_INPUT[0:31] | I/O inputs |
| 64:67 | TCPWM_32_TR_OUT1[0:3] | 32-bit TCPWM0 counters |
| 68:79 | TCPWM_16M_TR_OUT1[0:11] | 16-bit Motor enhanced TCPWM0 counters |
| MUX Group 7: CAN TT sync triggers | | |
| 1:3 | CAN0_TT_TR_OUT[0:2] | CAN0 TT Sync Outputs |
| 4:6 | CAN1_TT_TR_OUT[0:2] | CAN1 TT Sync Outputs |
| MUX Group 8: DebugMain (Debug Multiplexer) | | |
| 1:5 | TR_GROUP9_OUTPUT[0:4] | Output from debug reduction multiplexer #1 |
| 6:10 | TR_GROUP10_OUTPUT[0:4] | Output from debug reduction multiplexer #2 |
| MUX Group 9: DebugReduction1 (Debug Reduction #1) | | |
| 1:89 | PDMA0_TR_OUT[0:88] | P-DMA0 triggers |
| 90:97 | SCB_TX_TR_OUT[0:7] | SCB TTCAN tx Triggers |
| 98:105 | SCB_RX_TR_OUT[0:7] | SCB TTCAN rx Triggers |
| 106:113 | SCB_I2C_SCL_TR_OUT[0:7] | SCB I ² C triggers |
| 114:116 | CAN0_DBG_TR_OUT[0:2] | CAN0 P-DMA |
| 117:119 | CAN0_FIFO0_TR_OUT[0:2] | CAN0 FIFO0 |
| 120:122 | CAN0_FIFO1_TR_OUT[0:2] | CAN0 FIFO1 |
| 123:125 | CAN0_TT_TR_OUT[0:2] | CAN TT Sync Outputs |
| 126:128 | CAN1_DBG_TR_OUT[0:2] | CAN1 P-DMA |
| 129:131 | CAN1_FIFO0_TR_OUT[0:2] | CAN1 FIFO0 |
| 132:134 | CAN1_FIFO1_TR_OUT[0:2] | CAN1 FIFO1 |
| 135:137 | CAN1_TT_TR_OUT[0:2] | CAN TT Sync Outputs |
| 138:139 | CTI_TR_OUT[0:1] | Trace events |
| 140:143 | FAULT_TR_OUT[0:3] | Fault events |
| 144:147 | TCPWM_32_TR_OUT0[0:3] | 32-bit TCPWM0 counters |
| 148:159 | TCPWM_16M_TR_OUT0[0:11] | 16-bit Motor enhanced TCPWM0 counters |
| 160:222 | TCPWM_16_TR_OUT0[0:62] | 16-bit TCPWM0 counters |
| MUX Group 10: DebugReduction2 (Debug Reduction #2) | | |
| 1:33 | PDMA1_TR_OUT[0:32] | 16-bit Motor enhanced TCPWM0 counters |
| 34:37 | MDMA_TR_OUT[0:3] | 16-bit TCPWM0 counters |
| 38:41 | TCPWM_32_TR_OUT1[0:3] | 32-bit TCPWM0 counters |
| 42:53 | TCPWM_16M_TR_OUT1[0:11] | 16-bit Motor enhanced TCPWM0 counters |
| 54:116 | TCPWM_16_TR_OUT1[0:62] | 16-bit TCPWM0 counters |
| 117:122 | PASS_GEN_TR_OUT[0:5] | PASS SAR conversion complete events |
| 123:133 | EVTGEN_TR_OUT[0:10] | EVTGEN Triggers |

Triggers group outputs

18 Triggers group outputs

Table 18-1 Trigger outputs

| Output | Trigger Label (TRIG_LABEL) | Description |
|---|------------------------------------|------------------------------------|
| MUX Group 0: PDMA0_TR (P-DMA0 trigger multiplexer) | | |
| 0:7 | PDMA0_TR_IN[0:7] | Triggers to P-DMA0[0:7] |
| MUX Group 1: PDMA1_TR (P-DMA1 trigger multiplexer) | | |
| 0:7 | PDMA1_TR_IN[0:7] | Triggers to P-DMA1[0:7] |
| MUX Group 2: MDMA (M-DMA0 trigger multiplexer) | | |
| 0:3 | MDMA_TR_IN[0:3] | Triggers to M-DMA0 |
| MUX Group 3: TCPWM_TO_PDMA0 (TCPWM0 to P-DMA0 trigger multiplexer) | | |
| 0:7 | PDMA0_TR_IN[8:15] | Triggers to P-DMA0[8:15] |
| MUX Group 4: TCPWM_OUT (TCPWM0 loop back multiplexer) | | |
| 0:15 | TCPWM_ALL_CNT_TR_IN[0:15] | All counters trigger input |
| MUX Group 5: TCPWM_IN (TCPWM0 Trigger Multiplexer) | | |
| 0:10 | TCPWM_ALL_CNT_TR_IN[16:26] | Triggers to TCPWM0 |
| MUX Group 6: PASS (PASS SAR trigger multiplexer) | | |
| 0:11 | PASS_GEN_TR_IN[0:11] | Triggers to SAR ADCs |
| MUX Group 7: CANTT (CAN TT Sync) | | |
| 0:2 | CAN0_TT_TR_IN[0:2] | CAN0 TT Sync Inputs |
| 3:5 | CAN1_TT_TR_IN[0:2] | CAN1 TT Sync Inputs |
| MUX Group 8: DebugMain (Debug Multiplexer) | | |
| 0:1 | HSIOM_IO_OUTPUT[0:1] | To HSIOM as an output |
| 2:3 | CTI_TR_IN[0:1] | To CPU Cross Trigger system |
| 4 | PERI_DEBUG_FREEZE_TR_IN | Signal to Freeze PERI operation |
| 5 | PASS_DEBUG_FREEZE_TR_IN | Signal to Freeze SAR ADC operation |
| 6 | SRSS_WDT_DEBUG_FREEZE_TR_IN | Signal to Freeze WDT operation |
| 7:8 | SRSS_MCWDT_DEBUG_FREEZE_TR_IN[0:1] | Signal to Freeze MCWDT operation |
| 9 | TCPWM_DEBUG_FREEZE_TR_IN | Signal to Freeze TCPWM0 operation |
| MUX Group 9: DebugReduction1 (Debug Reduction #1) | | |
| 0:4 | TR_GROUP8_INPUT[1:5] | To main debug multiplexer |
| MUX Group 10: DebugReduction2 (Debug Reduction #2) | | |
| 0:4 | TR_GROUP8_INPUT[6:10] | To main debug multiplexer |

Triggers one-to-one

19 Triggers one-to-one

Table 19-1 Triggers 1:1

| Input | Trigger In | Trigger Out | Description |
|--|------------------------------|------------------------------|---|
| MUX Group 0: TCPWM0 to LIN0 Triggers | | | |
| 0:7 | TCPWM0_16_TR_OUT0[0:7] | LIN0_CMD_TR_IN[0:7] | TCPWM0 (Group #0 Counter #00 to #07) to LIN0 |
| MUX Group 1: TCPWM0 to PASS SARx direct connect | | | |
| 0 | TCPWM0_16M_TR_OUT1[0] | PASS0_CH_TR_IN[0] | TCPWM0 Group #1 Counter #00 (PWM0_M_0) to SAR0 ch#0 |
| 1 | TCPWM0_16M_TR_OUT1[1] | PASS0_CH_TR_IN[1] | TCPWM0 Group #1 Counter #03 (PWM0_M_3) to SAR0 ch#1 |
| 2 | TCPWM0_16M_TR_OUT1[2] | PASS0_CH_TR_IN[2] | TCPWM0 Group #1 Counter #06 (PWM0_M_6) to SAR0 ch#2 |
| 3 | TCPWM0_16M_TR_OUT1[3] | PASS0_CH_TR_IN[3] | TCPWM0 Group #1 Counter #09 (PWM0_M_9) to SAR0 ch#3 |
| 4:23 | TCPWM0_16_TR_OUT1[0:19] | PASS0_CH_TR_IN[4:23] | TCPWM0 Group #0 Counter #00 through 19 (PWM0_0 to PWM0_19) to SAR0 ch#4 through SAR0 ch#23 |
| 24 | TCPWM0_16M_TR_OUT1[4] | PASS0_CH_TR_IN[32] | TCPWM0 Group #1 Counter #01 (PWM0_M_1) to SAR1 ch#0 |
| 25 | TCPWM0_16M_TR_OUT1[5] | PASS0_CH_TR_IN[33] | TCPWM0 Group #1 Counter #04 (PWM0_M_4) to SAR1 ch#1 |
| 26 | TCPWM0_16M_TR_OUT1[6] | PASS0_CH_TR_IN[34] | TCPWM0 Group #1 Counter #07 (PWM0_M_7) to SAR1 ch#2 |
| 27 | TCPWM0_16M_TR_OUT1[7] | PASS0_CH_TR_IN[35] | TCPWM0 Group #1 Counter #10 (PWM0_M_10) to SAR1 ch#3 |
| 28:55 | TCPWM0_16_TR_OUT1[20:47] | PASS0_CH_TR_IN[36:63] | TCPWM0 Group #0 Counter #20 through 47 (PWM0_20 to PWM0_47) to SAR1 ch#4 through SAR1 ch#31 |
| 56 | TCPWM0_16M_TR_OUT1[8] | PASS0_CH_TR_IN[64] | TCPWM0 Group #1 Counter #02 (PWM0_M_2) to SAR2 ch#0 |
| 57 | TCPWM0_16M_TR_OUT1[9] | PASS0_CH_TR_IN[65] | TCPWM0 Group #1 Counter #05 (PWM0_M_5) to SAR2 ch#1 |
| 58 | TCPWM0_16M_TR_OUT1[10] | PASS0_CH_TR_IN[66] | TCPWM0 Group #1 Counter #08 (PWM0_M_8) to SAR2 ch#2 |
| 59 | TCPWM0_16M_TR_OUT1[11] | PASS0_CH_TR_IN[67] | TCPWM0 Group #1 Counter #11 (PWM0_M_11) to SAR2 ch#3 |
| 60:63 | TCPWM0_16_TR_OUT1[48:51] | PASS0_CH_TR_IN[68:71] | TCPWM0 Group #0 Counter #48 through 51 (PWM0_48 to PWM0_51) to SAR2 ch#4 through SAR2 ch#7 |
| MUX Group 2: PASS SARx to P-DMA0 direct connect | | | |
| 0:23 | PASS0_CH_DONE_TR_OUT[0:23] | PDMA0_TR_IN[25:48] | PASS SAR0 [0:23] to P-DMA0 direct connect |
| 24:55 | PASS0_CH_DONE_TR_OUT[32:63] | PDMA0_TR_IN[49:80] | PASS SAR1 [0:31] to P-DMA0 direct connect |
| 56:63 | PASS0_CH_DONE_TR_OUT[64:71] | PDMA0_TR_IN[81:88] | PASS SAR2 [0:7] to P-DMA0 direct connect |
| MUX Group 3: PASS SARx to TCPWM0 direct connect | | | |
| 0 | PASS0_CH_RANGEVIO_TR_OUT[0] | TCPWM0_16M_ONE_CNT_TR_IN[0] | SAR0 ch#0 ^[33] , range violation to TCPWM0 Group #1 Counter #00 trig=2 |
| 1 | PASS0_CH_RANGEVIO_TR_OUT[1] | TCPWM0_16M_ONE_CNT_TR_IN[3] | SAR0 ch#1, range violation to TCPWM0 Group #1 Counter #03 trig=2 |
| 2 | PASS0_CH_RANGEVIO_TR_OUT[2] | TCPWM0_16M_ONE_CNT_TR_IN[6] | SAR0 ch#2, range violation to TCPWM0 Group #1 Counter #06 trig=2 |
| 3 | PASS0_CH_RANGEVIO_TR_OUT[3] | TCPWM0_16M_ONE_CNT_TR_IN[9] | SAR0 ch#3, range violation to TCPWM0 Group #1 Counter #09 trig=2 |
| 4 | PASS0_CH_RANGEVIO_TR_OUT[4] | TCPWM0_16M_ONE_CNT_TR_IN[0] | SAR0 ch#4, range violation to TCPWM0 Group #0 Counter #00 trig=2 |
| 5 | PASS0_CH_RANGEVIO_TR_OUT[5] | TCPWM0_16M_ONE_CNT_TR_IN[1] | SAR0 ch#5, range violation to TCPWM0 Group #0 Counter #01 trig=2 |
| 6 | PASS0_CH_RANGEVIO_TR_OUT[6] | TCPWM0_16M_ONE_CNT_TR_IN[2] | SAR0 ch#6, range violation to TCPWM0 Group #0 Counter #02 trig=2 |
| 7 | PASS0_CH_RANGEVIO_TR_OUT[7] | TCPWM0_16M_ONE_CNT_TR_IN[3] | SAR0 ch#7, range violation to TCPWM0 Group #0 Counter #03 trig=2 |
| 8 | PASS0_CH_RANGEVIO_TR_OUT[8] | TCPWM0_16M_ONE_CNT_TR_IN[4] | SAR0 ch#8, range violation to TCPWM0 Group #0 Counter #04 trig=2 |
| 9 | PASS0_CH_RANGEVIO_TR_OUT[9] | TCPWM0_16M_ONE_CNT_TR_IN[5] | SAR0 ch#9, range violation to TCPWM0 Group #0 Counter #05 trig=2 |
| 10 | PASS0_CH_RANGEVIO_TR_OUT[10] | TCPWM0_16M_ONE_CNT_TR_IN[6] | SAR0 ch#10, range violation to TCPWM0 Group #0 Counter #06 trig=2 |
| 11 | PASS0_CH_RANGEVIO_TR_OUT[11] | TCPWM0_16M_ONE_CNT_TR_IN[7] | SAR0 ch#11, range violation to TCPWM0 Group #0 Counter #07 trig=2 |
| 12 | PASS0_CH_RANGEVIO_TR_OUT[12] | TCPWM0_16M_ONE_CNT_TR_IN[8] | SAR0 ch#12, range violation to TCPWM0 Group #0 Counter #08 trig=2 |
| 13 | PASS0_CH_RANGEVIO_TR_OUT[13] | TCPWM0_16M_ONE_CNT_TR_IN[9] | SAR0 ch#13, range violation to TCPWM0 Group #0 Counter #09 trig=2 |
| 14 | PASS0_CH_RANGEVIO_TR_OUT[14] | TCPWM0_16M_ONE_CNT_TR_IN[10] | SAR0 ch#14, range violation to TCPWM0 Group #0 Counter #10 trig=2 |
| 15 | PASS0_CH_RANGEVIO_TR_OUT[15] | TCPWM0_16M_ONE_CNT_TR_IN[11] | SAR0 ch#15, range violation to TCPWM0 Group #0 Counter #11 trig=2 |
| 16 | PASS0_CH_RANGEVIO_TR_OUT[16] | TCPWM0_16M_ONE_CNT_TR_IN[12] | SAR0 ch#16, range violation to TCPWM0 Group #0 Counter #12 trig=2 |
| 17 | PASS0_CH_RANGEVIO_TR_OUT[17] | TCPWM0_16M_ONE_CNT_TR_IN[13] | SAR0 ch#17, range violation to TCPWM0 Group #0 Counter #13 trig=2 |
| 18 | PASS0_CH_RANGEVIO_TR_OUT[18] | TCPWM0_16M_ONE_CNT_TR_IN[14] | SAR0 ch#18, range violation to TCPWM0 Group #0 Counter #14 trig=2 |
| 19 | PASS0_CH_RANGEVIO_TR_OUT[19] | TCPWM0_16M_ONE_CNT_TR_IN[15] | SAR0 ch#19, range violation to TCPWM0 Group #0 Counter #15 trig=2 |
| 20 | PASS0_CH_RANGEVIO_TR_OUT[20] | TCPWM0_16M_ONE_CNT_TR_IN[16] | SAR0 ch#20, range violation to TCPWM0 Group #0 Counter #16 trig=2 |
| 21 | PASS0_CH_RANGEVIO_TR_OUT[21] | TCPWM0_16M_ONE_CNT_TR_IN[17] | SAR0 ch#21, range violation to TCPWM0 Group #0 Counter #17 trig=2 |
| 22 | PASS0_CH_RANGEVIO_TR_OUT[22] | TCPWM0_16M_ONE_CNT_TR_IN[18] | SAR0 ch#22, range violation to TCPWM0 Group #0 Counter #18 trig=2 |
| 23 | PASS0_CH_RANGEVIO_TR_OUT[23] | TCPWM0_16M_ONE_CNT_TR_IN[19] | SAR0 ch#23, range violation to TCPWM0 Group #0 Counter #19 trig=2 |
| 24 | PASS0_CH_RANGEVIO_TR_OUT[32] | TCPWM0_16M_ONE_CNT_TR_IN[1] | SAR1 ch#0, range violation to TCPWM0 Group #1 Counter #01 trig=2 |

Note

33. Each logical channel of SAR ADC[x] can be connected to any of the SAR ADC[x]_y external pin. (x = 0, or 1, or 2 and y=0 to max 31)

Triggers one-to-one

Table 19-1 Triggers 1:1 (continued)

| Input | Trigger In | Trigger Out | Description |
|---|------------------------------|------------------------------|---|
| 25 | PASS0_CH_RANGEVIO_TR_OUT[33] | TCPWM0_16M_ONE_CNT_TR_IN[4] | SAR1 ch#1, range violation to TCPWM0 Group #1 Counter #04 trig=2 |
| 26 | PASS0_CH_RANGEVIO_TR_OUT[34] | TCPWM0_16M_ONE_CNT_TR_IN[7] | SAR1 ch#2, range violation to TCPWM0 Group #1 Counter #07 trig=2 |
| 27 | PASS0_CH_RANGEVIO_TR_OUT[35] | TCPWM0_16M_ONE_CNT_TR_IN[10] | SAR1 ch#3, range violation to TCPWM0 Group #1 Counter #10 trig=2 |
| 28 | PASS0_CH_RANGEVIO_TR_OUT[36] | TCPWM0_16M_ONE_CNT_TR_IN[20] | SAR1 ch#4, range violation to TCPWM0 Group #0 Counter #20 trig=2 |
| 29 | PASS0_CH_RANGEVIO_TR_OUT[37] | TCPWM0_16M_ONE_CNT_TR_IN[21] | SAR1 ch#5, range violation to TCPWM0 Group #0 Counter #21 trig=2 |
| 30 | PASS0_CH_RANGEVIO_TR_OUT[38] | TCPWM0_16M_ONE_CNT_TR_IN[22] | SAR1 ch#6, range violation to TCPWM0 Group #0 Counter #22 trig=2 |
| 31 | PASS0_CH_RANGEVIO_TR_OUT[39] | TCPWM0_16M_ONE_CNT_TR_IN[23] | SAR1 ch#7, range violation to TCPWM0 Group #0 Counter #23 trig=2 |
| 32 | PASS0_CH_RANGEVIO_TR_OUT[40] | TCPWM0_16M_ONE_CNT_TR_IN[24] | SAR1 ch#8, range violation to TCPWM0 Group #0 Counter #24 trig=2 |
| 33 | PASS0_CH_RANGEVIO_TR_OUT[41] | TCPWM0_16M_ONE_CNT_TR_IN[25] | SAR1 ch#9, range violation to TCPWM0 Group #0 Counter #25 trig=2 |
| 34 | PASS0_CH_RANGEVIO_TR_OUT[42] | TCPWM0_16M_ONE_CNT_TR_IN[26] | SAR1 ch#10, range violation to TCPWM0 Group #0 Counter #26 trig=2 |
| 35 | PASS0_CH_RANGEVIO_TR_OUT[43] | TCPWM0_16M_ONE_CNT_TR_IN[27] | SAR1 ch#11, range violation to TCPWM0 Group #0 Counter #27 trig=2 |
| 36 | PASS0_CH_RANGEVIO_TR_OUT[44] | TCPWM0_16M_ONE_CNT_TR_IN[28] | SAR1 ch#12, range violation to TCPWM0 Group #0 Counter #28 trig=2 |
| 37 | PASS0_CH_RANGEVIO_TR_OUT[45] | TCPWM0_16M_ONE_CNT_TR_IN[29] | SAR1 ch#13, range violation to TCPWM0 Group #0 Counter #29 trig=2 |
| 38 | PASS0_CH_RANGEVIO_TR_OUT[46] | TCPWM0_16M_ONE_CNT_TR_IN[30] | SAR1 ch#14, range violation to TCPWM0 Group #0 Counter #30 trig=2 |
| 39 | PASS0_CH_RANGEVIO_TR_OUT[47] | TCPWM0_16M_ONE_CNT_TR_IN[31] | SAR1 ch#15, range violation to TCPWM0 Group #0 Counter #31 trig=2 |
| 40 | PASS0_CH_RANGEVIO_TR_OUT[48] | TCPWM0_16M_ONE_CNT_TR_IN[32] | SAR1 ch#16, range violation to TCPWM0 Group #0 Counter #32 trig=2 |
| 41 | PASS0_CH_RANGEVIO_TR_OUT[49] | TCPWM0_16M_ONE_CNT_TR_IN[33] | SAR1 ch#17, range violation to TCPWM0 Group #0 Counter #33 trig=2 |
| 42 | PASS0_CH_RANGEVIO_TR_OUT[50] | TCPWM0_16M_ONE_CNT_TR_IN[34] | SAR1 ch#18, range violation to TCPWM0 Group #0 Counter #34 trig=2 |
| 43 | PASS0_CH_RANGEVIO_TR_OUT[51] | TCPWM0_16M_ONE_CNT_TR_IN[35] | SAR1 ch#19, range violation to TCPWM0 Group #0 Counter #35 trig=2 |
| 44 | PASS0_CH_RANGEVIO_TR_OUT[52] | TCPWM0_16M_ONE_CNT_TR_IN[36] | SAR1 ch#20, range violation to TCPWM0 Group #0 Counter #36 trig=2 |
| 45 | PASS0_CH_RANGEVIO_TR_OUT[53] | TCPWM0_16M_ONE_CNT_TR_IN[37] | SAR1 ch#21, range violation to TCPWM0 Group #0 Counter #37 trig=2 |
| 46 | PASS0_CH_RANGEVIO_TR_OUT[54] | TCPWM0_16M_ONE_CNT_TR_IN[38] | SAR1 ch#22, range violation to TCPWM0 Group #0 Counter #38 trig=2 |
| 47 | PASS0_CH_RANGEVIO_TR_OUT[55] | TCPWM0_16M_ONE_CNT_TR_IN[39] | SAR1 ch#23, range violation to TCPWM0 Group #0 Counter #39 trig=2 |
| 48 | PASS0_CH_RANGEVIO_TR_OUT[56] | TCPWM0_16M_ONE_CNT_TR_IN[40] | SAR1 ch#24, range violation to TCPWM0 Group #0 Counter #40 trig=2 |
| 49 | PASS0_CH_RANGEVIO_TR_OUT[57] | TCPWM0_16M_ONE_CNT_TR_IN[41] | SAR1 ch#25, range violation to TCPWM0 Group #0 Counter #41 trig=2 |
| 50 | PASS0_CH_RANGEVIO_TR_OUT[58] | TCPWM0_16M_ONE_CNT_TR_IN[42] | SAR1 ch#26, range violation to TCPWM0 Group #0 Counter #42 trig=2 |
| 51 | PASS0_CH_RANGEVIO_TR_OUT[59] | TCPWM0_16M_ONE_CNT_TR_IN[43] | SAR1 ch#27, range violation to TCPWM0 Group #0 Counter #43 trig=2 |
| 52 | PASS0_CH_RANGEVIO_TR_OUT[60] | TCPWM0_16M_ONE_CNT_TR_IN[44] | SAR1 ch#28, range violation to TCPWM0 Group #0 Counter #44 trig=2 |
| 53 | PASS0_CH_RANGEVIO_TR_OUT[61] | TCPWM0_16M_ONE_CNT_TR_IN[45] | SAR1 ch#29, range violation to TCPWM0 Group #0 Counter #45 trig=2 |
| 54 | PASS0_CH_RANGEVIO_TR_OUT[62] | TCPWM0_16M_ONE_CNT_TR_IN[46] | SAR1 ch#30, range violation to TCPWM0 Group #0 Counter #46 trig=2 |
| 55 | PASS0_CH_RANGEVIO_TR_OUT[63] | TCPWM0_16M_ONE_CNT_TR_IN[47] | SAR1 ch#31, range violation to TCPWM0 Group #0 Counter #47 trig=2 |
| 56 | PASS0_CH_RANGEVIO_TR_OUT[64] | TCPWM0_16M_ONE_CNT_TR_IN[2] | SAR2 ch#0, range violation to TCPWM0 Group #1 Counter #02 trig=2 |
| 57 | PASS0_CH_RANGEVIO_TR_OUT[65] | TCPWM0_16M_ONE_CNT_TR_IN[5] | SAR2 ch#1, range violation to TCPWM0 Group #1 Counter #05 trig=2 |
| 58 | PASS0_CH_RANGEVIO_TR_OUT[66] | TCPWM0_16M_ONE_CNT_TR_IN[8] | SAR2 ch#2, range violation to TCPWM0 Group #1 Counter #08 trig=2 |
| 59 | PASS0_CH_RANGEVIO_TR_OUT[67] | TCPWM0_16M_ONE_CNT_TR_IN[11] | SAR2 ch#3, range violation to TCPWM0 Group #1 Counter #11 trig=2 |
| 60 | PASS0_CH_RANGEVIO_TR_OUT[68] | TCPWM0_16M_ONE_CNT_TR_IN[48] | SAR2 ch#4, range violation to TCPWM0 Group #0 Counter #48 trig=2 |
| 61 | PASS0_CH_RANGEVIO_TR_OUT[69] | TCPWM0_16M_ONE_CNT_TR_IN[49] | SAR2 ch#5, range violation to TCPWM0 Group #0 Counter #49 trig=2 |
| 62 | PASS0_CH_RANGEVIO_TR_OUT[70] | TCPWM0_16M_ONE_CNT_TR_IN[50] | SAR2 ch#6, range violation to TCPWM0 Group #0 Counter #50 trig=2 |
| 63 | PASS0_CH_RANGEVIO_TR_OUT[71] | TCPWM0_16M_ONE_CNT_TR_IN[51] | SAR2 ch#7, range violation to TCPWM0 Group #0 Counter #51 trig=2 |
| MUX Group 4: CAN0 to P-DMA0 Triggers | | | |
| 0 | CAN0_DBG_TR_OUT[0] | PDMA0_TR_IN[16] | CAN0, Channel #0 P-DMA0 trigger |
| 1 | CAN0_FIFO0_TR_OUT[0] | PDMA0_TR_IN[17] | CAN0, Channel #0 FIFO0 trigger |
| 2 | CAN0_FIFO1_TR_OUT[0] | PDMA0_TR_IN[18] | CAN0, Channel #0 FIFO1 trigger |
| 3 | CAN0_DBG_TR_OUT[1] | PDMA0_TR_IN[19] | CAN0, Channel #1 P-DMA0 trigger |
| 4 | CAN0_FIFO0_TR_OUT[1] | PDMA0_TR_IN[20] | CAN0, Channel #1 FIFO0 trigger |
| 5 | CAN0_FIFO1_TR_OUT[1] | PDMA0_TR_IN[21] | CAN0, Channel #1 FIFO1 trigger |
| 6 | CAN0_DBG_TR_OUT[2] | PDMA0_TR_IN[22] | CAN0, Channel #2 P-DMA0 trigger |
| 7 | CAN0_FIFO0_TR_OUT[2] | PDMA0_TR_IN[23] | CAN0, Channel #2 FIFO0 trigger |
| 8 | CAN0_FIFO1_TR_OUT[2] | PDMA0_TR_IN[24] | CAN0, Channel #2 FIFO1 trigger |
| MUX Group 5: CAN1 to P-DMA1 triggers | | | |
| 0 | CAN1_DBG_TR_OUT[0] | PDMA1_TR_IN[24] | CAN1, Channel #0 P-DMA01 trigger |
| 1 | CAN1_FIFO0_TR_OUT[0] | PDMA1_TR_IN[25] | CAN1, Channel #0 FIFO0 trigger |
| 2 | CAN1_FIFO1_TR_OUT[0] | PDMA1_TR_IN[26] | CAN1, Channel #0 FIFO1 trigger |
| 3 | CAN1_DBG_TR_OUT[1] | PDMA1_TR_IN[27] | CAN1, Channel #1 P-DMA1 trigger |
| 4 | CAN1_FIFO0_TR_OUT[1] | PDMA1_TR_IN[28] | CAN1, Channel #1 FIFO0 trigger |

Triggers one-to-one

Table 19-1 Triggers 1:1 (continued)

| Input | Trigger In | Trigger Out | Description |
|--|----------------------|--------------------|-------------------------------------|
| 5 | CAN1_FIFO1_TR_OUT[1] | PDMA1_TR_IN[29] | CAN1, Channel #1 FIFO1 trigger |
| 6 | CAN1_DBG_TR_OUT[2] | PDMA1_TR_IN[30] | CAN1, Channel #2 P-DMA1 trigger |
| 7 | CAN1_FIFO0_TR_OUT[2] | PDMA1_TR_IN[31] | CAN1, Channel #2 FIFO0 trigger |
| 8 | CAN1_FIFO1_TR_OUT[2] | PDMA1_TR_IN[32] | CAN1, Channel #2 FIFO1 trigger |
| MUX Group 6: Acknowledge triggers from P-DMA0 to CAN0 | | | |
| 0 | PDMA0_TR_OUT[16] | CAN0_DBG_TR_ACK[0] | CAN0, Channel #0 P-DMA0 acknowledge |
| 1 | PDMA0_TR_OUT[19] | CAN0_DBG_TR_ACK[1] | CAN0, Channel #1 P-DMA0 acknowledge |
| 2 | PDMA0_TR_OUT[22] | CAN0_DBG_TR_ACK[2] | CAN0, Channel #2 P-DMA0 acknowledge |
| MUX Group 7: Acknowledge triggers from P-DMA1 to CAN1 | | | |
| 0 | PDMA1_TR_OUT[24] | CAN1_DBG_TR_ACK[0] | CAN1, Channel #0 P-DMA1 acknowledge |
| 1 | PDMA1_TR_OUT[27] | CAN1_DBG_TR_ACK[1] | CAN1, Channel #1 P-DMA1 acknowledge |
| 2 | PDMA1_TR_OUT[30] | CAN1_DBG_TR_ACK[2] | CAN1, Channel #2 P-DMA1 acknowledge |
| MUX Group 8: SCBx to P-DMA1 Triggers | | | |
| 0 | SCB0_TX_TR_OUT | PDMA1_TR_IN[8] | SCB0 TX to P-DMA1 Trigger |
| 1 | SCB0_RX_TR_OUT | PDMA1_TR_IN[9] | SCB0 RX to P-DMA1 Trigger |
| 2 | SCB1_TX_TR_OUT | PDMA1_TR_IN[10] | SCB1 TX to P-DMA1 Trigger |
| 3 | SCB1_RX_TR_OUT | PDMA1_TR_IN[11] | SCB1 RX to P-DMA1 Trigger |
| 4 | SCB2_TX_TR_OUT | PDMA1_TR_IN[12] | SCB2 TX to P-DMA1 Trigger |
| 5 | SCB2_RX_TR_OUT | PDMA1_TR_IN[13] | SCB2 RX to P-DMA1 Trigger |
| 6 | SCB3_TX_TR_OUT | PDMA1_TR_IN[14] | SCB3 TX to P-DMA1 Trigger |
| 7 | SCB3_RX_TR_OUT | PDMA1_TR_IN[15] | SCB3 RX to P-DMA1 Trigger |
| 8 | SCB4_TX_TR_OUT | PDMA1_TR_IN[16] | SCB4 TX to P-DMA1 Trigger |
| 9 | SCB4_RX_TR_OUT | PDMA1_TR_IN[17] | SCB4 RX to P-DMA1 Trigger |
| 10 | SCB5_TX_TR_OUT | PDMA1_TR_IN[18] | SCB5 TX to P-DMA1 Trigger |
| 11 | SCB5_RX_TR_OUT | PDMA1_TR_IN[19] | SCB5 RX to P-DMA1 Trigger |
| 12 | SCB6_TX_TR_OUT | PDMA1_TR_IN[20] | SCB6 TX to P-DMA1 Trigger |
| 13 | SCB6_RX_TR_OUT | PDMA1_TR_IN[21] | SCB6 RX to P-DMA1 Trigger |
| 14 | SCB7_TX_TR_OUT | PDMA1_TR_IN[22] | SCB7 TX to P-DMA1 Trigger |
| 15 | SCB7_RX_TR_OUT | PDMA1_TR_IN[23] | SCB7 RX to P-DMA1 Trigger |

20 Peripheral clocks

Table 20-1 Peripheral clock assignments

| Output | Destination | Description |
|--------|---------------------------|-----------------------------|
| 0 | PCLK_CPUSS_CLOCK_TRACE_IN | Trace clock |
| 1 | PCLK_SMARTIO12_CLOCK | SMART I/O #12 |
| 2 | PCLK_SMARTIO13_CLOCK | SMART I/O #13 |
| 3 | PCLK_SMARTIO14_CLOCK | SMART I/O #14 |
| 4 | PCLK_SMARTIO15_CLOCK | SMART I/O #15 |
| 5 | PCLK_SMARTIO16_CLOCK | SMART I/O #16 |
| 6 | PCLK_CANFD0_CLOCK_CAN0 | CAN0, Channel #0 |
| 7 | PCLK_CANFD0_CLOCK_CAN1 | CAN0, Channel #1 |
| 8 | PCLK_CANFD0_CLOCK_CAN2 | CAN0, Channel #2 |
| 9 | PCLK_CANFD1_CLOCK_CAN0 | CAN1, Channel #0 |
| 10 | PCLK_CANFD1_CLOCK_CAN1 | CAN1, Channel #1 |
| 11 | PCLK_CANFD1_CLOCK_CAN2 | CAN1, Channel #2 |
| 12 | PCLK_LIN0_CLOCK_CH_EN0 | LIN0, Channel #0 |
| 13 | PCLK_LIN0_CLOCK_CH_EN1 | LIN0, Channel #1 |
| 14 | PCLK_LIN0_CLOCK_CH_EN2 | LIN0, Channel #2 |
| 15 | PCLK_LIN0_CLOCK_CH_EN3 | LIN0, Channel #3 |
| 16 | PCLK_LIN0_CLOCK_CH_EN4 | LIN0, Channel #4 |
| 17 | PCLK_LIN0_CLOCK_CH_EN5 | LIN0, Channel #5 |
| 18 | PCLK_LIN0_CLOCK_CH_EN6 | LIN0, Channel #6 |
| 19 | PCLK_LIN0_CLOCK_CH_EN7 | LIN0, Channel #7 |
| 20 | PCLK_SCB0_CLOCK | SCB0 |
| 21 | PCLK_SCB1_CLOCK | SCB1 |
| 22 | PCLK_SCB2_CLOCK | SCB2 |
| 23 | PCLK_SCB3_CLOCK | SCB3 |
| 24 | PCLK_SCB4_CLOCK | SCB4 |
| 25 | PCLK_SCB5_CLOCK | SCB5 |
| 26 | PCLK_SCB6_CLOCK | SCB6 |
| 27 | PCLK_SCB7_CLOCK | SCB7 |
| 28 | PCLK_PASS0_CLOCK_SAR0 | SAR0 |
| 29 | PCLK_PASS0_CLOCK_SAR1 | SAR1 |
| 30 | PCLK_PASS0_CLOCK_SAR2 | SAR2 |
| 31 | PCLK_TCPWM0_CLOCKS0 | TCPWM0 Group #0, Counter #0 |
| 32 | PCLK_TCPWM0_CLOCKS1 | TCPWM0 Group #0, Counter #1 |
| 33 | PCLK_TCPWM0_CLOCKS2 | TCPWM0 Group #0, Counter #2 |
| 34 | PCLK_TCPWM0_CLOCKS3 | TCPWM0 Group #0, Counter #3 |
| 35 | PCLK_TCPWM0_CLOCKS4 | TCPWM0 Group #0, Counter #4 |
| 36 | PCLK_TCPWM0_CLOCKS5 | TCPWM0 Group #0, Counter #5 |
| 37 | PCLK_TCPWM0_CLOCKS6 | TCPWM0 Group #0, Counter #6 |
| 38 | PCLK_TCPWM0_CLOCKS7 | TCPWM0 Group #0, Counter #7 |

Table 20-1 Peripheral clock assignments (continued)

| Output | Destination | Description |
|--------|----------------------|------------------------------|
| 39 | PCLK_TCPWM0_CLOCKS8 | TCPWM0 Group #0, Counter #8 |
| 40 | PCLK_TCPWM0_CLOCKS9 | TCPWM0 Group #0, Counter #9 |
| 41 | PCLK_TCPWM0_CLOCKS10 | TCPWM0 Group #0, Counter #10 |
| 42 | PCLK_TCPWM0_CLOCKS11 | TCPWM0 Group #0, Counter #11 |
| 43 | PCLK_TCPWM0_CLOCKS12 | TCPWM0 Group #0, Counter #12 |
| 44 | PCLK_TCPWM0_CLOCKS13 | TCPWM0 Group #0, Counter #13 |
| 45 | PCLK_TCPWM0_CLOCKS14 | TCPWM0 Group #0, Counter #14 |
| 46 | PCLK_TCPWM0_CLOCKS15 | TCPWM0 Group #0, Counter #15 |
| 47 | PCLK_TCPWM0_CLOCKS16 | TCPWM0 Group #0, Counter #16 |
| 48 | PCLK_TCPWM0_CLOCKS17 | TCPWM0 Group #0, Counter #17 |
| 49 | PCLK_TCPWM0_CLOCKS18 | TCPWM0 Group #0, Counter #18 |
| 50 | PCLK_TCPWM0_CLOCKS19 | TCPWM0 Group #0, Counter #19 |
| 51 | PCLK_TCPWM0_CLOCKS20 | TCPWM0 Group #0, Counter #20 |
| 52 | PCLK_TCPWM0_CLOCKS21 | TCPWM0 Group #0, Counter #21 |
| 53 | PCLK_TCPWM0_CLOCKS22 | TCPWM0 Group #0, Counter #22 |
| 54 | PCLK_TCPWM0_CLOCKS23 | TCPWM0 Group #0, Counter #23 |
| 55 | PCLK_TCPWM0_CLOCKS24 | TCPWM0 Group #0, Counter #24 |
| 56 | PCLK_TCPWM0_CLOCKS25 | TCPWM0 Group #0, Counter #25 |
| 57 | PCLK_TCPWM0_CLOCKS26 | TCPWM0 Group #0, Counter #26 |
| 58 | PCLK_TCPWM0_CLOCKS27 | TCPWM0 Group #0, Counter #27 |
| 59 | PCLK_TCPWM0_CLOCKS28 | TCPWM0 Group #0, Counter #28 |
| 60 | PCLK_TCPWM0_CLOCKS29 | TCPWM0 Group #0, Counter #29 |
| 61 | PCLK_TCPWM0_CLOCKS30 | TCPWM0 Group #0, Counter #30 |
| 62 | PCLK_TCPWM0_CLOCKS31 | TCPWM0 Group #0, Counter #31 |
| 63 | PCLK_TCPWM0_CLOCKS32 | TCPWM0 Group #0, Counter #32 |
| 64 | PCLK_TCPWM0_CLOCKS33 | TCPWM0 Group #0, Counter #33 |
| 65 | PCLK_TCPWM0_CLOCKS34 | TCPWM0 Group #0, Counter #34 |
| 66 | PCLK_TCPWM0_CLOCKS35 | TCPWM0 Group #0, Counter #35 |
| 67 | PCLK_TCPWM0_CLOCKS36 | TCPWM0 Group #0, Counter #36 |
| 68 | PCLK_TCPWM0_CLOCKS37 | TCPWM0 Group #0, Counter #37 |
| 69 | PCLK_TCPWM0_CLOCKS38 | TCPWM0 Group #0, Counter #38 |
| 70 | PCLK_TCPWM0_CLOCKS39 | TCPWM0 Group #0, Counter #39 |
| 71 | PCLK_TCPWM0_CLOCKS40 | TCPWM0 Group #0, Counter #40 |
| 72 | PCLK_TCPWM0_CLOCKS41 | TCPWM0 Group #0, Counter #41 |
| 73 | PCLK_TCPWM0_CLOCKS42 | TCPWM0 Group #0, Counter #42 |
| 74 | PCLK_TCPWM0_CLOCKS43 | TCPWM0 Group #0, Counter #43 |
| 75 | PCLK_TCPWM0_CLOCKS44 | TCPWM0 Group #0, Counter #44 |
| 76 | PCLK_TCPWM0_CLOCKS45 | TCPWM0 Group #0, Counter #45 |
| 77 | PCLK_TCPWM0_CLOCKS46 | TCPWM0 Group #0, Counter #46 |
| 78 | PCLK_TCPWM0_CLOCKS47 | TCPWM0 Group #0, Counter #47 |
| 79 | PCLK_TCPWM0_CLOCKS48 | TCPWM0 Group #0, Counter #48 |

Table 20-1 **Peripheral clock assignments** *(continued)*

| Output | Destination | Description |
|--------|-----------------------|------------------------------|
| 80 | PCLK_TCPWM0_CLOCKS49 | TCPWM0 Group #0, Counter #49 |
| 81 | PCLK_TCPWM0_CLOCKS50 | TCPWM0 Group #0, Counter #50 |
| 82 | PCLK_TCPWM0_CLOCKS51 | TCPWM0 Group #0, Counter #51 |
| 83 | PCLK_TCPWM0_CLOCKS52 | TCPWM0 Group #0, Counter #52 |
| 84 | PCLK_TCPWM0_CLOCKS53 | TCPWM0 Group #0, Counter #53 |
| 85 | PCLK_TCPWM0_CLOCKS54 | TCPWM0 Group #0, Counter #54 |
| 86 | PCLK_TCPWM0_CLOCKS55 | TCPWM0 Group #0, Counter #55 |
| 87 | PCLK_TCPWM0_CLOCKS56 | TCPWM0 Group #0, Counter #56 |
| 88 | PCLK_TCPWM0_CLOCKS57 | TCPWM0 Group #0, Counter #57 |
| 89 | PCLK_TCPWM0_CLOCKS58 | TCPWM0 Group #0, Counter #58 |
| 90 | PCLK_TCPWM0_CLOCKS59 | TCPWM0 Group #0, Counter #59 |
| 91 | PCLK_TCPWM0_CLOCKS60 | TCPWM0 Group #0, Counter #60 |
| 92 | PCLK_TCPWM0_CLOCKS61 | TCPWM0 Group #0, Counter #61 |
| 93 | PCLK_TCPWM0_CLOCKS62 | TCPWM0 Group #0, Counter #62 |
| 94 | PCLK_TCPWM0_CLOCKS256 | TCPWM0 Group #1, Counter #0 |
| 95 | PCLK_TCPWM0_CLOCKS257 | TCPWM0 Group #1, Counter #1 |
| 96 | PCLK_TCPWM0_CLOCKS258 | TCPWM0 Group #1, Counter #2 |
| 97 | PCLK_TCPWM0_CLOCKS259 | TCPWM0 Group #1, Counter #3 |
| 98 | PCLK_TCPWM0_CLOCKS260 | TCPWM0 Group #1, Counter #4 |
| 99 | PCLK_TCPWM0_CLOCKS261 | TCPWM0 Group #1, Counter #5 |
| 100 | PCLK_TCPWM0_CLOCKS262 | TCPWM0 Group #1, Counter #6 |
| 101 | PCLK_TCPWM0_CLOCKS263 | TCPWM0 Group #1, Counter #7 |
| 102 | PCLK_TCPWM0_CLOCKS264 | TCPWM0 Group #1, Counter #8 |
| 103 | PCLK_TCPWM0_CLOCKS265 | TCPWM0 Group #1, Counter #9 |
| 104 | PCLK_TCPWM0_CLOCKS266 | TCPWM0 Group #1, Counter #10 |
| 105 | PCLK_TCPWM0_CLOCKS267 | TCPWM0 Group #1, Counter #11 |
| 106 | PCLK_TCPWM0_CLOCKS512 | TCPWM0 Group #2, Counter #0 |
| 107 | PCLK_TCPWM0_CLOCKS513 | TCPWM0 Group #2, Counter #1 |
| 108 | PCLK_TCPWM0_CLOCKS514 | TCPWM0 Group #2, Counter #2 |
| 109 | PCLK_TCPWM0_CLOCKS515 | TCPWM0 Group #2, Counter #3 |

21 Faults

Table 21-1 Fault Assignments

| Fault | Source | Description |
|-------|------------------|---|
| 0 | CPUSS_MPU_VIO_0 | CM0+ S MPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': S MPU violation. |
| 1 | CPUSS_MPU_VIO_1 | Crypto S MPU violation. See CPUSS_MPU_VIO_0 description. |
| 2 | CPUSS_MPU_VIO_2 | P-DMA0 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description. |
| 3 | CPUSS_MPU_VIO_3 | P-DMA1 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description. |
| 4 | CPUSS_MPU_VIO_4 | M-DMA0 MPU/S MPU violation. See CPUSS_MPU_VIO_0 description. |
| 15 | CPUSS_MPU_VIO_15 | Test Controller MPU/S MPU violation. See CPUSS_MPU_VIO_0 description. |
| 16 | CPUSS_MPU_VIO_16 | CM4 system bus AHB-Lite interface MPU violation. See CPUSS_MPU_VIO_0 description. |
| 17 | CPUSS_MPU_VIO_17 | CM4 code bus AHB-Lite interface MPU violation for non flash controller accesses. See CPUSS_MPU_VIO_0 description. |
| 18 | CPUSS_MPU_VIO_18 | CM4 code bus AHB-Lite interface MPU violation for flash controller accesses. See CPUSS_MPU_VIO_0 description. |
| 26 | PERI_PERI_C_ECC | Peripheral protection SRAM correctable ECC violation DATA0[10:0]: Violating address. DATA1[7:0]: Syndrome of SRAM word. |
| 27 | PERI_PERI_NC_ECC | Peripheral protection SRAM non-correctable ECC violation |
| 28 | PERI_MS_VIO_0 | CM0+ Peripheral Master Interface PPU violation DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": master interface, PPU violation, "1": timeout detected, "2": bus error, other: undefined. |
| 29 | PERI_MS_VIO_1 | CM4 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description. |
| 30 | PERI_MS_VIO_2 | P-DMA0 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description. |
| 31 | PERI_MS_VIO_3 | P-DMA1 Peripheral Master Interface PPU violation. See PERI_MS_VIO_0 description. |
| 32 | PERI_GROUP_VIO_0 | Peripheral Group #0 violation. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31:28]: "0": decoder or peripheral bus error, other: undefined. |
| 33 | PERI_GROUP_VIO_1 | Peripheral Group #1 violation. See PERI_GROUP_VIO_0 description. |
| 34 | PERI_GROUP_VIO_2 | Peripheral Group #2 violation. See PERI_GROUP_VIO_0 description. |
| 35 | PERI_GROUP_VIO_3 | Peripheral Group #3 violation. See PERI_GROUP_VIO_0 description. |
| 37 | PERI_GROUP_VIO_5 | Peripheral Group #5 violation. See PERI_GROUP_VIO_0 description. |
| 38 | PERI_GROUP_VIO_6 | Peripheral Group #6 violation. See PERI_GROUP_VIO_0 description. |
| 41 | PERI_GROUP_VIO_9 | Peripheral Group #9 violation. See PERI_GROUP_VIO_0 description. |

Faults

Table 21-1 Fault Assignments (continued)

| Fault | Source | Description |
|-------|-----------------------------|--|
| 48 | CPUSS_FLASHC_MAIN_BUS_ERROR | Flash controller main flash bus error FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. FAULT_DATA1[11:8]: Master identifier. |
| 49 | CPUSS_FLASHC_MAIN_C_ECC | Flash controller main flash correctable ECC violation DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00). DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08). DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10). DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18). |
| 50 | CPUSS_FLASHC_MAIN_NC_ECC | Flash controller main flash non-correctable ECC violation. See CPUSS_FLASHC_MAIN_C_ECC description. |
| 51 | CPUSS_FLASHC_WORK_BUS_ERROR | Flash controller work-flash bus error. See CPUSS_FLASHC_MAIN_BUS_ERR description. |
| 52 | CPUSS_FLASHC_WORK_C_ECC | Flash controller work flash correctable ECC violation. DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address. DATA1[6:0]: Syndrome of 32-bit word. |
| 53 | CPUSS_FLASHC_WORK_NC_ECC | Flash controller work-flash non-correctable ECC violation. See CPUSS_FLASHC_WORK_C_ECC description. |
| 54 | CPUSS_FLASHC_CM0_CA_C_ECC | Flash controller CM0+ cache correctable ECC violation. DATA0[26:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0). DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4). DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8). DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc). |
| 55 | CPUSS_FLASHC_CM0_CA_NC_ECC | Flash controller CM0+ cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description. |
| 56 | CPUSS_FLASHC_CM4_CA_C_ECC | Flash controller CM4 cache correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description. |
| 57 | CPUSS_FLASHC_CM4_CA_NC_ECC | Flash controller CM4 cache non-correctable ECC violation. See CPUSS_FLASHC_CM0_CA_C_ECC description. |
| 58 | CPUSS_RAMC0_C_ECC | System memory controller 0 correctable ECC violation: DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of 32-bit SRAM code word. |
| 59 | CPUSS_RAMC0_NC_ECC | System memory controller 0 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description. |
| 60 | CPUSS_RAMC1_C_ECC | System memory controller 1 correctable ECC violation. See CPUSS_RAMC0_C_ECC description. |
| 61 | CPUSS_RAMC1_NC_ECC | System memory controller 1 non-correctable ECC violation. See CPUSS_RAMC0_C_ECC description. |
| 64 | CPUSS_CRYPT0_C_ECC | Crypto memory correctable ECC violation. DATA0[31:0]: Violating address. DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM. DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM. |
| 65 | CPUSS_CRYPT0_NC_ECC | Crypto memory non-correctable ECC violation. See CPUSS_CRYPT0_C_ECC description. |
| 70 | CPUSS_DW0_C_ECC | P-DMA0 memory correctable ECC violation: DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable). DATA1[6:0]: Syndrome of 32-bit SRAM code word. |
| 71 | CPUSS_DW0_NC_ECC | P-DMA0 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description. |
| 72 | CPUSS_DW1_C_ECC | P-DMA1 memory correctable ECC violation. See CPUSS_DW0_C_ECC description. |
| 73 | CPUSS_DW1_NC_ECC | P-DMA1 memory non-correctable ECC violation. See CPUSS_DW0_C_ECC description. |
| 74 | CPUSS_FM_SRAM_C_ECC | Flash code storage SRAM memory correctable ECC violation: DATA0[15:0]: Address location in the eCT Flash SRAM. DATA1[6:0]: Syndrome of 32-bit SRAM word. |
| 75 | CPUSS_FM_SRAM_NC_ECC | Flash code storage SRAM memory non-correctable ECC violation: See CPUSS_FM_SRAMC_C_ECC description. |
| 80 | CANFD_0_CAN_C_ECC | CAN0 message buffer correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM. DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA1[31:0]: ECC violating data[31:0] from MRAM. |

Table 21-1 Fault Assignments (continued)

| Fault | Source | Description |
|-------|--------------------|--|
| 81 | CANFD_0_CAN_NC_ECC | CAN0 message buffer non-correctable ECC violation: DATA0[15:0]: Violating address. DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error). DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F DATA0[30]: Write access, only possible for Address Error DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error). |
| 82 | CANFD_1_CAN_C_ECC | CAN1 message buffer correctable ECC violation. See CANFD_0_CAN_C_ECC description. |
| 83 | CANFD_1_CAN_NC_ECC | CAN1 message buffer non-correctable ECC violation. See CANFD_0_CAN_NC_ECC description. |
| 90 | SRSS_FAULT_CSV | Consolidated fault output for clock supervisors. Multiple CSV can detect a violation at the same time. DATA0[15:0]: CLK_HF* root CSV violation flags. DATA0[24]: CLK_REF CSV violation flag (reference clock for CLK_HF CSVs) DATA0[25]: CLK_LF CSV violation flag DATA0[26]: CLK_HVILO CSV violation flag |
| 91 | SRSS_FAULT_SSV | Consolidated fault output for supply supervisors. Multiple CSV can detect a violation at the same time. DATA0[0]: BOD on VDDA DATA[1]: OVD on VDDA DATA[16]: LVD/HVD #1 DATA0[17]: LVD/HVD #2 |
| 92 | SRSS_FAULT_MCWDT0 | Fault output for MCWDT0 (all sub-counters) Multiple counters can detect a violation at the same time. DATA0[0]: MCWDT sub counter 0 LOWER_LIMIT DATA0[1]: MCWDT sub counter 0 UPPER_LIMIT DATA0[2]: MCWDT sub counter 1 LOWER_LIMIT DATA0[3]: MCWDT sub counter 1 UPPER_LIMIT |
| 93 | SRSS_FAULT_MCWDT1 | Fault output for MCWDT1 (all sub-counters). See SRSS_FAULT_MCWDT0 description. |

22 Peripheral Protection Unit Fixed Structure Pairs

Protection pair is a pair PPU structures, a master and a slave structure. The master structure protects the slave structure, and the slave structure protects resources such as peripheral registers, or the peripheral itself.

Table 22-1 PPU Fixed Structure Pairs

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|---|------------|------------|----------------------------------|
| 0 | PERI_MS_PPU_FX_PERI_MAIN | 0x40000000 | 0x00002000 | Peripheral Interconnect main |
| 1 | PERI_MS_PPU_FX_PERI_SECURE | 0x40002000 | 0x00000004 | Peripheral interconnect secure |
| 2 | PERI_MS_PPU_FX_PERI_GRP0_GROUP | 0x40004010 | 0x00000004 | Peripheral Group #0 main |
| 3 | PERI_MS_PPU_FX_PERI_GRP1_GROUP | 0x40004030 | 0x00000004 | Peripheral Group #1 main |
| 4 | PERI_MS_PPU_FX_PERI_GRP2_GROUP | 0x40004050 | 0x00000004 | Peripheral Group #2 main |
| 5 | PERI_MS_PPU_FX_PERI_GRP3_GROUP | 0x40004060 | 0x00000020 | Peripheral Group #3 main |
| 6 | PERI_MS_PPU_FX_PERI_GRP5_GROUP | 0x400040A0 | 0x00000020 | Peripheral Group #5 main |
| 7 | PERI_MS_PPU_FX_PERI_GRP6_GROUP | 0x400040C0 | 0x00000020 | Peripheral Group #6 main |
| 8 | PERI_MS_PPU_FX_PERI_GRP9_GROUP | 0x40004120 | 0x00000020 | Peripheral Group #9 main |
| 9 | PERI_MS_PPU_FX_PERI_TR | 0x40008000 | 0x00008000 | Peripheral trigger multiplexer |
| 10 | PERI_MS_PPU_FX_CRYPT0_MAIN | 0x40100000 | 0x00000400 | Crypto main |
| 11 | PERI_MS_PPU_FX_CRYPT0_CRYPT0 | 0x40101000 | 0x00000800 | Crypto MMIO (Memory Mapped I/O) |
| 12 | PERI_MS_PPU_FX_CRYPT0_BOOT | 0x40102000 | 0x00000100 | Crypto boot |
| 13 | PERI_MS_PPU_FX_CRYPT0_KEY0 | 0x40102100 | 0x00000004 | Crypto Key #0 |
| 14 | PERI_MS_PPU_FX_CRYPT0_KEY1 | 0x40102120 | 0x00000004 | Crypto Key #1 |
| 15 | PERI_MS_PPU_FX_CRYPT0_BUF | 0x40108000 | 0x00002000 | Crypto buffer |
| 16 | PERI_MS_PPU_FX_CPUS0_CM4 | 0x40200000 | 0x00000400 | CM4 CPU core |
| 17 | PERI_MS_PPU_FX_CPUS0_CM0 | 0x40201000 | 0x00001000 | CM0+ CPU core |
| 18 | PERI_MS_PPU_FX_CPUS0_BOOT ^[34] | 0x40202000 | 0x00000200 | CPUS0 boot |
| 19 | PERI_MS_PPU_FX_CPUS0_CM0_INTR | 0x40208000 | 0x00000800 | CPUS0 CM0+ interrupts |
| 20 | PERI_MS_PPU_FX_CPUS0_CM4_INTR | 0x4020A000 | 0x00000800 | CPUS0 CM4 interrupts |
| 21 | PERI_MS_PPU_FX_FAULT_STRUCT0_MAIN | 0x40210000 | 0x00000100 | CPUS0 Fault Structure #0 main |
| 22 | PERI_MS_PPU_FX_FAULT_STRUCT1_MAIN | 0x40210100 | 0x00000100 | CPUS0 Fault Structure #1 main |
| 23 | PERI_MS_PPU_FX_FAULT_STRUCT2_MAIN | 0x40210200 | 0x00000100 | CPUS0 Fault Structure #2 main |
| 24 | PERI_MS_PPU_FX_FAULT_STRUCT3_MAIN | 0x40210300 | 0x00000100 | CPUS0 Fault Structure #3 main |
| 25 | PERI_MS_PPU_FX_IPC_STRUCT0_IPC | 0x40220000 | 0x00000020 | CPUS0 IPC Structure #0 |
| 26 | PERI_MS_PPU_FX_IPC_STRUCT1_IPC | 0x40220020 | 0x00000020 | CPUS0 IPC Structure #1 |
| 27 | PERI_MS_PPU_FX_IPC_STRUCT2_IPC | 0x40220040 | 0x00000020 | CPUS0 IPC Structure #2 |
| 28 | PERI_MS_PPU_FX_IPC_STRUCT3_IPC | 0x40220060 | 0x00000020 | CPUS0 IPC Structure #3 |
| 29 | PERI_MS_PPU_FX_IPC_STRUCT4_IPC | 0x40220080 | 0x00000020 | CPUS0 IPC Structure #4 |
| 30 | PERI_MS_PPU_FX_IPC_STRUCT5_IPC | 0x402200A0 | 0x00000020 | CPUS0 IPC Structure #5 |
| 31 | PERI_MS_PPU_FX_IPC_STRUCT6_IPC | 0x402200C0 | 0x00000020 | CPUS0 IPC Structure #6 |
| 32 | PERI_MS_PPU_FX_IPC_STRUCT7_IPC | 0x402200E0 | 0x00000020 | CPUS0 IPC Structure #7 |
| 33 | PERI_MS_PPU_FX_IPC_INTR_STRUCT0_INTR | 0x40221000 | 0x00000010 | CPUS0 IPC Interrupt Structure #0 |
| 34 | PERI_MS_PPU_FX_IPC_INTR_STRUCT1_INTR | 0x40221020 | 0x00000010 | CPUS0 IPC Interrupt Structure #1 |
| 35 | PERI_MS_PPU_FX_IPC_INTR_STRUCT2_INTR | 0x40221040 | 0x00000010 | CPUS0 IPC Interrupt Structure #2 |
| 36 | PERI_MS_PPU_FX_IPC_INTR_STRUCT3_INTR | 0x40221060 | 0x00000010 | CPUS0 IPC Interrupt Structure #3 |
| 37 | PERI_MS_PPU_FX_IPC_INTR_STRUCT4_INTR | 0x40221080 | 0x00000010 | CPUS0 IPC Interrupt Structure #4 |
| 38 | PERI_MS_PPU_FX_IPC_INTR_STRUCT5_INTR | 0x402210A0 | 0x00000010 | CPUS0 IPC Interrupt Structure #5 |

Note

34.Fixed PPU is configured inside the Boot and user is not allowed to change the attributes of this PPU.

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|---|------------|------------|------------------------------------|
| 39 | PERI_MS_PPU_FX_IPC_INTR_STRUCT6_INTR | 0x402210C0 | 0x00000010 | CPUSS IPC Interrupt Structure #6 |
| 40 | PERI_MS_PPU_FX_IPC_INTR_STRUCT7_INTR | 0x402210E0 | 0x00000010 | CPUSS IPC Interrupt Structure #7 |
| 41 | PERI_MS_PPU_FX_PROT_SMPU_MAIN | 0x40230000 | 0x00000040 | Peripheral protection SMPU main |
| 42 | PERI_MS_PPU_FX_PROT_MPU0_MAIN | 0x40234000 | 0x00000004 | Peripheral protection MPU #0 main |
| 43 | PERI_MS_PPU_FX_PROT_MPU14_MAIN | 0x40237800 | 0x00000004 | Peripheral protection MPU #14 main |
| 44 | PERI_MS_PPU_FX_PROT_MPU15_MAIN | 0x40237C00 | 0x00000400 | Peripheral protection MPU #15 main |
| 45 | PERI_MS_PPU_FX_FLASHC_MAIN | 0x40240000 | 0x00000008 | Flash controller main |
| 46 | PERI_MS_PPU_FX_FLASHC_CMD | 0x40240008 | 0x00000004 | Flash controller command |
| 47 | PERI_MS_PPU_FX_FLASHC_DFT | 0x40240200 | 0x00000100 | Flash controller tests |
| 48 | PERI_MS_PPU_FX_FLASHC_CM0 | 0x40240400 | 0x00000080 | Flash controller CM0+ |
| 49 | PERI_MS_PPU_FX_FLASHC_CM4 | 0x40240480 | 0x00000080 | Flash controller CM4 |
| 50 | PERI_MS_PPU_FX_FLASHC_CRYPT0 | 0x40240500 | 0x00000004 | Flash controller Crypto |
| 51 | PERI_MS_PPU_FX_FLASHC_DW0 | 0x40240580 | 0x00000004 | Flash controller P-DMA0 |
| 52 | PERI_MS_PPU_FX_FLASHC_DW1 | 0x40240600 | 0x00000004 | Flash controller P-DMA1 |
| 53 | PERI_MS_PPU_FX_FLASHC_DMAC | 0x40240680 | 0x00000004 | Flash controller M-DMA0 |
| 54 | PERI_MS_PPU_FX_FLASHC_FlashMgmt ^[34] | 0x4024F000 | 0x00000080 | Flash management |
| 55 | PERI_MS_PPU_FX_FLASHC_MainSafety | 0x4024F400 | 0x00000008 | Flash controller code-flash safety |
| 56 | PERI_MS_PPU_FX_FLASHC_WorkSafety | 0x4024F500 | 0x00000004 | Flash controller work-flash safety |
| 57 | PERI_MS_PPU_FX_SRSS_GENERAL | 0x40260000 | 0x00000400 | SRSS General |
| 58 | PERI_MS_PPU_FX_SRSS_MAIN | 0x40261000 | 0x00001000 | SRSS main |
| 59 | PERI_MS_PPU_FX_SRSS_SECURE | 0x40262000 | 0x00002000 | SRSS secure |
| 60 | PERI_MS_PPU_FX_MCWDT0_CONFIG | 0x40268000 | 0x00000080 | MCWDT #0 configuration |
| 61 | PERI_MS_PPU_FX_MCWDT1_CONFIG | 0x40268100 | 0x00000080 | MCWDT #1 configuration |
| 62 | PERI_MS_PPU_FX_MCWDT0_MAIN | 0x40268080 | 0x00000040 | MCWDT #0 main |
| 63 | PERI_MS_PPU_FX_MCWDT1_MAIN | 0x40268180 | 0x00000040 | MCWDT #1 main |
| 64 | PERI_MS_PPU_FX_WDT_CONFIG | 0x4026C000 | 0x00000020 | System WDT configuration |
| 65 | PERI_MS_PPU_FX_WDT_MAIN | 0x4026C040 | 0x00000020 | System WDT main |
| 66 | PERI_MS_PPU_FX_BACKUP_BACKUP | 0x40270000 | 0x00010000 | SRSS backup |
| 67 | PERI_MS_PPU_FX_DW0_DW | 0x40280000 | 0x00000100 | P-DMA0 main |
| 68 | PERI_MS_PPU_FX_DW1_DW | 0x40290000 | 0x00000100 | P-DMA1 main |
| 69 | PERI_MS_PPU_FX_DW0_DW_CRC | 0x40280100 | 0x00000080 | P-DMA0 CRC |
| 70 | PERI_MS_PPU_FX_DW1_DW_CRC | 0x40290100 | 0x00000080 | P-DMA1 CRC |
| 71 | PERI_MS_PPU_FX_DW0_CH_STRUCT0_CH | 0x40288000 | 0x00000040 | P-DMA0 Channel #0 |
| 72 | PERI_MS_PPU_FX_DW0_CH_STRUCT1_CH | 0x40288040 | 0x00000040 | P-DMA0 Channel #1 |
| 73 | PERI_MS_PPU_FX_DW0_CH_STRUCT2_CH | 0x40288080 | 0x00000040 | P-DMA0 Channel #2 |
| 74 | PERI_MS_PPU_FX_DW0_CH_STRUCT3_CH | 0x402880C0 | 0x00000040 | P-DMA0 Channel #3 |
| 75 | PERI_MS_PPU_FX_DW0_CH_STRUCT4_CH | 0x40288100 | 0x00000040 | P-DMA0 Channel #4 |
| 76 | PERI_MS_PPU_FX_DW0_CH_STRUCT5_CH | 0x40288140 | 0x00000040 | P-DMA0 Channel #5 |
| 77 | PERI_MS_PPU_FX_DW0_CH_STRUCT6_CH | 0x40288180 | 0x00000040 | P-DMA0 Channel #6 |
| 78 | PERI_MS_PPU_FX_DW0_CH_STRUCT7_CH | 0x402881C0 | 0x00000040 | P-DMA0 Channel #7 |
| 79 | PERI_MS_PPU_FX_DW0_CH_STRUCT8_CH | 0x40288200 | 0x00000040 | P-DMA0 Channel #8 |
| 80 | PERI_MS_PPU_FX_DW0_CH_STRUCT9_CH | 0x40288240 | 0x00000040 | P-DMA0 Channel #9 |
| 81 | PERI_MS_PPU_FX_DW0_CH_STRUCT10_CH | 0x40288280 | 0x00000040 | P-DMA0 Channel #10 |
| 82 | PERI_MS_PPU_FX_DW0_CH_STRUCT11_CH | 0x402882C0 | 0x00000040 | P-DMA0 Channel #11 |
| 83 | PERI_MS_PPU_FX_DW0_CH_STRUCT12_CH | 0x40288300 | 0x00000040 | P-DMA0 Channel #12 |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|--------------------|
| 84 | PERI_MS_PPU_FX_DW0_CH_STRUCT13_CH | 0x40288340 | 0x00000040 | P-DMA0 Channel #13 |
| 85 | PERI_MS_PPU_FX_DW0_CH_STRUCT14_CH | 0x40288380 | 0x00000040 | P-DMA0 Channel #14 |
| 86 | PERI_MS_PPU_FX_DW0_CH_STRUCT15_CH | 0x402883C0 | 0x00000040 | P-DMA0 Channel #15 |
| 87 | PERI_MS_PPU_FX_DW0_CH_STRUCT16_CH | 0x40288400 | 0x00000040 | P-DMA0 Channel #16 |
| 88 | PERI_MS_PPU_FX_DW0_CH_STRUCT17_CH | 0x40288440 | 0x00000040 | P-DMA0 Channel #17 |
| 89 | PERI_MS_PPU_FX_DW0_CH_STRUCT18_CH | 0x40288480 | 0x00000040 | P-DMA0 Channel #18 |
| 90 | PERI_MS_PPU_FX_DW0_CH_STRUCT19_CH | 0x402884C0 | 0x00000040 | P-DMA0 Channel #19 |
| 91 | PERI_MS_PPU_FX_DW0_CH_STRUCT20_CH | 0x40288500 | 0x00000040 | P-DMA0 Channel #20 |
| 92 | PERI_MS_PPU_FX_DW0_CH_STRUCT21_CH | 0x40288540 | 0x00000040 | P-DMA0 Channel #21 |
| 93 | PERI_MS_PPU_FX_DW0_CH_STRUCT22_CH | 0x40288580 | 0x00000040 | P-DMA0 Channel #22 |
| 94 | PERI_MS_PPU_FX_DW0_CH_STRUCT23_CH | 0x402885C0 | 0x00000040 | P-DMA0 Channel #23 |
| 95 | PERI_MS_PPU_FX_DW0_CH_STRUCT24_CH | 0x40288600 | 0x00000040 | P-DMA0 Channel #24 |
| 96 | PERI_MS_PPU_FX_DW0_CH_STRUCT25_CH | 0x40288640 | 0x00000040 | P-DMA0 Channel #25 |
| 97 | PERI_MS_PPU_FX_DW0_CH_STRUCT26_CH | 0x40288680 | 0x00000040 | P-DMA0 Channel #26 |
| 98 | PERI_MS_PPU_FX_DW0_CH_STRUCT27_CH | 0x402886C0 | 0x00000040 | P-DMA0 Channel #27 |
| 99 | PERI_MS_PPU_FX_DW0_CH_STRUCT28_CH | 0x40288700 | 0x00000040 | P-DMA0 Channel #28 |
| 100 | PERI_MS_PPU_FX_DW0_CH_STRUCT29_CH | 0x40288740 | 0x00000040 | P-DMA0 Channel #29 |
| 101 | PERI_MS_PPU_FX_DW0_CH_STRUCT30_CH | 0x40288780 | 0x00000040 | P-DMA0 Channel #30 |
| 102 | PERI_MS_PPU_FX_DW0_CH_STRUCT31_CH | 0x402887C0 | 0x00000040 | P-DMA0 Channel #31 |
| 103 | PERI_MS_PPU_FX_DW0_CH_STRUCT32_CH | 0x40288800 | 0x00000040 | P-DMA0 Channel #32 |
| 104 | PERI_MS_PPU_FX_DW0_CH_STRUCT33_CH | 0x40288840 | 0x00000040 | P-DMA0 Channel #33 |
| 105 | PERI_MS_PPU_FX_DW0_CH_STRUCT34_CH | 0x40288880 | 0x00000040 | P-DMA0 Channel #34 |
| 106 | PERI_MS_PPU_FX_DW0_CH_STRUCT35_CH | 0x402888C0 | 0x00000040 | P-DMA0 Channel #35 |
| 107 | PERI_MS_PPU_FX_DW0_CH_STRUCT36_CH | 0x40288900 | 0x00000040 | P-DMA0 Channel #36 |
| 108 | PERI_MS_PPU_FX_DW0_CH_STRUCT37_CH | 0x40288940 | 0x00000040 | P-DMA0 Channel #37 |
| 109 | PERI_MS_PPU_FX_DW0_CH_STRUCT38_CH | 0x40288980 | 0x00000040 | P-DMA0 Channel #38 |
| 110 | PERI_MS_PPU_FX_DW0_CH_STRUCT39_CH | 0x402889C0 | 0x00000040 | P-DMA0 Channel #39 |
| 111 | PERI_MS_PPU_FX_DW0_CH_STRUCT40_CH | 0x40288A00 | 0x00000040 | P-DMA0 Channel #40 |
| 112 | PERI_MS_PPU_FX_DW0_CH_STRUCT41_CH | 0x40288A40 | 0x00000040 | P-DMA0 Channel #41 |
| 113 | PERI_MS_PPU_FX_DW0_CH_STRUCT42_CH | 0x40288A80 | 0x00000040 | P-DMA0 Channel #42 |
| 114 | PERI_MS_PPU_FX_DW0_CH_STRUCT43_CH | 0x40288AC0 | 0x00000040 | P-DMA0 Channel #43 |
| 115 | PERI_MS_PPU_FX_DW0_CH_STRUCT44_CH | 0x40288B00 | 0x00000040 | P-DMA0 Channel #44 |
| 116 | PERI_MS_PPU_FX_DW0_CH_STRUCT45_CH | 0x40288B40 | 0x00000040 | P-DMA0 Channel #45 |
| 117 | PERI_MS_PPU_FX_DW0_CH_STRUCT46_CH | 0x40288B80 | 0x00000040 | P-DMA0 Channel #46 |
| 118 | PERI_MS_PPU_FX_DW0_CH_STRUCT47_CH | 0x40288BC0 | 0x00000040 | P-DMA0 Channel #47 |
| 119 | PERI_MS_PPU_FX_DW0_CH_STRUCT48_CH | 0x40288C00 | 0x00000040 | P-DMA0 Channel #48 |
| 120 | PERI_MS_PPU_FX_DW0_CH_STRUCT49_CH | 0x40288C40 | 0x00000040 | P-DMA0 Channel #49 |
| 121 | PERI_MS_PPU_FX_DW0_CH_STRUCT50_CH | 0x40288C80 | 0x00000040 | P-DMA0 Channel #50 |
| 122 | PERI_MS_PPU_FX_DW0_CH_STRUCT51_CH | 0x40288CC0 | 0x00000040 | P-DMA0 Channel #51 |
| 123 | PERI_MS_PPU_FX_DW0_CH_STRUCT52_CH | 0x40288D00 | 0x00000040 | P-DMA0 Channel #52 |
| 124 | PERI_MS_PPU_FX_DW0_CH_STRUCT53_CH | 0x40288D40 | 0x00000040 | P-DMA0 Channel #53 |
| 125 | PERI_MS_PPU_FX_DW0_CH_STRUCT54_CH | 0x40288D80 | 0x00000040 | P-DMA0 Channel #54 |
| 126 | PERI_MS_PPU_FX_DW0_CH_STRUCT55_CH | 0x40288DC0 | 0x00000040 | P-DMA0 Channel #55 |
| 127 | PERI_MS_PPU_FX_DW0_CH_STRUCT56_CH | 0x40288E00 | 0x00000040 | P-DMA0 Channel #56 |
| 128 | PERI_MS_PPU_FX_DW0_CH_STRUCT57_CH | 0x40288E40 | 0x00000040 | P-DMA0 Channel #57 |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|--------------------|
| 129 | PERI_MS_PPU_FX_DW0_CH_STRUCT58_CH | 0x40288E80 | 0x00000040 | P-DMA0 Channel #58 |
| 130 | PERI_MS_PPU_FX_DW0_CH_STRUCT59_CH | 0x40288EC0 | 0x00000040 | P-DMA0 Channel #59 |
| 131 | PERI_MS_PPU_FX_DW0_CH_STRUCT60_CH | 0x40288F00 | 0x00000040 | P-DMA0 Channel #60 |
| 132 | PERI_MS_PPU_FX_DW0_CH_STRUCT61_CH | 0x40288F40 | 0x00000040 | P-DMA0 Channel #61 |
| 133 | PERI_MS_PPU_FX_DW0_CH_STRUCT62_CH | 0x40288F80 | 0x00000040 | P-DMA0 Channel #62 |
| 134 | PERI_MS_PPU_FX_DW0_CH_STRUCT63_CH | 0x40288FC0 | 0x00000040 | P-DMA0 Channel #63 |
| 135 | PERI_MS_PPU_FX_DW0_CH_STRUCT64_CH | 0x40289000 | 0x00000040 | P-DMA0 Channel #64 |
| 136 | PERI_MS_PPU_FX_DW0_CH_STRUCT65_CH | 0x40289040 | 0x00000040 | P-DMA0 Channel #65 |
| 137 | PERI_MS_PPU_FX_DW0_CH_STRUCT66_CH | 0x40289080 | 0x00000040 | P-DMA0 Channel #66 |
| 138 | PERI_MS_PPU_FX_DW0_CH_STRUCT67_CH | 0x402890C0 | 0x00000040 | P-DMA0 Channel #67 |
| 139 | PERI_MS_PPU_FX_DW0_CH_STRUCT68_CH | 0x40289100 | 0x00000040 | P-DMA0 Channel #68 |
| 140 | PERI_MS_PPU_FX_DW0_CH_STRUCT69_CH | 0x40289140 | 0x00000040 | P-DMA0 Channel #69 |
| 141 | PERI_MS_PPU_FX_DW0_CH_STRUCT70_CH | 0x40289180 | 0x00000040 | P-DMA0 Channel #70 |
| 142 | PERI_MS_PPU_FX_DW0_CH_STRUCT71_CH | 0x402891C0 | 0x00000040 | P-DMA0 Channel #71 |
| 143 | PERI_MS_PPU_FX_DW0_CH_STRUCT72_CH | 0x40289200 | 0x00000040 | P-DMA0 Channel #72 |
| 144 | PERI_MS_PPU_FX_DW0_CH_STRUCT73_CH | 0x40289240 | 0x00000040 | P-DMA0 Channel #73 |
| 145 | PERI_MS_PPU_FX_DW0_CH_STRUCT74_CH | 0x40289280 | 0x00000040 | P-DMA0 Channel #74 |
| 146 | PERI_MS_PPU_FX_DW0_CH_STRUCT75_CH | 0x402892C0 | 0x00000040 | P-DMA0 Channel #75 |
| 147 | PERI_MS_PPU_FX_DW0_CH_STRUCT76_CH | 0x40289300 | 0x00000040 | P-DMA0 Channel #76 |
| 148 | PERI_MS_PPU_FX_DW0_CH_STRUCT77_CH | 0x40289340 | 0x00000040 | P-DMA0 Channel #77 |
| 149 | PERI_MS_PPU_FX_DW0_CH_STRUCT78_CH | 0x40289380 | 0x00000040 | P-DMA0 Channel #78 |
| 150 | PERI_MS_PPU_FX_DW0_CH_STRUCT79_CH | 0x402893C0 | 0x00000040 | P-DMA0 Channel #79 |
| 151 | PERI_MS_PPU_FX_DW0_CH_STRUCT80_CH | 0x40289400 | 0x00000040 | P-DMA0 Channel #80 |
| 152 | PERI_MS_PPU_FX_DW0_CH_STRUCT81_CH | 0x40289440 | 0x00000040 | P-DMA0 Channel #81 |
| 153 | PERI_MS_PPU_FX_DW0_CH_STRUCT82_CH | 0x40289480 | 0x00000040 | P-DMA0 Channel #82 |
| 154 | PERI_MS_PPU_FX_DW0_CH_STRUCT83_CH | 0x402894C0 | 0x00000040 | P-DMA0 Channel #83 |
| 155 | PERI_MS_PPU_FX_DW0_CH_STRUCT84_CH | 0x40289500 | 0x00000040 | P-DMA0 Channel #84 |
| 156 | PERI_MS_PPU_FX_DW0_CH_STRUCT85_CH | 0x40289540 | 0x00000040 | P-DMA0 Channel #85 |
| 157 | PERI_MS_PPU_FX_DW0_CH_STRUCT86_CH | 0x40289580 | 0x00000040 | P-DMA0 Channel #86 |
| 158 | PERI_MS_PPU_FX_DW0_CH_STRUCT87_CH | 0x402895C0 | 0x00000040 | P-DMA0 Channel #87 |
| 159 | PERI_MS_PPU_FX_DW0_CH_STRUCT88_CH | 0x40289600 | 0x00000040 | P-DMA0 Channel #88 |
| 160 | PERI_MS_PPU_FX_DW1_CH_STRUCT0_CH | 0x40298000 | 0x00000040 | P-DMA1 Channel #0 |
| 161 | PERI_MS_PPU_FX_DW1_CH_STRUCT1_CH | 0x40298040 | 0x00000040 | P-DMA1 Channel #1 |
| 162 | PERI_MS_PPU_FX_DW1_CH_STRUCT2_CH | 0x40298080 | 0x00000040 | P-DMA1 Channel #2 |
| 163 | PERI_MS_PPU_FX_DW1_CH_STRUCT3_CH | 0x402980C0 | 0x00000040 | P-DMA1 Channel #3 |
| 164 | PERI_MS_PPU_FX_DW1_CH_STRUCT4_CH | 0x40298100 | 0x00000040 | P-DMA1 Channel #4 |
| 165 | PERI_MS_PPU_FX_DW1_CH_STRUCT5_CH | 0x40298140 | 0x00000040 | P-DMA1 Channel #5 |
| 166 | PERI_MS_PPU_FX_DW1_CH_STRUCT6_CH | 0x40298180 | 0x00000040 | P-DMA1 Channel #6 |
| 167 | PERI_MS_PPU_FX_DW1_CH_STRUCT7_CH | 0x402981C0 | 0x00000040 | P-DMA1 Channel #7 |
| 168 | PERI_MS_PPU_FX_DW1_CH_STRUCT8_CH | 0x40298200 | 0x00000040 | P-DMA1 Channel #8 |
| 169 | PERI_MS_PPU_FX_DW1_CH_STRUCT9_CH | 0x40298240 | 0x00000040 | P-DMA1 Channel #9 |
| 170 | PERI_MS_PPU_FX_DW1_CH_STRUCT10_CH | 0x40298280 | 0x00000040 | P-DMA1 Channel #10 |
| 171 | PERI_MS_PPU_FX_DW1_CH_STRUCT11_CH | 0x402982C0 | 0x00000040 | P-DMA1 Channel #11 |
| 172 | PERI_MS_PPU_FX_DW1_CH_STRUCT12_CH | 0x40298300 | 0x00000040 | P-DMA1 Channel #12 |
| 173 | PERI_MS_PPU_FX_DW1_CH_STRUCT13_CH | 0x40298340 | 0x00000040 | P-DMA1 Channel #13 |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|--------------------|
| 174 | PERI_MS_PPU_FX_DW1_CH_STRUCT14_CH | 0x40298380 | 0x00000040 | P-DMA1 Channel #14 |
| 175 | PERI_MS_PPU_FX_DW1_CH_STRUCT15_CH | 0x402983C0 | 0x00000040 | P-DMA1 Channel #15 |
| 176 | PERI_MS_PPU_FX_DW1_CH_STRUCT16_CH | 0x40298400 | 0x00000040 | P-DMA1 Channel #16 |
| 177 | PERI_MS_PPU_FX_DW1_CH_STRUCT17_CH | 0x40298440 | 0x00000040 | P-DMA1 Channel #17 |
| 178 | PERI_MS_PPU_FX_DW1_CH_STRUCT18_CH | 0x40298480 | 0x00000040 | P-DMA1 Channel #18 |
| 179 | PERI_MS_PPU_FX_DW1_CH_STRUCT19_CH | 0x402984C0 | 0x00000040 | P-DMA1 Channel #19 |
| 180 | PERI_MS_PPU_FX_DW1_CH_STRUCT20_CH | 0x40298500 | 0x00000040 | P-DMA1 Channel #20 |
| 181 | PERI_MS_PPU_FX_DW1_CH_STRUCT21_CH | 0x40298540 | 0x00000040 | P-DMA1 Channel #21 |
| 182 | PERI_MS_PPU_FX_DW1_CH_STRUCT22_CH | 0x40298580 | 0x00000040 | P-DMA1 Channel #22 |
| 183 | PERI_MS_PPU_FX_DW1_CH_STRUCT23_CH | 0x402985C0 | 0x00000040 | P-DMA1 Channel #23 |
| 184 | PERI_MS_PPU_FX_DW1_CH_STRUCT24_CH | 0x40298600 | 0x00000040 | P-DMA1 Channel #24 |
| 185 | PERI_MS_PPU_FX_DW1_CH_STRUCT25_CH | 0x40298640 | 0x00000040 | P-DMA1 Channel #25 |
| 186 | PERI_MS_PPU_FX_DW1_CH_STRUCT26_CH | 0x40298680 | 0x00000040 | P-DMA1 Channel #26 |
| 187 | PERI_MS_PPU_FX_DW1_CH_STRUCT27_CH | 0x402986C0 | 0x00000040 | P-DMA1 Channel #27 |
| 188 | PERI_MS_PPU_FX_DW1_CH_STRUCT28_CH | 0x40298700 | 0x00000040 | P-DMA1 Channel #28 |
| 189 | PERI_MS_PPU_FX_DW1_CH_STRUCT29_CH | 0x40298740 | 0x00000040 | P-DMA1 Channel #29 |
| 190 | PERI_MS_PPU_FX_DW1_CH_STRUCT30_CH | 0x40298780 | 0x00000040 | P-DMA1 Channel #30 |
| 191 | PERI_MS_PPU_FX_DW1_CH_STRUCT31_CH | 0x402987C0 | 0x00000040 | P-DMA1 Channel #31 |
| 192 | PERI_MS_PPU_FX_DW1_CH_STRUCT32_CH | 0x40298800 | 0x00000040 | P-DMA1 Channel #32 |
| 193 | PERI_MS_PPU_FX_DMAC_TOP | 0x402A0000 | 0x00000010 | M-DMA0 main |
| 194 | PERI_MS_PPU_FX_DMAC_CH0_CH | 0x402A1000 | 0x00000100 | M-DMA0 Channel #0 |
| 195 | PERI_MS_PPU_FX_DMAC_CH1_CH | 0x402A1100 | 0x00000100 | M-DMA0 Channel #1 |
| 196 | PERI_MS_PPU_FX_DMAC_CH2_CH | 0x402A1200 | 0x00000100 | M-DMA0 Channel #2 |
| 197 | PERI_MS_PPU_FX_DMAC_CH3_CH | 0x402A1300 | 0x00000100 | M-DMA0 Channel #3 |
| 198 | PERI_MS_PPU_FX_EFUSE_CTL | 0x402C0000 | 0x00000200 | EFUSE control |
| 199 | PERI_MS_PPU_FX_EFUSE_DATA | 0x402C0800 | 0x00000200 | EFUSE data |
| 200 | PERI_MS_PPU_FX_BIST | 0x402F0000 | 0x00001000 | Built-in self test |
| 201 | PERI_MS_PPU_FX_HSIOM_PRT0_PRT | 0x40300000 | 0x00000008 | HSIOm Port #0 |
| 202 | PERI_MS_PPU_FX_HSIOM_PRT1_PRT | 0x40300010 | 0x00000008 | HSIOm Port #1 |
| 203 | PERI_MS_PPU_FX_HSIOM_PRT2_PRT | 0x40300020 | 0x00000008 | HSIOm Port #2 |
| 204 | PERI_MS_PPU_FX_HSIOM_PRT3_PRT | 0x40300030 | 0x00000008 | HSIOm Port #3 |
| 205 | PERI_MS_PPU_FX_HSIOM_PRT4_PRT | 0x40300040 | 0x00000008 | HSIOm Port #4 |
| 206 | PERI_MS_PPU_FX_HSIOM_PRT5_PRT | 0x40300050 | 0x00000008 | HSIOm Port #5 |
| 207 | PERI_MS_PPU_FX_HSIOM_PRT6_PRT | 0x40300060 | 0x00000008 | HSIOm Port #6 |
| 208 | PERI_MS_PPU_FX_HSIOM_PRT7_PRT | 0x40300070 | 0x00000008 | HSIOm Port #7 |
| 209 | PERI_MS_PPU_FX_HSIOM_PRT8_PRT | 0x40300080 | 0x00000008 | HSIOm Port #8 |
| 210 | PERI_MS_PPU_FX_HSIOM_PRT9_PRT | 0x40300090 | 0x00000008 | HSIOm Port #9 |
| 211 | PERI_MS_PPU_FX_HSIOM_PRT10_PRT | 0x403000A0 | 0x00000008 | HSIOm Port #10 |
| 212 | PERI_MS_PPU_FX_HSIOM_PRT11_PRT | 0x403000B0 | 0x00000008 | HSIOm Port #11 |
| 213 | PERI_MS_PPU_FX_HSIOM_PRT12_PRT | 0x403000C0 | 0x00000008 | HSIOm Port #12 |
| 214 | PERI_MS_PPU_FX_HSIOM_PRT13_PRT | 0x403000D0 | 0x00000008 | HSIOm Port #13 |
| 215 | PERI_MS_PPU_FX_HSIOM_PRT14_PRT | 0x403000E0 | 0x00000008 | HSIOm Port #14 |
| 216 | PERI_MS_PPU_FX_HSIOM_PRT15_PRT | 0x403000F0 | 0x00000008 | HSIOm Port #15 |
| 217 | PERI_MS_PPU_FX_HSIOM_PRT16_PRT | 0x40300100 | 0x00000008 | HSIOm Port #16 |
| 218 | PERI_MS_PPU_FX_HSIOM_PRT17_PRT | 0x40300110 | 0x00000008 | HSIOm Port #17 |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|--------------------------------|------------|------------|---------------------------------|
| 219 | PERI_MS_PPU_FX_HSIOM_PRT18_PRT | 0x40300120 | 0x00000008 | HSIOm Port #18 |
| 220 | PERI_MS_PPU_FX_HSIOM_PRT19_PRT | 0x40300130 | 0x00000008 | HSIOm Port #19 |
| 221 | PERI_MS_PPU_FX_HSIOM_PRT20_PRT | 0x40300140 | 0x00000008 | HSIOm Port #20 |
| 222 | PERI_MS_PPU_FX_HSIOM_PRT21_PRT | 0x40300150 | 0x00000008 | HSIOm Port #21 |
| 223 | PERI_MS_PPU_FX_HSIOM_PRT22_PRT | 0x40300160 | 0x00000008 | HSIOm Port #22 |
| 224 | PERI_MS_PPU_FX_HSIOM_PRT23_PRT | 0x40300170 | 0x00000008 | HSIOm Port #23 |
| 225 | PERI_MS_PPU_FX_HSIOM_AMUX | 0x40302000 | 0x00000010 | HSIOm Analog multiplexer |
| 226 | PERI_MS_PPU_FX_HSIOM_MON | 0x40302200 | 0x00000010 | HSIOm monitor |
| 227 | PERI_MS_PPU_FX_HSIOM_ALTJTAG | 0x40302240 | 0x00000004 | HSIOm Alternate JTAG |
| 228 | PERI_MS_PPU_FX_GPIO_PRT0_PRT | 0x40310000 | 0x00000040 | GPIO_ENH Port #0 |
| 229 | PERI_MS_PPU_FX_GPIO_PRT1_PRT | 0x40310080 | 0x00000040 | GPIO_STD Port #1 |
| 230 | PERI_MS_PPU_FX_GPIO_PRT2_PRT | 0x40310100 | 0x00000040 | GPIO_STD Port #2 |
| 231 | PERI_MS_PPU_FX_GPIO_PRT3_PRT | 0x40310180 | 0x00000040 | GPIO_STD Port #3 |
| 232 | PERI_MS_PPU_FX_GPIO_PRT4_PRT | 0x40310200 | 0x00000040 | GPIO_STD Port #4 |
| 233 | PERI_MS_PPU_FX_GPIO_PRT5_PRT | 0x40310280 | 0x00000040 | GPIO_STD Port #5 |
| 234 | PERI_MS_PPU_FX_GPIO_PRT6_PRT | 0x40310300 | 0x00000040 | GPIO_STD Port #6 |
| 235 | PERI_MS_PPU_FX_GPIO_PRT7_PRT | 0x40310380 | 0x00000040 | GPIO_STD Port #7 |
| 236 | PERI_MS_PPU_FX_GPIO_PRT8_PRT | 0x40310400 | 0x00000040 | GPIO_STD Port #8 |
| 237 | PERI_MS_PPU_FX_GPIO_PRT9_PRT | 0x40310480 | 0x00000040 | GPIO_STD Port #9 |
| 238 | PERI_MS_PPU_FX_GPIO_PRT10_PRT | 0x40310500 | 0x00000040 | GPIO_STD Port #10 |
| 239 | PERI_MS_PPU_FX_GPIO_PRT11_PRT | 0x40310580 | 0x00000040 | GPIO_STD Port #11 |
| 240 | PERI_MS_PPU_FX_GPIO_PRT12_PRT | 0x40310600 | 0x00000040 | GPIO_STD Port #12 |
| 241 | PERI_MS_PPU_FX_GPIO_PRT13_PRT | 0x40310680 | 0x00000040 | GPIO_STD Port #13 |
| 242 | PERI_MS_PPU_FX_GPIO_PRT14_PRT | 0x40310700 | 0x00000040 | GPIO_STD Port #14 |
| 243 | PERI_MS_PPU_FX_GPIO_PRT15_PRT | 0x40310780 | 0x00000040 | GPIO_STD Port #15 |
| 244 | PERI_MS_PPU_FX_GPIO_PRT16_PRT | 0x40310800 | 0x00000040 | GPIO_STD Port #16 |
| 245 | PERI_MS_PPU_FX_GPIO_PRT17_PRT | 0x40310880 | 0x00000040 | GPIO_STD Port #17 |
| 246 | PERI_MS_PPU_FX_GPIO_PRT18_PRT | 0x40310900 | 0x00000040 | GPIO_STD Port #18 |
| 247 | PERI_MS_PPU_FX_GPIO_PRT19_PRT | 0x40310980 | 0x00000040 | GPIO_STD Port #19 |
| 248 | PERI_MS_PPU_FX_GPIO_PRT20_PRT | 0x40310A00 | 0x00000040 | GPIO_STD Port #20 |
| 249 | PERI_MS_PPU_FX_GPIO_PRT21_PRT | 0x40310A80 | 0x00000040 | GPIO_STD Port #21 |
| 250 | PERI_MS_PPU_FX_GPIO_PRT22_PRT | 0x40310B00 | 0x00000040 | GPIO_STD Port #22 |
| 251 | PERI_MS_PPU_FX_GPIO_PRT23_PRT | 0x40310B80 | 0x00000040 | GPIO_STD Port #23 |
| 252 | PERI_MS_PPU_FX_GPIO_PRT0_CFG | 0x40310040 | 0x00000020 | GPIO_ENH Port #0 configuration |
| 253 | PERI_MS_PPU_FX_GPIO_PRT1_CFG | 0x403100C0 | 0x00000020 | GPIO_STD Port #1 configuration |
| 254 | PERI_MS_PPU_FX_GPIO_PRT2_CFG | 0x40310140 | 0x00000020 | GPIO_STD Port #2 configuration |
| 255 | PERI_MS_PPU_FX_GPIO_PRT3_CFG | 0x403101C0 | 0x00000020 | GPIO_STD Port #3 configuration |
| 256 | PERI_MS_PPU_FX_GPIO_PRT4_CFG | 0x40310240 | 0x00000020 | GPIO_STD Port #4 configuration |
| 257 | PERI_MS_PPU_FX_GPIO_PRT5_CFG | 0x403102C0 | 0x00000020 | GPIO_STD Port #5 configuration |
| 258 | PERI_MS_PPU_FX_GPIO_PRT6_CFG | 0x40310340 | 0x00000020 | GPIO_STD Port #6 configuration |
| 259 | PERI_MS_PPU_FX_GPIO_PRT7_CFG | 0x403103C0 | 0x00000020 | GPIO_STD Port #7 configuration |
| 260 | PERI_MS_PPU_FX_GPIO_PRT8_CFG | 0x40310440 | 0x00000020 | GPIO_STD Port #8 configuration |
| 261 | PERI_MS_PPU_FX_GPIO_PRT9_CFG | 0x403104C0 | 0x00000020 | GPIO_STD Port #9 configuration |
| 262 | PERI_MS_PPU_FX_GPIO_PRT10_CFG | 0x40310540 | 0x00000020 | GPIO_STD Port #10 configuration |
| 263 | PERI_MS_PPU_FX_GPIO_PRT11_CFG | 0x403105C0 | 0x00000020 | GPIO_STD Port #11 configuration |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|--------------------------------------|------------|------------|---------------------------------|
| 264 | PERI_MS_PPU_FX_GPIO_PRT12_CFG | 0x40310640 | 0x00000020 | GPIO_STD Port #12 configuration |
| 265 | PERI_MS_PPU_FX_GPIO_PRT13_CFG | 0x403106C0 | 0x00000020 | GPIO_STD Port #13 configuration |
| 266 | PERI_MS_PPU_FX_GPIO_PRT14_CFG | 0x40310740 | 0x00000020 | GPIO_STD Port #14 configuration |
| 267 | PERI_MS_PPU_FX_GPIO_PRT15_CFG | 0x403107C0 | 0x00000020 | GPIO_STD Port #15 configuration |
| 268 | PERI_MS_PPU_FX_GPIO_PRT16_CFG | 0x40310840 | 0x00000020 | GPIO_STD Port #16 configuration |
| 269 | PERI_MS_PPU_FX_GPIO_PRT17_CFG | 0x403108C0 | 0x00000020 | GPIO_STD Port #17 configuration |
| 270 | PERI_MS_PPU_FX_GPIO_PRT18_CFG | 0x40310940 | 0x00000020 | GPIO_STD Port #18 configuration |
| 271 | PERI_MS_PPU_FX_GPIO_PRT19_CFG | 0x403109C0 | 0x00000020 | GPIO_STD Port #19 configuration |
| 272 | PERI_MS_PPU_FX_GPIO_PRT20_CFG | 0x40310A40 | 0x00000020 | GPIO_STD Port #20 configuration |
| 273 | PERI_MS_PPU_FX_GPIO_PRT21_CFG | 0x40310AC0 | 0x00000020 | GPIO_STD Port #21 configuration |
| 274 | PERI_MS_PPU_FX_GPIO_PRT22_CFG | 0x40310B40 | 0x00000020 | GPIO_STD Port #22 configuration |
| 275 | PERI_MS_PPU_FX_GPIO_PRT23_CFG | 0x40310BC0 | 0x00000020 | GPIO_STD Port #23 configuration |
| 276 | PERI_MS_PPU_FX_GPIO_GPIO | 0x40314000 | 0x00000040 | GPIO main |
| 277 | PERI_MS_PPU_FX_GPIO_TEST | 0x40315000 | 0x00000008 | GPIO test |
| 278 | PERI_MS_PPU_FX_SMARTIO_PRT12_PRT | 0x40320C00 | 0x00000100 | SMART I/O #12 |
| 279 | PERI_MS_PPU_FX_SMARTIO_PRT13_PRT | 0x40320D00 | 0x00000100 | SMART I/O #13 |
| 280 | PERI_MS_PPU_FX_SMARTIO_PRT14_PRT | 0x40320E00 | 0x00000100 | SMART I/O #14 |
| 281 | PERI_MS_PPU_FX_SMARTIO_PRT15_PRT | 0x40320F00 | 0x00000100 | SMART I/O #15 |
| 282 | PERI_MS_PPU_FX_SMARTIO_PRT17_PRT | 0x40321100 | 0x00000100 | SMART I/O #17 |
| 283 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT0_CNT | 0x40380000 | 0x00000080 | TCPWM0 Group #0, Counter #0 |
| 284 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT1_CNT | 0x40380080 | 0x00000080 | TCPWM0 Group #0, Counter #1 |
| 285 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT2_CNT | 0x40380100 | 0x00000080 | TCPWM0 Group #0, Counter #2 |
| 286 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT3_CNT | 0x40380180 | 0x00000080 | TCPWM0 Group #0, Counter #3 |
| 287 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT4_CNT | 0x40380200 | 0x00000080 | TCPWM0 Group #0, Counter #4 |
| 288 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT5_CNT | 0x40380280 | 0x00000080 | TCPWM0 Group #0, Counter #5 |
| 289 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT6_CNT | 0x40380300 | 0x00000080 | TCPWM0 Group #0, Counter #6 |
| 290 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT7_CNT | 0x40380380 | 0x00000080 | TCPWM0 Group #0, Counter #7 |
| 291 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT8_CNT | 0x40380400 | 0x00000080 | TCPWM0 Group #0, Counter #8 |
| 292 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT9_CNT | 0x40380480 | 0x00000080 | TCPWM0 Group #0, Counter #9 |
| 293 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT10_CNT | 0x40380500 | 0x00000080 | TCPWM0 Group #0, Counter #10 |
| 294 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT11_CNT | 0x40380580 | 0x00000080 | TCPWM0 Group #0, Counter #11 |
| 295 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT12_CNT | 0x40380600 | 0x00000080 | TCPWM0 Group #0, Counter #12 |
| 296 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT13_CNT | 0x40380680 | 0x00000080 | TCPWM0 Group #0, Counter #13 |
| 297 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT14_CNT | 0x40380700 | 0x00000080 | TCPWM0 Group #0, Counter #14 |
| 298 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT15_CNT | 0x40380780 | 0x00000080 | TCPWM0 Group #0, Counter #15 |
| 299 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT16_CNT | 0x40380800 | 0x00000080 | TCPWM0 Group #0, Counter #16 |
| 300 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT17_CNT | 0x40380880 | 0x00000080 | TCPWM0 Group #0, Counter #17 |
| 301 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT18_CNT | 0x40380900 | 0x00000080 | TCPWM0 Group #0, Counter #18 |
| 302 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT19_CNT | 0x40380980 | 0x00000080 | TCPWM0 Group #0, Counter #19 |
| 303 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT20_CNT | 0x40380A00 | 0x00000080 | TCPWM0 Group #0, Counter #20 |
| 304 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT21_CNT | 0x40380A80 | 0x00000080 | TCPWM0 Group #0, Counter #21 |
| 305 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT22_CNT | 0x40380B00 | 0x00000080 | TCPWM0 Group #0, Counter #22 |
| 306 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT23_CNT | 0x40380B80 | 0x00000080 | TCPWM0 Group #0, Counter #23 |
| 307 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT24_CNT | 0x40380C00 | 0x00000080 | TCPWM0 Group #0, Counter #24 |
| 308 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT25_CNT | 0x40380C80 | 0x00000080 | TCPWM0 Group #0, Counter #25 |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|--------------------------------------|------------|------------|------------------------------|
| 309 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT26_CNT | 0x40380D00 | 0x00000080 | TCPWM0 Group #0, Counter #26 |
| 310 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT27_CNT | 0x40380D80 | 0x00000080 | TCPWM0 Group #0, Counter #27 |
| 311 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT28_CNT | 0x40380E00 | 0x00000080 | TCPWM0 Group #0, Counter #28 |
| 312 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT29_CNT | 0x40380E80 | 0x00000080 | TCPWM0 Group #0, Counter #29 |
| 313 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT30_CNT | 0x40380F00 | 0x00000080 | TCPWM0 Group #0, Counter #30 |
| 314 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT31_CNT | 0x40380F80 | 0x00000080 | TCPWM0 Group #0, Counter #31 |
| 315 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT32_CNT | 0x40381000 | 0x00000080 | TCPWM0 Group #0, Counter #32 |
| 316 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT33_CNT | 0x40381080 | 0x00000080 | TCPWM0 Group #0, Counter #33 |
| 317 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT34_CNT | 0x40381100 | 0x00000080 | TCPWM0 Group #0, Counter #34 |
| 318 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT35_CNT | 0x40381180 | 0x00000080 | TCPWM0 Group #0, Counter #35 |
| 319 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT36_CNT | 0x40381200 | 0x00000080 | TCPWM0 Group #0, Counter #36 |
| 320 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT37_CNT | 0x40381280 | 0x00000080 | TCPWM0 Group #0, Counter #37 |
| 321 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT38_CNT | 0x40381300 | 0x00000080 | TCPWM0 Group #0, Counter #38 |
| 322 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT39_CNT | 0x40381380 | 0x00000080 | TCPWM0 Group #0, Counter #39 |
| 323 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT40_CNT | 0x40381400 | 0x00000080 | TCPWM0 Group #0, Counter #40 |
| 324 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT41_CNT | 0x40381480 | 0x00000080 | TCPWM0 Group #0, Counter #41 |
| 325 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT42_CNT | 0x40381500 | 0x00000080 | TCPWM0 Group #0, Counter #42 |
| 326 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT43_CNT | 0x40381580 | 0x00000080 | TCPWM0 Group #0, Counter #43 |
| 327 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT44_CNT | 0x40381600 | 0x00000080 | TCPWM0 Group #0, Counter #44 |
| 328 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT45_CNT | 0x40381680 | 0x00000080 | TCPWM0 Group #0, Counter #45 |
| 329 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT46_CNT | 0x40381700 | 0x00000080 | TCPWM0 Group #0, Counter #46 |
| 330 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT47_CNT | 0x40381780 | 0x00000080 | TCPWM0 Group #0, Counter #47 |
| 331 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT48_CNT | 0x40381800 | 0x00000080 | TCPWM0 Group #0, Counter #48 |
| 332 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT49_CNT | 0x40381880 | 0x00000080 | TCPWM0 Group #0, Counter #49 |
| 333 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT50_CNT | 0x40381900 | 0x00000080 | TCPWM0 Group #0, Counter #50 |
| 334 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT51_CNT | 0x40381980 | 0x00000080 | TCPWM0 Group #0, Counter #51 |
| 335 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT52_CNT | 0x40381A00 | 0x00000080 | TCPWM0 Group #0, Counter #52 |
| 336 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT53_CNT | 0x40381A80 | 0x00000080 | TCPWM0 Group #0, Counter #53 |
| 337 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT54_CNT | 0x40381B00 | 0x00000080 | TCPWM0 Group #0, Counter #54 |
| 338 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT55_CNT | 0x40381B80 | 0x00000080 | TCPWM0 Group #0, Counter #55 |
| 339 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT56_CNT | 0x40381C00 | 0x00000080 | TCPWM0 Group #0, Counter #56 |
| 340 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT57_CNT | 0x40381C80 | 0x00000080 | TCPWM0 Group #0, Counter #57 |
| 341 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT58_CNT | 0x40381D00 | 0x00000080 | TCPWM0 Group #0, Counter #58 |
| 342 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT59_CNT | 0x40381D80 | 0x00000080 | TCPWM0 Group #0, Counter #59 |
| 343 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT60_CNT | 0x40381E00 | 0x00000080 | TCPWM0 Group #0, Counter #60 |
| 344 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT61_CNT | 0x40381E80 | 0x00000080 | TCPWM0 Group #0, Counter #61 |
| 345 | PERI_MS_PPU_FX_TCPWM0_GRP0_CNT62_CNT | 0x40381F00 | 0x00000080 | TCPWM0 Group #0, Counter #62 |
| 346 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT0_CNT | 0x40388000 | 0x00000080 | TCPWM0 Group #1, Counter #0 |
| 347 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT1_CNT | 0x40388080 | 0x00000080 | TCPWM0 Group #1, Counter #1 |
| 348 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT2_CNT | 0x40388100 | 0x00000080 | TCPWM0 Group #1, Counter #2 |
| 349 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT3_CNT | 0x40388180 | 0x00000080 | TCPWM0 Group #1, Counter #3 |
| 350 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT4_CNT | 0x40388200 | 0x00000080 | TCPWM0 Group #1, Counter #4 |
| 351 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT5_CNT | 0x40388280 | 0x00000080 | TCPWM0 Group #1, Counter #5 |
| 352 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT6_CNT | 0x40388300 | 0x00000080 | TCPWM0 Group #1, Counter #6 |
| 353 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT7_CNT | 0x40388380 | 0x00000080 | TCPWM0 Group #1, Counter #7 |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|--------------------------------------|------------|------------|------------------------------|
| 354 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT8_CNT | 0x40388400 | 0x00000080 | TCPWM0 Group #1, Counter #8 |
| 355 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT9_CNT | 0x40388480 | 0x00000080 | TCPWM0 Group #1, Counter #9 |
| 356 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT10_CNT | 0x40388500 | 0x00000080 | TCPWM0 Group #1, Counter #10 |
| 357 | PERI_MS_PPU_FX_TCPWM0_GRP1_CNT11_CNT | 0x40388580 | 0x00000080 | TCPWM0 Group #1, Counter #11 |
| 358 | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT0_CNT | 0x40390000 | 0x00000080 | TCPWM0 Group #2, Counter #0 |
| 359 | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT1_CNT | 0x40390080 | 0x00000080 | TCPWM0 Group #2, Counter #1 |
| 360 | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT2_CNT | 0x40390100 | 0x00000080 | TCPWM0 Group #2, Counter #2 |
| 361 | PERI_MS_PPU_FX_TCPWM0_GRP2_CNT3_CNT | 0x40390180 | 0x00000080 | TCPWM0 Group #2, Counter #3 |
| 362 | PERI_MS_PPU_FX_EVTGEN0 | 0x403F0000 | 0x00001000 | Event generator #0 |
| 363 | PERI_MS_PPU_FX_LIN0_MAIN | 0x40500000 | 0x00000008 | LIN0, main |
| 364 | PERI_MS_PPU_FX_LIN0_CH0_CH | 0x40508000 | 0x00000100 | LIN0, Channel #0 |
| 365 | PERI_MS_PPU_FX_LIN0_CH1_CH | 0x40508100 | 0x00000100 | LIN0, Channel #1 |
| 366 | PERI_MS_PPU_FX_LIN0_CH2_CH | 0x40508200 | 0x00000100 | LIN0, Channel #2 |
| 367 | PERI_MS_PPU_FX_LIN0_CH3_CH | 0x40508300 | 0x00000100 | LIN0, Channel #3 |
| 368 | PERI_MS_PPU_FX_LIN0_CH4_CH | 0x40508400 | 0x00000100 | LIN0, Channel #4 |
| 369 | PERI_MS_PPU_FX_LIN0_CH5_CH | 0x40508500 | 0x00000100 | LIN0, Channel #5 |
| 370 | PERI_MS_PPU_FX_LIN0_CH6_CH | 0x40508600 | 0x00000100 | LIN0, Channel #6 |
| 371 | PERI_MS_PPU_FX_LIN0_CH7_CH | 0x40508700 | 0x00000100 | LIN0, Channel #7 |
| 372 | PERI_MS_PPU_FX_CANFD0_CH0_CH | 0x40520000 | 0x00000200 | CAN0, Channel #0 |
| 373 | PERI_MS_PPU_FX_CANFD0_CH1_CH | 0x40520200 | 0x00000200 | CAN0, Channel #1 |
| 374 | PERI_MS_PPU_FX_CANFD0_CH2_CH | 0x40520400 | 0x00000200 | CAN0, Channel #2 |
| 375 | PERI_MS_PPU_FX_CANFD1_CH0_CH | 0x40540000 | 0x00000200 | CAN1, Channel #0 |
| 376 | PERI_MS_PPU_FX_CANFD1_CH1_CH | 0x40540200 | 0x00000200 | CAN1, Channel #1 |
| 377 | PERI_MS_PPU_FX_CANFD1_CH2_CH | 0x40540400 | 0x00000200 | CAN1, Channel #2 |
| 378 | PERI_MS_PPU_FX_CANFD0_MAIN | 0x40521000 | 0x00000100 | CAN0 main |
| 379 | PERI_MS_PPU_FX_CANFD1_MAIN | 0x40541000 | 0x00000100 | CAN1 main |
| 380 | PERI_MS_PPU_FX_CANFD0_BUF | 0x40530000 | 0x00010000 | CAN0 buffer |
| 381 | PERI_MS_PPU_FX_CANFD1_BUF | 0x40550000 | 0x00010000 | CAN1 buffer |
| 382 | PERI_MS_PPU_FX_SCB0 | 0x40600000 | 0x00010000 | SCB0 |
| 383 | PERI_MS_PPU_FX_SCB1 | 0x40610000 | 0x00010000 | SCB1 |
| 384 | PERI_MS_PPU_FX_SCB2 | 0x40620000 | 0x00010000 | SCB2 |
| 385 | PERI_MS_PPU_FX_SCB3 | 0x40630000 | 0x00010000 | SCB3 |
| 386 | PERI_MS_PPU_FX_SCB4 | 0x40640000 | 0x00010000 | SCB4 |
| 387 | PERI_MS_PPU_FX_SCB5 | 0x40650000 | 0x00010000 | SCB5 |
| 388 | PERI_MS_PPU_FX_SCB6 | 0x40660000 | 0x00010000 | SCB6 |
| 389 | PERI_MS_PPU_FX_SCB7 | 0x40670000 | 0x00010000 | SCB7 |
| 390 | PERI_MS_PPU_FX_PASS0_SAR0_SAR | 0x40900000 | 0x00000400 | PASS SAR0 |
| 391 | PERI_MS_PPU_FX_PASS0_SAR1_SAR | 0x40901000 | 0x00000400 | PASS SAR1 |
| 392 | PERI_MS_PPU_FX_PASS0_SAR2_SAR | 0x40902000 | 0x00000400 | PASS SAR2 |
| 393 | PERI_MS_PPU_FX_PASS0_SAR0_CH0_CH | 0x40900800 | 0x00000040 | SAR0, Channel #0 |
| 394 | PERI_MS_PPU_FX_PASS0_SAR0_CH1_CH | 0x40900840 | 0x00000040 | SAR0, Channel #1 |
| 395 | PERI_MS_PPU_FX_PASS0_SAR0_CH2_CH | 0x40900880 | 0x00000040 | SAR0, Channel #2 |
| 396 | PERI_MS_PPU_FX_PASS0_SAR0_CH3_CH | 0x409008C0 | 0x00000040 | SAR0, Channel #3 |
| 397 | PERI_MS_PPU_FX_PASS0_SAR0_CH4_CH | 0x40900900 | 0x00000040 | SAR0, Channel #4 |
| 398 | PERI_MS_PPU_FX_PASS0_SAR0_CH5_CH | 0x40900940 | 0x00000040 | SAR0, Channel #5 |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|-------------------|
| 399 | PERI_MS_PPU_FX_PASS0_SAR0_CH6_CH | 0x40900980 | 0x00000040 | SAR0, Channel #6 |
| 400 | PERI_MS_PPU_FX_PASS0_SAR0_CH7_CH | 0x409009C0 | 0x00000040 | SAR0, Channel #7 |
| 401 | PERI_MS_PPU_FX_PASS0_SAR0_CH8_CH | 0x40900A00 | 0x00000040 | SAR0, Channel #8 |
| 402 | PERI_MS_PPU_FX_PASS0_SAR0_CH9_CH | 0x40900A40 | 0x00000040 | SAR0, Channel #9 |
| 403 | PERI_MS_PPU_FX_PASS0_SAR0_CH10_CH | 0x40900A80 | 0x00000040 | SAR0, Channel #10 |
| 404 | PERI_MS_PPU_FX_PASS0_SAR0_CH11_CH | 0x40900AC0 | 0x00000040 | SAR0, Channel #11 |
| 405 | PERI_MS_PPU_FX_PASS0_SAR0_CH12_CH | 0x40900B00 | 0x00000040 | SAR0, Channel #12 |
| 406 | PERI_MS_PPU_FX_PASS0_SAR0_CH13_CH | 0x40900B40 | 0x00000040 | SAR0, Channel #13 |
| 407 | PERI_MS_PPU_FX_PASS0_SAR0_CH14_CH | 0x40900B80 | 0x00000040 | SAR0, Channel #14 |
| 408 | PERI_MS_PPU_FX_PASS0_SAR0_CH15_CH | 0x40900BC0 | 0x00000040 | SAR0, Channel #15 |
| 409 | PERI_MS_PPU_FX_PASS0_SAR0_CH16_CH | 0x40900C00 | 0x00000040 | SAR0, Channel #16 |
| 410 | PERI_MS_PPU_FX_PASS0_SAR0_CH17_CH | 0x40900C40 | 0x00000040 | SAR0, Channel #17 |
| 411 | PERI_MS_PPU_FX_PASS0_SAR0_CH18_CH | 0x40900C80 | 0x00000040 | SAR0, Channel #18 |
| 412 | PERI_MS_PPU_FX_PASS0_SAR0_CH19_CH | 0x40900CC0 | 0x00000040 | SAR0, Channel #19 |
| 413 | PERI_MS_PPU_FX_PASS0_SAR0_CH20_CH | 0x40900D00 | 0x00000040 | SAR0, Channel #20 |
| 414 | PERI_MS_PPU_FX_PASS0_SAR0_CH21_CH | 0x40900D40 | 0x00000040 | SAR0, Channel #21 |
| 415 | PERI_MS_PPU_FX_PASS0_SAR0_CH22_CH | 0x40900D80 | 0x00000040 | SAR0, Channel #22 |
| 416 | PERI_MS_PPU_FX_PASS0_SAR0_CH23_CH | 0x40900DC0 | 0x00000040 | SAR0, Channel #23 |
| 417 | PERI_MS_PPU_FX_PASS0_SAR1_CH0_CH | 0x40901800 | 0x00000040 | SAR1, Channel #0 |
| 418 | PERI_MS_PPU_FX_PASS0_SAR1_CH1_CH | 0x40901840 | 0x00000040 | SAR1, Channel #1 |
| 419 | PERI_MS_PPU_FX_PASS0_SAR1_CH2_CH | 0x40901880 | 0x00000040 | SAR1, Channel #2 |
| 420 | PERI_MS_PPU_FX_PASS0_SAR1_CH3_CH | 0x409018C0 | 0x00000040 | SAR1, Channel #3 |
| 421 | PERI_MS_PPU_FX_PASS0_SAR1_CH4_CH | 0x40901900 | 0x00000040 | SAR1, Channel #4 |
| 422 | PERI_MS_PPU_FX_PASS0_SAR1_CH5_CH | 0x40901940 | 0x00000040 | SAR1, Channel #5 |
| 423 | PERI_MS_PPU_FX_PASS0_SAR1_CH6_CH | 0x40901980 | 0x00000040 | SAR1, Channel #6 |
| 424 | PERI_MS_PPU_FX_PASS0_SAR1_CH7_CH | 0x409019C0 | 0x00000040 | SAR1, Channel #7 |
| 425 | PERI_MS_PPU_FX_PASS0_SAR1_CH8_CH | 0x40901A00 | 0x00000040 | SAR1, Channel #8 |
| 426 | PERI_MS_PPU_FX_PASS0_SAR1_CH9_CH | 0x40901A40 | 0x00000040 | SAR1, Channel #9 |
| 427 | PERI_MS_PPU_FX_PASS0_SAR1_CH10_CH | 0x40901A80 | 0x00000040 | SAR1, Channel #10 |
| 428 | PERI_MS_PPU_FX_PASS0_SAR1_CH11_CH | 0x40901AC0 | 0x00000040 | SAR1, Channel #11 |
| 429 | PERI_MS_PPU_FX_PASS0_SAR1_CH12_CH | 0x40901B00 | 0x00000040 | SAR1, Channel #12 |
| 430 | PERI_MS_PPU_FX_PASS0_SAR1_CH13_CH | 0x40901B40 | 0x00000040 | SAR1, Channel #13 |
| 431 | PERI_MS_PPU_FX_PASS0_SAR1_CH14_CH | 0x40901B80 | 0x00000040 | SAR1, Channel #14 |
| 432 | PERI_MS_PPU_FX_PASS0_SAR1_CH15_CH | 0x40901BC0 | 0x00000040 | SAR1, Channel #15 |
| 433 | PERI_MS_PPU_FX_PASS0_SAR1_CH16_CH | 0x40901C00 | 0x00000040 | SAR1, Channel #16 |
| 434 | PERI_MS_PPU_FX_PASS0_SAR1_CH17_CH | 0x40901C40 | 0x00000040 | SAR1, Channel #17 |
| 435 | PERI_MS_PPU_FX_PASS0_SAR1_CH18_CH | 0x40901C80 | 0x00000040 | SAR1, Channel #18 |
| 436 | PERI_MS_PPU_FX_PASS0_SAR1_CH19_CH | 0x40901CC0 | 0x00000040 | SAR1, Channel #19 |
| 437 | PERI_MS_PPU_FX_PASS0_SAR1_CH20_CH | 0x40901D00 | 0x00000040 | SAR1, Channel #20 |
| 438 | PERI_MS_PPU_FX_PASS0_SAR1_CH21_CH | 0x40901D40 | 0x00000040 | SAR1, Channel #21 |
| 439 | PERI_MS_PPU_FX_PASS0_SAR1_CH22_CH | 0x40901D80 | 0x00000040 | SAR1, Channel #22 |
| 440 | PERI_MS_PPU_FX_PASS0_SAR1_CH23_CH | 0x40901DC0 | 0x00000040 | SAR1, Channel #23 |
| 441 | PERI_MS_PPU_FX_PASS0_SAR1_CH24_CH | 0x40901E00 | 0x00000040 | SAR1, Channel #24 |
| 442 | PERI_MS_PPU_FX_PASS0_SAR1_CH25_CH | 0x40901E40 | 0x00000040 | SAR1, Channel #25 |
| 443 | PERI_MS_PPU_FX_PASS0_SAR1_CH26_CH | 0x40901E80 | 0x00000040 | SAR1, Channel #26 |

Table 22-1 PPU Fixed Structure Pairs (continued)

| Pair No. | PPU Fixed Structure Pair | Address | Size | Description |
|----------|-----------------------------------|------------|------------|-------------------|
| 444 | PERI_MS_PPU_FX_PASS0_SAR1_CH27_CH | 0x40901EC0 | 0x00000040 | SAR1, Channel #27 |
| 445 | PERI_MS_PPU_FX_PASS0_SAR1_CH28_CH | 0x40901F00 | 0x00000040 | SAR1, Channel #28 |
| 446 | PERI_MS_PPU_FX_PASS0_SAR1_CH29_CH | 0x40901F40 | 0x00000040 | SAR1, Channel #29 |
| 447 | PERI_MS_PPU_FX_PASS0_SAR1_CH30_CH | 0x40901F80 | 0x00000040 | SAR1, Channel #30 |
| 448 | PERI_MS_PPU_FX_PASS0_SAR1_CH31_CH | 0x40901FC0 | 0x00000040 | SAR1, Channel #31 |
| 449 | PERI_MS_PPU_FX_PASS0_SAR2_CH0_CH | 0x40902800 | 0x00000040 | SAR2, Channel #0 |
| 450 | PERI_MS_PPU_FX_PASS0_SAR2_CH1_CH | 0x40902840 | 0x00000040 | SAR2, Channel #1 |
| 451 | PERI_MS_PPU_FX_PASS0_SAR2_CH2_CH | 0x40902880 | 0x00000040 | SAR2, Channel #2 |
| 452 | PERI_MS_PPU_FX_PASS0_SAR2_CH3_CH | 0x409028C0 | 0x00000040 | SAR2, Channel #3 |
| 453 | PERI_MS_PPU_FX_PASS0_SAR2_CH4_CH | 0x40902900 | 0x00000040 | SAR2, Channel #4 |
| 454 | PERI_MS_PPU_FX_PASS0_SAR2_CH5_CH | 0x40902940 | 0x00000040 | SAR2, Channel #5 |
| 455 | PERI_MS_PPU_FX_PASS0_SAR2_CH6_CH | 0x40902980 | 0x00000040 | SAR2, Channel #6 |
| 456 | PERI_MS_PPU_FX_PASS0_SAR2_CH7_CH | 0x409029C0 | 0x00000040 | SAR2, Channel #7 |
| 457 | PERI_MS_PPU_FX_PASS0_TOP | 0x409F0000 | 0x00001000 | PASS0 SAR main |

23 Bus masters

The Arbiter (part of flash controller) performs priority-based arbitration based on the master identifier. Each bus master has a dedicated 4-bit master identifier. This master identifier is used for bus arbitration and IPC functionality.

Table 23-1 Bus masters for access and protection control

| ID No. | Master ID | Description |
|--------|--------------------|----------------------------------|
| 0 | CPUSS_MS_ID_CM0 | Master ID for CM0+ |
| 1 | CPUSS_MS_ID_CRYPT0 | Master ID for Crypto |
| 2 | CPUSS_MS_ID_DW0 | Master ID for P-DMA 0 |
| 3 | CPUSS_MS_ID_DW1 | Master ID for P-DMA 1 |
| 4 | CPUSS_MS_ID_DMAC | Master ID for M-DMA0 |
| 14 | CPUSS_MS_ID_CM4 | Master ID for CM4 |
| 15 | CPUSS_MS_ID_TC | Master ID for DAP Tap Controller |

24 Miscellaneous configuration

Table 24-1 Miscellaneous configuration for CYT2B7 devices

| Sl. No. | Configuration | Number/ Instances | Description |
|---------|-------------------------------------|----------------------|---|
| 0 | SRSS_NUM_CLKPATH | 4 | Number of clock paths. One for each of FLL, PLL, Direct and CSV |
| 1 | SRSS_NUM_HFROOT | 3 | Number of CLK_HFs present |
| 2 | PERI_PC_NR | 8 | Number of protection contexts |
| 3 | PERI_CLOCK_NR | 110 | Number of programmable clocks (outputs) |
| 4 | PERI_DIV_8_NR | 32 | Number of divide-by-8 clock dividers |
| 5 | PERI_DIV_16_NR | 16 | Number of divide-by-16 clock dividers |
| 6 | PERI_DIV_24_5_NR | 8 | Number of divide-by-24.5 clock dividers |
| 7 | CPUSS_CM0P_MPU_NR | 8 | Number of MPU regions in CM0+ |
| 8 | CPUSS_CM4_MPU_NR | 8 | Number of MPU regions in CM4 |
| 9 | CPUSS_CRYPT0_BUFF_SIZE | 2048 | Number of 32-bit words in the IP internal memory buffer (to allow for a 256-B, 512-B, 1-KB, 2-KB, 4-KB, 8-KB, 16-KB, and 32-KB memory buffer) |
| 10 | CPUSS_FAULT_FAULT_NR | 4 | Number of fault structures |
| 11 | CPUSS_IPC_IPC_NR | 8 | Number of IPC structures 0 - Reserved for CM0+ access 1 - Reserved for CM4 access 2 - Reserved for DAP access Remaining for user purposes |
| 12 | SCB0_EZ_DATA_NR | 256 | Number of EZ memory bytes. This memory is used in EZ mode, CMD_RESP mode and FIFO mode. Note: Only SCB0 supports EZ mode |
| 13 | CPUSS_PROT_SMPU_STRUCT_NR | 16 | Number of SMPU protection structures |
| 14 | TCPWM_TR_ONE_CNT_NR | 3 | Number of input triggers per counter, routed to one counter |
| 15 | TCPWM_TR_ALL_CNT_NR | 27 | Number of input triggers routed to all counters, based on the pin package |
| 16 | TCPWM_GRP_NR | 3 | Number of TCPWM0 counter groups |
| 17 | TCPWM_GRP_NR0_GRP_GRP_CNT_NR | 63 | Number of counters per TCPWM0 Group #0 |
| 18 | TCPWM_GRP_NR0_CNT_GRP_CNT_WIDTH | 16 | Counter width in number of bits per TCPWM0 Group #0 |
| 19 | TCPWM_GRP_NR1_GRP_GRP_CNT_NR | 12 | Number of counters per TCPWM0 Group #1 |
| 20 | TCPWM_GRP_NR1_CNT_GRP_CNT_WIDTH | 16 | Counter width in number of bits per TCPWM0 Group #1 |
| 21 | TCPWM_GRP_NR2_GRP_GRP_CNT_NR | 4 | Number of counters per TCPWM0 Group #2 |
| 22 | TCPWM_GRP_NR2_CNT_GRP_CNT_WIDTH | 32 | Counter width in number of bits per TCPWM0 Group #2 |
| 23 | CANFD0_MRAM_SIZE / CANFD1_MRAM_SIZE | 24 | Message RAM size in KB shared by all the channels |
| 24 | EVTGEN_COMP_STRUCT_NR | 11 | Number of Event Generator comparator structures |

25 Development support

CYT2B7 has a rich set of documentation, programming tools, and online resources to assist during the development process. Visit www.infineon.com to find out more.

25.1 Documentation

A suite of documentation supports CYT2B7 to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

25.1.1 Software user guide

A step-by-step guide for using the sample driver library along with third-party IDEs such as IAR EWARM and GHS Multi.

25.1.2 Technical reference manual

The Technical Reference Manual (TRM) contains all the technical detail needed to use a CYT2B7 device, including a complete description of all registers. The TRM is available in the documentation section at www.infineon.com.

25.2 Tools

CYT2B7 is supported on third-party development tool ecosystems such as IAR and GHS. CYT2B7 is also supported by Cypress programming utilities for programming, erasing, or reading using Cypress' MiniProg4 or Segger J-link. More details are available in the documentation section at www.infineon.com.

26 Electrical specifications

26.1 Absolute maximum ratings

Use of this device under conditions outside the min and max limits listed in [Table 26-1](#) may cause permanent damage to the device. Exposure to conditions within the limits of [Table 26-1](#) but beyond those of normal operation for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When operated under conditions within the limits of [Table 26-1](#) but beyond those of normal operation, the device may not operate to specification.

Power considerations

The average chip-junction temperature, T_J , in °C, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Equation. 1

Where:

T_A is the ambient temperature in °C.

θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and P_{IO} ($P_D = P_{INT} + P_{IO}$).

P_{INT} is the chip internal power. ($P_{INT} = V_{DDD} \times I_{DD} + V_{DDA} \times I_A$)

P_{IO} represents the power dissipation on input and output pins; user determined.

For most applications, $P_{IO} < P_{INT}$ and may be neglected.

On the other hand, P_{IO} may be significant if the device is configured to continuously drive external modules and/or memories.

Table 26-1 Absolute maximum ratings

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|---|-----------------|-----|---------------------|-------|--|
| SID10 | V_{DDD_ABS} | V_{DDD} power supply voltage ^[35] | $V_{SSD} - 0.3$ | – | $V_{SSD} + 6.0$ | V | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23 |
| SID10B | $V_{DDIO_1_ABS}$ | V_{DDIO_1} power supply voltage ^[35] | $V_{SSD} - 0.3$ | – | $V_{SSD} + 6.0$ | V | $V_{DDIO_1} \geq V_{DDD}$ For ports 6, 7, 8, 9 ^[36] |
| SID10C1 | $V_{DDIO_2_ABS}$ | V_{DDIO_2} power supply voltage ^[35] | $V_{SSD} - 0.3$ | – | $V_{SSD} + 6.0$ | V | For ports 10, 11, 12, 13, 14, 15 |
| SID11 | V_{DDA_ABS} | V_{DDA} analog power supply voltage ^[35] | $V_{SSA} - 0.3$ | – | $V_{SSA} + 6.0$ | V | $V_{DDIO_2} = V_{DDA}$ |
| SID12 | V_{REFH_ABS} | Analog reference voltage, HIGH ^[35] | $V_{SSA} - 0.3$ | – | $V_{SSA} + 6.0$ | V | $V_{REFH} \leq V_{DDA} + 0.3$ V |
| SID12A | V_{REFL_ABS} | Analog reference voltage, LOW ^[35] | $V_{SSA} - 0.3$ | – | $V_{SSA} + 0.3$ | V | |
| SID15A | V_{I0_ABS0} | Input voltage ^[35] | $V_{SSD} - 0.5$ | – | $V_{DDD} + 0.5$ | V | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23 |
| SID15B | V_{I1_ABS1} | Input voltage ^[35] | $V_{SSD} - 0.5$ | – | $V_{DDIO_1} + 0.5$ | V | For ports 6, 7, 8, 9 ^[36] |
| SID15C | V_{I2_ABS2} | Input voltage ^[35] | $V_{SSD} - 0.5$ | – | $V_{DDIO_2} + 0.5$ | V | For ports 10, 11, 12, 13, 14, 15 |
| SID16 | V_{IA_ABS} | Analog input voltage ^[35] | $V_{SSA} - 0.3$ | – | $V_{DDA} + 0.3$ | V | |
| SID17A | V_{O0_ABS0} | Output voltage ^[35] | $V_{SSD} - 0.3$ | – | $V_{DDD} + 0.3$ | | For ports 0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 20, 21, 22, 23 |
| SID17B | V_{O1_ABS1} | Output voltage ^[35] | $V_{SSD} - 0.3$ | – | $V_{DDIO_1} + 0.3$ | V | For ports 6, 7, 8, 9 ^[36] |
| SID17C | V_{O2_ABS2} | Output voltage ^[35] | $V_{SSD} - 0.3$ | – | $V_{DDIO_2} + 0.3$ | V | For ports 10, 11, 12, 13, 14, 15 |

Notes

35. These parameters are based on the condition that $V_{SSD} = V_{SSA} = 0.0$ V.

36. The I/Os in V_{DDIO_1} domain are referred to the V_{DDD} domain in 64-LQFP package.

37. A current-limiting resistor must be provided such that the current at the I/O pin does not exceed rated values at any time, including during power transients. Refer to [Figure 26-1](#) for more information on the recommended circuit.

38. V_{DDIO} and V_{DDD} must be sufficiently loaded or protected to prevent them from being pulled out of the recommended operating range by the clamp current.

39. When the conditions of [42], [43], and SID18A/B/C/D are met, $|I_{CLAMP_ABS}|$ supersedes V_{IA_ABS} and V_{I_ABS} .

40. The definition of “closer” depends on the package. In LQFP packaging, “closest” is determined by counting pins. For example, in a 176-LQFP package, P17.4 (pin 120) is closer to the V_{DDD} on pin 110 than on pin 132. Ports 11 and 21 should not be used for injection currents. The impact of injection currents is only defined for GPIO_STD/GPIO_ENH type I/Os.

Electrical specifications

Table 26-1 Absolute maximum ratings (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------------------|---|------|-----|------|-------|--|
| SID18 | I _{CLAMP_ABS} | Maximum clamp current ^[37, 38, 39] | -5 | - | 5 | mA | |
| SID18A | I _{CLAMP_SUPPLY_POS_ABS} | Maximum positive clamp current per I/O supply pin. Limit applies to I/O supply pin closest to the B+ injected current ^[40] | - | - | 10 | mA | +B injected DC currents are not allowed for Ports 11 and 21. |
| SID18B | I _{CLAMP_SUPPLY_NEG_ABS} | Maximum negative clamp current per I/O ground pin. Limit applies to I/O supply pin closest to the B+ injected current ^[40] | - | - | 10 | mA | +B injected DC currents are not allowed for Ports 11 and 21. |
| SID18C | I _{CLAMP_TOT_POS_ABS} | Maximum positive clamp current per I/O supply, if not limited by the per supply pin (based on SID18A). | - | - | 50 | mA | |
| SID18D | I _{CLAMP_TOT_NEG_ABS} | Maximum negative clamp current per I/O ground, if not limited by the per supply pin (based on SID18B). | - | - | 50 | mA | |
| SID20A | I _{OL1A_ABS} | LOW-level maximum output current ^[41] | - | - | 6 | mA | For GPIO_STD, configured for drive_sel<1:0>= 0b0X |
| SID20B | I _{OL1B_ABS} | LOW-level maximum output current ^[41] | - | - | 2 | mA | For GPIO_STD, configured for drive_sel<1:0>= 0b10 |
| SID20C | I _{OL1C_ABS} | LOW-level maximum output current ^[41] | - | - | 1 | mA | For GPIO_STD, configured for drive_sel<1:0>= 0b11 |
| SID21A | I _{OL2A_ABS} | LOW-level maximum output current ^[41] | - | - | 6 | mA | For GPIO_ENH, configured for drive_sel<1:0>= 0b0X |
| SID21B | I _{OL2B_ABS} | LOW-level maximum output current ^[41] | - | - | 2 | mA | For GPIO_ENH, configured for drive_sel<1:0>= 0b10 |
| SID21C | I _{OL2C_ABS} | LOW-level maximum output current ^[41] | - | - | 1 | mA | For GPIO_ENH, configured for drive_sel<1:0>= 0b11 |
| SID26A | ΣI _{OL_ABS_GPIO} | LOW-level total output current ^[42] | - | - | 50 | mA | |
| SID27A | I _{OH1A_ABS} | HIGH-level maximum output current ^[41] | - | - | -5 | mA | For GPIO_STD, configured for drive_sel<1:0>= 0b0X |
| SID27B | I _{OH1B_ABS} | HIGH-level maximum output current ^[41] | - | - | -2 | mA | For GPIO_STD, configured for drive_sel<1:0>= 0b10 |
| SID27C | I _{OH1C_ABS} | HIGH-level maximum output current ^[41] | - | - | -1 | mA | For GPIO_STD, configured for drive_sel<1:0>= 0b11 |
| SID28A | I _{OH2A_ABS} | HIGH-level maximum output current ^[41] | - | - | -5 | mA | For GPIO_ENH, configured for drive_sel<1:0>= 0b0X |
| SID28B | I _{OH2B_ABS} | HIGH-level maximum output current ^[41] | - | - | -2 | mA | For GPIO_ENH, configured for drive_sel<1:0>= 0b10 |
| SID28C | I _{OH2C_ABS} | HIGH-level maximum output current ^[41] | - | - | -1 | mA | For GPIO_ENH, configured for drive_sel<1:0>= 0b11 |
| SID33A | ΣI _{OH_ABS_GPIO} | HIGH-level total output current ^[42] | - | - | -50 | mA | |
| SID34 | P _D | Power dissipation | - | - | 1000 | mW | T _J should not exceed 150 °C |
| SID35 | T _A | Ambient temperature | -40 | - | 105 | °C | For S-grade devices |
| SID36 | T _A | Ambient temperature | -40 | - | 125 | °C | For E-grade devices |
| SID37 | T _{STG} | Storage temperature | -55 | - | 150 | °C | |
| SID38 | T _J | Operating Junction temperature | -40 | - | 150 | °C | |
| SID39A | V _{ESD_HBM} | Electrostatic discharge human body model | 2000 | - | - | V | |
| SID39B1 | V _{ESD_CDM1} | Electrostatic discharge charged device model for corner pins | 750 | - | - | V | |
| SID39B2 | V _{ESD_CDM2} | Electrostatic discharge charged device model for all other pins | 500 | - | - | V | |
| SID39C | I _{LU} | The maximum pin current the device can tolerate before triggering a latch-up | -100 | - | 100 | mA | |

Notes

41. The maximum output current is the peak current flowing through any one I/O.

42. The total output current is the maximum current flowing through all I/Os (GPIO_STD, and GPIO_ENH).

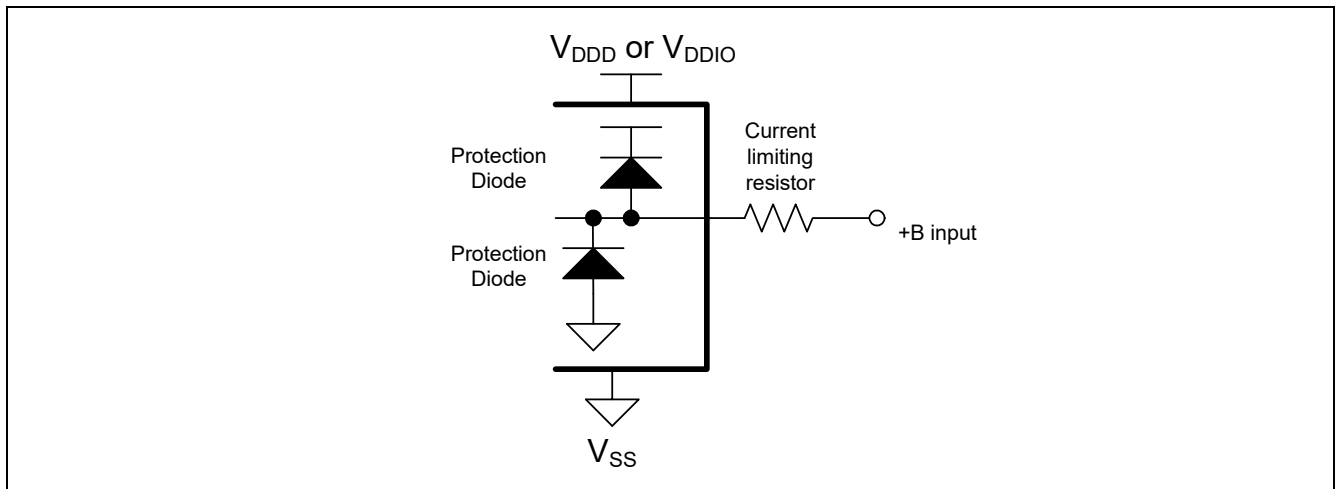


Figure 26-1 Example of a recommended circuit^[43]

WARNING:

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current, or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

26.2 Device-level specifications

Table 26-2 Recommended operating conditions

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---|--|---------------------|-----|---------------------|-------|--------------------|
| SID40 | V_{DDDD} , V_{DDDA} , V_{DDIO_1} , V_{DDIO_2} | Power supply voltage ^[44] | 2.7 ^[45] | – | 5.5 ^[46] | V | |
| SID40A | $V_{DDIO_1_EFP}$ | Power supply voltage for eFuse programming ^[47] | 3 | – | 5.5 | V | |
| SID41 | C_{S1} | Smoothing capacitor ^[48, 49] | 3.76 | – | 11 | μF | |

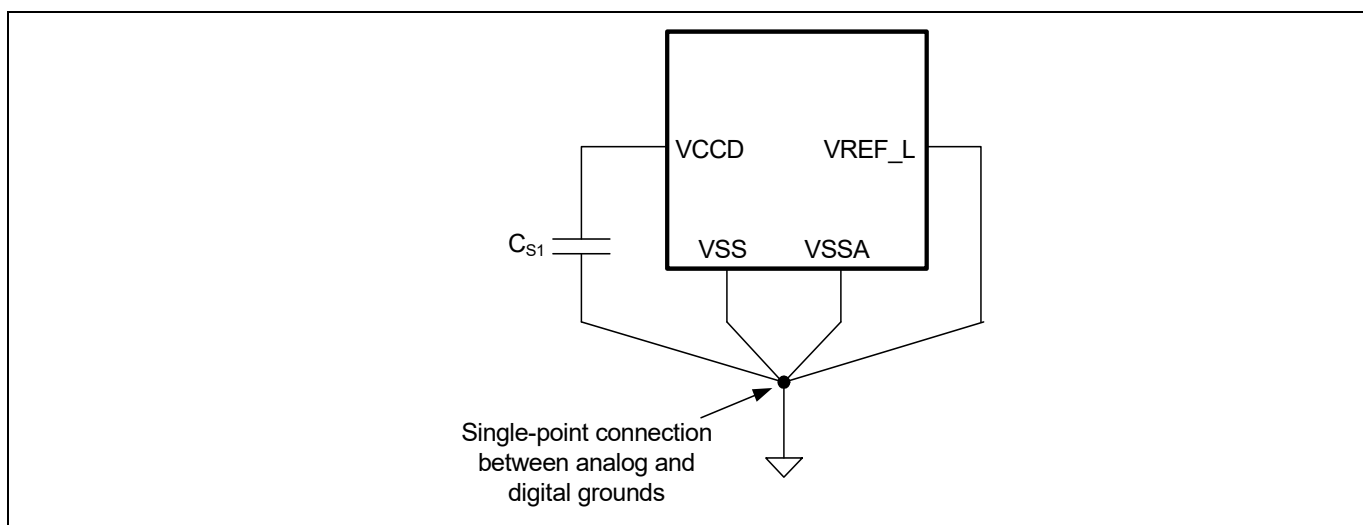


Figure 26-2 Smoothing capacitor

Smoothing capacitor should be placed as close as possible to the V_{CCD} pin.

Notes

43. +B is the positive battery voltage around 45 V.
44. V_{DDDD} , V_{DDIO_1} , V_{DDIO_2} , and V_{DDA} do not have any sequencing limitation and can establish in any order. These supplies (except for V_{DDA} and V_{DDIO_2}) are independent in voltage level. See 12-Bit SAR ADC DC Specifications when using ADC units.
45. 3.0 V $\pm 10\%$ is supported with a lower BOD setting option for V_{DDDD} and V_{DDA} . This setting provides robust protection for internal timing but BOD reset occurs at a voltage below the specified operating conditions. A higher BOD setting option is available (consistent with down to 3.0 V) and guarantees that all operating conditions are met.
46. 5.0 V $\pm 10\%$ is supported with a higher OVD setting option for V_{DDDD} and V_{DDA} . This setting provides robust protection for internal and interface timing, but OVD reset occurs at a voltage above the specified operating conditions. A lower OVD setting option is available (consistent with up to 5.0 V) and guarantees that all operating conditions are met.
47. eFuse programming must be executed with the part in a “quiet” state, with minimal activity (preferably only JTAG or a single LIN/CAN channel on V_{DDDD} domain, no activity on V_{DDIO_1}).
48. Smoothing capacitor, C_{S1} is required per chip (not per V_{CCD} pin). The V_{CCD} pins must be connected together to ensure a low-impedance connection (see the requirement in [Figure 26-2](#)).
49. Capacitors used for power supply decoupling or filtering are operated under a continuous DC-bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device, ensure that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design. While the temperature coefficient is normally found within a parts catalog (such as, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to operate to less than datasheet specifications.

26.3 DC specifications

Table 26-3 DC specifications, CPU current and transition time specifications

All specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|------------------------|---|-----|-----|-----|-------|--|
| SID49C1A | $I_{DD1_CM04_8_1A}$ | LP Active mode (CM4 and CM0+ at 8 MHz, all peripherals are disabled) | – | 4 | 9 | mA | CM0+ and CM4 clocked at 8 MHz with IMO. All peripherals are disabled. No IO toggling. TYP: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT), CM0+ and CM4 executing Dhrystone from flash with cache enabled MAX: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF), CM0+ and CM4 executing Dhrystone from flash with cache enabled. |
| SID49CA | $I_{DD1_CM04_8A}$ | LP Active mode (CM4 and CM0+ at 8 MHz, all peripherals are enabled) | – | 5 | 51 | mA | CM0+ and CM4 clocked at 8 MHz with IMO. All peripherals are enabled. No IO toggling. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. TYP: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT), CM0+ and CM4 executing Dhrystone from flash with cache enabled MAX: $T_A = 125^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF), CM0+ and CM4 executing max_power.c from flash with cache enabled. |
| SID49E1 | $I_{DD1_F160_1M}$ | Active mode (CM4 at 160 MHz, CM0+ at 80 MHz, all peripherals are enabled) | – | 39 | 102 | mA | PLL enabled at 160 MHz with ECO reference. All peripherals are enabled. No I/O toggling. M-DMA transferring data from code + work flash, P-DMA chains with maximum trigger activity. TYP: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT), CM4 and CM0+ executing Dhrystone from flash with cache enabled. MAX: $T_A = 125^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF), CM4 and CM0+ executing max_power.c from flash with cache enabled |
| SID53A1 | $I_{DD2_8_1}$ | All CPUs in Sleep mode | – | 3 | 46 | mA | PLL disabled, CM4 and CM0+ are sleeping at 8 MHz with IMO. All peripherals, peripheral clocks, interrupts, CSV, DMA, FLL, ECO are disabled. No I/O toggling. Typ: $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $T_A = 125^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF) |

Note

50. At cold temperature -5°C to -40°C , the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 μs .

Table 26-3 DC specifications, CPU current and transition time specifications (continued)

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------------------|-----------------|--|-----|-----|-----|---------------|--|
| SID56A | I_{DD_CWU2} | Average current for cyclic wake-up operation This is the average current for the specified LP Active mode and DeepSleep mode (RTC, WDT, and Event generator operating). | – | 46 | 136 | μA | $V_{DD} = 5.5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, 64-KB SRAM, ILO0 operation in DeepSleep, Smart IO operations with ILO0, CM0+, CM4: Retained TYP: process typ (TT) MAX: process worst (FF) This average current is achieved under the following conditions. 1. MCU repetitively goes from DeepSleep to LP Active with a period of 32 ms. 2. One of the I/Os is toggled using Smart I/O to activate an external sensor connected to an analog input of A/D in DeepSleep 3. After 200 μs delay, the CM4 wakes up by event generator trigger to LP Active mode with IMO and A/D conversion is triggered by software. 4. Group A/D conversion is performed on 5 channels with the sampling time of 1 μs each. 5. Once the group A/D conversion is finished, and the results fit in the window of the range comparator, the I/O is toggled back by software to de-activate the sensor and the CM4 goes back to DeepSleep. |
| SID59A | I_{DD_DS64B} | 64-KB SRAM retention, ILO0 operation in DeepSleep mode | – | 35 | 130 | μA | DeepSleep Mode (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), $T_A = 25\text{ }^{\circ}\text{C}$, CM0+, CM4: Retained Typ: $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $V_{DD} = 5.5\text{ V}$, process worst (FF) |
| SID61A | I_{DD_DS64D} | 64-KB SRAM retention, ILO0 operation in DeepSleep mode | – | 0.9 | 3.5 | mA | DeepSleep Mode steady state at $T_A = 125\text{ }^{\circ}\text{C}$ (RTC, WDT, and event generator operating, all other peripherals are off except for retention registers), CM0+, CM4: Retained Typ: $V_{DD} = 5.0\text{ V}$, process typ (TT) Max: $V_{DD} = 5.5\text{ V}$, process worst (FF) |
| Hibernate Mode | | | | | | | |
| SID62 | I_{DD_HIB1} | Hibernate Mode | – | 5 | – | μA | ILO0/WDT operating. All other peripherals, and all CPUs are off. $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process typ (TT) |
| SID62A | I_{DD_HIB2} | Hibernate Mode | – | – | 130 | μA | ILO0/WDT operating. All other peripherals, and all CPUs are off. $T_A = 125\text{ }^{\circ}\text{C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF) |
| Power mode transition times | | | | | | | |
| SID65 | t_{ACT_DS} | Power down time from Active to DeepSleep | – | – | 2.5 | μs | When the IMO is already running and all HFCLK roots are at least 8 MHz. HFCLK roots that are slower than this will require additional time to turn off. |

Electrical specifications

Table 26-3 DC specifications, CPU current and transition time specifications (continued)

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------------|---|-----|-----|----------------------|-------|--|
| SID63 | t_{DS_ACT} | DeepSleep to Active transition time (IMO clock, SRAM execution) | – | – | 10 ^[50] | μs | When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until wakeup. |
| SID63C | t_{DS_ACT} | DeepSleep to Active transition time (IMO clock, flash execution) | – | – | 20 ^[50] | μs | When using the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution. |
| SID63A | $t_{DS_ACT_FLL}$ | DeepSleep to Active transition time (FLL clock, SRAM execution) | – | – | 15 ^[50] | μs | When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the FLL locks. |
| SID63D | $t_{DS_ACT_FLL1}$ | DeepSleep to Active transition time (FLL clock, flash execution) | – | – | 21.5 ^[50] | μs | When using the FLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until flash execution. |
| SID63B | $t_{DS_ACT_PLL}$ | DeepSleep to Active transition time (PLL clock, SRAM or flash execution) | – | – | 60 ^[50] | μs | When using the PLL to generate 96 MHz from the 8-MHz IMO. Measured from wakeup interrupt during DeepSleep until the PLL locks. |
| SID68 | t_{HVR_ACT} | Release time from HV reset (POR, BOD, OVD, OCD, WDT, Hibernate wakeup, or XRES_L) release until CM0+ begins executing ROM boot | – | – | 265 | μs | Without boot runtime. Guaranteed by design |
| SID68A | t_{LVR_ACT} | Release time from LV reset (Fault, Internal system reset, MCWDT, or CSV) during Active/Sleep until CM0+ begins executing ROM boot | – | – | 10 | μs | Without boot runtime. Guaranteed by design |
| SID68B | t_{LVR_DS} | Release time from LV reset (Fault, or MCWDT) during DeepSleep until CM0+ begins executing ROM boot | – | – | 15 | μs | Without boot runtime. Guaranteed by design |
| SID80A | t_{RB_N} | ROM boot startup time or wakeup time from hibernate in NORMAL protection state | – | – | 1800 | μs | Guaranteed by Design, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later) |
| SID80B | t_{RB_S} | ROM boot startup time or wakeup time from hibernate in SECURE protection state | – | – | 2740 | μs | Guaranteed by Design, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later) |
| SID81A | t_{FB} | Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state | – | – | 80 | μs | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later), Listen window = 0 ms |

Table 26-3 DC specifications, CPU current and transition time specifications (continued)

All specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|-----------------------|---|-----|-----|-------|---------------|---|
| SID81B | $t_{\text{FB_A}}$ | Flash boot with app authentication time in NORMAL/SECURE protection state | – | – | 5000 | μs | Guaranteed by Design, TOC2_FLAGS=0x24F, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later), Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA2K. |
| SID80A_2 | $t_{\text{RB_N_2}}$ | ROM boot startup time or wakeup time from hibernate in NORMAL protection state | – | – | 2930 | μs | Guaranteed by Design, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.556) |
| SID80B_2 | $t_{\text{RB_S_2}}$ | ROM boot startup time or wakeup time from hibernate in SECURE protection state | – | – | 4680 | μs | Guaranteed by Design, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.556) |
| SID81A_2 | $t_{\text{FB_2}}$ | Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state | – | – | 200 | μs | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.556), Listen window = 0 ms |
| SID81B_2 | $t_{\text{FB_A_2}}$ | Flash boot with app authentication time in NORMAL/SECURE protection state | – | – | 10000 | μs | Guaranteed by Design, TOC2_FLAGS=0x24F, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.556), Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA2K. |

Regulator specifications

| | | | | | | | |
|--------|------------------------|--|------|-----|------|---------------|--|
| SID600 | V_{CCD} | Core supply voltage | 1.05 | 1.1 | 1.15 | V | |
| SID601 | $I_{\text{DD_ACT}}$ | Regulator operating current in Active/Sleep mode | – | 80 | 150 | μA | Guaranteed by design |
| SID602 | $I_{\text{DD_DPSLP}}$ | Regulator operating current in DeepSleep mode | – | 1.5 | 20 | μA | Guaranteed by design |
| SID604 | I_{OUT} | Available regulator output current for operation | – | – | 150 | mA | Without triggering OVD |
| SID603 | I_{RUSH} | In-rush current | – | – | 375 | mA | Average V_{DD} current until C_{S1} (connected to V_{CCD} pin) is charged after Active regulator is turned on |

26.4 Reset specifications

All specifications are valid for $-40\text{ °C} \leq T_A \leq 125\text{ °C}$ and for 2.7 V to 5.5 V except where noted.

Table 26-4 XRES_L reset

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------------------------|-----------------|--|----------------------|-----|---------------------|-------|---|
| XRES_L DC specifications | | | | | | | |
| SID73 | I_{DD_XRES} | I_{DD} when XRES_L asserted | – | – | 0.9 | mA | $T_A = 125\text{ °C}$, $V_{DD} = 5.5\text{ V}$, process worst (FF) |
| SID74 | V_{IH} | Input voltage HIGH threshold | $0.7 \times V_{DD}$ | – | – | V | CMOS input |
| SID75 | V_{IL} | Input voltage LOW threshold | – | – | $0.3 \times V_{DD}$ | V | CMOS input |
| SID76 | R_{PULLUP} | Pull-up resistor | 7 | – | 20 | kΩ | |
| SID77 | C_{IN} | Input capacitance | – | – | 5 | pF | |
| SID78 | $V_{HYSXRES}$ | Input voltage hysteresis | $0.05 \times V_{DD}$ | – | – | V | |
| XRES_L AC specifications | | | | | | | |
| SID70 | t_{XRES_ACT} | XRES_L release to Active transition time | – | – | 265 | μs | Without boot runtime. Guaranteed by design |
| SID71 | t_{XRES_PW} | XRES_L pulse width | 5 | – | – | μs | |
| SID72 | t_{XRES_FT} | Pulse suppression width | 100 | – | – | ns | |

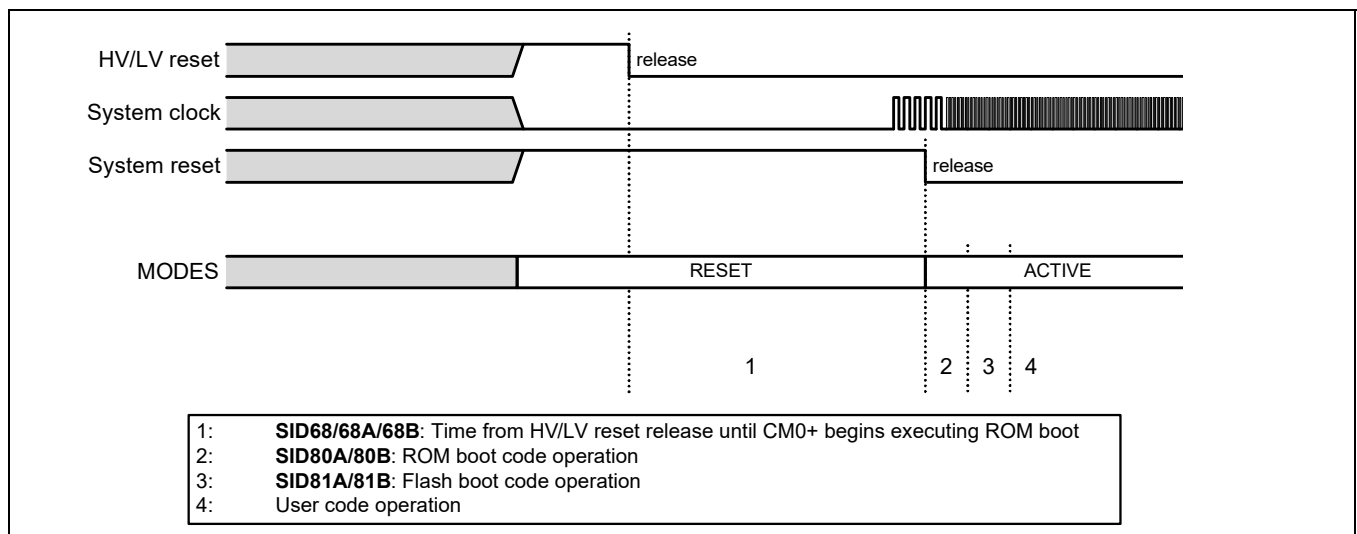


Figure 26-3 Reset sequence

26.5 I/O

All specifications are valid for $-40\text{ °C} \leq T_A \leq 125\text{ °C}$ and for 2.7 V to 5.5 V except where noted.

Table 26-5 I/O specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|----------------------------|---------------------------|--|-----|-----|-------|---|
| GPIO_STD Specifications for ports P1 through P23 | | | | | | | |
| SID650 | V _{OL1_GPIO_STD} | Output voltage LOW level | – | – | 0.6 | V | I _{OL} = 6 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID650C | V _{OL1C_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID651 | V _{OL2_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 2 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID652 | V _{OL3_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID652C | V _{OL3C_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID653 | V _{OL4_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID653C | V _{OL4C_GPIO_STD} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID654 | V _{OH1_GPIO_STD} | Output voltage HIGH level | (V _{DD} or V _{DDIO_1} or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –2 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID655 | V _{OH2_GPIO_STD} | Output voltage HIGH level | (V _{DD} or V _{DDIO_1} or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID656 | V _{OH3_GPIO_STD} | Output voltage HIGH level | (V _{DD} or V _{DDIO_1} or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID656C | V _{OH3C_GPIO_STD} | Output voltage HIGH level | (V _{DD} or V _{DDIO_1} or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID657 | V _{OH4_GPIO_STD} | Output voltage HIGH level | (V _{DD} or V _{DDIO_1} or V _{DDIO_2}) – 0.5 | – | – | V | I _{OH} = –0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |

Table 26-5 I/O specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------------------------|---|--|------|---|-------|--|
| SID657C | V _{OH4C_GPIO_STD} | Output voltage HIGH level | (V _{DDD} or V _{DDIO_1} or V _{DDIO_2}) - 0.5 | – | – | V | I _{OH} = –1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V _{DDD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID658 | R _{PD_GPIO_STD} | Pull-down resistance | 25 | 50 | 100 | kΩ | |
| SID659 | R _{PU_GPIO_STD} | Pull-up resistance | 25 | 50 | 100 | kΩ | |
| SID660 | V _{IH_CMOS_GPIO_STD} | Input voltage HIGH threshold in CMOS mode | 0.7 × (V _{DDD} or V _{DDIO_1} or V _{DDIO_2}) | – | – | V | |
| SID661 | V _{IH_TTL_GPIO_STD} | Input voltage HIGH threshold in TTL mode | 2.0 | – | – | V | |
| SID662 | V _{IH_AUTO_GPIO_STD} | Input voltage HIGH threshold in AUTO mode | 0.8 × (V _{DDD} or V _{DDIO_1} or V _{DDIO_2}) | – | – | V | |
| SID663 | V _{IL_CMOS_GPIO_STD} | Input voltage LOW threshold in CMOS mode | – | – | 0.3 × (V _{DDD} or V _{DDIO_1} or V _{DDIO_2}) | V | |
| SID664 | V _{IL_TTL_GPIO_STD} | Input voltage LOW threshold in TTL mode | – | – | 0.8 | V | |
| SID665 | V _{IL_AUTO_GPIO_STD} | Input voltage LOW threshold in AUTO mode | – | – | 0.5 × (V _{DDD} or V _{DDIO_1} or V _{DDIO_2}) | V | |
| SID666 | V _{HYST_CMOS_GPIO_STD} | Hysteresis in CMOS mode | 0.05 × (V _{DDD} or V _{DDIO_1} or V _{DDIO_2}) | – | – | V | |
| SID668 | V _{HYST_AUTO_GPIO_STD} | Hysteresis in AUTO mode | 0.05 × (V _{DDD} or V _{DDIO_1} or V _{DDIO_2}) | – | – | V | |
| SID669 | C _{in_GPIO_STD} | Input pin capacitance | – | – | 5 | pF | For 10 MHz and 100 MHz |
| SID670 | I _{IL_GPIO_STD} | Input leakage current | –250 | 0.02 | 250 | nA | For GPIO_STD except P21.0, P21.1, P21.2, P21.3, P21.4, P23.3, P23.4. V _{DDIO_1} = V _{DDIO_2} = V _{DDD} = V _{DDA} = 5.5 V, V _{SSD} < V _I < V _{DDD} , V _{DDIO_1} , V _{DDIO_2} –40 °C ≤ T _A ≤ 125 °C TYP: T _A = 25 °C, V _{DDIO_1} = V _{DDIO_2} = V _{DDD} = V _{DDA} = 5.0 V |

Table 26-5 I/O specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--|--|------|------|-----|-------|---|
| SID670C | $I_{IL_GPIO_STD_B}$ | Input leakage current | -700 | 0.02 | 700 | nA | Only for P21.0, P21.1, P21.2, P21.3, P21.4, P23.3, P23.4. $V_{DDIO_1} = V_{DDIO_2} = V_{DDD} = V_{DDA} = 5.5\text{ V}$, $V_{SSD} < V_I < V_{DDD}$, V_{DDIO_1} , V_{DDIO_2} $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ TYP: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DDIO_1} = V_{DDIO_2} = V_{DDD} = V_{DDA} = 5.0\text{ V}$ |
| SID671 | t_R or t_F (fast) _{20_0_GPIO-STD} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | - | 10 | ns | 20-pF load, drive_sel<1:0> = 0b00 |
| SID672 | t_R or t_F (fast) _{50_0_GPIO-STD} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | - | 20 | ns | 50-pF load, drive_sel<1:0> = 0b00 |
| SID673 | t_R or t_F (fast) _{20_1_GPIO-STD} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | - | 20 | ns | 20-pF load, drive_sel<1:0> = 0b01, guaranteed by design |
| SID674 | t_R or t_F (fast) _{10_2_GPIO-STD} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | - | 20 | ns | 10-pF load, drive_sel<1:0> = 0b10, guaranteed by design |
| SID675 | t_R or t_F (fast) _{6_3_GPIO-STD} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | - | 20 | ns | 6-pF load, drive_sel<1:0> = 0b11, guaranteed by design |
| SID676 | t_F (fast) _{100_GPIO-STD} | Fall time (30% to 70% of V_{DDIO}) | 0.35 | - | 250 | ns | 10-pF to 400-pF load, RPU = 767 Ω , drive_sel<1:0> = 0b00, Freq = 100 kHz |
| SID677 | t_F (fast) _{400_GPIO-STD} | Fall time (30% to 70% of V_{DDIO}) | 0.35 | - | 250 | ns | 10-pF to 400-pF load, RPU = 350 Ω , drive_sel<1:0> = 0b00, Freq = 400 kHz |
| SID678 | $f_{IN_GPIO_STD}$ | Input frequency | - | - | 100 | MHz | |
| SID679 | $f_{OUT_GPIO_STD0H}$ | Output frequency | - | - | 50 | MHz | 20-pF load, drive_sel<1:0> = 00, $4.5\text{ V} \leq V_{DDD}$ or V_{DDIO_1} or $V_{DDIO_2} \leq 5.5\text{ V}$ |
| SID680 | $f_{OUT_GPIO_STD0L}$ | Output frequency | - | - | 32 | MHz | 20-pF load, drive_sel<1:0> = 00, $2.7\text{ V} \leq V_{DDD}$ or V_{DDIO_1} or $V_{DDIO_2} < 4.5\text{ V}$ |
| SID681 | $f_{OUT_GPIO_STD1H}$ | Output frequency | - | - | 25 | MHz | 20-pF load, drive_sel<1:0> = 01, $4.5\text{ V} \leq V_{DDD}$ or V_{DDIO_1} or $V_{DDIO_2} \leq 5.5\text{ V}$ |

Table 26-5 I/O specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|-----------------------------|------------------------------|-----------------------|-----|-----|-------|--|
| SID682 | f _{OUT_GPIO_STD1L} | Output frequency | – | – | 15 | MHz | 20-pF load, drive_sel<1:0>= 01, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID683 | f _{OUT_GPIO_STD2H} | Output frequency | – | – | 25 | MHz | 10-pF load, drive_sel<1:0>= 10, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID684 | f _{OUT_GPIO_STD2L} | Output frequency | – | – | 15 | MHz | 10-pF load, drive_sel<1:0>= 10, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| SID685 | f _{OUT_GPIO_STD3H} | Output frequency | – | – | 15 | MHz | 6-pF load, drive_sel<1:0>= 11, 4.5 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} ≤ 5.5 V |
| SID686 | f _{OUT_GPIO_STD3L} | Output frequency | – | – | 10 | MHz | 6-pF load, drive_sel<1:0>= 11, 2.7 V ≤ V _{DD} or V _{DDIO_1} or V _{DDIO_2} < 4.5 V |
| GPIO_ENH specifications only for P0 | | | | | | | |
| SID650A | V _{OL1_GPIO_ENH} | Output voltage LOW level | – | – | 0.6 | V | I _{OL} = 6 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V _{DD} ≤ 5.5 V |
| SID650D | V _{OL1D_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DD} ≤ 5.5 V |
| SID651A | V _{OL2_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 2 mA, 3 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V _{DD} < 4.5 V |
| SID652A | V _{OL3_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V _{DD} < 4.5 V |
| SID652D | V _{OL3D_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V _{DD} ≤ 5.5 V |
| SID653A | V _{OL4_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V _{DD} < 4.5 V |
| SID653D | V _{OL4D_GPIO_ENH} | Output voltage LOW level | – | – | 0.4 | V | I _{OL} = 1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V _{DD} ≤ 5.5 V |
| SID654A | V _{OH1_GPIO_ENH} | Output voltage HIGH level | V _{DD} – 0.5 | – | – | V | I _{OL} = –2 mA drive_sel<1:0> = 0b0X, 2.7 V ≤ V _{DD} < 4.5 V |
| SID655A | V _{OH2_GPIO_ENH} | Output voltage HIGH level | V _{DD} – 0.5 | – | – | V | I _{OL} = –5 mA drive_sel<1:0> = 0b0X, 4.5 V ≤ V _{DD} ≤ 5.5 V |

Table 26-5 I/O specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---|---|-------------------------|-------|------------------------|-------|---|
| SID656A | V _{OH3_GPIO_ENH} | Output voltage HIGH level | V _{DDD} - 0.5 | – | – | V | I _{OL} = -1 mA drive_sel<1:0> = 0b10, 2.7 V ≤ V _{DDD} < 4.5 V |
| SID656D | V _{OH3D_GPIO_ENH} | Output voltage HIGH level | V _{DDD} - 0.5 | – | – | V | I _{OL} = -2 mA drive_sel<1:0> = 0b10, 4.5 V ≤ V _{DDD} ≤ 5.5 V |
| SID657A | V _{OH4_GPIO_ENH} | Output voltage HIGH level | V _{DDD} - 0.5 | – | – | V | I _{OL} = -0.5 mA drive_sel<1:0> = 0b11, 2.7 V ≤ V _{DDD} < 4.5 V |
| SID657D | V _{OH4D_GPIO_ENH} | Output voltage HIGH level | V _{DDD} - 0.5 | – | – | V | I _{OL} = -1 mA drive_sel<1:0> = 0b11, 4.5 V ≤ V _{DDD} ≤ 5.5 V |
| SID658A | R _{PD_GPIO_ENH} | Pull-down resistance | 25 | 50 | 100 | kΩ | |
| SID659A | R _{PU_GPIO_ENH} | Pull-up resistance | 25 | 50 | 100 | kΩ | |
| SID660A | V _{IH_CMOS_GPI-O_ENH} | Input voltage HIGH threshold in CMOS mode | 0.7 × V _{DDD} | – | – | V | |
| SID661A | V _{IH_TTL_GPIO_ENH} | Input voltage HIGH threshold in TTL mode | 2 | – | – | V | |
| SID662A | V _{IH_AUTO_GPI-O_ENH} | Input voltage HIGH threshold in AUTO mode | 0.8 × V _{DDD} | – | – | V | |
| SID663A | V _{IL_CMOS_GPIO_ENH} | Input voltage LOW threshold in CMOS mode | – | – | 0.3 × V _{DDD} | V | |
| SID664A | V _{IL_TTL_GPIO_ENH} | Input voltage LOW threshold in TTL mode | – | – | 0.8 | V | |
| SID665A | V _{IL_AUTO_GPIO_ENH} | Input voltage LOW threshold in AUTO mode | – | – | 0.5 × V _{DDD} | V | |
| SID666A | V _{HYST_CMOS_GPI-O_ENH} | Hysteresis in CMOS mode | 0.05 × V _{DDD} | – | – | V | |
| SID668A | V _{HYST_AUTO_GPI-O_ENH} | Hysteresis in AUTO mode | 0.05 × V _{DDD} | – | – | V | |
| SID669A | C _{in_GPIO_ENH} | Input pin capacitance | – | – | 5 | pF | For 10 MHz and 100 MHz |
| SID670A | I _{IL_GPIO_ENH} | Input leakage current | -350 | 0.055 | 350 | nA | V _{DDD} = V _{DDA} = 5.5 V, V _{SSD} < V _I < V _{DDD} , -40 °C ≤ T _A ≤ 125 °C TYP: T _A = 25 °C, V _{DDD} = V _{DDA} = 5.0 V |
| SID671A | t _R or t _F (fast) _{20_0_GPI-O_ENH} | Rise time or fall time (10% to 90% of V _{DDIO}) | 1 | – | 10 | ns | 20-pF load, drive_sel<1:0> = 0b00, slow = 0 |
| SID672A | t _R or t _F (fast) _{50_0_GPI-O_ENH} | Rise time or fall time (10% to 90% of V _{DDIO}) | 1 | – | 20 | ns | 50-pF load, drive_sel<1:0> = 0b00, slow = 0 |

Table 26-5 I/O specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--|--|----------------------------|-----|-----|-------|--|
| SID673A | t_R or t_F (fast) _{_20_1_GPI-O_ENH} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | – | 20 | ns | 20-pF load, drive_sel<1:0> = 0b01, slow = 0, guaranteed by design |
| SID674A | t_R or t_F (fast) _{_10_2_GPI-O_ENH} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | – | 20 | ns | 10-pF load, drive_sel<1:0> = 0b10, slow = 0, guaranteed by design |
| SID675A | t_R or t_F (fast) _{_6_3_GPI-O_ENH} | Rise time or fall time (10% to 90% of V_{DDIO}) | 1 | – | 20 | ns | 6-pF load, drive_sel<1:0> = 0b11, slow = 0, guaranteed by design |
| SID676A | t_{F_I2C} (slow) _{_GPIO_ENH} | Fall time (30% to 70% of V_{DDIO}) | $20 \times (V_{DD} / 5.5)$ | – | 250 | ns | 10-pF to 400-pF load, drive_sel<1:0> = 0b00, slow = 1, minimum $R_{PU} = 400 \Omega$ |
| SID677A | t_R or t_F (slow) _{_20_GPI-O_ENH} | Rise time or fall time (10% to 90% of V_{DDIO}) | $20 \times (V_{DD} / 5.5)$ | – | 160 | ns | 20-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 1 MHz |
| SID678A | t_R or t_F (slow) _{_400_GPI-O_ENH} | Rise time or fall time (10% to 90% of V_{DDIO}) | $20 \times (V_{DD} / 5.5)$ | – | 250 | ns | 400-pF load, drive_sel<1:0> = 0b00, slow = 1, output frequency = 400 kHz |
| SID679A | $f_{IN_GPIO_ENH}$ | Input frequency | – | – | 100 | MHz | |
| SID680A | $f_{OUT_GPIO_ENH0H}$ | Output frequency | – | – | 50 | MHz | 20-pF load, drive_sel<1:0> = 0b00, $4.5 V \leq V_{DD} \leq 5.5 V$ |
| SID681A | $f_{OUT_GPIO_ENH0L}$ | Output frequency | – | – | 32 | MHz | 20-pF load, drive_sel<1:0> = 0b00, $2.7 V \leq V_{DD} < 4.5 V$ |
| SID682A | $f_{OUT_GPIO_ENH1H}$ | Output frequency | – | – | 25 | MHz | 20-pF load, drive_sel<1:0> = 0b01, $4.5 V \leq V_{DD} \leq 5.5 V$ |
| SID683A | $f_{OUT_GPIO_ENH1L}$ | Output frequency | – | – | 15 | MHz | 20-pF load, drive_sel<1:0> = 0b01, $2.7 V \leq V_{DD} < 4.5 V$ |
| SID684A | $f_{OUT_GPIO_ENH2H}$ | Output frequency | – | – | 25 | MHz | 10-pF load, drive_sel<1:0> = 0b10, $4.5 V \leq V_{DD} \leq 5.5 V$ |
| SID685A | $f_{OUT_GPIO_ENH2L}$ | Output frequency | – | – | 15 | MHz | 10-pF load, drive_sel<1:0> = 0b10, $2.7 V \leq V_{DD} < 4.5 V$ |

Table 26-5 I/O specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------------|------------------|-----|-----|-----|-------|--|
| SID686A | f _{OUT_GPIO_ENH3H} | Output frequency | – | – | 15 | MHz | 6-pF load, drive_sel<1:0>= 0b11, 4.5 V ≤ V _{DD} ≤ 5.5 V |
| SID687A | f _{OUT_GPIO_ENH3L} | Output frequency | – | – | 10 | MHz | 6-pF load, drive_sel<1:0>= 0b11, 2.7 V ≤ V _{DD} < 4.5 V |

GPIO input specifications

| | | | | | | | |
|-------|------------------|--|-----|---|--------------------|----|---------------------------|
| SID98 | t _{FT} | Analog glitch filter (pulse suppression width) | – | – | 50 ^[51] | ns | One filter per port group |
| SID99 | t _{INT} | Minimum pulse width for GPIO interrupt | 160 | – | – | ns | |

Note

51. If longer pulse suppression width is required, use Smart I/O.

26.6 Analog peripherals

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

26.6.1 SAR ADC

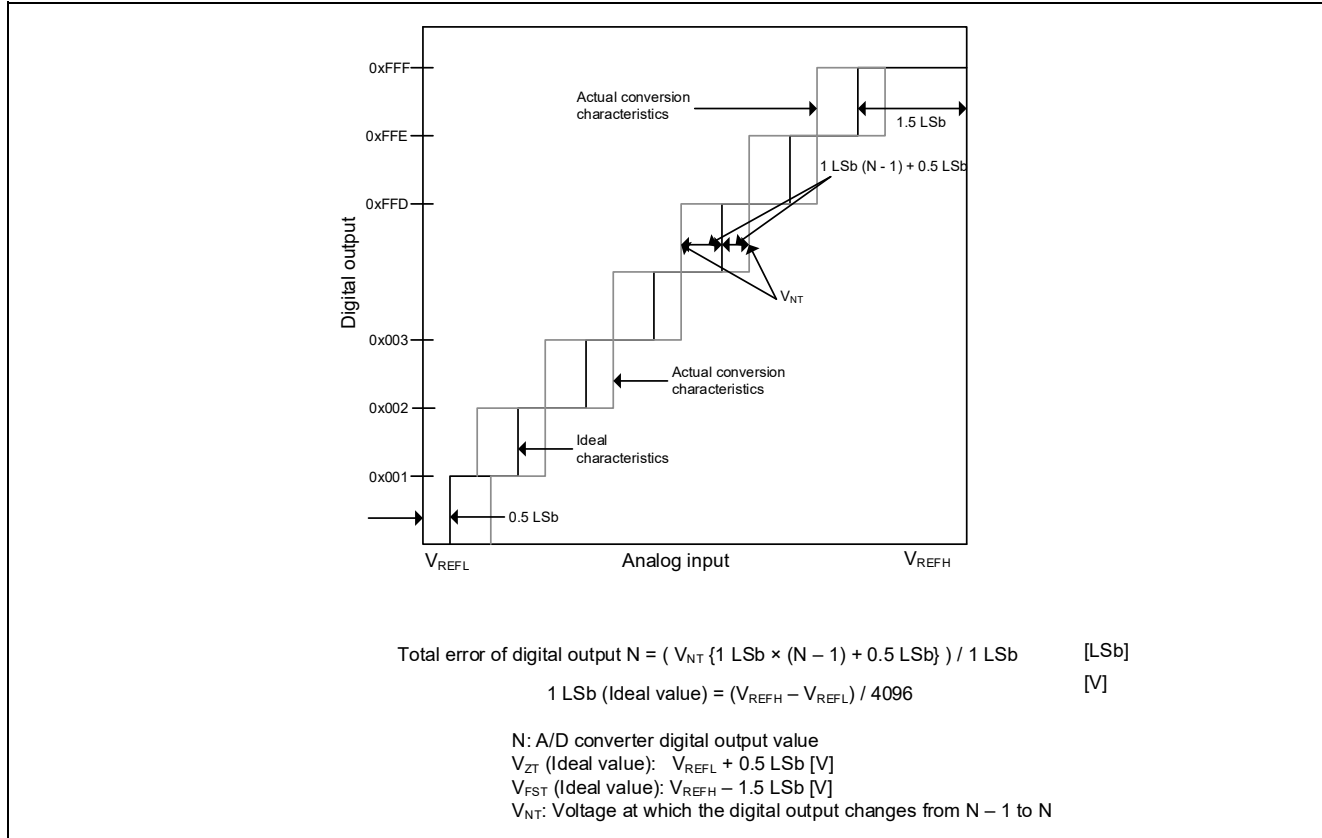


Figure 26-4 ADC characteristics and error definitions

Table 26-6 12-Bit SAR ADC DC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------------------|---|-------------------|-----|-------------------|-------|--|
| SID100 | A_RES | SAR ADC resolution | – | – | 12 | bits | |
| SID101 | A_V _{INS} | Input voltage range | V _{REFL} | – | V _{REFH} | V | |
| SID102 | A_V _{REFH} | V _{REFH} voltage range | 2.7 | – | V _{DDA} | V | ADC performance degrades when high reference is higher than supply |
| SID102A | A_V _{DDA} ^[52] | V _{DDA} voltage range | 2.7 | – | 5.5 | V | |
| SID103 | A_V _{REFL} | V _{REFL} voltage range | V _{SSA} | – | V _{SSA} | V | ADC performance degrades when low reference is lower than ground |
| SID103A | V _{band_gap} | Internal band gap reference voltage | 0.882 | 0.9 | 0.918 | V | |
| SID19A | CLAMP_COU-PLING_RATIO_POS | Ratio of current collected on a pin to the positive current injected into a neighboring pin | – | – | 0.25 | % | |
| SID19B | CLAMP_COU-PLING_RATIO_NEG | Ratio of current collected on a pin to the negative current injected into a neighboring pin | – | – | 1.2 | % | |
| SID19C | R _{CLAMP_INTERNAL} | Internal pin resistance to current collection point | – | – | 50 | Ω | |

26.6.2 Calculating the impact of neighboring pins

The three ADC specifications based on SID19A, SID19B, and SID19C, can be used to calculate the pin leakage and resulting ADC offset caused by injection current using the below formula:

$$I_{\text{LEAK}} = I_{\text{INJECTED}} \times \text{CLAMP_COUPLING_RATIO}$$

$$V_{\text{ERROR}} = I_{\text{LEAK}} \times (R_{\text{CLAMP_INTERNAL}} + R_{\text{SOURCE}})$$

$$\text{Code Error} = V_{\text{ERROR}} \times 2^{12} / V_{\text{REF}}$$

Where:

I_{INJECTED} is the injected current in mA.

I_{LEAK} is the calculated leakage current in mA.

V_{ERROR} is the voltage error calculated due to leakage currents in V.

V_{REF} is the ADC reference voltage in V.

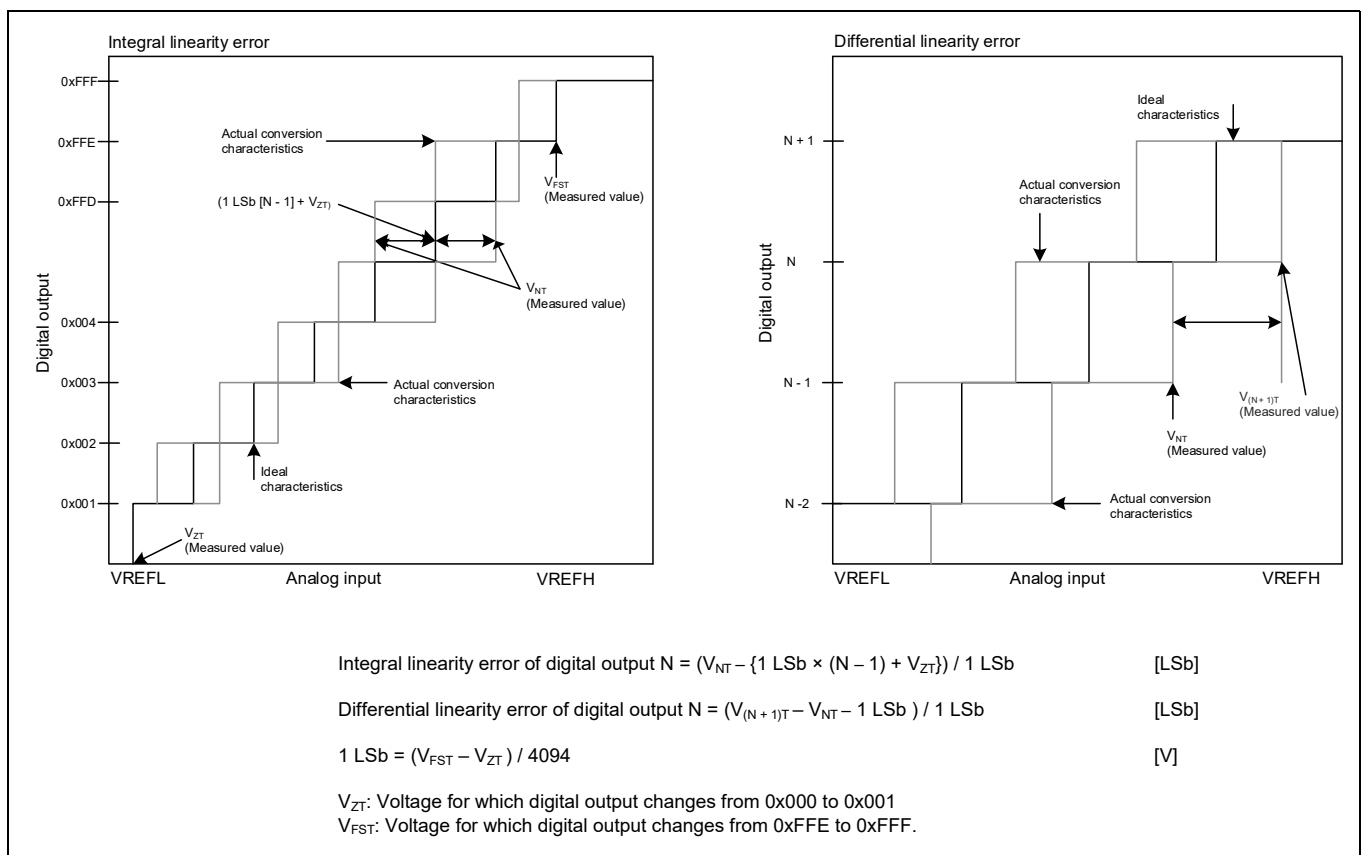


Figure 26-5 Integral and differential linearity errors

Note

52. V_{DD} must be greater than $0.8 \times V_{\text{DDA}}$ when ADC[2] is enabled. V_{DDIO_1} must be greater than $0.8 \times V_{\text{DDA}}$ when ADC[0] is enabled.

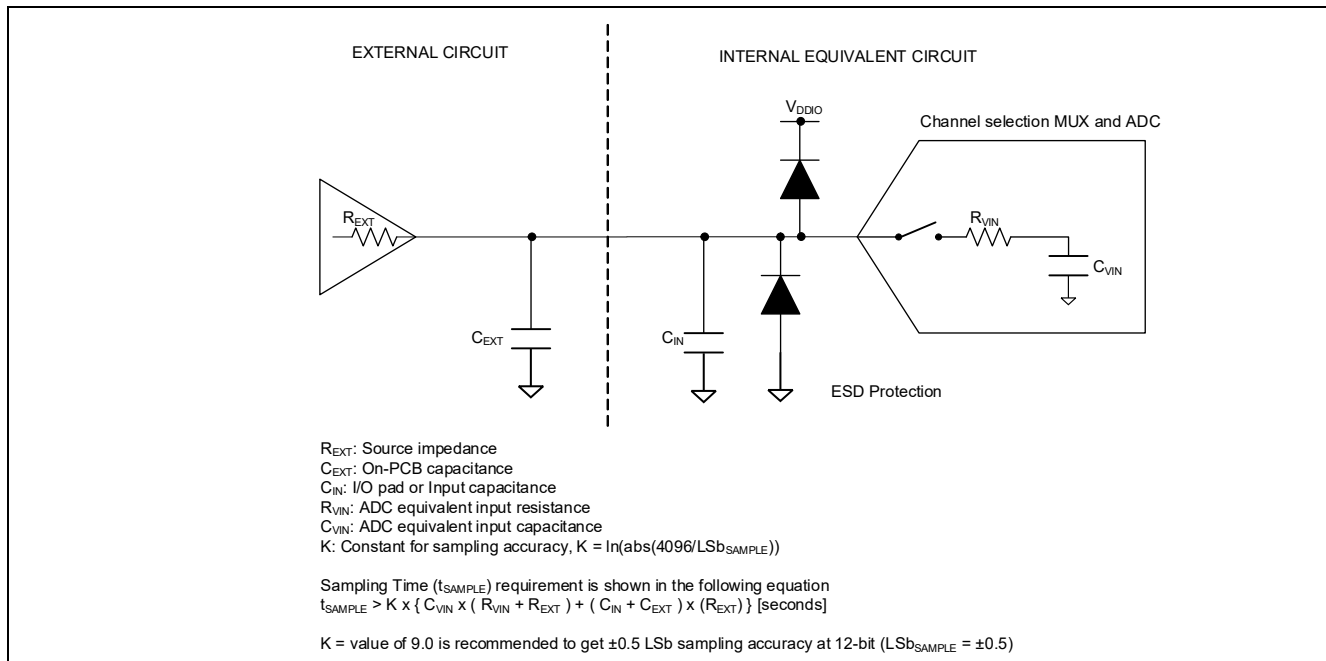


Figure 26-6 ADC equivalent circuit for analog input

Table 26-7 SAR ADC AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------------|--|-----|-----|-------|---------------|---|
| SID104 | V_{ZT} | Zero transition voltage | -20 | - | 20 | mV | $V_{DDA} = 2.7 \text{ V to } 5.5 \text{ V}$, $-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C}$ before offset adjustment |
| SID105 | V_{FST} | Full-scale transition voltage | -20 | - | 20 | mV | $V_{DDA} = 2.7 \text{ V to } 5.5 \text{ V}$, $-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C}$ before offset adjustment |
| SID114 | $f_{\text{ADC_4P5}}$ | ADC operating frequency | 2 | - | 26.67 | MHz | $4.5 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$ |
| SID114A | $f_{\text{ADC_2P7}}$ | ADC operating frequency | 2 | - | 13.34 | MHz | $2.7 \text{ V} \leq V_{DDA} < 4.5 \text{ V}$ |
| SID113 | $t_{\text{S_4P5}}$ | Analog input sample time | 412 | - | - | ns | $4.5 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$ Guaranteed by design |
| SID113A | $t_{\text{S_2P7}}$ | Analog input sample time | 600 | - | - | ns | $2.7 \text{ V} \leq V_{DDA} < 4.5 \text{ V}$ Guaranteed by design |
| SID113B | $t_{\text{S_DR_4P5}}$ | Analog input sample time when input is from diagnostic reference | 2 | - | - | μs | $4.5 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$ Guaranteed by design |
| SID113C | $t_{\text{S_DR_2P7}}$ | Analog input sample time when input is from diagnostic reference | 2.5 | - | - | μs | $2.7 \text{ V} \leq V_{DDA} < 4.5 \text{ V}$ Guaranteed by design |
| SID113D | $t_{\text{S_TS}}$ | Analog input sample time for temperature sensor | 3 | - | - | μs | $2.7 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$ Guaranteed by design |
| SID106 | $t_{\text{ST_4P5}}$ | Max throughput (Sample per second) | - | - | 1 | Msp/s | $4.5 \text{ V} \leq V_{DDA} \leq 5.5 \text{ V}$, 80 MHz / 3 = 26.67 MHz, 11 sampling cycles, 15 conversion cycles |

Table 26-7 SAR ADC AC specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---|-------|-----|------|-------|--|
| SID106A | t_{ST_2P7} | Max throughput (Sample per second) | – | – | 0.5 | Msp/s | $2.7\text{ V} \leq V_{DDA} < 4.5\text{ V}$ 80 MHz / 6 = 13.3 MHz, 11 sampling cycles, 15 conversion cycles |
| SID107 | C_{VIN} | ADC input sampling capacitance | – | – | 4.8 | pF | Guaranteed by design |
| SID108 | R_{VIN1} | Input path ON resistance (4.5 V to 5.5 V) | – | – | 9.4 | kΩ | Guaranteed by design |
| SID108A | R_{VIN2} | Input path ON resistance (2.7 V to 4.5 V) | – | – | 13.9 | kΩ | Guaranteed by design |
| SID108B | R_{DREF1} | Diagnostic path ON resistance (4.5 V to 5.5 V) | – | – | 40 | kΩ | Guaranteed by design |
| SID108C | R_{DREF2} | Diagnostic path ON resistance (2.7 V to 4.5 V) | – | – | 50 | kΩ | Guaranteed by design |
| SID119 | ACC_RLAD | Diagnostic reference resistor ladder accuracy | –4 | – | 4 | % | |
| SID109 | A_TE | Total error | –5 | – | 5 | LSb | $V_{DDA} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $V_{REFL} = V_{SSA}$ $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ Total error after offset and gain adjustment at 12 bit resolution mode |
| SID109A | A_TEB | Total error | –12 | – | 12 | LSb | $V_{DDA} = V_{REFH} = 2.7\text{ V}$ to 5.5 V , $V_{REFL} = V_{SSA}$ $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ Total error before offset and gain adjustment at 12 bit resolution mode |
| SID110 | A_INL | Integral nonlinearity | –2.5 | – | 2.5 | LSb | $V_{DDA} = 2.7\text{ V}$ to 5.5 V , $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ |
| SID111 | A_DNL | Differential nonlinearity | –0.99 | – | 1.9 | LSb | $V_{DDA} = 2.7\text{ V}$ to 5.5 V , $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ |
| SID112 | A_CE | Channel-to-channel variation (for channels connected to same ADC) | –1 | – | 1 | LSb | $V_{DDA} = 2.7\text{ V}$ to 5.5 V , $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ |
| SID115 | I_{AIC} | Analog input leakage current | –350 | 70 | 350 | nA | When input pad is selected for conversion |
| SID116 | $I_{DIAGREF}$ | Diagnostic reference current | – | – | 70 | μA | |
| SID117 | I_{VDDA} | Analog power supply current while ADC is operating | – | 360 | 550 | μA | Per enabled ADC |
| SID117A | I_{VDDA_DS} | Analog power supply current while ADC is not operating | – | – | 21 | μA | Per enabled ADC |
| SID118 | I_{VREF} | Analog reference voltage current while ADC is operating | – | 360 | 550 | μA | Per enabled ADC |
| SID118A | I_{VREF_LEAK} | Analog reference voltage current while ADC is not operating | – | 1.8 | 5 | μA | Per enabled ADC |

26.6.3 Temperature sensor

Table 26-8 Temperature sensor specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|-------------------------------|-----|-----|-----|-------|--|
| SID200 | T _{SENSACC1} | Temperature sensor accuracy 1 | -2 | - | 2 | °C | T _J = 150 °C This spec is valid when using ADC[0] (V _{DDIO_1}), ADC[1] (V _{DDIO_2}) or ADC[2] (V _{DD}) with the following conditions: a. 3.0 V ≤ V _{DD} , V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 3.6 V or b. 4.5 V ≤ V _{DD} , V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 5.5 V |
| SID201 | T _{SENSACC2} | Temperature sensor accuracy 2 | -5 | - | 5 | °C | -40 °C ≤ T _J < 150 °C This spec is valid when using ADC[0] (V _{DDIO_1}), ADC[1] (V _{DDIO_2}) or ADC[2] (V _{DD}) with the following conditions: a. 3.0 V ≤ V _{DD} , V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 3.6 V or b. 4.5 V ≤ V _{DD} , V _{DDIO_1} or V _{DDIO_2} = V _{DDA} = V _{REFH} ≤ 5.5 V |
| SID201A | T _{SENSACC3} | Temperature sensor accuracy 3 | -10 | - | 10 | °C | -40 °C ≤ T _J ≤ 150 °C This spec is valid when using ADC[0] (V _{DDIO_1}) or ADC[2] (V _{DD}) with the following condition: 2.7 V ≤ V _{DD} or V _{DDIO_1} ≤ 5.5 V and 2.7 V ≤ V _{DDA} = V _{REFH} ≤ 5.5 V and 0.8 × V _{DDA} ≤ V _{DD} or V _{DDIO_1} |

26.6.4 Voltage divider accuracy

Table 26-9 Voltage divider accuracy

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------------|--|-----|-----|-----|-------|--|
| SID202 | V _{MONDIV} | Uncorrected monitor voltage divider accuracy (measured by ADC), compared to ideal supply/2 | -20 | 2 | 20 | % | Any HV supply pad within 2.7-V–5.5-V operating range |

26.7 AC specifications

Unless otherwise noted, the timings are defined with the guidelines mentioned in the [Figure 26-7](#).

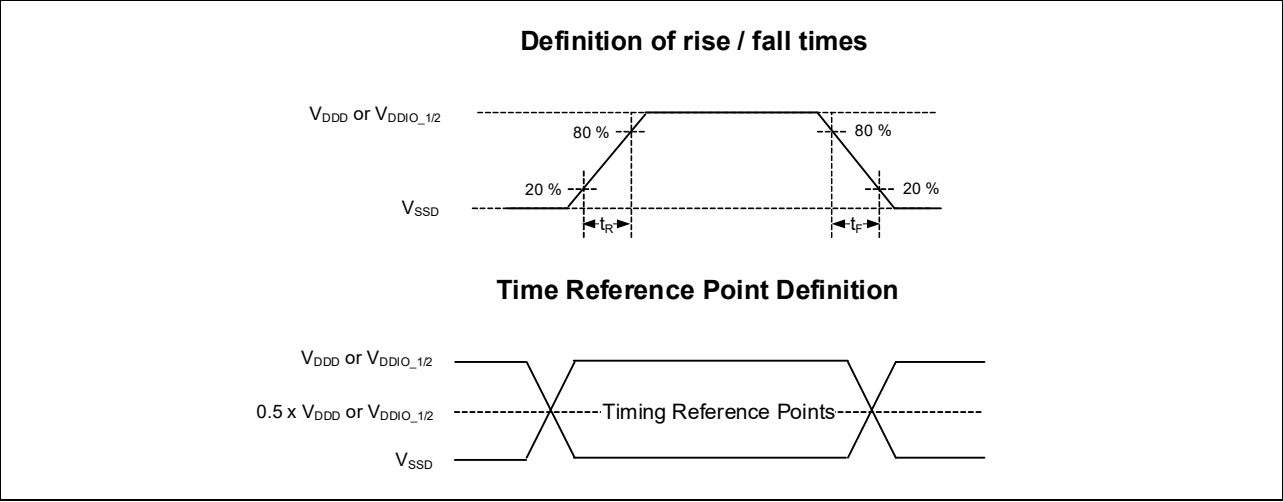


Figure 26-7 AC timings specifications

26.8 Digital peripherals

All specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ and for 2.7 V to 5.5 V except where noted.

Table 26-10 Timer/counter/PWM (TCPWM) specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|--|-----------|-----|-----|-------|--|
| SID120 | f_C | TCPWM operating frequency | – | – | 100 | MHz | f_C = peripheral clock |
| SID121 | t_{PWMENEXT} | Input trigger pulse width for all trigger events | $2 / f_C$ | – | – | ns | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. |
| SID122 | t_{PWMEXT} | Output trigger pulse widths | $2 / f_C$ | – | – | ns | Minimum possible width of Overflow, Underflow, and Counter = Compare (CC) value trigger outputs |
| SID123 | t_{CRES} | Resolution of counter | $1 / f_C$ | – | – | ns | Minimum time between successive counts |
| SID124 | t_{PWMRES} | PWM resolution | $1 / f_C$ | – | – | ns | Minimum pulse width of PWM output |
| SID125 | t_{QRES} | Quadrature inputs resolution | $2 / f_C$ | – | – | ns | Minimum pulse width between Quadrature phase inputs. |

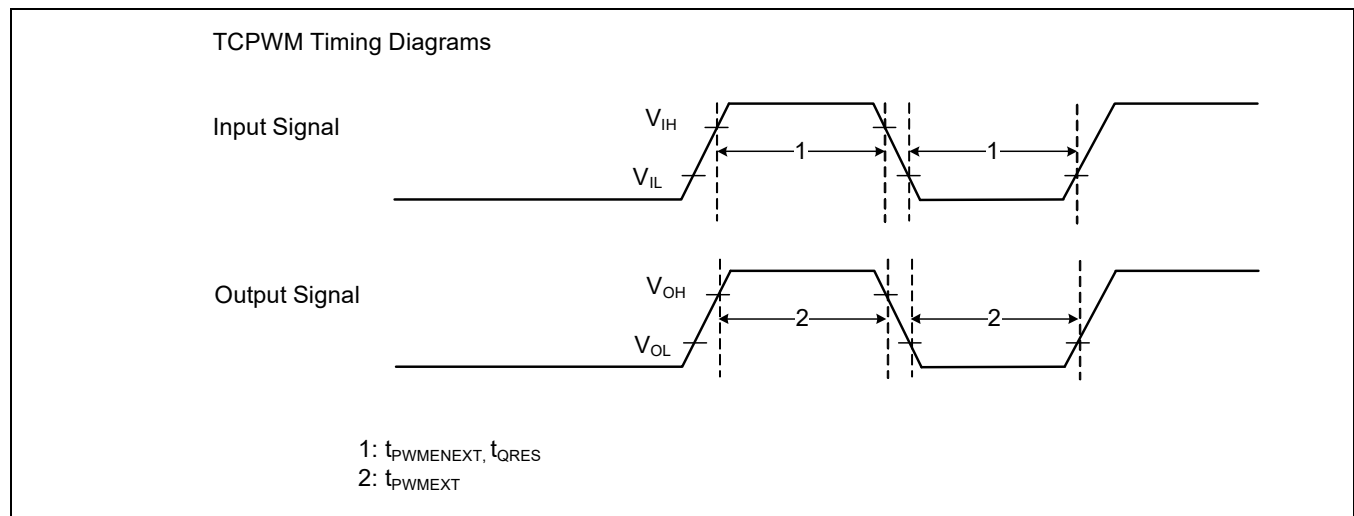


Figure 26-8 TCPWM timing diagrams

Table 26-11 Serial communication block (SCB) specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-----------------------|---|------------------------------|-----|------|-------|--|
| SID129 | f _{SCB} | SCB operating frequency | – | – | 100 | MHz | |
| I²C Interface-Standard-mode | | | | | | | |
| SID130 | f _{SCL} | SCL clock frequency | – | – | 100 | kHz | |
| SID131 | t _{HD;STA} | Hold time, START condition | 4000 | – | – | ns | |
| SID132 | t _{LOW} | Low period of SCL | 4700 | – | – | ns | |
| SID133 | t _{HIGH} | High period of SCL | 4000 | – | – | ns | |
| SID134 | t _{SU;STA} | Setup time for a repeated START | 4700 | – | – | ns | |
| SID135 | t _{HD;DAT} | Data hold time, for receiver | 0 | – | – | ns | |
| SID136 | t _{SU;DAT} | Data setup time | 250 | – | – | ns | |
| SID138 | t _F | Fall time of SCL and SDA | – | – | 300 | ns | Input and output |
| SID139 | t _{SU;STO} | Setup time for STOP | 4000 | – | – | ns | |
| SID140 | t _{BUF} | Bus-free time between START and STOP | 4700 | – | – | ns | |
| SID141 | C _B | Capacitive load for each bus line | – | – | 400 | pF | |
| SID142 | t _{VD;DAT} | Time for data signal from SCL LOW to SDA output | – | – | 3450 | ns | |
| SID143 | t _{VD;ACK} | Data valid acknowledge time | – | – | 3450 | ns | |
| SID144 | V _{OL} | LOW level output voltage | 0 | – | 0.4 | V | Open-drain at 3 mA sink current |
| SID145 | I _{OL} | LOW level output current | 3 | – | – | mA | V _{OL} = 0.4 V |
| I²C Interface-Fast-mode | | | | | | | |
| SID150 | f _{SCL_F} | SCL clock frequency | – | – | 400 | kHz | |
| SID151 | t _{HD;STA_F} | Hold time, START condition | 600 | – | – | ns | |
| SID152 | t _{LOW_F} | Low period of SCL | 1300 | – | – | ns | |
| SID153 | t _{HIGH_F} | High period of SCL | 600 | – | – | ns | |
| SID154 | t _{SU;STA_F} | Setup time for a repeated START | 600 | – | – | ns | |
| SID155 | t _{HD;DAT_F} | Data hold time, for receiver | 0 | – | – | ns | |
| SID156 | t _{SU;DAT_F} | Data setup time | 100 | – | – | ns | |
| SID158 | t _{F_F} | Fall time of SCL and SDA | 20 × (V _{DD} / 5.5) | – | 300 | ns | Input and output, GPIO_ENH: slow mode, 400 pF load |

Table 26-11 Serial communication block (SCB) specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------|---|------|-----|-----|-------|---|
| SID158A | t_{FA_F} | Fall time of SCL and SDA | 0.35 | – | 300 | ns | Input and output GPIO_STD: drive_sel<1:0>= 0b00 MIN: 10 pF load, RPU = 35.41 kΩ MAX: 400 pF load, RPU = 350 Ω |
| SID159 | $t_{SU;STO_F}$ | Setup time for STOP | 600 | – | – | ns | Input and output |
| SID160 | t_{BUF_F} | Bus free time between START and STOP | 1300 | – | – | ns | |
| SID161 | C_{B_F} | Capacitive load for each bus line | – | – | 400 | pF | |
| SID162 | $t_{VD;DAT_F}$ | Time for data signal from SCL LOW to SDA output | – | – | 900 | ns | |
| SID163 | $t_{VD;ACK_F}$ | Data valid acknowledge time | – | – | 900 | ns | |
| SID164 | t_{SP_F} | Pulse width of spikes that must be suppressed by the input filter | – | – | 50 | ns | |
| SID165 | V_{OL_F} | LOW level output voltage | 0 | – | 0.4 | V | Open-drain at 3 mA sink current |
| SID165 | I_{OL_F} | LOW level output current | 3 | – | – | mA | $V_{OL} = 0.4\text{ V}$ |
| SID167 | I_{OL2_F} | LOW level output current | 6 | – | – | mA | $V_{OL} = 0.6\text{ V}^{[53]}$ |

I²C Interface-Fast-Plus mode

| | | | | | | | |
|--------|------------------|---|--------------------------|---|-----|-----|---|
| SID170 | f_{SCL_FP} | SCL clock frequency | – | – | 1 | MHz | |
| SID171 | $t_{HD;STA_FP}$ | Hold time, START condition | 260 | – | – | ns | |
| SID172 | t_{LOW_FP} | Low period of SCL | 500 | – | – | ns | |
| SID173 | t_{HIGH_FP} | High period of SCL | 260 | – | – | ns | |
| SID174 | $t_{SU;STA_FP}$ | Setup time for a repeated START | 260 | – | – | ns | |
| SID175 | $t_{HD;DAT_FP}$ | Data hold time, for receiver | 0 | – | – | ns | |
| SID176 | $t_{SU;DAT_FP}$ | Data setup time | 50 | – | – | ns | |
| SID178 | t_{F_FP} | Fall time of SCL and SDA | $20 \times (V_{DD}/5.5)$ | – | 160 | ns | Input and output 20-pF load GPIO_ENH: slow mode |
| SID179 | $t_{SU;STO_FP}$ | Setup time for STOP | 260 | – | – | ns | Input and output |
| SID180 | t_{BUF_FP} | Bus free time between START and STOP | 500 | – | – | ns | |
| SID181 | C_{B_FP} | Capacitive load for each bus line | – | – | 20 | pF | |
| SID182 | $t_{VD;DAT_FP}$ | Time for data signal from SCL LOW to SDA output | – | – | 450 | ns | |

Table 26-11 Serial communication block (SCB) specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|----------------------|---|--------------------------|----------------------------|------|-------|--|
| SID183 | $t_{VD;ACK_FP}$ | Data valid acknowledge time | – | – | 450 | ns | |
| SID184 | t_{SP_FP} | Pulse width of spikes that must be suppressed by the input filter | – | – | 50 | ns | |
| SID186 | V_{OL_FP} | LOW level output voltage | 0 | – | 0.4 | V | Open-drain at 3 mA sink current |
| SID187 | I_{OL_FP} | LOW level output current | 3 | – | – | mA | $V_{OL} = 0.4 \text{ V}^{[54]}$ |
| SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1) [Conditions: drive_sel<1:0>= 0x] | | | | | | | |
| SID190 | f_{SPI} | SPI operating frequency | – | – | 12.5 | MHz | Do not use half-clock mode: LATE_MISO_SAMPLE = 0 |
| SID191 | t_{DMO} | SPI Master: MOSI valid after SCLK driving edge | – | – | 15 | ns | |
| SID192 | t_{DSI} | SPI Master: MISO valid before SCLK capturing edge | 40 | – | – | ns | |
| SID193 | t_{HMO} | SPI Master: Previous MOSI data hold time | 0 | – | – | ns | |
| SID194 | $t_{W_SCLK_H_L}$ | SPI SCLK pulse width HIGH or LOW | – | $0.4 \times (1 / f_{SPI})$ | – | ns | |
| SID196 | t_{DHI} | SPI Master: MISO hold time after SCLK capturing edge | 0 | – | – | ns | |
| SID198 | t_{EN_SETUP} | SSEL valid, before the first SCK capturing edge | $0.5 \times (1/f_{SPI})$ | – | – | ns | Min is half clock period |
| SID199 | t_{EN_SHOLD} | SSEL hold, after the last SCK capturing edge | $0.5 \times (1/f_{SPI})$ | – | – | ns | Min is half clock period |
| SID195 | C_{SPIM_MS} | SPI capacitive load | – | – | 10 | pF | |
| SPI Interface Slave (internally clocked) [Conditions: drive_sel<1:0>= 0x] | | | | | | | |
| SID205 | f_{SPI_INT} | SPI operating frequency | – | – | 10 | MHz | |
| SID206 | t_{DMI_INT} | SPI Slave: MOSI Valid before Sclock capturing edge | 5 | – | – | ns | |
| SID207 | t_{DSO_INT} | SPI Slave: MISO Valid after Sclock driving edge, in the internal-clocked mode | – | – | 62 | ns | |
| SID208 | t_{HSP} | SPI Slave: Previous MISO data hold time | 3 | – | – | ns | |
| SID209 | $t_{EN_SETUP_INT}$ | SPI Slave: SSEL valid to first SCK valid edge | 33 | – | – | ns | |

Notes

53. In order to drive full bus load at 400 kHz, 6 mA I_{OL} is required at 0.6 V V_{OL} .

54. In order to drive full bus load at 1 MHz, 20 mA I_{OL} is required at 0.4 V V_{OL} . However, this device does not support it.

Table 26-11 Serial communication block (SCB) specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|---------------------------|---|-----|-----|------|-------|--------------------|
| SID210 | t _{EN_HOLD_INT} | SPI Slave Select active (LOW) from last SCLK hold | 33 | – | – | ns | |
| SID211 | t _{EN_SETUP_PRE} | SPI Slave: from SSEL valid, to SCK falling edge before the first data bit | 20 | – | – | ns | |
| SID212 | t _{EN_HOLD_PRE} | SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid | 20 | – | – | ns | |
| SID213 | t _{EN_SETUP_CO} | SPI Slave: from SSEL valid, to SCK falling edge in the first data bit | 20 | – | – | ns | |
| SID214 | t _{EN_HOLD_CO} | SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid | 20 | – | – | ns | |
| SID215 | t _{W_DIS_INT} | SPI Slave Select inactive time | 40 | – | – | ns | |
| SID216 | t _{W_SCLKH_INT} | SPI SCLK pulse width HIGH | 20 | – | – | ns | |
| SID217 | t _{W_SCLKL_INT} | SPI SCLK pulse width LOW | 20 | – | – | ns | |
| SID218 | t _{SIH_INT} | SPI MOSI hold from SCLK | 12 | – | – | ns | |
| SID219 | C _{SPIS_INT} | SPI capacitive load | – | – | 10 | pF | |
| SPI Interface Slave (externally clocked) [Conditions: drive_sel<1:0>= 0x] | | | | | | | |
| SID220 | f _{SPI_EXT} | SPI operating frequency | – | – | 12.5 | MHz | |
| SID221 | t _{DMI_EXT} | SPI Slave: MOSI Valid before Sclock capturing edge | 5 | – | – | ns | |
| SID222 | t _{DSO_EXT} | SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode | – | – | 32 | ns | |
| SID223 | t _{HSO_EXT} | SPI Slave: Previous MISO data hold time | 3 | – | – | ns | |
| SID224 | t _{EN_SETUP_EXT} | SPI Slave: SSEL valid to first SCK valid edge | 40 | – | – | ns | |
| SID225 | t _{EN_HOLD_EXT} | SPI Slave Select active (LOW) from last SCLK hold | 40 | – | – | ns | |
| SID226 | t _{W_DIS_EXT} | SPI Slave Select inactive time | 80 | – | – | ns | |
| SID227 | t _{W_SCLKH_EXT} | SPI SCLK pulse width HIGH | 34 | – | – | ns | |
| SID228 | t _{W_SCLKL_EXT} | SPI SCLK pulse width LOW | 34 | – | – | ns | |
| SID229 | t _{SIH_EXT} | SPI MOSI hold from SCLK | 20 | – | – | ns | |

Table 26-11 Serial communication block (SCB) specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|--|-----|-----|-----|-------|--------------------|
| SID230 | C _{SPIS_EXT} | SPI capacitive load | – | – | 10 | pF | |
| SID231 | t _{VSS_EXT} | SPI Slave: MISO valid after SSEL falling edge (CPHA = 0) | – | – | 33 | ns | |

UART Interface

| | | | | | | | |
|--------|------------------|-----------|---|---|----|------|--|
| SID240 | f _{BPS} | Data rate | – | – | 10 | Mbps | |
|--------|------------------|-----------|---|---|----|------|--|

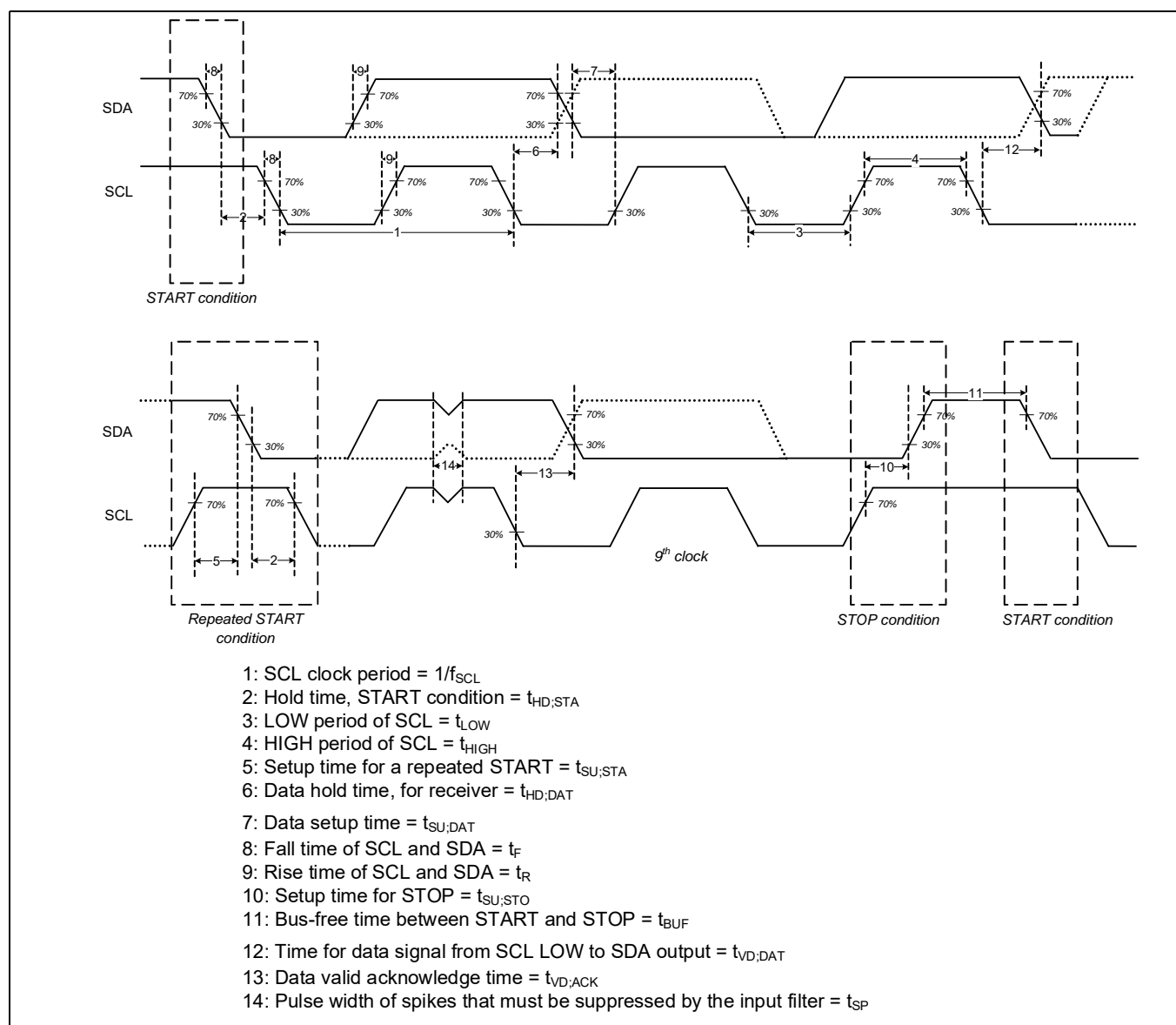


Figure 26-9 I²C timing diagrams

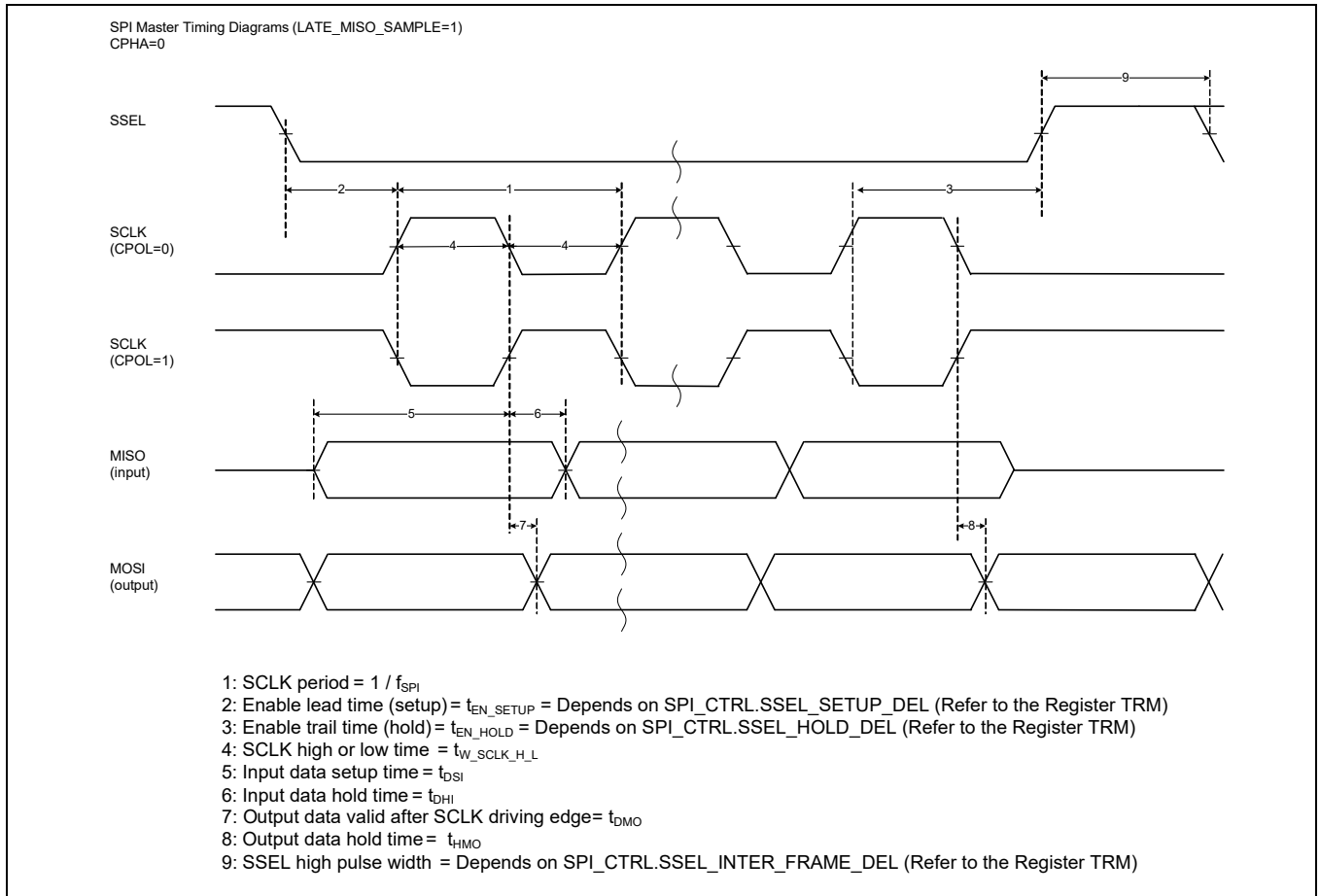


Figure 26-10 SPI master timing diagrams with LOW clock phase

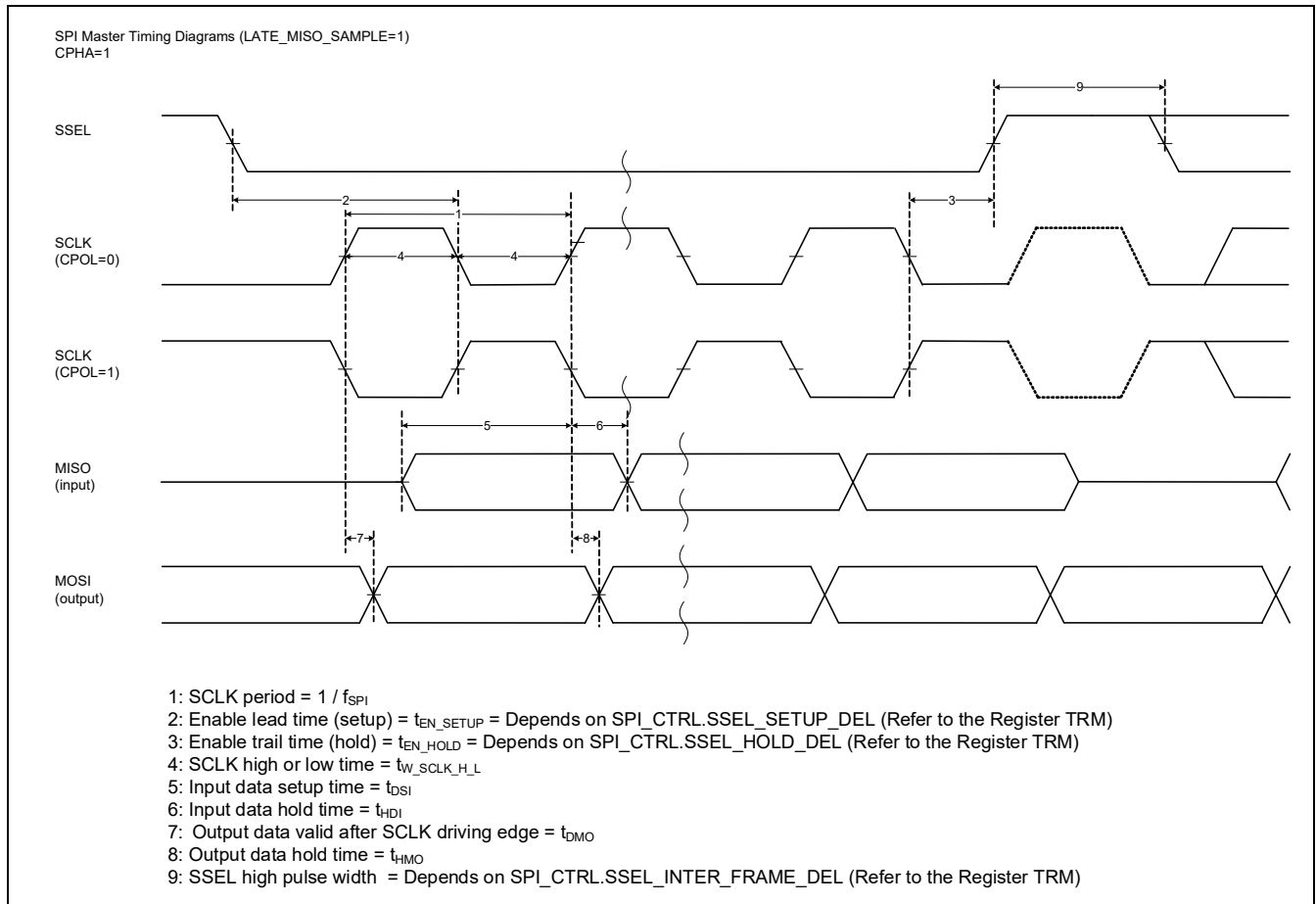


Figure 26-11 SPI master timing diagrams with HIGH clock phase

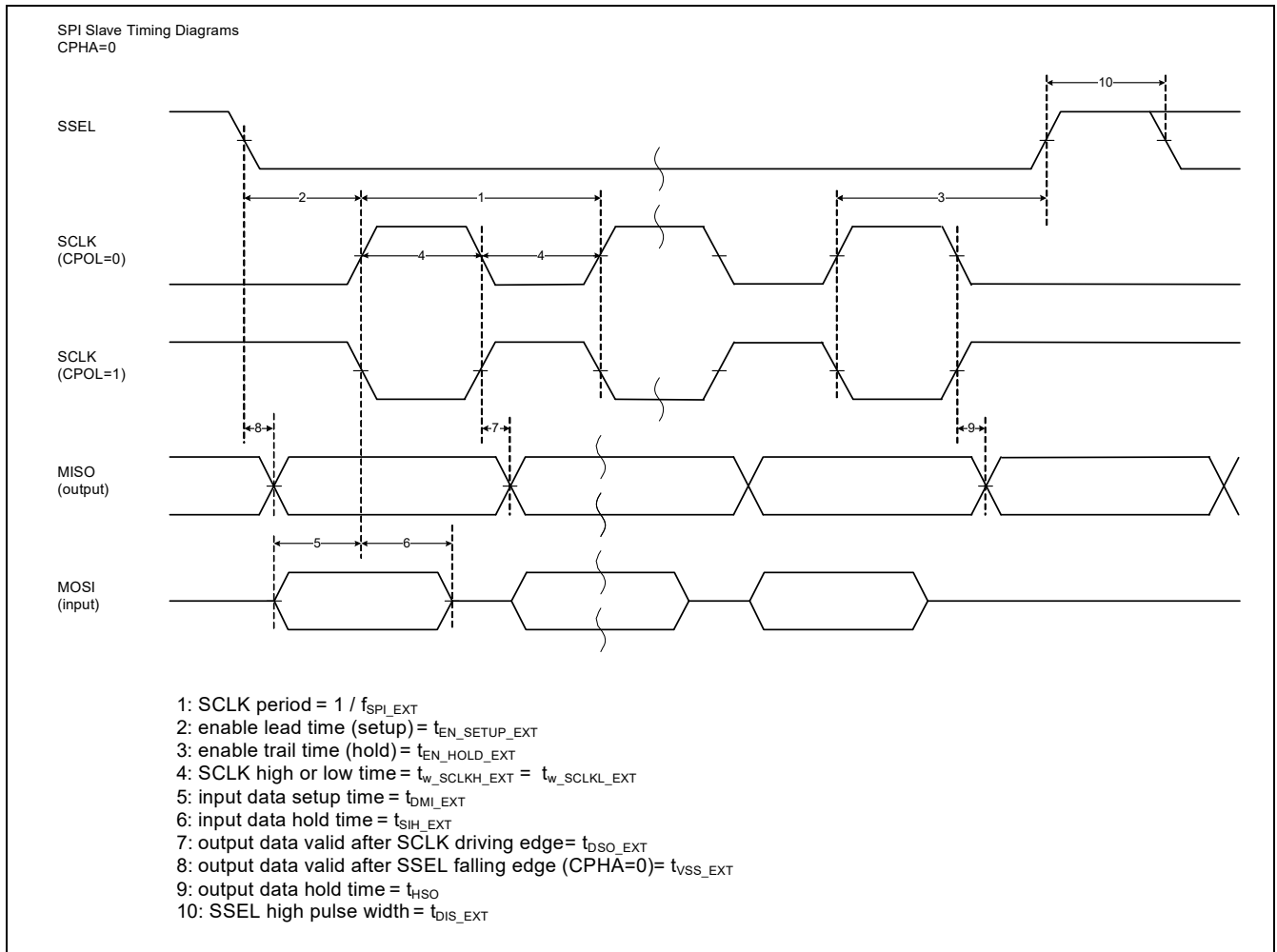


Figure 26-12 SPI slave timing diagrams with LOW clock phase

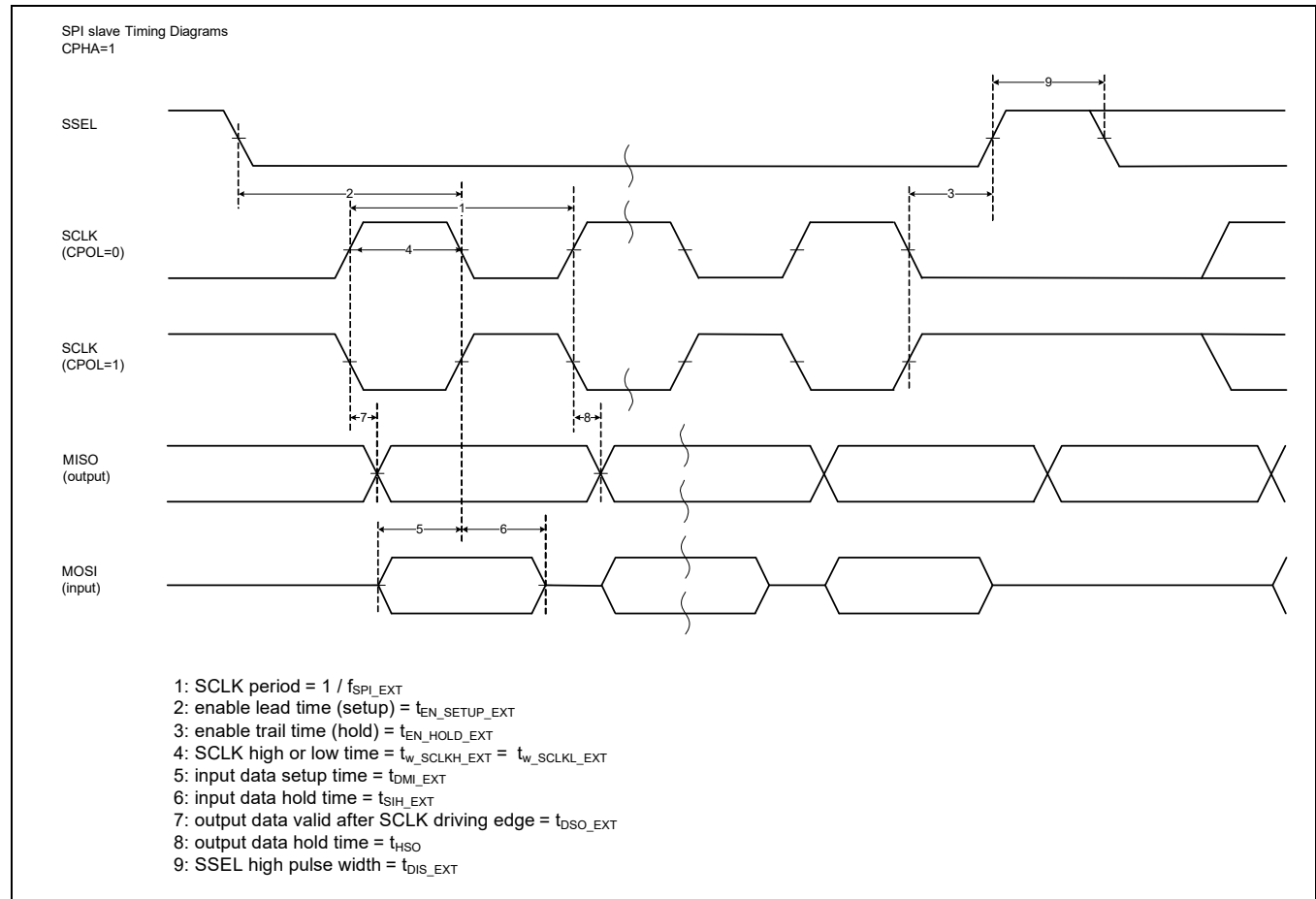


Figure 26-13 SPI slave timing diagrams with HIGH clock phase

26.8.1 LIN specifications

Table 26-12 LIN specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---|-----|-----|-------|-------|----------------------|
| SID249 | f_{LIN} | Internal clock frequency to the LIN block | – | – | 100 | MHz | |
| SID250 | BR_NOM | Bit rate on the LIN bus | 1 | – | 20 | kbps | Guaranteed by design |
| SID250A | BR_REF | Bit rate on the LIN bus (not in standard LIN specification) for re-flashing in LIN slave mode | 1 | – | 115.2 | kbps | Guaranteed by design |

26.8.2 CAN FD specifications

Table 26-13 CAN FD specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|------------------------|-----|-----|-----|-------|--|
| SID630 | f_{HCLK} | System clock frequency | – | – | 100 | MHz | $f_{\text{CCLK}} \leq f_{\text{HCLK}}$, Guaranteed by design |
| SID631 | f_{CCLK} | CAN clock frequency | – | – | 100 | MHz | $f_{\text{CCLK}} \leq f_{\text{HCLK}}$, Guaranteed by design |

26.9 Memory

All specifications are valid for $-40\text{ °C} \leq T_A \leq 125\text{ °C}$ and for 2.7 V to 5.5 V except where noted.

Table 26-14 Flash DC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------|---------------------------|-----|-----|-----|-------|--------------------|
| SID260 | V _{PE} | Erase and program voltage | 2.7 | – | 5.5 | V | |

Table 26-15 Flash AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|---------------------------|--|-----|-----|--------------|-------|--|
| SID257 | f _{FO} | Maximum flash memory operation frequency | – | – | 100 | MHz | Zero wait access to code-flash memory up to 100 MHz Zero wait access with cache hit up to 160 MHz |
| SID254 | t _{ERS_SUS} | Maximum time from erase suspend command till erase is indeed suspend | – | – | 37.5 | µs | |
| SID255 | t _{ERS_RES_SUS} | Minimum time allowed from erase resume to erase suspend | 250 | – | – | µs | Guaranteed by design |
| SID258 | t _{BC_WF} | Blank check time for N-bytes of work-flash | – | – | 10 + 0.3 × N | µs | At 100 MHz, N ≥ 4 and multiple of 4, excludes system overhead time |
| SID259 | t _{SECTORERASE1} | Sector erase time (Code-flash: 32 KB) | – | 45 | 90 | ms | Includes internal preprogramming time |
| SID259A | t _{SECTORERASE2} | Sector erase time (Code-flash: 8 KB) | – | 15 | 30 | ms | Includes internal preprogramming time |
| SID261 | t _{SECTORERASE3} | Sector erase time (Work-flash, 2 KB) | – | 80 | 160 | ms | Includes internal preprogramming time |
| SID262 | t _{SECTORERASE4} | Sector erase time (Work-flash, 128 bytes) | – | 5 | 15 | ms | Includes internal preprogramming time |
| SID263 | t _{WRITE1} | 64-bit write time (Code-flash) | – | 30 | 60 | µs | Excludes system overhead time |
| SID264 | t _{WRITE2} | 256-bit write time (Code-flash) | – | 40 | 70 | µs | Excludes system overhead time |
| SID265 | t _{WRITE3} | 4096-bit write time (Code-flash) ^[55] | – | 320 | 1200 | µs | Excludes system overhead time |
| SID266 | t _{WRITE4} | 32-bit write time (Work-flash) | – | 30 | 60 | µs | Excludes system overhead time |
| SID267 | t _{FRET1} | Code-flash retention. 1000 program/erase cycles | 20 | – | – | years | T _A (power on and off) ≤ 85 °C average |
| SID268 | t _{FRET3} | Work-flash retention. 125,000 program/erase cycles | 20 | – | – | years | T _A (power on and off) ≤ 85 °C average |
| SID269 | t _{FRET4} | Work-flash retention. 250,000 program/erase cycles | 10 | – | – | years | T _A (power on and off) ≤ 85 °C average |
| SID612 | I _{CC_ACT2} | Program operating current (Code or Work-flash) | – | 15 | 48 | mA | V _{DDD} = 5 V Guaranteed by design |
| SID613 | I _{CC_ACT3} | Erase operating current (Code or Work-flash) | – | 15 | 48 | mA | V _{DDD} = 5 V Guaranteed by design |

Note

55. The code-flash includes a 'Write Buffer' of 4096-bit. If the application software writes this buffer multiple times, to get the overall write time multiply one sector write time with the corresponding factor (say for factor 64, example, 64 x 512 B = 32 KB [one sector]).

26.10 System resources

All specifications are valid for $-40\text{ °C} \leq T_A \leq 125\text{ °C}$ and for 2.7 V to 5.5 V except where noted.

Table 26-16 System resources

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|----------------------------|---|-------|-------|-------|-------|--|
| Power-on-reset specifications | | | | | | | |
| SID270 | V _{POR_R} | V _{DDD} rising voltage to deassert POR | 1.5 | – | 2.35 | V | Guaranteed by design |
| SID276 | V _{POR_F} | V _{DDD} falling voltage to assert POR | 1.45 | – | 2.1 | V | |
| SID271 | V _{POR_H} | Level detection hysteresis | 20 | – | 300 | mV | Guaranteed by design |
| SID272 | t _{DLY_POR} | Delay between V _{DDD} rising through 2.3 V and an internal deassertion of POR | – | – | 3 | μs | Guaranteed by design |
| SID273 | t _{POFF} | V _{DDD} Power off time | 100 | – | – | μs | V _{DDD} < 1.45 V |
| SID274 | POR_RR1 | V _{DDD} power ramp rate with robust BOD (BOD operation is guaranteed) | – | – | 100 | mV/μs | This ramp supports robust BOD |
| SID275 | POR_RR2 | V _{DDD} power ramp rate without robust BOD | – | – | 1000 | mV/μs | This ramp does not support robust BOD t _{POFF} must be satisfied |
| High-voltage BOD (HV BOD) specifications | | | | | | | |
| SID500 | V _{TR_2P7_R} | HV BOD 2.7 V rising detection point for V _{DDD} and V _{DDA} (default) | 2.474 | 2.55 | 2.627 | V | |
| SID501 | V _{TR_2P7_F} | HV BOD 2.7 V falling detection point for V _{DDD} and V _{DDA} (default) | 2.449 | 2.525 | 2.601 | V | |
| SID502 | V _{TR_3P0_R} | HV BOD 3.0 V rising detection point for V _{DDD} and V _{DDA} | 2.765 | 2.85 | 2.936 | V | |
| SID503 | V _{TR_3P0_F} | HV BOD 3.0 V falling detection point for V _{DDD} and V _{DDA} | 2.74 | 2.825 | 2.91 | V | |
| SID505 | HVBOD_RR_A | Power ramp rate: V _{DDD} and V _{DDA} (Active) | – | – | 100 | mV/μs | |
| SID506 | HVBOD_RR_DS | Power ramp rate: V _{DDD} and V _{DDA} (DeepSleep) | – | – | 10 | mV/μs | |
| SID507 | t _{DLY_ACT_HVBOD} | Active mode delay between V _{DDD} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and an internal HV BOD signal transitioning | – | – | 0.5 | μs | Guaranteed by design |
| SID507A | t _{DLY_ACT_HVBOD} | Active mode delay between V _{DDA} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and internal HVBOD signal transitioning | – | – | 1 | μs | Guaranteed by design |
| SID507B | t _{DLY_DS_HVBOD} | DeepSleep mode delay between V _{DDD} /V _{DDA} falling/rising through V _{TR_2P7_F/R} or V _{TR_3P0_F/R} and an internal HV BOD signal transitioning | – | – | 4 | μs | Guaranteed by design |

Table 26-16 System resources (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|-----------------------|---|----------|-------|----------|-------|------------------------|
| SID508 | t_{RES_HVBOD} | Response time of HV BOD, V_{DDP}/V_{DDA} supply. (For falling-then-rising supply at max ramp rate; threshold is $V_{TR_2P7_F}$ or $V_{TR_3P0_F}$.) | 100 | – | – | ns | Guaranteed by design |
| Low-voltage BOD (LV BOD) specifications | | | | | | | |
| SID510 | $V_{TR_R_LVBOD}$ | LV BOD rising detection point for V_{CCD} | 0.917 | 0.945 | 0.973 | V | |
| SID511 | $V_{TR_F_LVBOD}$ | LV BOD falling detection point for V_{CCD} | 0.892 | 0.92 | 0.948 | V | |
| SID515 | $t_{DLY_ACT_LVBOD}$ | Active delay between V_{CCD} falling/rising through V_{TR_R/F_LVBOD} and an internal LV BOD signal transitioning | – | – | 1 | μs | Guaranteed by design |
| SID515A | $t_{DLY_DS_LVBOD}$ | DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_R/F_LVBOD} and an internal LV BOD signal transitioning | – | – | 12 | μs | Guaranteed by design |
| SID516 | t_{RES_LVBOD} | Response time of LV BOD. (For falling-then-rising supply at max ramp rate; threshold is $V_{TR_F_LVBOD}$.) | 100 | – | – | ns | Guaranteed by design |
| Low-voltage detector (LVD) DC specifications | | | | | | | |
| SID520 | $V_{TR_2P8_F}$ | LVD 2.8 V falling detection point for V_{DDD} | Typ – 4% | 2800 | Typ + 4% | mV | |
| SID521 | $V_{TR_2P9_F}$ | LVD 2.9 V falling detection point for V_{DDD} | Typ – 4% | 2900 | Typ + 4% | mV | |
| SID522 | $V_{TR_3P0_F}$ | LVD 3.0 V falling detection point for V_{DDD} | Typ – 4% | 3000 | Typ + 4% | mV | |
| SID523 | $V_{TR_3P1_F}$ | LVD 3.1 V falling detection point for V_{DDD} | Typ – 4% | 3100 | Typ + 4% | mV | |
| SID524 | $V_{TR_3P2_F}$ | LVD 3.2 V falling detection point for V_{DDD} | Typ – 4% | 3200 | Typ + 4% | mV | |
| SID525 | $V_{TR_3P3_F}$ | LVD 3.3 V falling detection point for V_{DDD} | Typ – 4% | 3300 | Typ + 4% | mV | |
| SID526 | $V_{TR_3P4_F}$ | LVD 3.4 V falling detection point for V_{DDD} | Typ – 4% | 3400 | Typ + 4% | mV | |
| SID527 | $V_{TR_3P5_F}$ | LVD 3.5 V falling detection point for V_{DDD} | Typ – 4% | 3500 | Typ + 4% | mV | |
| SID528 | $V_{TR_3P6_F}$ | LVD 3.6 V falling detection point for V_{DDD} | Typ – 4% | 3600 | Typ + 4% | mV | |
| SID529 | $V_{TR_3P7_F}$ | LVD 3.7 V falling detection point for V_{DDD} | Typ – 4% | 3700 | Typ + 4% | mV | |
| SID530 | $V_{TR_3P8_F}$ | LVD 3.8 V falling detection point for V_{DDD} | Typ – 4% | 3800 | Typ + 4% | mV | |
| SID531 | $V_{TR_3P9_F}$ | LVD 3.9 V falling detection point for V_{DDD} | Typ – 4% | 3900 | Typ + 4% | mV | |
| SID532 | $V_{TR_4P0_F}$ | LVD 4.0 V falling detection point for V_{DDD} | Typ – 4% | 4000 | Typ + 4% | mV | |

Table 26-16 System resources (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---------|-----------------------|--|----------|------|----------|-------|---------------------------------------|
| SID533 | V _{TR_4P1_F} | LVD 4.1 V falling detection point for V _{DDD} | Typ – 4% | 4100 | Typ + 4% | mV | |
| SID534 | V _{TR_4P2_F} | LVD 4.2 V falling detection point for V _{DDD} | Typ – 4% | 4200 | Typ + 4% | mV | |
| SID535 | V _{TR_4P3_F} | LVD 4.3 V falling detection point for V _{DDD} | Typ – 4% | 4300 | Typ + 4% | mV | |
| SID536 | V _{TR_4P4_F} | LVD 4.4 V falling detection point for V _{DDD} | Typ – 4% | 4400 | Typ + 4% | mV | |
| SID537 | V _{TR_4P5_F} | LVD 4.5 V falling detection point for V _{DDD} | Typ – 4% | 4500 | Typ + 4% | mV | |
| SID538 | V _{TR_4P6_F} | LVD 4.6 V falling detection point for V _{DDD} | Typ – 4% | 4600 | Typ + 4% | mV | |
| SID539 | V _{TR_4P7_F} | LVD 4.7 V falling detection point for V _{DDD} | Typ – 4% | 4700 | Typ + 4% | mV | |
| SID540 | V _{TR_4P8_F} | LVD 4.8 V falling detection point for V _{DDD} | Typ – 4% | 4800 | Typ + 4% | mV | |
| SID541 | V _{TR_4P9_F} | LVD 4.9 V falling detection point for V _{DDD} | Typ – 4% | 4900 | Typ + 4% | mV | |
| SID542 | V _{TR_5P0_F} | LVD 5.0 V falling detection point for V _{DDD} | Typ – 4% | 5000 | Typ + 4% | mV | |
| SID543 | V _{TR_5P1_F} | LVD 5.1 V falling detection point for V _{DDD} | Typ – 4% | 5100 | Typ + 4% | mV | |
| SID544 | V _{TR_5P2_F} | LVD 5.2 V falling detection point for V _{DDD} | Typ – 4% | 5200 | Typ + 4% | mV | |
| SID545 | V _{TR_5P3_F} | LVD 5.3 V falling detection point for V _{DDD} | Typ – 4% | 5300 | Typ + 4% | mV | |
| SID546 | V _{TR_2P8_R} | LVD 2.8 V rising detection point for V _{DDD} | Typ – 4% | 2825 | Typ + 4% | mV | Same as V _{TR_2P8_F} + 25 mV |
| SID547 | V _{TR_2P9_R} | LVD 2.9 V rising detection point for V _{DDD} | Typ – 4% | 2925 | Typ + 4% | mV | Same as V _{TR_2P9_F} + 25 mV |
| SID548 | V _{TR_3P0_R} | LVD 3.0 V rising detection point for V _{DDD} | Typ – 4% | 3025 | Typ + 4% | mV | Same as V _{TR_3P0_F} + 25 mV |
| SID549 | V _{TR_3P1_R} | LVD 3.1 V rising detection point for V _{DDD} | Typ – 4% | 3125 | Typ + 4% | mV | Same as V _{TR_3P1_F} + 25 mV |
| SID550 | V _{TR_3P2_R} | LVD 3.2 V rising detection point for V _{DDD} | Typ – 4% | 3225 | Typ + 4% | mV | Same as V _{TR_3P2_F} + 25 mV |
| SID551 | V _{TR_3P3_R} | LVD 3.3 V rising detection point for V _{DDD} | Typ – 4% | 3325 | Typ + 4% | mV | Same as V _{TR_3P3_F} + 25 mV |
| SID552 | V _{TR_3P4_R} | LVD 3.4 V rising detection point for V _{DDD} | Typ – 4% | 3425 | Typ + 4% | mV | Same as V _{TR_3P4_F} + 25 mV |
| SID553 | V _{TR_3P5_R} | LVD 3.5 V rising detection point for V _{DDD} | Typ – 4% | 3525 | Typ + 4% | mV | Same as V _{TR_3P5_F} + 25 mV |
| SID554 | V _{TR_3P6_R} | LVD 3.6 V rising detection point for V _{DDD} | Typ – 4% | 3625 | Typ + 4% | mV | Same as V _{TR_3P6_F} + 25 mV |
| SID555 | V _{TR_3P7_R} | LVD 3.7 V rising detection point for V _{DDD} | Typ – 4% | 3725 | Typ + 4% | mV | Same as V _{TR_3P7_F} + 25 mV |

Table 26-16 System resources (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---------|--------------------------|---|----------|------|----------|-------|---------------------------------------|
| SID556 | V _{TR_3P8_R} | LVD 3.8 V rising detection point for V _{DDD} | Typ – 4% | 3825 | Typ + 4% | mV | Same as V _{TR_3P8_F} + 25 mV |
| SID557 | V _{TR_3P9_R} | LVD 3.9 V rising detection point for V _{DDD} | Typ – 4% | 3925 | Typ + 4% | mV | Same as V _{TR_3P9_F} + 25 mV |
| SID558 | V _{TR_4P0_R} | LVD 4.0 V rising detection point for V _{DDD} | Typ – 4% | 4025 | Typ + 4% | mV | Same as V _{TR_4P0_F} + 25 mV |
| SID559 | V _{TR_4P1_R} | LVD 4.1 V rising detection point for V _{DDD} | Typ – 4% | 4125 | Typ + 4% | mV | Same as V _{TR_4P1_F} + 25 mV |
| SID560 | V _{TR_4P2_R} | LVD 4.2 V rising detection point for V _{DDD} | Typ – 4% | 4225 | Typ + 4% | mV | Same as V _{TR_4P2_F} + 25 mV |
| SID561 | V _{TR_4P3_R} | LVD 4.3 V rising detection point for V _{DDD} | Typ – 4% | 4325 | Typ + 4% | mV | Same as V _{TR_4P3_F} + 25 mV |
| SID562 | V _{TR_4P4_R} | LVD 4.4 V rising detection point for V _{DDD} | Typ – 4% | 4425 | Typ + 4% | mV | Same as V _{TR_4P4_F} + 25 mV |
| SID563 | V _{TR_4P5_R} | LVD 4.5 V rising detection point for V _{DDD} | Typ – 4% | 4525 | Typ + 4% | mV | Same as V _{TR_4P5_F} + 25 mV |
| SID564 | V _{TR_4P6_R} | LVD 4.6 V rising detection point for V _{DDD} | Typ – 4% | 4625 | Typ + 4% | mV | Same as V _{TR_4P6_F} + 25 mV |
| SID565 | V _{TR_4P7_R} | LVD 4.7 V rising detection point for V _{DDD} | Typ – 4% | 4725 | Typ + 4% | mV | Same as V _{TR_4P7_F} + 25 mV |
| SID566 | V _{TR_4P8_R} | LVD 4.8 V rising detection point for V _{DDD} | Typ – 4% | 4825 | Typ + 4% | mV | Same as V _{TR_4P8_F} + 25 mV |
| SID567 | V _{TR_4P9_R} | LVD 4.9 V rising detection point for V _{DDD} | Typ – 4% | 4925 | Typ + 4% | mV | Same as V _{TR_4P9_F} + 25 mV |
| SID568 | V _{TR_5P0_R} | LVD 5.0 V rising detection point for V _{DDD} | Typ – 4% | 5025 | Typ + 4% | mV | Same as V _{TR_5P0_F} + 25 mV |
| SID569 | V _{TR_5P1_R} | LVD 5.1 V rising detection point for V _{DDD} | Typ – 4% | 5125 | Typ + 4% | mV | Same as V _{TR_5P1_F} + 25 mV |
| SID570 | V _{TR_5P2_R} | LVD 5.2 V rising detection point for V _{DDD} | Typ – 4% | 5225 | Typ + 4% | mV | Same as V _{TR_5P2_F} + 25 mV |
| SID571 | V _{TR_5P3_R} | LVD 5.3 V rising detection point for V _{DDD} | Typ – 4% | 5325 | Typ + 4% | mV | Same as V _{TR_5P3_F} + 25 mV |
| SID573 | LVD_RR_A | Power ramp rate: V _{DDD} (Active) | – | – | 100 | mV/μs | |
| SID574 | LVD_RR_DS | Power ramp rate: V _{DDD} (DeepSleep) | – | – | 10 | mV/μs | |
| SID575 | t _{DLY_ACT_LVD} | Active mode delay between V _{DDD} falling/rising through LVD rising/falling point and an internal LVD signal transitioning | – | – | 1 | μs | Guaranteed by design |
| SID575A | t _{DLY_DS_LVD} | DeepSleep mode delay between V _{DDD} falling/rising through LVD rising/falling point and an internal LVD signal rising | – | – | 4 | μs | Guaranteed by design |

Table 26-16 System resources (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|--------------------------|--|-------|-------|-------|-------------|------------------------|
| SID576 | t_{RES_LVD} | Response time of LVD, V_{DD} supply. LVD guaranteed to generate pulse for V_{DD} pulse width greater than this. (For falling-then-rising supply at max ramp rate; pulse width is time below LVD falling point) | 100 | – | – | ns | Guaranteed by design |
| High-voltage OVD (HV OVD) specifications | | | | | | | |
| SID580 | $V_{TR_5P0_R}$ | HV OVD 5.0-V rising detection point for V_{DD} and V_{DDA} | 5.049 | 5.205 | 5.361 | V | |
| SID581 | $V_{TR_5P0_F}$ | HV OVD 5.0-V falling detection point for V_{DD} and V_{DDA} | 5.025 | 5.18 | 5.335 | V | |
| SID582 | $V_{TR_5P5_R}$ | HV OVD 5.5-V rising detection point for V_{DD} and V_{DDA} (default) | 5.548 | 5.72 | 5.892 | V | |
| SID583 | $V_{TR_5P5_F}$ | HV OVD 5.5-V falling detection point for V_{DD} and V_{DDA} (default) | 5.524 | 5.695 | 5.866 | V | |
| SID585 | HVOVD_RR_A | Power ramp rate: V_{DD} and V_{DDA} (Active) | – | – | 100 | mV/ μ s | |
| SID586 | HVOVD_RR_DS | Power ramp rate: V_{DD} and V_{DDA} (DeepSleep) | – | – | 10 | mV/ μ s | |
| SID587 | $t_{DLY_ACT_HVOVD}$ | Active mode delay between V_{DD} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD signal transitioning | – | – | 1 | μ s | Guaranteed by design |
| SID587A | $t_{DLY_ACT_HVOVD_A}$ | Active mode delay between V_{DDA} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD signal transitioning | – | – | 1.5 | μ s | Guaranteed by design |
| SID587B | $t_{DLY_DS_HVOVD}$ | DeepSleep mode delay between V_{DD}/V_{DDA} falling/rising through $V_{TR_5P0_F/R}$ or $V_{TR_5P5_F/R}$ and an internal HV OVD signal transitioning | – | – | 4 | μ s | Guaranteed by design |
| SID588 | t_{RES_HVOVD} | Response time of HV OVD. (For rising-then-falling supply at max ramp rate; threshold is $V_{TR_5P0_R}$ or $V_{TR_5P5_R}$) | 100 | – | – | ns | Guaranteed by design |
| Low-voltage OVD (LV OVD) specifications | | | | | | | |
| SID590 | $V_{TR_R_LVOVD}$ | LV OVD rising detection point for V_{CCD} | 1.261 | 1.3 | 1.339 | V | |
| SID591 | $V_{TR_F_LVOVD}$ | LV OVD falling detection point for V_{CCD} | 1.237 | 1.275 | 1.313 | V | |
| SID595 | $t_{DLY_ACT_LVOVD}$ | Active mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD signal transitioning | – | – | 1 | μ s | Guaranteed by design |

Table 26-16 System resources (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---------|----------------------|--|-----|-----|-----|---------|------------------------|
| SID595A | $t_{DLY_DS_LVOVD}$ | DeepSleep mode delay between V_{CCD} falling/rising through V_{TR_F/R_LVOVD} and an internal LV OVD signal transitioning | – | – | 12 | μs | Guaranteed by design |
| SID596 | t_{RES_LVOVD} | Response time of LV OVD. (For rising-then-falling supply at max ramp rate; threshold is $V_{TR_R_LVOVD}$.) | 100 | – | – | ns | Guaranteed by design |

Overcurrent detection (OCD) specifications

| | | | | | | | |
|--------|------------------|-----------------------------|-----|---|-----|----|----------------------|
| SID598 | I_{OCD} | OCD range for V_{CCD} | 156 | – | 315 | mA | Guaranteed by design |
| SID599 | I_{OCD_DPSLP} | OCD range in DeepSleep mode | 18 | – | 72 | mA | Guaranteed by design |

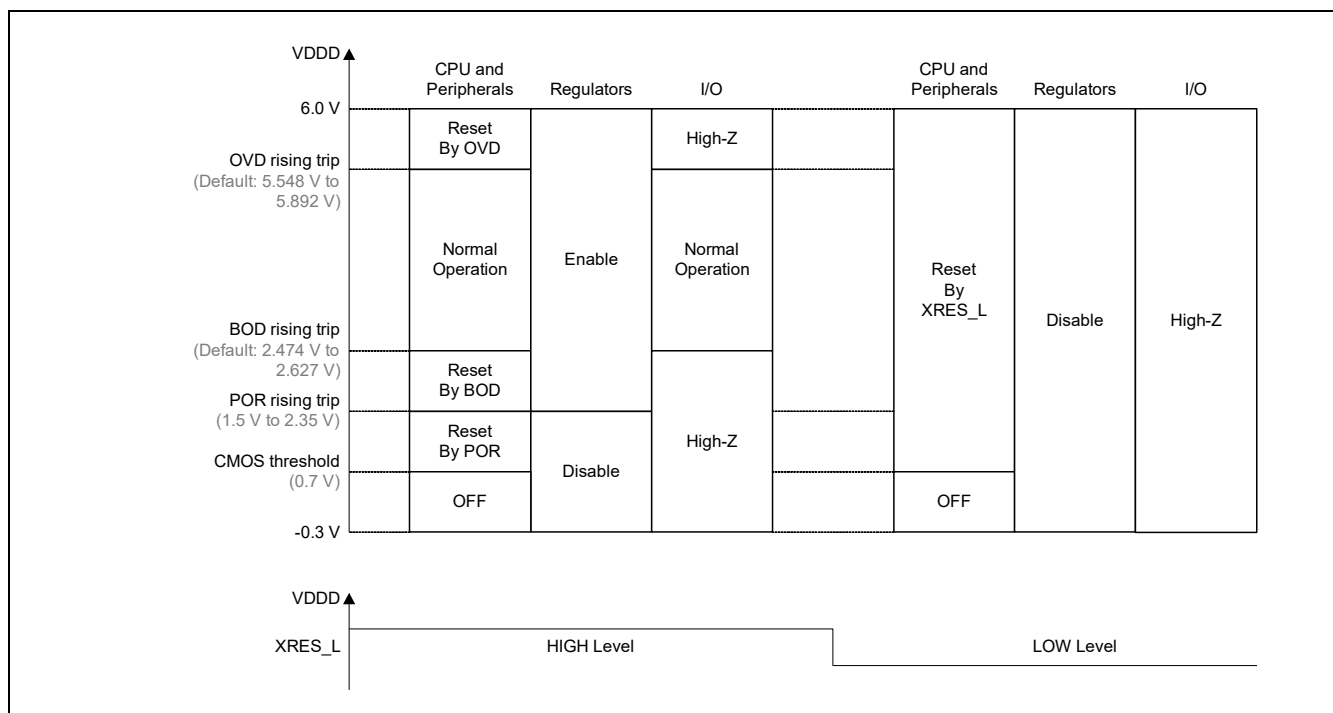


Figure 26-14 Device operations supply range

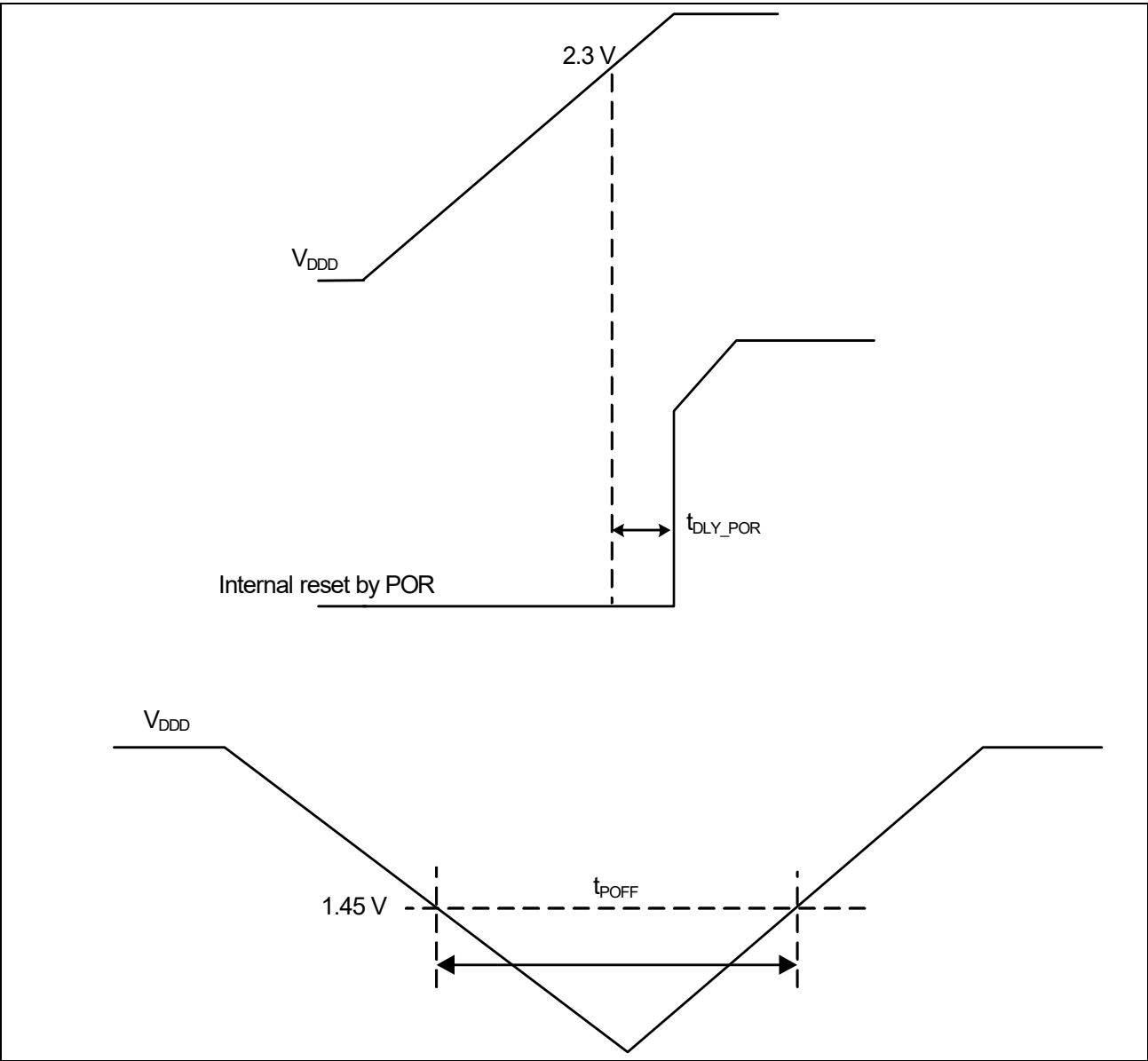


Figure 26-15 POR specifications

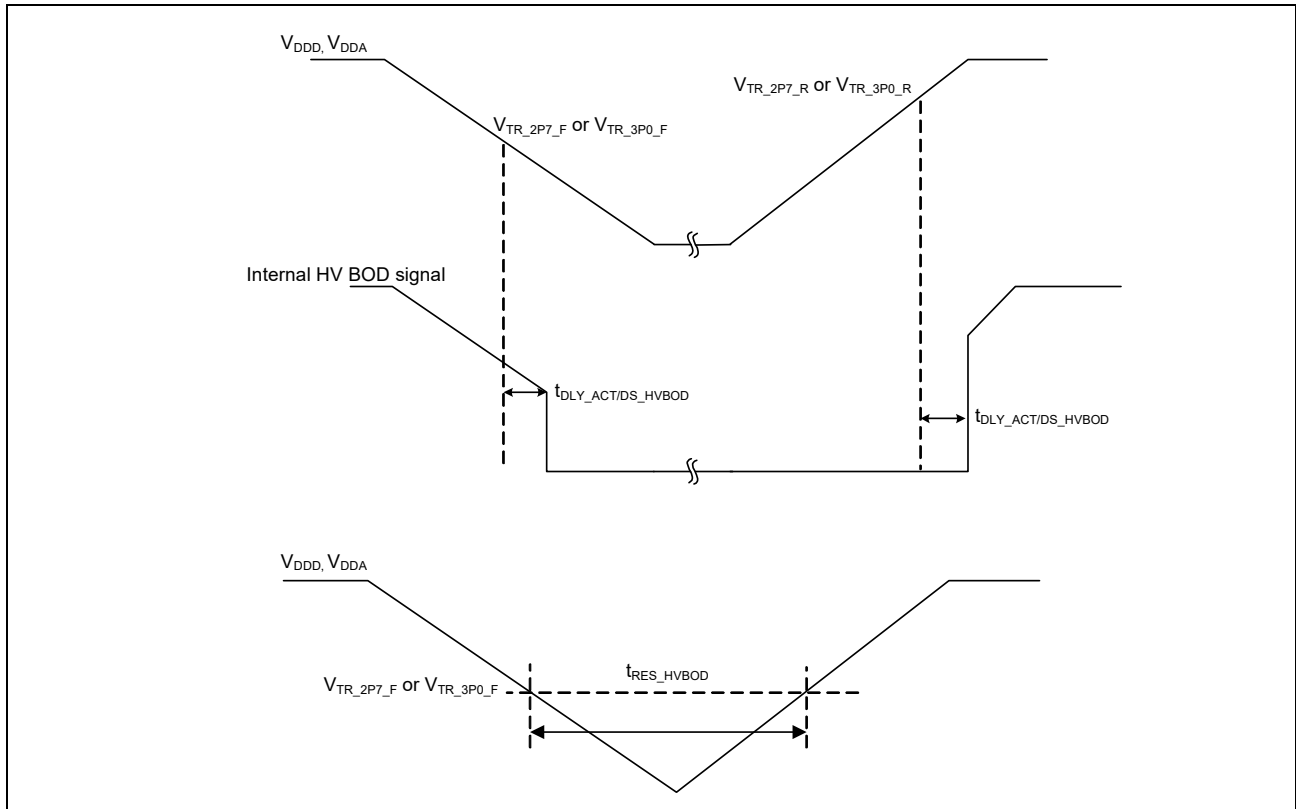


Figure 26-16 High-voltage BOD specifications

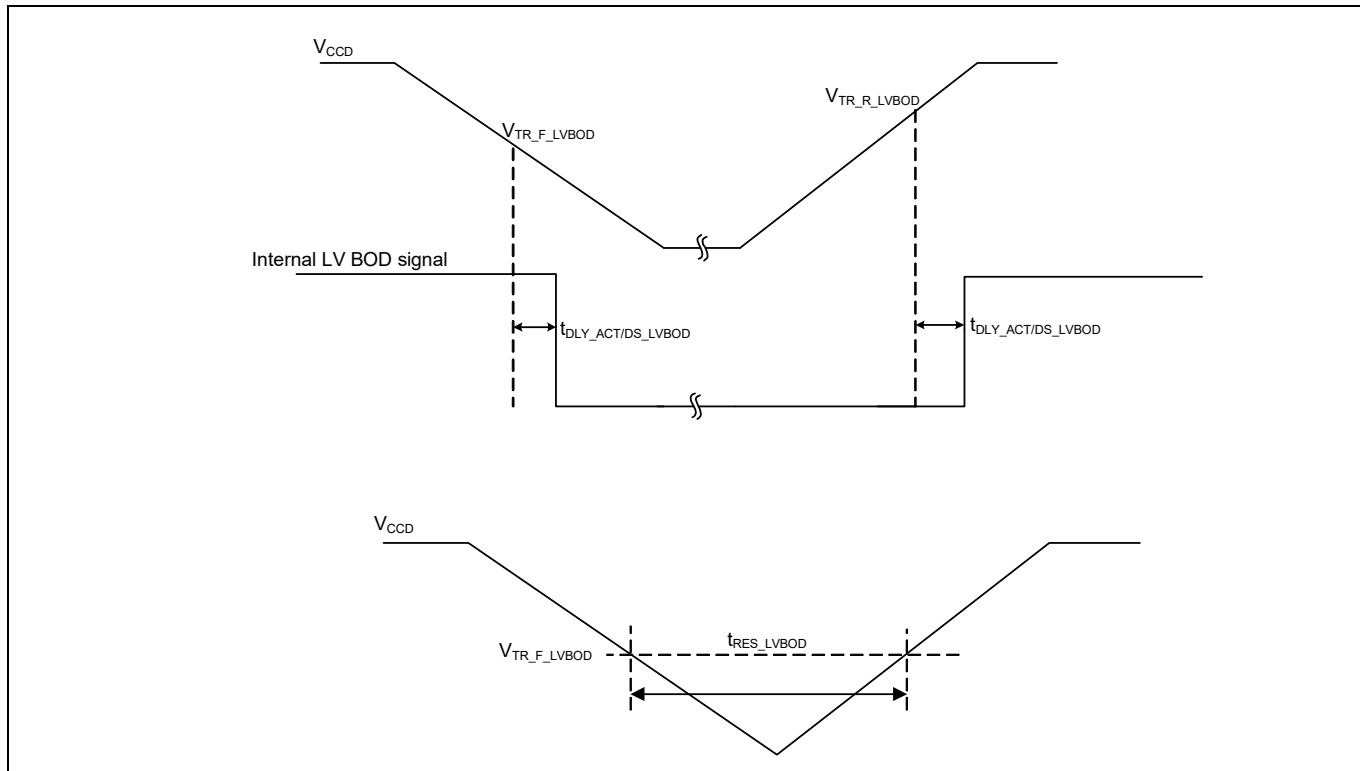


Figure 26-17 Low-voltage BOD specifications

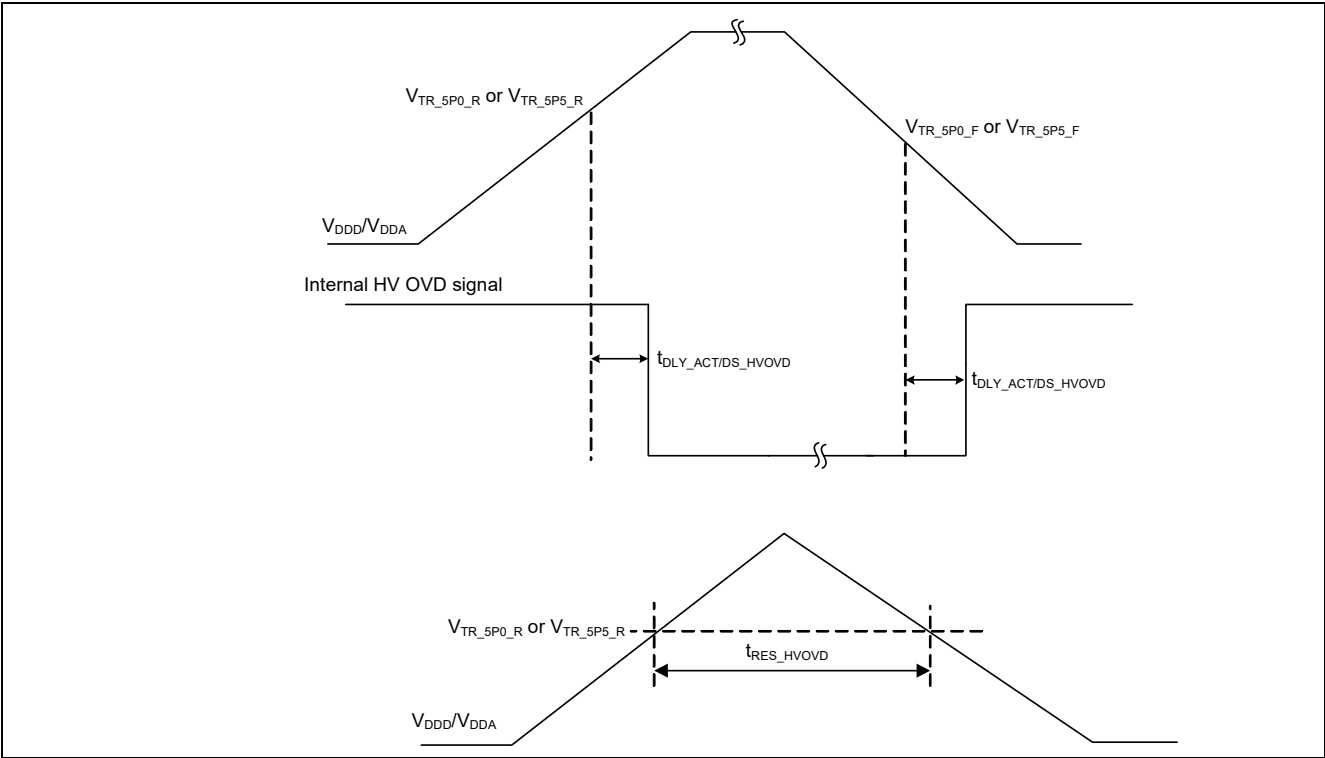


Figure 26-18 High-voltage OVD specifications

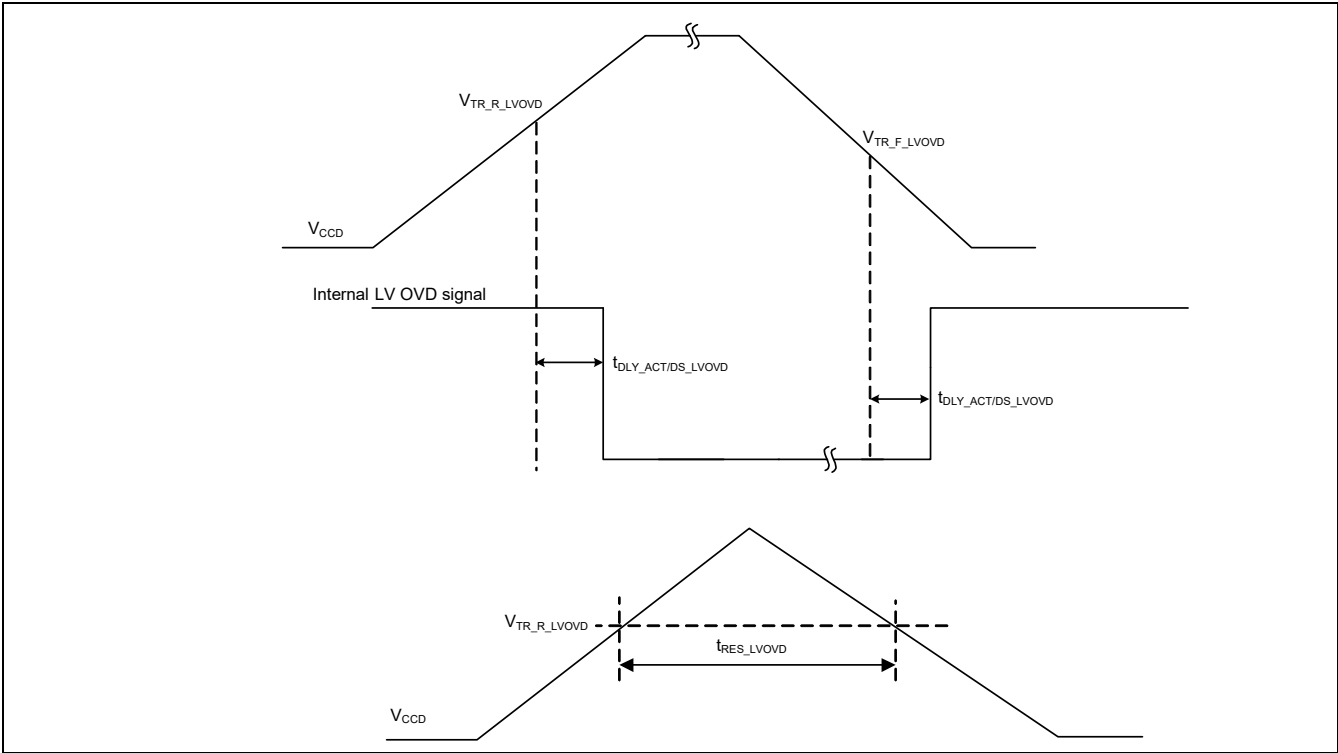


Figure 26-19 Low-voltage OVD specifications

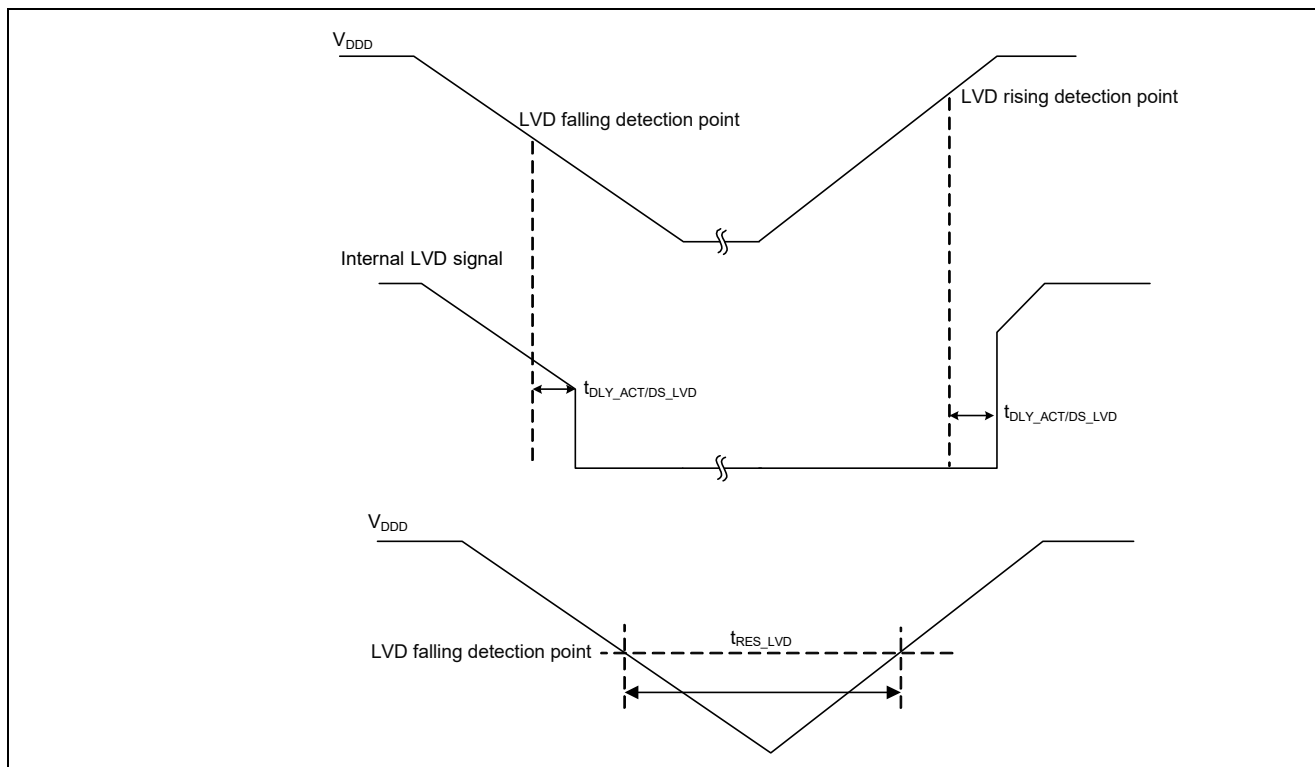


Figure 26-20 LVD specifications

26.11 Debug

All specifications are valid for $-40\text{ °C} \leq T_A \leq 125\text{ °C}$ and for 2.7 V to 5.5 V except where noted.

26.11.1 SWD

Table 26-17 SWD interface specifications [Conditions: drive_sel<1:0>= 00]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------------|---------------------------|-----------------|-----|----------------|-------|---|
| SID300 | f_{SWDCLK} | SWD clock input frequency | – | – | 10 | MHz | $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ |
| SID301 | $t_{\text{SWDI_SETUP}}$ | SWDI setup time | $0.25 \times T$ | – | – | ns | $T = 1 / f_{\text{SWDCLK}}$ |
| SID302 | $t_{\text{SWDI_HOLD}}$ | SWDI hold time | $0.25 \times T$ | – | – | ns | $T = 1 / f_{\text{SWDCLK}}$ |
| SID303 | $t_{\text{SWDO_VALID}}$ | SWDO valid time | – | – | $0.5 \times T$ | ns | $T = 1 / f_{\text{SWDCLK}}$ |
| SID304 | $t_{\text{SWDO_HOLD}}$ | SWDO hold time | 1 | – | – | ns | $T = 1 / f_{\text{SWDCLK}}$ |

26.11.2 JTAG

Table 26-18 JTAG AC specifications [Conditions: drive_sel<1:0>= 00]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------|----------------------|------|-----|-----|-------|--------------------|
| SID620 | t_{JCKH} | TCK HIGH time | 30 | – | – | ns | 30-pF load |
| SID621 | t_{JCKL} | TCK LOW time | 30 | – | – | ns | 30-pF load |
| SID622 | t_{JCP} | TCK clock period | 66.7 | – | – | ns | 30-pF load |
| SID623 | t_{JSU} | TDI/TMS setup time | 12 | – | – | ns | 30-pF load |
| SID624 | t_{JH} | TDI/TMS hold time | 12 | – | – | ns | 30-pF load |
| SID625 | t_{JZX} | TDO High-Z to active | – | – | 30 | ns | 30-pF load |
| SID626 | t_{JXZ} | TDO active to High-Z | – | – | 30 | ns | 30-pF load |
| SID627 | t_{JCO} | TDO clock to output | – | – | 30 | ns | 30-pF load |

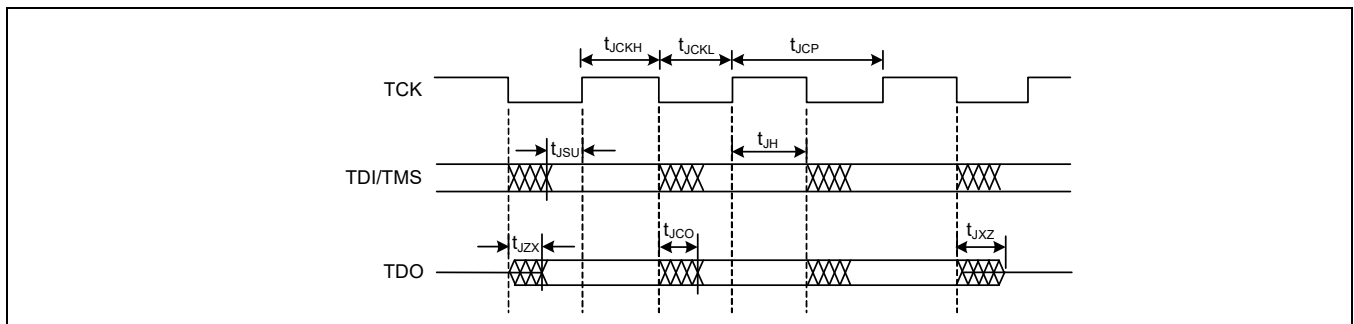


Figure 26-21 JTAG timing diagram

26.11.3 Trace

Table 26-19 Trace specifications [Conditions: drive_sel<1:0>= 00]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|--------------------|------------------------------|-----|-----|-----|-------|-----------------------------------|
| SID1412A | C_{TRACE} | Trace capacitive load | – | – | 30 | pF | |
| SID1412 | t_{TRACE_CYC} | Trace clock period | 40 | – | – | ns | Trace clock cycle time for 25 MHz |
| SID1413 | t_{TRACE_CLKL} | Trace clock LOW pulse width | 2 | – | – | ns | Clock low pulse width |
| SID1414 | t_{TRACE_CLKH} | Trace clock HIGH pulse width | 2 | – | – | ns | Clock high pulse width |
| SID1415A | t_{TRACE_SETUP} | Trace data setup time | 3 | – | – | ns | Trace data setup time |
| SID1416A | t_{TRACE_HOLD} | Trace data hold time | 2 | – | – | ns | Trace data hold time |

26.12 Clock specifications

All specifications are valid for $-40\text{ °C} \leq T_A \leq 125\text{ °C}$ and for 2.7 V to 5.5 V except where noted.

The following is a basic requirement on the clock frequency dependency of the cores: Cortex-M0+ core should run at an integer divider from the Cortex-M4 core clock.

Example combinations are listed in the [Table 26-20](#).

Table 26-20 Clock requirements

| Core Cortex-M4 Clock (MHz) | Core Cortex-M0+ Clock (MHz) |
|----------------------------|-----------------------------|
| 160 | 80 |
| 120 | 60 |
| 100 | 100 |
| 80 | 80 |

Table 26-21 Root and intermediate clocks^[56]

| Clock | Max Frequency (MHz) | Description |
|----------|---------------------|---|
| CLK_HF0 | 160 | Root clock for CPUSS, PERI |
| CLK_HF1 | 100 | Event generator (CLK_REF), Clock output on EXT_CLK pins (when used as output) |
| CLK_HF2 | 2 | CSV |
| CLK_FAST | 160 | Generated by dividing CLK_HF0, intermediate clock for CM4 |
| CLK_SLOW | 100 | Generated by clock gating CLK_PERI, intermediate clock for CM0+, Crypto, P-DMA, M-DMA |
| CLK_PERI | 100 | Generated by clock gating CLK_HF0, intermediate clock for LIN, SCB, PASS, CAN, TCPWM, IOSS, CPU trace |

Table 26-22 IMO AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|-------------------------|------|------|------|-------|--|
| SID310 | f_{IMOTOL} | IMO operating frequency | 7.92 | 8 | 8.08 | MHz | |
| SID311 | t_{STARTIMO} | IMO startup time | – | – | 7.5 | μs | Startup time to 90% of final frequency |
| SID312 | $I_{\text{IMO_ACT}}$ | IMO current | – | 13.5 | 22 | μA | Guaranteed by design |

Table 26-23 ILO AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|-------------------------|---------|--------|---------|-------|--|
| SID320 | f_{ILOTRIM} | ILO operating frequency | 31.1296 | 32.768 | 34.4064 | kHz | |
| SID321 | t_{STARTILO} | ILO startup time | – | 8 | 12 | μs | Startup time to 90% of final frequency |
| SID323 | I_{ILO} | ILO current | – | 500 | 2800 | nA | Guaranteed by design |

Note

56. Intermediate clocks that are not listed have the same limitations as that of their parent clock.

Electrical specifications

Table 26-24 ECO specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------------|---|-------|-----|-------|---------------|--|
| SID330 | f_{ECO} | Crystal frequency range | 3.988 | – | 33.34 | MHz | |
| SID332 | R_{FDBK} | Feedback resistor value. Min: RTRIM = 3; Max: RTRIM = 0 with 100-k Ω step size on RTRIM | 100 | – | 400 | k Ω | Guaranteed by design |
| SID333 | I_{ECO3} | ECO current at $T_J = 150\text{ }^{\circ}\text{C}$ | – | – | 2000 | μA | Maximum operation current with a 33-MHz crystal, max 18-pF load |
| SID334 | $t_{\text{START_4M}}$ | 4-MHz ECO startup time ^[57] | – | – | 10 | ms | Time from set CLK_ECO_- CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READ Y is set to 1 (See Clock Timing Diagrams) |
| SID335 | $t_{\text{START_33M}}$ | 33-MHz ECO startup time ^[57] | – | – | 1 | ms | Time from set CLK_ECO_- CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READ Y is set to 1 (See Clock Timing Diagrams) |

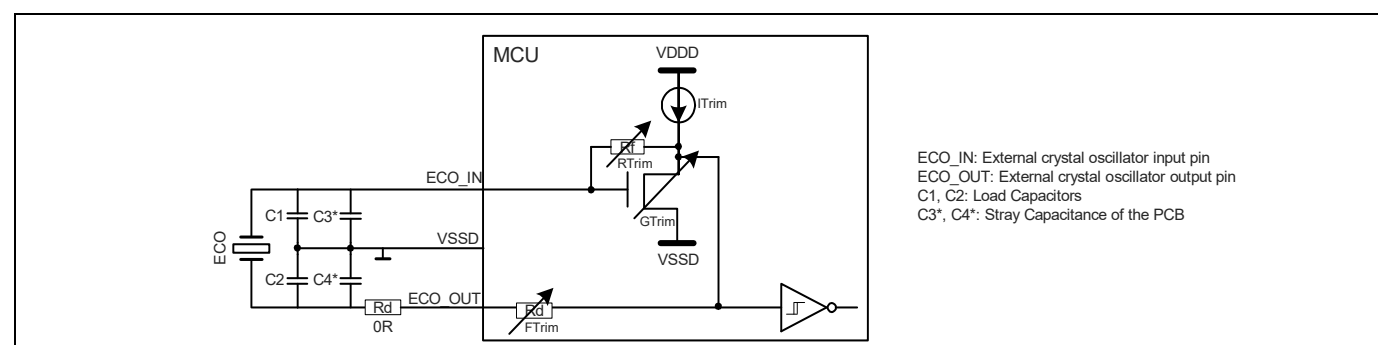


Figure 26-22 ECO connection scheme^[58]

Table 26-25 PLL specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|---------------------------------|-------|-----|------|-------|---|
| SID340 | PLL_LOCK | Time to achieve PLL lock | – | – | 35 | μs | |
| SID341 | f _{PLL_OUT} | Output frequency from PLL block | 11 | – | 160 | MHz | |
| SID342 | PLL_LJIT1 | Long term jitter | –0.25 | – | 0.25 | ns | For 125 ns f _{PLL_VCO} : 320 MHz f _{PLL_OUT} : 40 MHz to 160 MHz f _{PLL_PFD} : 8 MHz f _{PLL_IN} : ECO |
| SID343 | PLL_LJIT2 | Long term jitter | –0.5 | – | 0.5 | ns | For 500 ns f _{PLL_VCO} : 320 MHz f _{PLL_OUT} : 40 MHz to 160 MHz f _{PLL_PFD} : 8 MHz f _{PLL_IN} : ECO |

Notes

57. Mainly depends on the external crystal.

58. Please refer to the family-specific Architecture TRM for more information on crystal requirements (002-19314, TRAVEO™ T2G Automotive Body Controller Entry Family Architecture Technical Reference Manual (TRM)).

Table 26-25 PLL specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---|-------|-----|-------|---------|---|
| SID344 | PLL_LJIT3 | Long term jitter | -0.5 | - | 0.5 | ns | For 1000 ns f_{PLL_VCO} : 320 MHz f_{PLL_OUT} : 40 MHz to 160 MHz f_{PLL_PFD} : 8 MHz f_{PLL_IN} : ECO |
| SID345A | PLL_LJIT5 | Long term jitter | -0.75 | - | 0.75 | ns | For 10000 ns f_{PLL_VCO} : 320 MHz f_{PLL_OUT} : 40 MHz to 160 MHz f_{PLL_PFD} : 8 MHz f_{PLL_IN} : ECO |
| SID346 | f_{PLL_IN} | PLL input frequency | 3.988 | - | 33.34 | MHz | |
| SID347 | I_{PLL_160M1} | PLL operating current ($f_{OUT} = 160$ MHz) | - | 740 | 1110 | μA | $f_{IN} = 4$ MHz, $f_{PFD} = 4$ MHz, $f_{VCO} = 320$ MHz, $f_{OUT} = 160$ MHz |
| SID347A | I_{PLL_160M2} | PLL operating current ($f_{OUT} = 160$ MHz) | - | 750 | 1125 | μA | $f_{IN} = 8$ MHz, $f_{PFD} = 8$ MHz, $f_{VCO} = 320$ MHz, $f_{OUT} = 160$ MHz |
| SID347B | I_{PLL_160M3} | PLL operating current ($f_{OUT} = 160$ MHz) | - | 750 | 1125 | μA | $f_{IN} = 16$ MHz, $f_{PFD} = 8$ MHz, $f_{VCO} = 320$ MHz, $f_{OUT} = 160$ MHz |
| SID339 | I_{PLL_100M1} | PLL operating current ($f_{OUT} = 100$ MHz) | - | 520 | 780 | μA | $f_{IN} = 4$ MHz, $f_{PFD} = 4$ MHz, $f_{VCO} = 200$ MHz, $f_{OUT} = 100$ MHz |
| SID339A | I_{PLL_100M2} | PLL operating current ($f_{OUT} = 100$ MHz) | - | 530 | 795 | μA | $f_{IN} = 8$ MHz, $f_{PFD} = 8$ MHz, $f_{VCO} = 200$ MHz, $f_{OUT} = 100$ MHz |
| SID339B | I_{PLL_100M3} | PLL operating current ($f_{OUT} = 100$ MHz) | - | 530 | 795 | μA | $f_{IN} = 16$ MHz, $f_{PFD} = 8$ MHz, $f_{VCO} = 200$ MHz, $f_{OUT} = 100$ MHz |
| SID348 | I_{PLL_80M1} | PLL operating current ($f_{OUT} = 80$ MHz) | - | 520 | 780 | μA | $f_{IN} = 4$ MHz, $f_{PFD} = 4$ MHz, $f_{VCO} = 240$ MHz, $f_{OUT} = 80$ MHz |
| SID348A | I_{PLL_80M2} | PLL operating current ($f_{OUT} = 80$ MHz) | - | 530 | 795 | μA | $f_{IN} = 8$ MHz, $f_{PFD} = 8$ MHz, $f_{VCO} = 240$ MHz, $f_{OUT} = 80$ MHz |
| SID348B | I_{PLL_80M3} | PLL operating current ($f_{OUT} = 80$ MHz) | - | 530 | 795 | μA | $f_{IN} = 16$ MHz, $f_{PFD} = 8$ MHz, $f_{VCO} = 240$ MHz, $f_{OUT} = 80$ MHz |
| SID348C | f_{PLL_VCO} | VCO frequency | 170 | - | 400 | MHz | |
| SID349C | f_{PLL_PFD} | PFD frequency | 3.988 | - | 8 | MHz | |

Table 26-28 External clock input specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|--------------------------------|------|-----|-----|-------|---|
| SID366 | f_{EXT} | External clock input frequency | 0.25 | – | 80 | MHz | For EXT_CLK pin (all input level settings: CMOS, TTL, Automotive) |
| SID367 | EXT_DC | External clock duty cycle | 45 | – | 55 | % | |

26.12.1 Clock timing diagrams

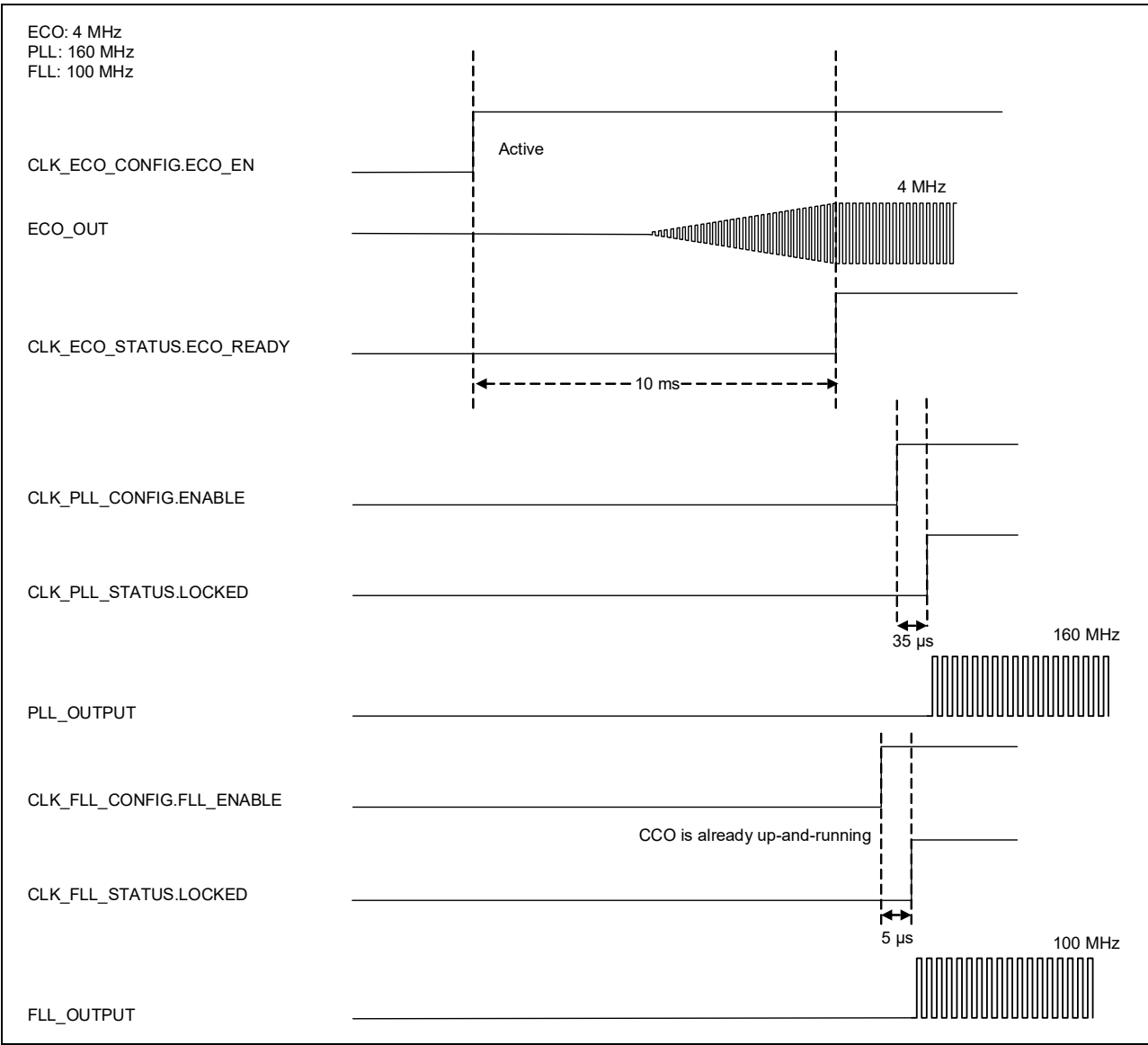


Figure 26-24 ECO to PLL or FLL diagram

Electrical specifications

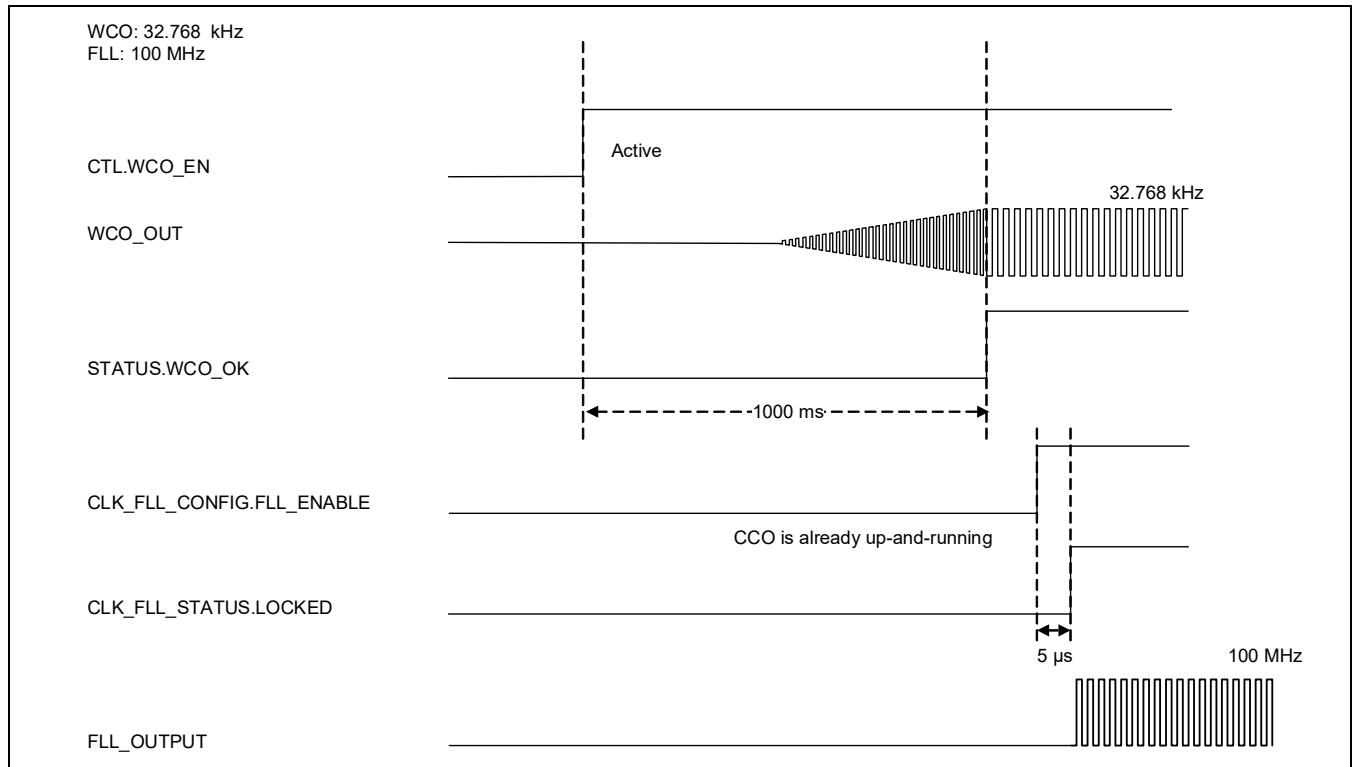


Figure 26-25 WCO to FLL Diagram

Table 26-29 MCWDT timeout specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------|-----------------------|-------|-----|------|-------|---|
| SID410 | t_{MCWDT1} | Minimum MCWDT timeout | 58.12 | – | – | μs | When using the ILO (32.768 kHz + 5%) and 16-bit MCWDT counter Guaranteed by design |
| SID411 | t_{MCWDT2} | Maximum MCWDT timeout | – | – | 2.11 | s | When using the ILO (32.768 kHz – 5%) and 16-bit MCWDT counter Guaranteed by design |

Table 26-30 WDT timeout specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------|---------------------|-------|------|-------|-------|--|
| SID412 | t_{WDT1} | Minimum WDT timeout | 58.12 | – | – | μs | When using the ILO (32.768 kHz + 5%) and 32-bit WDT counter Guaranteed by design |
| SID413 | t_{WDT2} | Maximum WDT timeout | – | – | 38.33 | h | When using the ILO (32.768 kHz – 5%) and 32-bit WDT counter Guaranteed by design |
| SID414 | t_{WDT3} | Default WDT timeout | – | 1000 | – | ms | When using the ILO and 32-bit WDT counter at 0x8000 (default value), guaranteed by design |

27 Ordering information

The CYT2B7 microcontroller part numbers and features are listed in [Table 27-1](#). The Arm® TAP JTAG ID is 0x6BA0 0477.

Table 27-1 CYT2B7 ordering information

| Device Code | Ordering Code ^[61] | Package | Code-flash (KB) | Work-flash (KB) | RAM (KB) | ADC Channels | SCB Channels | LIN Channels | CANFD Channels | eSHE/HSM | Temperature Grade | JTAG ID CODE |
|----------------------------|-------------------------------|----------|----------------------|--------------------|----------|--------------|--------------|--------------|----------------|----------|-------------------|----------------------------|
| CYT2B73BAS ^[62] | CYT2B73BADQ0A25GS | 64-LQFP | 1088 ^[63] | 96 ^[64] | 128 | 27 | 5 | 6 | 5 | eSHE | S ^[65] | 0x2E3C9069 ^[67] |
| CYT2B73BAE ^[62] | CYT2B73BADQ0A2EGS | 64-LQFP | 1088 | 96 | 128 | 27 | 5 | 6 | 5 | eSHE | E ^[66] | 0x2E3C9069 |
| CYT2B73CAS | CYT2B73CADQ0A25GS | 64-LQFP | 1088 | 96 | 128 | 27 | 5 | 6 | 5 | HSM | S | 0x2E3CA069 |
| CYT2B73CAE | CYT2B73CADQ0A2EGS | 64-LQFP | 1088 | 96 | 128 | 27 | 5 | 6 | 5 | HSM | E | 0x2E3CA069 |
| CYT2B74BAS ^[62] | CYT2B74BADQ0A25GS | 80-LQFP | 1088 | 96 | 128 | 34 | 6 | 7 | 6 | eSHE | S | 0x2E3D1069 |
| CYT2B74BAE ^[62] | CYT2B74BADQ0A2EGS | 80-LQFP | 1088 | 96 | 128 | 34 | 6 | 7 | 6 | eSHE | E | 0x2E3D1069 |
| CYT2B74CAS | CYT2B74CADQ0A25GS | 80-LQFP | 1088 | 96 | 128 | 34 | 6 | 7 | 6 | HSM | S | 0x2E3D2069 |
| CYT2B74CAE | CYT2B74CADQ0A2EGS | 80-LQFP | 1088 | 96 | 128 | 34 | 6 | 7 | 6 | HSM | E | 0x2E3D2069 |
| CYT2B75BAS ^[62] | CYT2B75BADQ0A25GS | 100-LQFP | 1088 | 96 | 128 | 39 | 8 | 7 | 6 | eSHE | S | 0x2E3D9069 |
| CYT2B75BAE ^[62] | CYT2B75BADQ0A2EGS | 100-LQFP | 1088 | 96 | 128 | 39 | 8 | 7 | 6 | eSHE | E | 0x2E3D9069 |
| CYT2B75CAS | CYT2B75CADQ0A25GS | 100-LQFP | 1088 | 96 | 128 | 39 | 8 | 7 | 6 | HSM | S | 0x2E3DA069 |
| CYT2B75CAE | CYT2B75CADQ0A2EGS | 100-LQFP | 1088 | 96 | 128 | 39 | 8 | 7 | 6 | HSM | E | 0x2E3DA069 |
| CYT2B77BAS ^[62] | CYT2B77BADQ0A25GS | 144-LQFP | 1088 | 96 | 128 | 54 | 8 | 8 | 6 | eSHE | S | 0x2E3E1069 |
| CYT2B77BAE ^[62] | CYT2B77BADQ0A2EGS | 144-LQFP | 1088 | 96 | 128 | 54 | 8 | 8 | 6 | eSHE | E | 0x2E3E1069 |
| CYT2B77CAS | CYT2B77CADQ0A25GS | 144-LQFP | 1088 | 96 | 128 | 54 | 8 | 8 | 6 | HSM | S | 0x2E3E2069 |
| CYT2B77CAE | CYT2B77CADQ0A2EGS | 144-LQFP | 1088 | 96 | 128 | 54 | 8 | 8 | 6 | HSM | E | 0x2E3E2069 |
| CYT2B78BAS ^[62] | CYT2B78BADQ0A25GS | 176-LQFP | 1088 | 96 | 128 | 64 | 8 | 8 | 6 | eSHE | S | 0x2E3E9069 |
| CYT2B78BAE ^[62] | CYT2B78BADQ0A2EGS | 176-LQFP | 1088 | 96 | 128 | 64 | 8 | 8 | 6 | eSHE | E | 0x2E3E9069 |
| CYT2B78CAS | CYT2B78CADQ0A25GS | 176-LQFP | 1088 | 96 | 128 | 64 | 8 | 8 | 6 | HSM | S | 0x2E3EA069 |
| CYT2B78CAE | CYT2B78CADQ0A2EGS | 176-LQFP | 1088 | 96 | 128 | 64 | 8 | 8 | 6 | HSM | E | 0x2E3EA069 |

Notes

61. Supported shipment types are "Tray" (default) and "Tape and Reel". Add the character "T" at the end to get the ordering code for "Tape and Reel" shipment type.
62. 3DES/SHA-1/SHA-2/SHA-3/CRC/Vector unit for asymmetric cryptography features are not supported.
63. Code-flash size 1088 KB = 32 KB × 30 (Large Sectors) + 8 KB × 16 (Small Sectors)
64. Work-flash size 96 KB = 2 KB × 36 (Large Sectors) + 128 B × 192 (Small Sectors).
65. S-grade Temperature (–40 °C to 105 °C).
66. E-grade Temperature (–40 °C to 125 °C).
67. JTAG ID CODE bits 12 through 27, represents the Silicon ID of the device.

27.1 Part number nomenclature

Table 27-2 Device code nomenclature

| Field | Description | Value | Meaning |
|-------|-------------------------------------|-------|--------------------------------|
| CY | Cypress Prefix | CY | |
| T | Category | T | TRAVEO™ |
| 2 | Family Name | 2 | TRAVEO™ T2G (Core M4) |
| B | Application | B | Body |
| D | Code-flash/Work-flash/SRAM quantity | 7 | 1088 KB / 96 KB / 128 KB |
| P | Packages | 3 | 64-LQFP |
| | | 4 | 80-LQFP |
| | | 5 | 100-LQFP |
| | | 7 | 144-LQFP |
| | | 8 | 176-LQFP |
| H | Hardware Option | B | eSHE – on, HSM – off, RSA - 2K |
| | | C | eSHE – on, HSM – on, RSA - 2K |
| I | Marketing Option | A | No options |
| C | Temperature Grade | S | S-grade (–40 °C to 105 °C) |
| | | E | E-grade (–40 °C to 125 °C) |

Table 27-3 Ordering code nomenclature

| Field | Description | Value | Meaning |
|-------|-------------------------------------|-------|--------------------------------|
| CY | Cypress Prefix | CY | |
| T | Category | T | TRAVEO™ |
| 2 | Family Name | 2 | TRAVEO™ T2G (Core M4) |
| B | Application | B | Body |
| D | Code-flash/Work-flash/SRAM quantity | 7 | 1088 KB / 96 KB / 128 KB |
| P | Packages | 3 | 64 LQFP |
| | | 4 | 80 LQFP |
| | | 5 | 100 LQFP |
| | | 7 | 144 LQFP |
| | | 8 | 176 LQFP |
| H | Hardware Option | B | eSHE – on, HSM – off, RSA - 2K |
| | | C | eSHE – on, HSM – on, RSA - 2K |
| I | Marketing Option | A | No options |
| R | Revision | A | First revision |
| | | B | Second revision |
| | | C | Third revision |
| | | D | Fourth revision |
| F | Fab Location | Q | UMC (Fab 12i) Singapore |
| X | Reserved | 0 | Reserved |
| K | Package Code | AZ | LQFP |
| C | Temperature Grade | S | S-grade (–40 °C to 105 °C) |
| | | E | E-grade (–40 °C to 125 °C) |
| Q | Quality Grade | ES | Engineering samples |
| | | GS | Standard grade of automotive |
| S | Shipment Type | Blank | Tray shipment |
| | | T | Tape and Reel shipment |

28 Packaging

CYT2B7 is offered in the packages listed in the [Table 28-1](#).

Table 28-1 Package Information

| Package | Dimensions | Contact/Lead pitch | Coefficient of thermal expansion | I/O Pins |
|----------|------------------------|--------------------|--|----------|
| 176-LQFP | 24 × 24 × 1.7 mm (max) | 0.5 mm | $a1^{[70]} = 8.5 \text{ ppm/}^\circ\text{C}$, $a2^{[71]} = 33.8 \text{ ppm/}^\circ\text{C}$ | 152 |
| 144-LQFP | 20 × 20 × 1.7 mm (max) | 0.5 mm | $a1^{[70]} = 8.5 \text{ ppm/}^\circ\text{C}$, $a2^{[71]} = 33.7 \text{ ppm/}^\circ\text{C}$ | 122 |
| 100-LQFP | 14 × 14 × 1.7 mm (max) | 0.5 mm | $a1^{[70]} = 8.5 \text{ ppm/}^\circ\text{C}$, $a2^{[71]} = 33.6 \text{ ppm/}^\circ\text{C}$ | 78 |
| 80-LQFP | 12 × 12 × 1.7 mm (max) | 0.5 mm | $a1^{[70]} = 8.5 \text{ ppm/}^\circ\text{C}$, $a2^{[71]} = 33.5 \text{ ppm/}^\circ\text{C}$ | 63 |
| 64-LQFP | 10 × 10 × 1.7 mm (max) | 0.5 mm | $a1^{[70]} = 8.5 \text{ ppm/}^\circ\text{C}$, $a2^{[71]} = 33.2 \text{ ppm/}^\circ\text{C}$ | 49 |

Table 28-2 Package Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------------|---|------------|-----|-----|------|---------|
| T_A | Operating ambient temperature | S-grade | -40 | – | 105 | °C |
| T_A | Operating ambient temperature | E-grade | -40 | – | 125 | °C |
| T_J | Operating junction temperature | – | – | – | 150 | °C |
| $R_{\theta JA}$ | Package thermal resistance, junction to ambient θ_{JA} ^[68, 69] | 64 LQFP | – | – | 37.6 | °C/Watt |
| | | 80 LQFP | – | – | 32.7 | °C/Watt |
| | | 100 LQFP | – | – | 29.8 | °C/Watt |
| | | 144 LQFP | – | – | 26.2 | °C/Watt |
| | | 176 LQFP | – | – | 25.9 | °C/Watt |
| $R_{\theta JB}$ | Package θ_{JB} | 64 LQFP | – | – | 32.0 | °C/Watt |
| | | 80 LQFP | – | – | 26.7 | °C/Watt |
| | | 100 LQFP | – | – | 21.3 | °C/Watt |
| | | 144 LQFP | – | – | 20.9 | °C/Watt |
| | | 176 LQFP | – | – | 20.8 | °C/Watt |
| $R_{\theta JC}$ | Package thermal resistance, junction to case θ_{JC} | 64 LQFP | – | – | 7.8 | °C/Watt |
| | | 80 LQFP | – | – | 6.6 | °C/Watt |
| | | 100 LQFP | – | – | 5.6 | °C/Watt |
| | | 144 LQFP | – | – | 4.2 | °C/Watt |
| | | 176 LQFP | – | – | 3.8 | °C/Watt |

Notes

68.Board condition complies to JESD51-7(4 Layers)

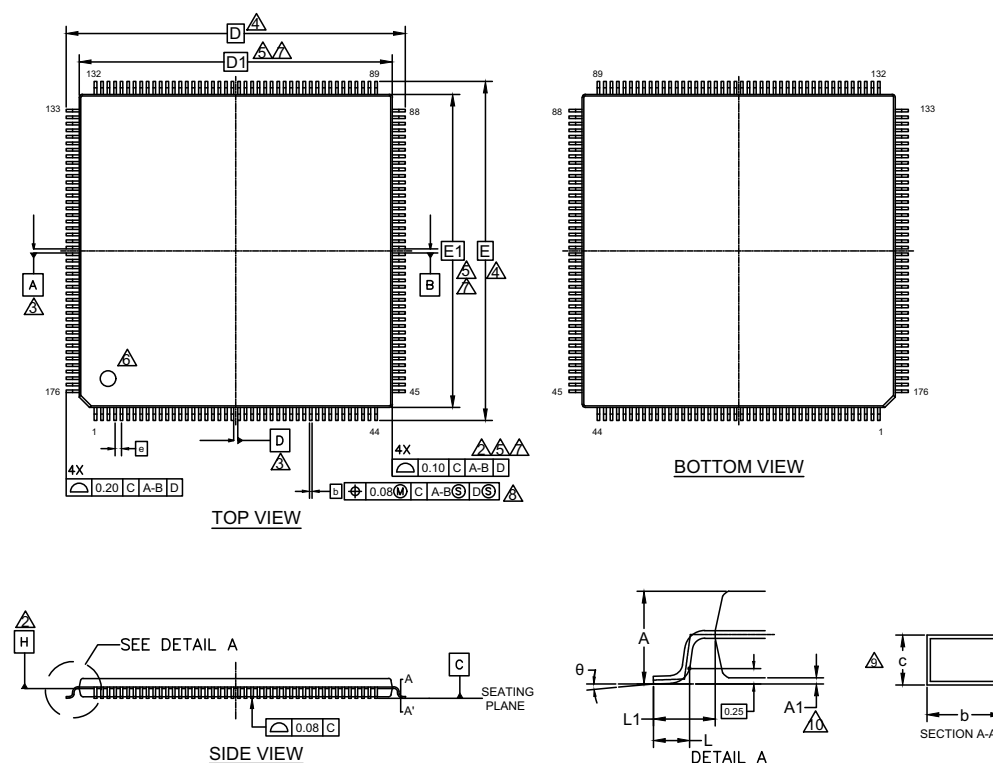
69.Maximum value °C/Watt shown is for $T_A = 125^\circ\text{C}$.

70. $a1$ = CTE (Coefficient of Thermal Expansion) value below T_g (ppm/°C) (T_g is glass transition temperature which is 131°C).

71. $a2$ = CTE value above T_g (ppm/°C).

Table 28-3 Solder Reflow Peak Temperature, Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | Maximum Peak Temperature (°C) | Maximum Time at Peak Temperature (seconds) | MSL |
|----------|-------------------------------|--|-----|
| 176 LQFP | 260 | 30 seconds | 3 |
| 144 LQFP | 260 | 30 seconds | 3 |
| 100 LQFP | 260 | 30 seconds | 3 |
| 80 LQFP | 260 | 30 seconds | 3 |
| 64 LQFP | 260 | 30 seconds | 3 |



NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 *A

Figure 28-1 176-LQFP package outline

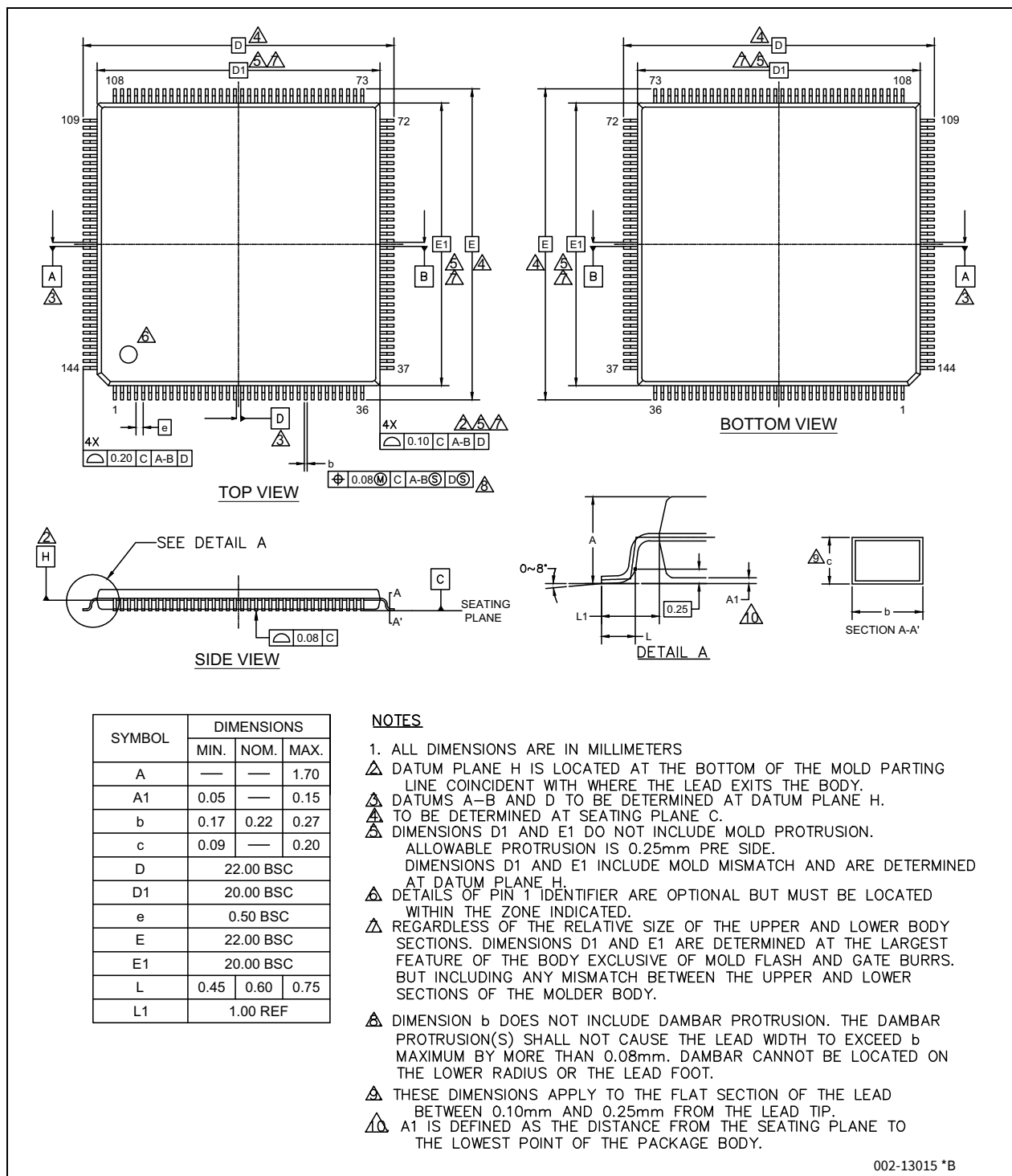


Figure 28-2 144-LQFP package outline

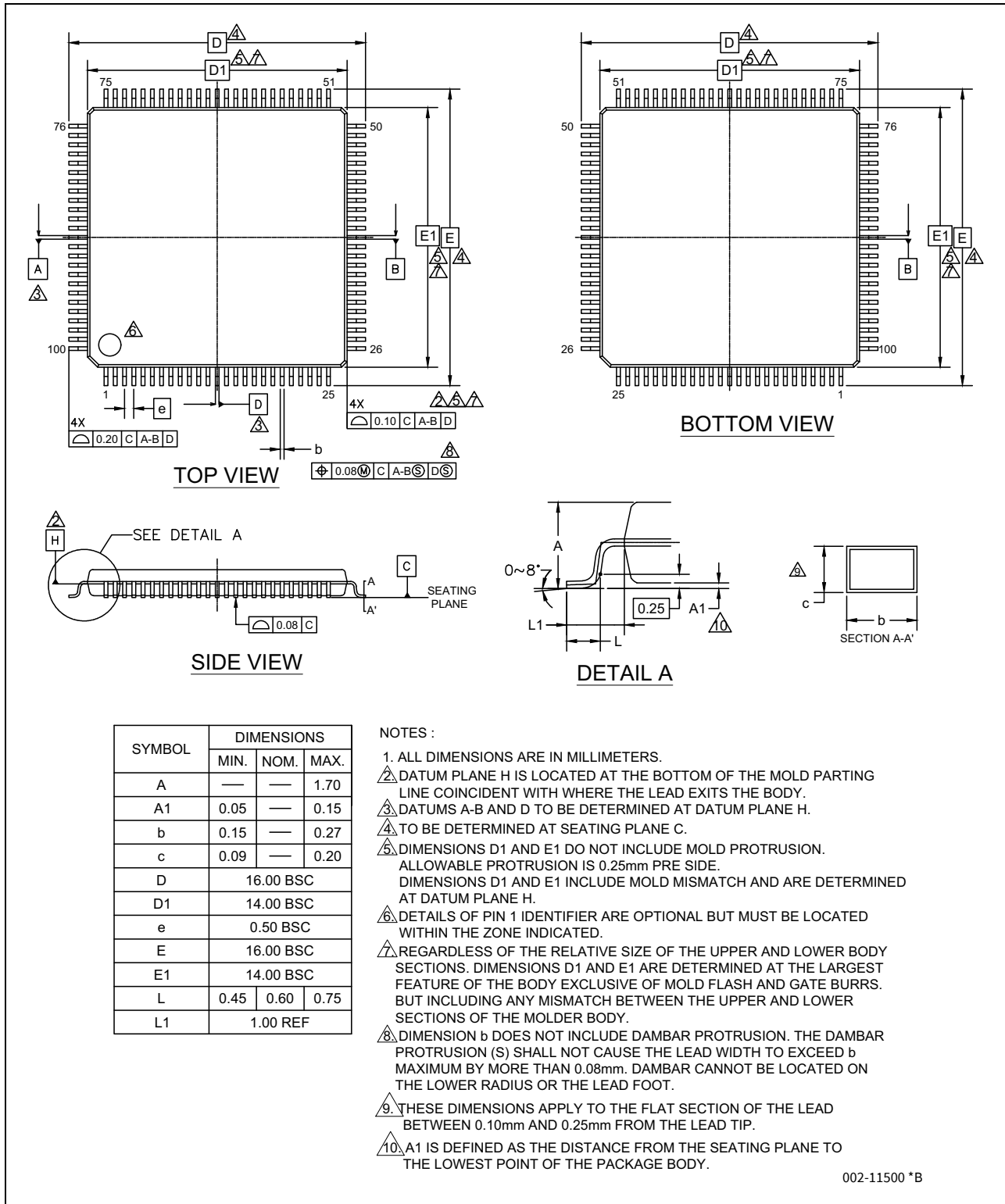
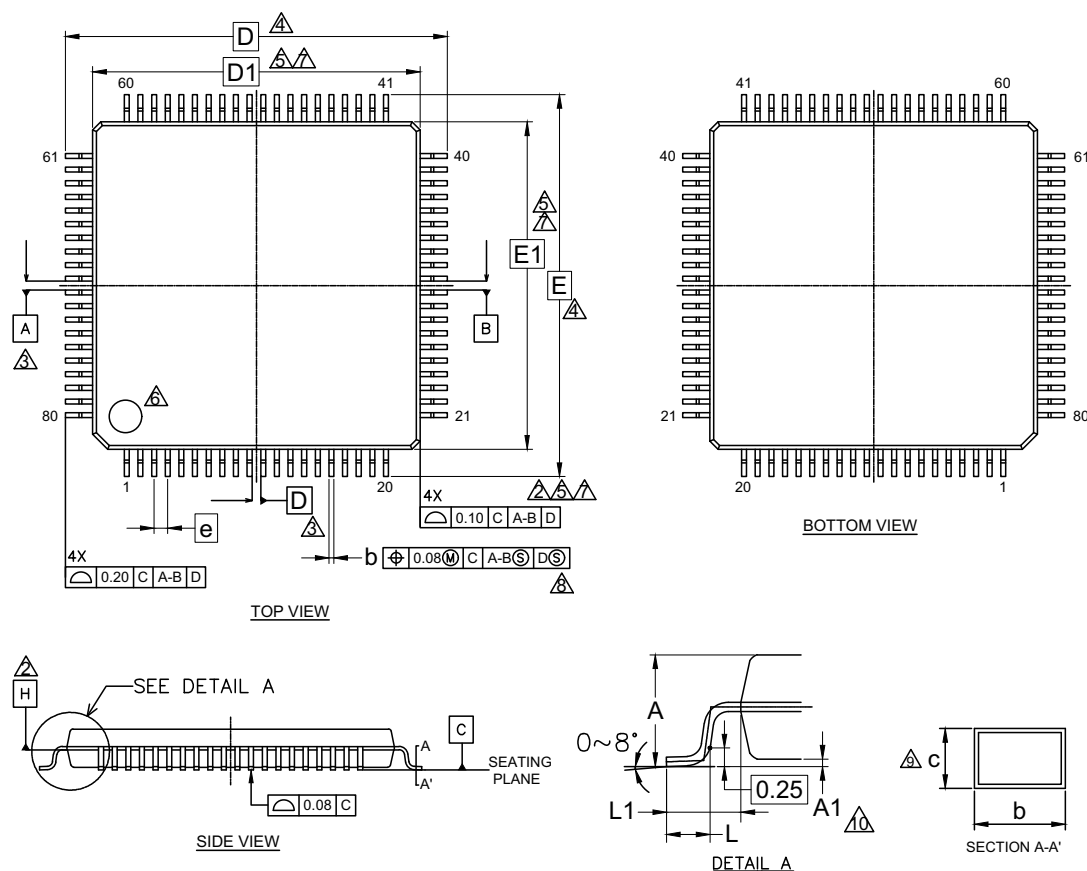


Figure 28-3 100-LQFP package outline

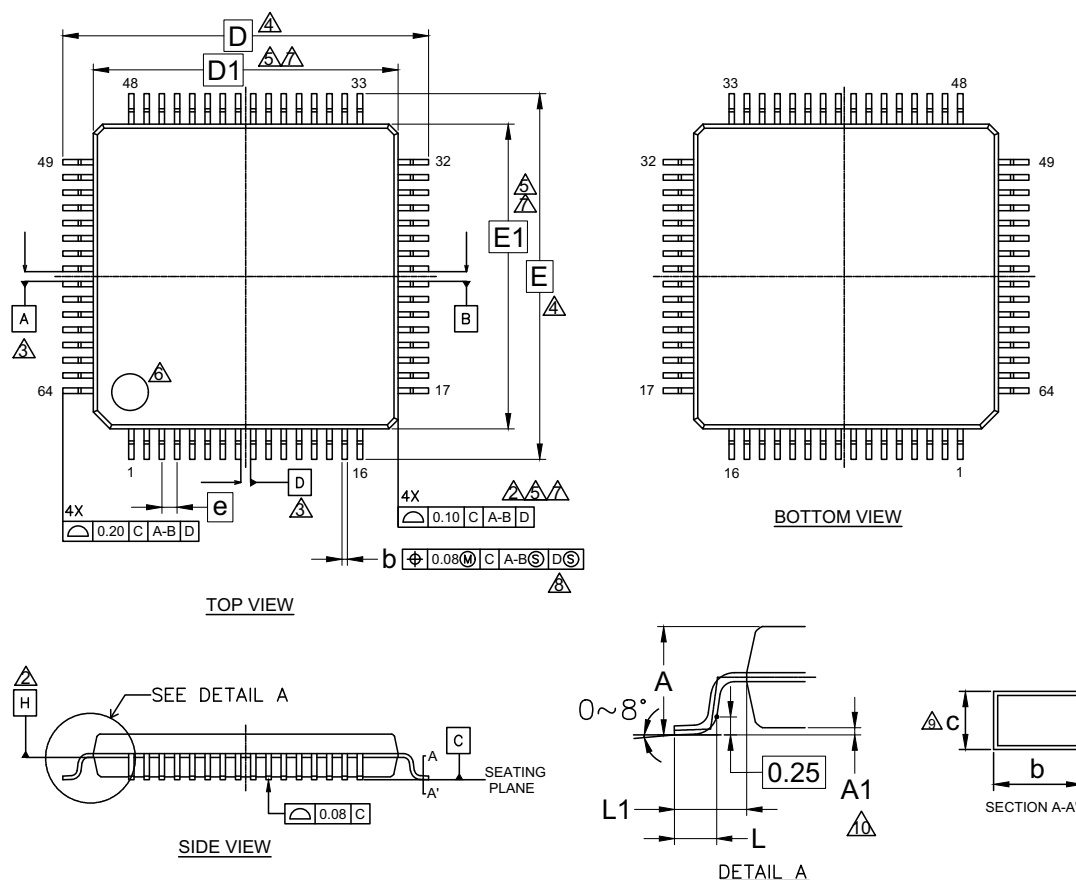


NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
1. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
3. TO BE DETERMINED AT SEATING PLANE C.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
6. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11501 *A

Figure 28-4 80-LQFP package outline



NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 *A

Figure 28-5 64-LQFP package outline

29 Appendix

29.1 Bootloading or end-of-line programming

- Triggered at device startup, if a trigger condition is applied
- Either CAN or LIN communication may be used
- Bootloader polls for the communication on CAN or LIN at separate time frames, until the overall 300-second timeout is reached
- If a bootloader command is received on either communication interface, the polling stops and bootloader starts using this interface

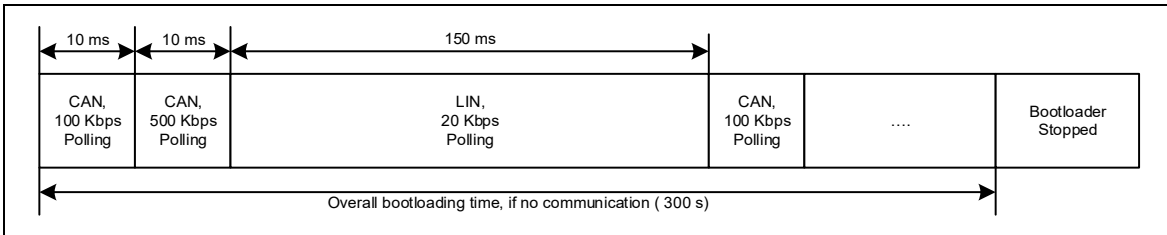


Figure 29-1 Bootloading sequence

Table 29-1 CAN interface details

| Sl. No. | CAN interface | Configuration |
|---------|---------------------------------|-----------------------------|
| 1 | CAN Mode | Classic CAN |
| 2 | CAN Instance | CAN0, Channel#1 |
| 3 | CAN TX | P0.2 / CAN0_1_TX |
| 4 | CAN RX | P0.3 / CAN0_1_RX |
| 5 | CAN Transceiver NSTB / EN (Low) | P23.3 (optional) |
| 6 | CAN Transceiver EN / EN (High) | P2.1 (optional) |
| 7 | CAN RX Message ID | 0x1A1 |
| 8 | CAN TX Message ID | 0x1B1 |
| 9 | Baud | 100 or 500 kbps alternating |

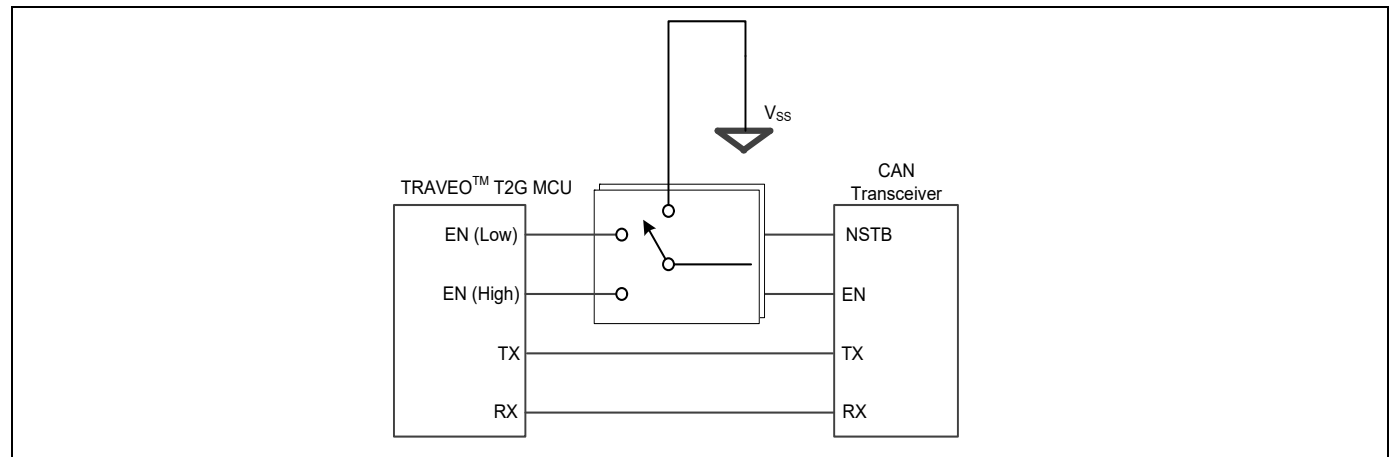


Figure 29-2 MCU to CAN transceiver connections

Table 29-2 LIN interface details

| Sl. No. | LIN interface | Configuration |
|---------|------------------------|------------------|
| 1 | LIN Type | LIN0, Channel#1 |
| 2 | LIN Mode | Slave |
| 3 | LIN Checksum Type | Classic |
| 4 | LIN TX | P0.1 / LIN1_TX |
| 5 | LIN RX | P0.0 / LIN1_RX |
| 6 | LIN EN / EN (High) | P2.1 (optional) |
| 7 | LIN EN (Low) | P23.3 (optional) |
| 8 | LIN TX PID | 0x46 |
| 9 | LIN RX PID | 0x45 |
| 10 | Baud | 20 or 115.2 kbps |
| 11 | Break Field Length | 11 |
| 12 | Break Delimiter Length | 1 bit |

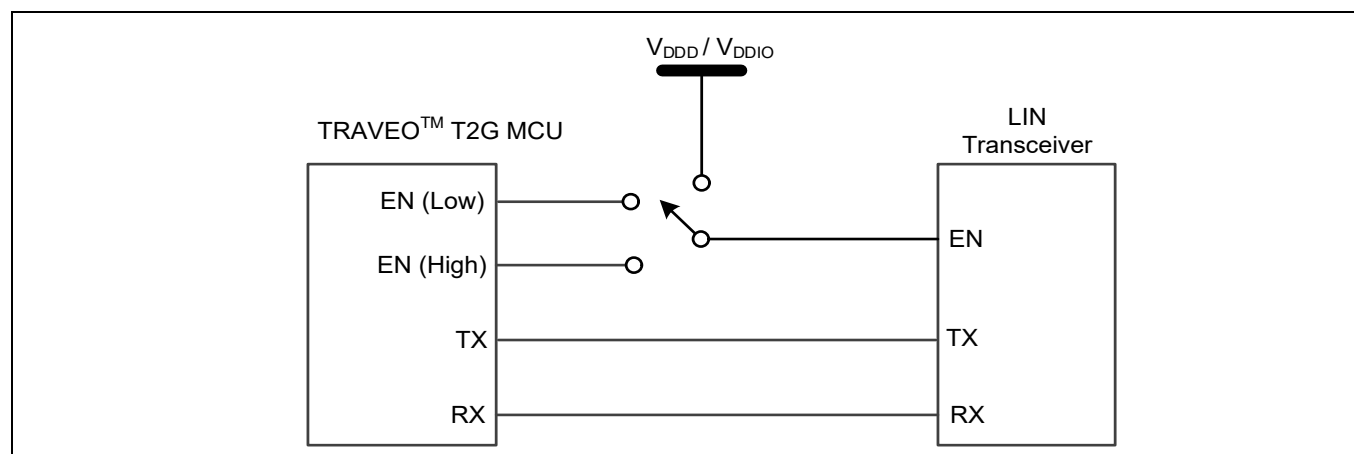


Figure 29-3 MCU to LIN transceiver connections

29.2 External IP revisions

Table 29-3 IP revisions

| Module | IP | Revision | Vendor |
|------------------|----------------|--------------------------------|--------|
| CANFD | mxttcanfd | M_TTCAN IP revision: Rev.3.2.3 | Bosch |
| Arm® Cortex®-M0+ | armcm0p | Cortex®-M0+-r0p1 | Arm® |
| Arm® Cortex®-M4 | armcm4 | Cortex®-M4-r0p1 | Arm® |
| Arm® Coresight | armcoresighttk | CoreSight-SoC-TM100-r3p2 | Arm® |

30 Acronyms

Table 30-1 Acronyms used in the Document

| Acronym | Description | Acronym | Description |
|---------|---|---------|---|
| A/D | Analog to Digital | JTAG | Joint test action group |
| ABS | Absolute | LDO | Low drop out regulators |
| ADC | Analog to Digital converter | LIN | Local Interconnect Network, a communications protocol |
| AES | Advanced encryption standard | LVD | Low voltage detection |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, Arm® data transfer bus | OTA | Over-the-air programming |
| Arm® | Advanced RISC machine, a CPU architecture | OTP | One-time programmable |
| ASIL | Automotive safety integrity level | OVD | Over voltage detection |
| BOD | Brown-out detection | P-DMA | Peripheral-Direct Memory Access same as DW |
| CAN FD | Controller Area Network with Flexible Data rate | PLL | Phase-locked loop |
| CMOS | Complementary metal-oxide-semiconductor | POR | Power-on reset |
| CPU | Central Processing Unit | PPU | Peripheral protection unit |
| CRC | Cyclic redundancy check, an error-checking protocol | PRNG | Pseudorandom number generator |
| CSV | Clock supervisor | PWM | Pulse-width modulation |
| CTI | Cross trigger interface | MCU | Microcontroller Unit |
| DES | Data encryption standard | MCWDT | Multi-counter watchdog timer |
| DFT | Design-For-Test | M-DMA | Memory-Direct Memory Access |
| DW | Datwire same as P-DMA | MISO | SPI Master-in slave-out |
| ECC | Error correcting code/Elliptical curve cryptography | MMIO | Memory mapped I/O |
| ECO | External crystal oscillator | MOSI | SPI Master-out slave-in |
| ETM | Embedded Trace Macrocell | MPU | Memory protection unit |
| EVTGEN | Event Generator | MTB | Micro trace buffer |
| FLL | Frequency-locked loop | MUL | Multiplier |
| FPU | Floating point unit | MUX | Multiplexer |
| GHS | Green Hills tool chain with Multi IDE | NVIC | Nested vectored interrupt controller |
| GPIO | General purpose input/output | RAM | Random access memory |
| HSM | Hardware security module | RISC | Reduced-instruction-set computing |
| I/O | Input/output | ROM | Read only memory |
| I²C | Inter-Integrated Circuit, a communications protocol | RSA | Rivest-Shamir-Adleman Public Key Encryption Algorithm |
| ILO | Internal low-speed oscillator | RTC | Real-time clock |
| IMO | Internal main oscillator | SAR | Successive approximation register |

Table 30-1 Acronyms used in the Document *(continued)*

| Acronym | Description | Acronym | Description |
|---------|--|---------|---|
| IOSS | Input/output sub-system | SCB | Serial communication block |
| IPC | Inter-processor communication | SCL | I ² C serial clock |
| IrDA | Infrared interface | SDA | I ² C serial data |
| IRQ | Interrupt request | SECCED | Single error correction, double error detection |
| SHA | Secure hash algorithm | TCPWM | Timer/Counter Pulse-width modulator |
| SHE | Secure hardware extension | TTL | Transistor-transistor logic |
| SMPU | Shared memory protection unit | TRNG | True random number generator |
| SPI | Serial peripheral interface, a communications protocol | UART | Universal Asynchronous Transmitter Receiver |
| SRAM | Static random access memory | WCO | Watch crystal oscillator |
| SWD | Serial wire debug | WDT | Watchdog timer reset |
| SWJ | Serial wire JTAG | | |

31 Errata

This section describes the errata for the CYT2B7 product family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Table 1.

| Part Number |
|------------------|
| All CYT2B7 parts |

CYT2B7 Qualification Status

Production samples

CYT2B7 Errata Summary

The following table defines the errata applicability to available CYT2B7 family devices. Click on an

| Items | Errata ID | CYT2B7 | Silicon Rev. | Fix Status |
|---|-----------|---|--------------|--|
| [1.] Crypto LSL1, LSR1, LSL1 WITH CARRY, & LSR1 WITH CARRY instructions may work incorrectly in certain scenarios | 53 | CYT2B73BADQ0AZSGS CYT2B73BADQ0AZECS CYT2B73CADQ0AZSGS CYT2B73CADQ0AZECS CYT2B74BADQ0AZSGS CYT2B74BADQ0AZECS CYT2B74CADQ0AZSGS CYT2B74CADQ0AZECS CYT2B75BADQ0AZSGS CYT2B75BADQ0AZECS CYT2B75CADQ0AZSGS CYT2B75CADQ0AZECS CYT2B77BADQ0AZSGS CYT2B77BADQ0AZECS CYT2B77CADQ0AZSGS CYT2B77CADQ0AZECS CYT2B78BADQ0AZSGS CYT2B78CADQ0AZSGS CYT2B78CADQ0AZECS | D | No silicon fix planned. Use workaround. |
| [2] Crypto MEM_BUF may be corrupted | 42 | | | No silicon fix planned. Use workaround. |
| [3] ConfigureFmInterrupt API assumes a parameter with 8 bytes boundary, but actual boundary is 4 bytes | 67 | | | No silicon fix planned. Use workaround. |
| [4] SMPU/MPU/PPU protection region size is limited to 2 GB | 68 | | | No silicon fix planned. Use workaround. |
| [5] DirectExecute API may return error if called with arguments placed in SRAM memory | 69 | | | No silicon fix planned. Use workaround. |
| [6] CAN FD RX FIFO top pointer feature does not function as expected | 96 | | | No silicon fix planned. Use workaround. |
| [7] CAN FD debug message handling state machine does not reset to Idle state when CANFD_CH_CCCR.INIT is set | 97 | | | No silicon fix planned. Use workaround. |
| [8] TPIU Peripheral ID mismatch | 98 | | | No fix planned |
| [9] Limitation of the memory hole in SCB register space | 124 | | | No silicon fix planned. Use workaround |
| [10] WDT service can be missed | 129 | | | No silicon fix planned. Use workaround |
| [11] CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID | 147 | | | No silicon fix planned. Use workaround |
| [12] CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID | 167 | | | No silicon fix planned. Use workaround. TRM will be updated. |

1. Crypto LSL1, LSR1, LSL1_WITH_CARRY, & LSR1_WITH_CARRY instructions may work incorrectly in certain scenarios

| | |
|-----------------------------|--|
| Problem Definition | LSL1, LSR1, LSL1_WITH_CARRY, & LSR1_WITH_CARRY instructions should ignore the value in IW[3:0] (shift by 1 instruction does not use these fields). But because of a HW issue, shift does not work if the register data field, pointed by IW[3:0], is '0' (destination data is same as source data). |
| Parameters Affected | NA |
| Trigger Condition(s) | Using LSL1, LSR1, LSL1_WITH_CARRY, & LSR1_WITH_CARRY instructions |
| Scope of Impact | The shift does not happen (destination data is same as source data). |
| Workaround | <p>IW[3:0] should be pointed to a dummy register where the data field of the register is non-zero value (rsrc0->data[12:0]).</p> <p>Since stack pointer(r15) points to a non-zero value (to use the LSL1 instruction you must have allocated at least one register, so that SP will not be zero), it is safe to use r15 as rsrc0.</p> <pre>static __forceinline void LSL1 (int rdst, int rsrc1) { AHB_WRITE_W (MMIO_CRYPTO_INSTR_FF_WR, (CRYPTO_VU_LSL_OPC << 24) (rdst << 12) (rsrc1 << 4) 15); }</pre> <p>This software workaround applies to other instructions such as LSR1, LSL1_WITH_CARRY & LSR1_WITH_CARRY as well.</p> |
| Fix Status | No silicon fix planned. Use workaround. |

2. Crypto MEM_BUF may be corrupted

| | |
|-----------------------------|---|
| Problem Definition | The SRAM in the Crypto block is 8 KB but the address decode is wired to create four 8-KB images of the SRAM within a 32-KB address space. Writes to memory space above the initial 8-KB image will corrupt SRAM contents. |
| Parameters Affected | NA |
| Trigger Condition(s) | Any write to address between 0x40108000 and 0x4010FFFF |
| Scope of Impact | CRYPTO MEM_BUF may be corrupted |
| Workaround | The software should ensure that there is no access beyond 8 KB MEM_BUF address range from either MMIO writes or address overflows while executing Crypto operations |
| Fix Status | No silicon fix planned. Use workaround. |

| 3. ConfigureFmInterrupt API assumes a parameter with 8 bytes boundary, but actual boundary is 4 bytes | |
|---|---|
| Problem Definition | STATUS_ADDR_PROTECTED will be returned if the ConfigureFmInterrupt API is called with arguments stored in SRAM with 4-byte boundary (available SRAM or protected boundary SRAM). |
| Parameters Affected | NA |
| Trigger Condition(s) | Call ConfigureFmInterrupt API with arguments stored in SRAM at 4 bytes boundary of available SRAM or protected boundary of SRAM. |
| Scope of Impact | ConfigureFmInterrupt API will fail by returning STATUS_ADDR_PROTECTED error status when called with argument having 4 bytes boundary of available SRAM or protected boundary of SRAM. |
| Workaround | Allow 4 bytes margin (that is, assume that the API parameter size is 8 and store the arguments) for ConfigureFmInterrupt API parameter. |
| Fix Status | No silicon fix planned. Use workaround. |

| 4. SMPU/MPU/PPU protection region size is limited to 2 GB | |
|---|---|
| Problem Definition | If SMPU/MPU/PPU protection block size is configured for 4 GB (PROT_SMPU_SMPU_STRUCT_ATT0.REGION.SIZE = 31), then during protection check in SRAM, the value of the internal uint32 variable will overflow (4G = 0x1 0000 0000). Therefore, SRAM assumes the protection size equals zero, and no protection will be applied. |
| Parameters Affected | NA |
| Trigger Condition(s) | Configure SMPU/MPU/PPU to protect with region size equal to 4 GB or the region size with value 31u. |
| Scope of Impact | If SMPU/MPU/PPU is configured to protect region size of 4 GB, then SRAM software does not apply any protection as per the request. |
| Workaround | Use two protection blocks of region size equal to 2 GB if 4-GB region size protection is required. |
| Fix Status | No silicon fix planned. Use workaround. |

| 5. DirectExecute API may return error if called with arguments placed in SRAM memory | |
|--|---|
| Problem Definition | If DirectExecute API is called in the master PC (other than PC0 or PC1) with arguments in SRAM_SCRATCH_ADDR, then the API will return STATUS_ADDR_PROTECTED status. |
| Parameters Affected | NA |
| Trigger Condition(s) | Call DirectExecute API with arguments in SRAM_SCRATCH_ADDR and master PC configured > 1. |
| Scope of Impact | DirectExecute API, if called with master PC configured > 1 and arguments in SRAM_SCRATCH_ADDR, the API will return STATUS_ADDR_PROTECTED. |
| Workaround | Call DirectExecute API with master PC0 or PC1, if arguments are stored in SRAM memory. |
| Fix Status | No silicon fix planned. Use workaround. |

6. CAN FD RX FIFO top pointer feature does not function as expected

| | |
|-----------------------------|--|
| Problem Definition | The RX FIFO top pointer function calculates the address for received messages in Message RAM by hardware. This address should restart back from the start address after reading all messages of RX FIFO n size (n: 0 or 1). However, the address does not restart back from the start address when RX FIFO n size is set to 1 (CANFD_CH_RXFnC.FnS = 0x01). This results in CPU/DMA reading messages from the wrong address in Message RAM. |
| Parameters Affected | NA |
| Trigger Condition(s) | RX FIFO top pointer function is used when RX FIFO n size is set to 1 element (CANFD_CH_RXFnC.FnS = 0x01). |
| Scope of Impact | Received message cannot be correctly read by using the RX FIFO top pointer function, when RX FIFO n size is set to 1 element. |
| Workaround | Any of the following. 1) Set RX FIFO n size to 2 or more when using the RX FIFO top pointer function. 2) Do not use the RX FIFO top pointer function when RX FIFO n size is set to 1 element. Instead of reading received messages from the RX FIFO top pointer, read directly from the Message RAM. |
| Fix Status | No silicon fix planned. Use workaround. |

7. CAN FD debug message handling state machine does not reset to Idle state when CANFD_CH_CCCR.INIT is set

| | |
|-----------------------------|---|
| Problem Definition | If either of the CANFD_CH_CCCR.INIT bits is set by the Host or when the M_TTCAN module enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Configuring the CANFD_CH_CCCR.CCE bit does not change CANFD_CH_RXF1S.DMS. |
| Parameters Affected | NA |
| Trigger Condition(s) | Either of the CANFD_CH_CCCR.INIT bits is set by the Host or when the M_TTCAN module enters BusOff state. |
| Scope of Impact | The errata is limited to the use case when the Debug on CAN functionality is active. Normal operation of the CAN module is not affected, in which case the debug message handling state machine always remains in Idle state. In the described use case, the debug message handling state machine is stopped and remains in the current state signaled by the CANFD_CH_RXF1S.DMS bit. If CANFD_CH_RXF1S.DMS is set to 0b11, the DMA request remains active. |
| Workaround | In case the debug message handling state machine stops while CANFD_CH_RXF1S.DMS is 0b01 or 0b10, it can be reset to Idle state by hardware reset or by reception of debug messages after CANFD_CH_CCCR.INIT is reset to zero. |
| Fix Status | No silicon fix planned. Use workaround. |

8. TPIU Peripheral ID mismatch

| | |
|-----------------------------|---|
| Problem Definition | TPIU peripheral ID indicates that it is M3-TPIU instead of M4-TPIU. |
| Parameters Affected | NA |
| Trigger Condition(s) | When the debugger reads PID registers for component identification. |
| Scope of Impact | The only impact is that the debuggers read the TPIU as M3-TPIU. |
| Workaround | No specific workaround required. Debuggers can use trace features. |
| Fix Status | No fix planned |

9. Limitation of the memory hole in SCB register space

| | |
|-----------------------------|---|
| Problem Definition | The memory hole [offset address: 0x1000 to 0xFFFF] inside the SCB register space is not aligned to the below defined spec. Since the offset address bits [15:12] are ignored and treated as 4'b0000, write/read access to the offset address [0x1000 to 0xFFFF] will actually happen to [0x0000 to 0x0FFF]. - Access to address gaps in mapped memory space: writes are ignored and any read returns a zero. |
| Parameters Affected | NA |
| Trigger Condition(s) | Access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space |
| Scope of Impact | The memory hole [offset address: 0x1000 to 0xFFFF] in the SCB register space is not aligned to other IP registers. |
| Workaround | Do not access to the memory hole [offset address: 0x1000 to 0xFFFF] in SCB register space. |
| Fix Status | No fix planned |

10. WDT service can be missed

| | |
|-----------------------------|---|
| Problem Definition | If WDT service happens within 4 ILO clock cycles before DeepSleep entry, it clears the counter but does not fully complete an internal handshake. A service after DeepSleep wakeup may then be missed if it occurs less than 2 ILO clock cycles after the processor resumes clocking. After this time, the internal handshake is complete and servicing works normally. |
| Parameters Affected | NA |
| Trigger Condition(s) | Service WDT within 4 ILO clock cycles before DeepSleep entry and within 2 ILO clock cycles of processor clock resuming |
| Scope of Impact | WDT service after DeepSleep wakeup may be ignored and WDT continues counting. This can cause unintended WARN_ACTION or UPPER_ACTION, including interrupt, fault, and/or reset. |
| Workaround | Wait 130 µs or more after DeepSleep wakeup. (for example, to measure 130 µs, software can read WDT_CNT register at wake up and make sure that WDT_CNT was incremented of 4 units before servicing WDT). Afterwards, write '1' to WDT service (WDT_SERVICE.SERVICE) after waiting until WDT service (WDT_SERVICE.SERVICE) reads '0'. |
| Fix Status | No silicon fix planned. Use workaround. |

| 11. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID | |
|--|--|
| Problem Definition | <p>Configuration: Several Tx Buffers are configured with the same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests.</p> <p>Expected behavior: When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first.</p> <p>Observed behavior: It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).</p> |
| Parameters Affected | NA |
| Trigger Condition(s) | When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests. |
| Scope of Impact | In the case described it may happen, that Tx Buffers configured with the same Message ID and pending Tx request are not transmitted with lowest Tx Buffer number first (message order inversion). |
| Workaround | <p>Any of the following:</p> <ol style="list-style-type: none"> 1) First write the group of Tx message with the same Message ID to the Message RAM and then afterwards request transmission of all these messages concurrently by a single write access to CANFDx_CHy_TXBAR. Before requesting a group of Tx messages with this Message ID ensure that no message with this Message ID has a pending Tx request. 2) Use the Tx FIFO instead of dedicated Tx Buffers for the transmission of several messages with the same Message ID in a specific order. <p>Applications not able to use workaround #1 or #2 can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.</p> |
| Fix Status | No silicon fix planned. Use workaround. |

12. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID

| | |
|-----------------------------|---|
| Problem Definition | <p>The following are the updated description in Sections "Dedicated Tx Buffers" and "Tx Queue" of the Architecture TRM related to the transmission from multiple buffers configured with the same Message ID.</p> <p>Dedicated Tx Buffers</p> <ul style="list-style-type: none"> - TRM Statement: If multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first. - Enhancement: These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to CANFDx_CHy_TXBAR. <p>Tx Queue</p> <ul style="list-style-type: none"> - TRM Statement: If multiple queue buffers are configured with the same Message ID, the queue buffer with the lowest buffer number is transmitted first. - Replacement: In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT Index, a prediction of the transmission order is not possible. - TRM Statement: An Add Request cyclically increments the Put Index to the next free Tx Buffer. - Replacement: The PUT Index always points to that free buffer of the Tx Queue with the lowest number. |
| Parameters Affected | NA |
| Trigger Condition(s) | Using multiple dedicated Tx Buffers or Tx Queue Buffers configured with the same Message ID. |
| Scope of Impact | In the case the dedicated Tx Buffers with the same Message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue Buffers with the same Message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first. |
| Workaround | In case a defined order of transmission is required the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx Buffers with the same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to CANFDx_CHy_TXBAR. Alternatively a single Tx Buffer can be used to transmit those messages one after the other. |
| Fix Status | No silicon fix planned. Use workaround. TRM will be updated accordingly. |

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|---|
| ** | 02/10/2017 | Advance datasheet |
| *A | 03/31/2017 | Extensive rewrite of all sections for better clarity |
| *B | 09/11/2017 | Updated Features . Minor corrections in Features list . Updated Blocks and functionality . Updated Functional description . Updated Memory Map to clarify single and dual bank mode functionality. Updated Electrical specifications . Added the following timing diagrams in Electrical specifications : Reset, TCPWM, SCB (I ² C, SPI), Crystal Connection Scheme, SAR ADC, System Resources, and JTAG. Updated Ordering information . Updated Packaging to include two formats: - Without alternate functions - With alternate functions Updated Package Characteristics . |
| *C | 02/12/2018 | Updated Ordering information . Updated title to "CYT2B5/B7 Datasheet 32-bit Arm® Cortex®-M4F Microcontroller TRAVEO™ T2G Family". Updated Electrical specifications . Updated SPI Diagrams. Added ADC equivalent circuit for analog input. |
| *D | 09/27/2018 | Updated Features list and Peripheral I/O map . Updated Pin assignment . Updated Alternate function pin assignments . Updated Functional description . Updated Trigger multiplexer and Interrupts and wake-up assignments . Added General P-DMA descriptions, Clock Dividers, and GPIO power port source information. Updated Clock diagram Added HSIOM connections reference table and references to it in alternate pin assignment. Update Electrical specifications . Updated Design Review. Added Errata . |
| *E | 07/25/2019 | Updated Features , Features list , and Functional description . Updated Peripheral I/O map . Updated Alternate function pin assignments . Updated Interrupts and wake-up assignments and Core interrupt types . Updated Trigger Groups and Peripheral clocks . Updated Peripheral Protection Unit Fixed Structure Pairs . Updated Bus masters . Updated Miscellaneous configuration . Updated Reset Sequence, ADC, and SPI Diagrams. Updated Table 26-21 and Table 26-24 . Updated Ordering information and Packaging . Updated Appendix . |

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|---|
| *F | 11/26/2019 | Updated SRAM in CYT2B7 address map . Updated PLL and FLL in Functional description . Updated Programmable PPU and SCB in Peripheral I/O map . Updated Package Characteristics . Updated affected MPNs in Errata . Updated sample revision in Ordering information . |
| *G | 04/23/2020 | Added eSHE footnote on page 1. Updated Block diagram . Updated SCB/UART content in Functional description . Added note for VCCD in Power pin assignments . Added Pin mux descriptions . Updated Fault Assignments table with detailed descriptions. Added JTAG ID and package support footnotes in Ordering information . Removed CM7 from Part number nomenclature . Updated Packaging . Updated Errata . |
| *H | 06/29/2020 | Updated Features list . Updated Clock system . Updated Electrical specifications . Updated Ordering information . Updated Appendix . For details, refer to Revision History Change Log . |
| *I | 10/13/2021 | Updated Features list . Updated Communication peripheral instance list . Updated High-speed I/O matrix connections . Updated Alternate function pin assignments . Updated Faults . Updated Electrical specifications . Updated Part number nomenclature . Updated Appendix . Added Errata . For details, refer to Rev *I updates in the Revision History Change Log . |

Revision History Change Log

Rev. *I Section Updates

| Section | Change Description | Current Spec (Rev. *H) | New Spec (Rev. *I) | Reason for change |
|--|---|---|---|--|
| 1. Features List | Renamed Features in Table 1-1 | LIN | LIN0 | Updated |
| 1.1 Communication Peripheral Instance List | Renamed module in Table 1-2 | LIN | LIN0 | Updated |
| 3.2.3 Clock System | Updated IMO Clock Source description | The IMO operates at a frequency of 8 MHz ±1%. The internal trim settings for the IMO can be dynamically updated to provide a tolerance < 1%. | The IMO operates at a frequency of around 8 MHz. | Updated |
| 3.2.6 Power Modes | Updated description | Hibernate – the device and I/Os are in High-Z state, the device resets on wakeup | Hibernate – the device and I/O states are frozen, the device resets on wakeup | Correction |
| 3.4 I/Os | Updated description | During power-on, Hibernate, and reset, the I/Os are forced to the High-Z state. | During power-on, and reset, the I/Os are forced to the High-Z state. During the Hibernate mode, I/Os are frozen. | Updated |
| 9. Pin Assignment | Updated Figure 9-2, 9-4, 9-6, 9-8, 9-10 | Identifier (n) does not present | Added identifier (n). | Added |
| 10. High-Speed I/O Matrix Connections | Updated Table 10-1 | Number: Description 1: GPIO controls 'out', DSI controls 'output enable' 2: DSI controls 'out' and 'output enable' 3: DSI controls 'out', GPIO controls 'output enable' 4: Analog multiplexer bus A 5: Analog multiplexer bus B 6: Analog multiplexer bus A, DSI control 7: Analog multiplexer bus B, DSI control | Number: Description 1: 2: 3: 4: Reserved 5: 6: 7: | Correction |
| 13. Alternate Function Pin Assignments | Updated Table 13-1 | (none) | Added note [28]: Refer to Table 13-2 for more information on pin multiplexer abbreviations used. | Added |
| 13. Alternate Function Pin Assignments | Updated Table 13-1 | Identifier (n) and note do not present | Added identifier (n). Added note [29]: For any function marked with an identifier (n), the AC timing is only guaranteed within the respective group "n". | Added |
| 13. Alternate Function Pin Assignments | Updated Table 13-1 | PWM_xx, PWM_xx_N, TC_xx_TR0, and TC_xx_TR1 | PWM0_xx, PWM0_xx_N, TC0_xx_TR0, and TC0_xx_TR1 | Updated |
| 21. Faults | Updated Table 21-1 | No.: Description 32: Peripheral Group #0 PPU violation. 33: Peripheral Group #1 PPU violation. 34: Peripheral Group #2 PPU violation. 35: Peripheral Group #3 PPU violation. 37: Peripheral Group #4 PPU violation. 38: Peripheral Group #5 PPU violation. 41: Peripheral Group #6 PPU violation. 49: Flash controller main flash cache correctable ECC violation 50: Flash controller main flash cache non-correctable ECC violation. 52: Flash controller work flash cache correctable ECC violation. 53: Flash controller work-flash cache non-correctable ECC violation. | No.: Description 32: Peripheral Group #0 violation. 33: Peripheral Group #1 violation. 34: Peripheral Group #2 violation. 35: Peripheral Group #3 violation. 37: Peripheral Group #5 violation. 38: Peripheral Group #6 violation. 41: Peripheral Group #9 violation. 49: Flash controller main flash correctable ECC violation 50: Flash controller main flash non-correctable ECC violation. 52: Flash controller work flash correctable ECC violation. 53: Flash controller work-flash non-correctable ECC violation. | Correction |
| 26. Electrical Specifications | Removed Table 26-3. Smoothing Capacitor Connections | Table 26-3. Smoothing Capacitor Connections | (none) | This table is provided in Hardware Design Guide (002-20270). |
| 26. Electrical Specifications | Added 26.7 AC Specifications | (none) | Added 26.7 AC Specifications | Added description |
| 26. Electrical Specifications | Updated Figure 26-8 | 1: tPWMBEXT, tQRES | 1: tPWMBEXT, tQRES | Updated |
| 26. Electrical Specifications | Updated Figure 26-10 to 26-13 | Time reference point: VOH/VOL, VIH/VIL | Time reference point: 50 % | Updated |
| 26. Electrical Specifications | Updated Table 26-17 title | SWD Interface Specifications | SWD Interface Specifications [Conditions: drive_sel<1:0>= 00] | Added condition |
| 26. Electrical Specifications | Updated Table 26-18 title | JTAG AC Specifications | JTAG AC Specifications [Conditions: drive_sel<1:0>= 00] | Added condition |

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Revision history

Rev. *I Section Updates (continued)

| Section | Change Description | Current Spec (Rev. *H) | New Spec (Rev. *I) | Reason for change |
|-------------------------------|-------------------------------------|---|---|-------------------|
| 26. Electrical Specifications | Updated Table 26-19 title | Trace Specifications | Trace Specifications [Conditions: drive_sel<1:0>= 00] | Added condition |
| 26. Electrical Specifications | Updated Table 26-21 | CLK_HF1 / Description: Event generator, ... CLK_HF2 / Max Frequency (MHz): 8 | CLK_HF1 / Description: Event generator (CLK_REF), ... CLK_HF2 / Max Frequency (MHz): 2 | Correction |
| 27.1 Part Number Nomenclature | Updated Table 27-2, 27-3 | Hardware Option: Value / Meaning B / eSHE – on, HSM – off C / eSHE – on, HSM – on | Hardware Option: Value / Meaning B / eSHE – on, HSM – off, RSA – 2K C / eSHE – on, HSM – on, RSA – 2K | Updated |
| 29. Appendix | Updated Table 29-1 | CAN Instance: CANFD0_CH1 CAN TX: P0.2 CAN RX: P0.3 CAN Transceiver NSTB: P23.3 CAN Transceiver EN: P2.1 | CAN Instance: CAN0, Channel#1 CAN TX: P0.2 / CAN0_1_TX CAN RX: P0.3 / CAN0_1_RX CAN Transceiver NSTB / EN (Low): P23.3 (optional) CAN Transceiver EN / EN (High): P2.1 (optional) | Updated |
| 29. Appendix | Updated Table 29-2 | LIN Type: LIN0_CH1 LIN TX: P0.1 LIN RX: P0.0 LIN EN: P2.1 | LIN Type: LIN0, Channel#1 LIN TX: P0.1 / LIN1_TX LIN RX: P0.0 / LIN1_RX LIN EN / EN (High): P2.1 (optional) LIN EN (Low): P23.3 (optional) | Updated |
| 29. Appendix | Updated Figure 29-3 | EN (LOW) and VDDIO line do not present. | Added EN (LOW) and VDDIO line | Updated |
| 31. Errata | Updated CYT2B7 Qualification Status | Engineering samples | Production samples | Updated |
| 31. Errata | Added errata | - | Added Errata ID 147 and 167. | Added errata |

Rev. *I Electrical Specification Updates

| Spec ID | Description | Changed Item | Current Spec (Rev. *H) | New Spec (Rev. *I) | Reason for Change |
|---|---|--------------------|---|--|---------------------|
| SID40 | Power Supply voltage | Note | 40] VDDD, VDDIO_1, VDDIO_2, and VDDA do not have any sequencing limitation and can establish in any order. These supplies (except VDDA and VDDIO_2) are independent in voltage level. For example, VDDIO_1 = 5.0 V, VDDD = 3.3 V, and VDDA = VDDIO_2 = 4.0 V are supported, as is any other combination of voltages between 2.7 V and 5.5 V inclusive. The presence of VDDA without VDDD can cause some leakage from VDDA. However, the device does not drive any analog or digital output. | 44] VDDD, VDDIO_1, VDDIO_2, and VDDA do not have any sequencing limitation and can establish in any order. These supplies (except VDDA and VDDIO_2) are independent in voltage level. See 12-Bit SAR ADC DC Specifications when using ADC units. | Updated description |
| SID49C1A | LP Active mode (CM4 and CM0+ at 8 MHz, all peripherals are disabled) | Details/Conditions | MAX: TA = 125 °C, VDDD = 5.5 V, process typ (FF) | MAX: TA = 25 °C, VDDD = 5.5 V, process worst (FF) | Correction |
| SID49CA | LP Active mode (CM4 and CM0+ at 8 MHz, all peripherals are enabled) | Details/Conditions | CM0+ and CM4 executing max_power.c from ARM with cache enabled. | CM0+ and CM4 executing max_power.c from flash with cache enabled. | Updated condition |
| SID56A | Average current for cyclic wake-up operation This is the average current for the specified LP Active mode and DeepSleep mode (RTC, WDT and Event generator operating). | Details/Conditions | MAX: process typ (FF) | MAX: process worst (FF) | Correction |
| SID62 | Hibernate Mode | Details/Conditions | TA = 25 °C, VDDD = 5.5 V | LLO0/WDT operating. All other peripherals, and all CPUs are off. TA = 25 °C, VDDD = 5.5 V, process typ (TT) | Updated condition |
| SID63 SID63A SID63B SID63C SID63D | DeepSleep to Active transition time | Note | (none) | Added Note[50]: At cold temperature -5°C to -40°C, the DeepSleep to Active transition time can be higher than the max time indicated by as much as 20 us | Added note |

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Revision history

Rev. *I Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec (Rev. *H) | New Spec (Rev. *I) | Reason for Change |
|----------|---|------------------------|--|--|-------------------|
| SID62A | Hibernate Mode | Max Details/Conditions | Max: 175 uA Details/Conditions: TA = 125 °C, VDDD = 5.5 V | Max: 130 uA Details/Conditions: ILO0/WDT operating. All other peripherals, and all CPUs are off. TA = 125 °C, VDDD = 5.5 V, process worst (FF) | Updated spec |
| SID80A | ROM boot startup time or wakeup time from hibernate in NORMAL protection state | Max Details/Conditions | Max: 1200 us Details/Conditions: Guaranteed by Design, CM0+ clocked at 100 MHz | Max: 1800 us Details/Conditions: Guaranteed by Design, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later) | Updated spec |
| SID80B | ROM boot startup time or wakeup time from hibernate in SECURE protection state | Max Details/Conditions | Max: 2050 us Details/Conditions: Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz | Max: 2740 us Details/Conditions: Guaranteed by Design, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later) | Updated spec |
| SID81A | Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state | Details/Conditions | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms | Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later), Listen window = 0 ms | Updated condition |
| SID81B | Flash boot with app authentication time in NORMAL/SECURE protection state | Max Details/Conditions | Max: 4070 us Details/Conditions: Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 100 MHz, Listen window = 0 ms, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 | Max: 5000 us Details/Conditions: Guaranteed by Design, TOC2_FLAGS=0x24F, CM0+ clocked at 100 MHz (Flash boot version 3.1.0.556 and later), Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA2K. | Updated spec |
| SID80A_2 | ROM boot startup time or wakeup time from hibernate in NORMAL protection state | All | (none) | SID80A_2 Parameter: tRB_N_2 Max: 2930 us Details/Conditions: Guaranteed by Design, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.556) | Added spec |
| SID80B_2 | ROM boot startup time or wakeup time from hibernate in SECURE protection state | All | (none) | SID80B_2 Parameter: tRB_S_2 Max: 4680 us Details/Conditions: Guaranteed by Design, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.556) | Added spec |
| SID81A_2 | Flash boot startup time or wakeup time from hibernate in NORMAL/SECURE protection state | All | (none) | SID81A_2 Parameter: tFB_2 Max: 200 us Details/Conditions: Guaranteed by Design, TOC2_FLAGS=0x2CF, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.556), Listen window = 0 ms | Added spec |

Rev. *I Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec (Rev. *H) | New Spec (Rev. *I) | Reason for Change |
|----------|---|--------------------|--|--|-------------------|
| SID81B_2 | Flash boot with app authentication time in NORMAL/SECURE protection state | All | (none) | SID81B_2 Parameter: tFB_A_2 Max: 10000 us Details/Conditions: Guaranteed by Design, TOC2_FLAGS=0x24F, CM0+ clocked at 50 MHz (Flash boot version earlier than 3.1.0.556), Listen window = 0 ms, Public key exponent e = 0x010001, App size is 64 KB with the last 256 bytes being a digital signature in RSASSA-PKCS1-v1.5 Valid for RSA2K. | Added spec |
| SID102A | VDDA voltage range | All | (none) | VDDA voltage range | Added spec |
| SID103A | Internal band gap reference voltage | All | (none) | Internal band gap reference voltage | Added spec |
| SID113D | Analog input sample time for temperature sensor | All | (none) | Analog input sample time for temperature sensor | Added spec |
| SID200 | Temperature Sensor accuracy 1 | Details/Conditions | TJ = 150 °C This spec is valid for the following conditions: a. 3.0 V ≤ VDDD=VDDA=VREFH ≤ 3.6 V or b. 4.5 V ≤ VDDD=VDDA=VREFH ≤ 5.5 V | TJ = 150 °C This spec is valid when using ADC[0] (VDDIO_1), ADC[1] (VDDIO_2) or ADC[2] (VDDD) with the following conditions: a. 3.0 V ≤ VDDD, VDDIO_1 or VDDIO_2 = VDDA = VREFH ≤ 3.6 V or b. 4.5 V ≤ VDDD, VDDIO_1 or VDDIO_2 = VDDA = VREFH ≤ 5.5 V | Updated condition |
| SID201 | Temperature Sensor accuracy 2 | Details/Conditions | -40 °C ≤ TJ ≤ 150 °C This spec is valid for the following conditions: a. 3.0 V ≤ VDDD=VDDA=VREFH ≤ 3.6 V or b. 4.5 V ≤ VDDD=VDDA=VREFH ≤ 5.5 V | -40 °C ≤ TJ ≤ 150 °C This spec is valid when using ADC[0] (VDDIO_1), ADC[1] (VDDIO_2) or ADC[2] (VDDD) with the following conditions: a. 3.0 V ≤ VDDD, VDDIO_1 or VDDIO_2 = VDDA = VREFH ≤ 3.6 V or b. 4.5 V ≤ VDDD, VDDIO_1 or VDDIO_2 = VDDA = VREFH ≤ 5.5 V | Updated condition |
| SID201A | Temperature Sensor accuracy 3 | Details/Conditions | -40 °C ≤ TJ ≤ 150 °C This spec is valid for the following conditions except SID201 conditions: 2.7 V ≤ VDDD ≤ 5.5 V and 2.7 V ≤ VDDA=VREFH ≤ 5.5 V | -40 °C ≤ TJ ≤ 150 °C This spec is valid when using ADC[0] (VDDIO_1) or ADC[2] (VDDD) with the following condition: 2.7 V ≤ VDDD or VDDIO_1 ≤ 5.5 V and 2.7 V ≤ VDDA = VREFH ≤ 5.5 V and 0.8 x VDDA < VDDD or VDDIO_1 | Updated condition |
| SID598 | Over current detection range in Active/Sleep mode | Details/Conditions | (None) | Guaranteed by Design | Added codition |
| SID599 | Over current detection range in DeepSleep mode | Details/Conditions | (None) | Guaranteed by Design | Added codition |
| SID332 | Feedback resistor vaule for ECO | Details/Conditions | (None) | Guaranteed by Design | Added codition |
| SID334 | 4-MHz ECO start-up time | Details/Conditions | Start-up time to 90% of final frequency | Time from set CLK_ECO_CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READY is set to 1. (See Clock Timing Diagrams) | Updated condition |
| SID335 | 33-MHz ECO start-up time | Details/Conditions | Start-up time to 90% of final frequency | Time from set CLK_ECO_CONFIG.ECO_EN to 1 until CLK_ECO_STATUS.ECO_READY is set to 1. (See Clock Timing Diagrams) | Updated condition |
| SID362 | WCO start up time | Details/Conditions | For Grade-S devices | For Grade-S devices Time from set CTL_WCO_EN to 1 until STATUS.WCO_OK is set to 1. (See Clock Timing Diagrams) | Updated condition |

Rev. *I Electrical Specification Updates (continued)

| Spec ID | Description | Changed Item | Current Spec (Rev. *H) | New Spec (Rev. *I) | Reason for Change |
|---------|---------------------|---------------------------|---|--|-------------------|
| SID362E | WCO start up time | Details/Conditions | For Grade-E devices | For Grade-E devices Time from set CTL.WCO_EN to 1 until STATUS.WCO_OK is set to 1. (See Clock Timing Diagrams) | Updated condition |
| SID349C | PFD frequency | Min | 4 MHz | 3.988 MHz | Correction |
| SID412 | Minimum WDT timeout | Details/Conditions | When using the ILO (32.768 kHz + 5 %) and 16-bit WDT counter. Guaranteed by Design. | When using the ILO (32.768 kHz + 5 %) and 32-bit WDT counter. Guaranteed by Design. | Correction |
| SID413 | Maximum WDT timeout | Details/Conditions | When using the ILO (32.768 kHz - 5 %) and 16-bit WDT counter. Guaranteed by Design. | When using the ILO (32.768 kHz - 5 %) and 32-bit WDT counter. Guaranteed by Design. | Correction |
| SID414 | Default WDT timeout | Typ Details/Conditions | Typ: 125 ms Details/Conditions: When using the ILO and 32-bit WDT counter at 0x1000 (default value). Guaranteed by Design. | Typ: 1000 ms Details/Conditions: When using the ILO and 32-bit WDT counter at 0x8000 (default value). Guaranteed by Design. | Correction |

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