EPSON

SPC7210F0E

SCSI Controller & Buffer Manager IC

- Powerful Buffer Management with Tabulation
- Sync/async Data Transmission
- Supported SCSI-II Interface

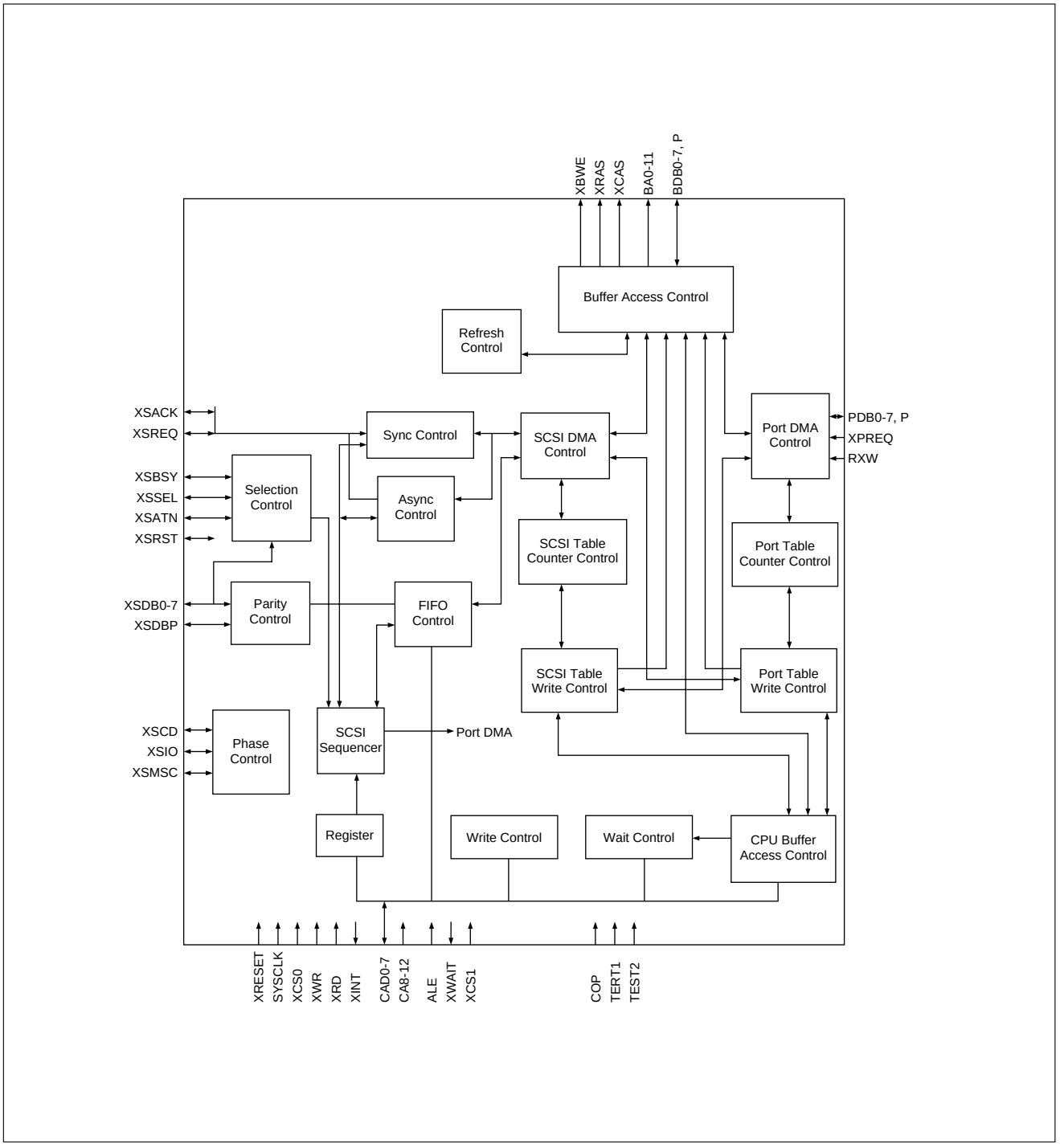
■ DESCRIPTION

The SPC7210F0E is a SCSI bus controller satisfying the new SCSI-II interface system. In the target mode, it allows easy firmware design for peripheral read/write operations.
The SPC7210F0E uses the standard SCSI control command format. It can execute the frequently used phase sequence by a single command issue, and the overhead due to CPU intervention can be minimized for SCSI control.
The SPC7210F0E has the powerful buffer manager functions with tabulation. It has two tables; one at the SCSI unit and the other one at the peripheral unit. Data is automatically copied between the two tables, and the parallel data transfer speed can greatly be increased between the host and buffer and between the disk and buffer.

■ FEATURES

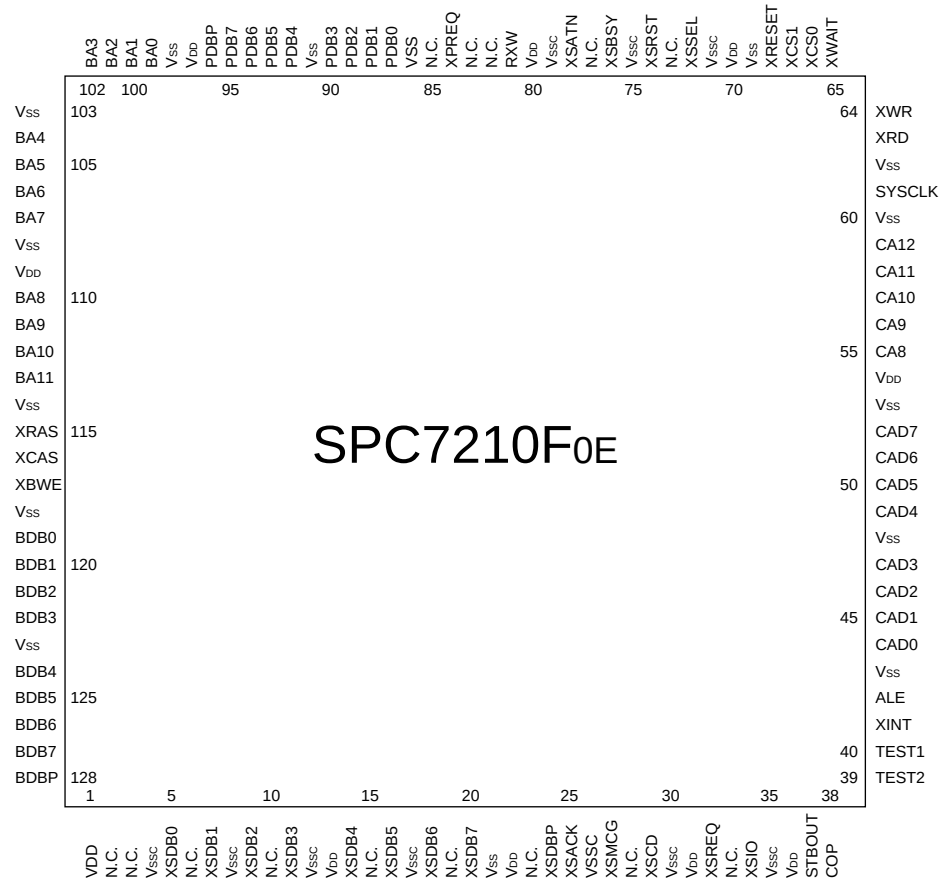
- Powerful buffer management with tabulation
- Sync/async data transmission
  - 10M bps (20 MHz) in sync mode,
  - 5M bps (20 MHz) in async mode.
- Built-in 48mA driver
- Programmable sync mode transfer rate and offset
- Automatic arbitration/selection/reselection by hardware
- Built-in selection/reselection timers
- Support of initiator/target mode
- Built-in 16 bytes FIFO
- Bus phase switching by commands
- Full isolation of buffer, CPU and peripheral buses
- Monitoring and direct control of SCSI control signals by CPU
- The Window function to allocate part of buffer memory (8K bytes MAX) in CPU memory space.
- Up to 16M bits of DRAM can be connected.
- Package: QFP5-128pin (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP5-12pin



■ PIN DESCRIPTION

● SCSI Interface

Pin No.	Pin Name	I/O	Function
5	XSDB0	I/OD	SCSI interface data signa
7	XSDB1	I/OD	
9	XSDB2	I/OD	XSDB0 (XSD bit 0) is the LSB, and XSDB7 (XSD bit 7)
11	XSDB3	I/OD	is the MSB.
14	XSDB4	I/OD	ACTIVE LOW
16	XSDB5	I/OD	
18	XSDB6	I/OD	
20	XSDB7	I/OD	
24	XSDBP	I/OD	SCSI data parity; active Low
25	XSACK	I/OD	SCSI Acknowledge; active Low
32	XSREQ	I/OD	SCSI Request; active Low
74	XSRST	I/OD	SCSI Reset; active Low
72	XSSEL	I/OD	SCSI Select; active Low
76	XSBSY	I/OD	SCSI Busy; active Low
27	XSMSG	I/OD	SCSI Message; active Low
29	XSCD	I/OD	SCSI Control/Data; active Low
34	XSIO	I/OD	SCSI Input/Output; active Low
78	XSATN	I/OD	SCSI Attention; active Low

● CPU Interface

Pin No.	Pin Name	I/O	Function
44	CAD0	IP/O	Address and data signals used for access to external register or buffer memory. CAD0 is the LSB, and CAD7 is the MSB. Addresses CAD0 to CAD4 are valid for access to an external register, but CAD5 to CAD7 are ignored.
45	CAD1	IP/O	
46	CAD2	IP/O	
47	CAD3	IP/O	
49	CAD4	IP/O	
50	CAD5	IP/O	
51	CAD6	IP/O	
52	CAD7	IP/O	
55	CA8	IP	Address signal used for access to buffer memory
56	CA9	IP	
57	CA10	IP	
58	CA11	IP	
59	CA12	IP	
66	XCS0	I	Chip Select signal for access to the internal SBIC register; active Low
67	XCSI	I	Chip Select signal for access to buffer memory; active Low
61	SYSCLK	I	16 to 20MHz system clock
65	XWAIT	OD	CPU wait signal, generated during access to the buffer memory; active Low; open drain output
68	XRESET	I	System Reset signal; active Low
64	XWR	I	Write Strobe signal
63	XRD	I	Read Strobe signal
41	XINT	OD	CPU Interrupt signal, generated during control command completion or buffer transfer event; active Low; open drain output
38	COP	I	Test signal; always Low
42	ALE	I	Address Latch Enable signal

● Buffer Interface

Pin No.	Pin Name	I/O	Function
119	BDB0	IP/O	Memory data buses. BDB0 is the LSB and BDB7 is the MSB
120	BDB1	IP/O	
121	BDB2	IP/O	
122	BDB3	IP/O	
124	BDB4	IP/O	
125	BDB5	IP/O	
126	BDB6	IP/O	
127	BDB7	IP/O	
128	BDBP	IP/O	Memory data bus parity; odd parity
117	XBWE	O	Memory write signal
99	BA0	O	Memory address buses. BA0 is the LSB and BA10 is the MSB. The row and column addresses are multiplexed, and up to 16M bits can be addressed.
100	BA1	O	
101	BA2	O	
102	BA3	O	
104	BA4	O	
105	BA5	O	
106	BA6	O	
107	BA7	O	
110	BA8	O	
111	BA9	O	
112	BA10	O	
113	BA11	O	
115	XRAS	O	Row address strobe signal to DRAM
116	XCAS	O	Column address strobe signal to DRAM

● PORT Interface

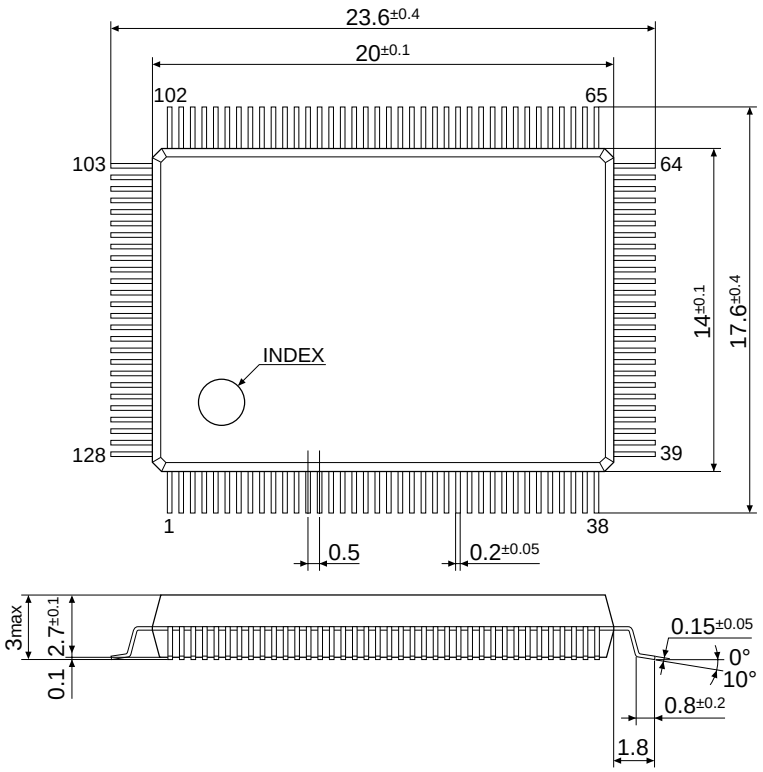
Pin No.	Pin Name	I/O	Function
87	PDB0	IP/O	Data buses; PDB0 is the LSB and PDB7 is the MSB.
88	PDB1	IP/O	
89	PDB2	IP/O	
90	PDB3	IP/O	
92	PDB4	IP/O	
93	PDB5	IP/O	
94	PDB6	IP/O	
95	PDB7	IP/O	
96	PDBP	IP/O	Port Data Parity; odd parity
84	XPREQ	I	Request signal input from port
81	RXW	I	Data direction switch signal from port equipment. When High, data is sent from SBIC to port; when Low, data is sent from port to SBIC.

● Others

Pin No.	Pin Name	I/O	Function
See assignment chart	V_{SSC}	–	11 SCSI interface GND pins; Nos. 4, 8, 12, 17, 26, 30, 35, 71, 75, 79.
See assignment chart	N.C.	–	No Connection; pins 2, 3, 6, 10, 15, 19, 23, 28, 33, 73, 77, 82, 83, 85.
See assignment chart	V_{DD}	–	10 Power pins; Nos. 1, 13, 22, 31, 36, 54, 70, 80, 97, 109.
See assignment chart	V_{SS}	–	14 GND pins; Nos. 43, 48, 53, 60, 62, 69, 86, 91, 98, 103, 108, 114, 118, 123.
37	STBOUT	O	Test Output pin; no connection
40	TEST1	I	Test pin. Test mode when High; usually Low.
39	TEST2	I	Test pin. Test mode when High; usually Low.

■ PACKAGE DIMENSIONS

Plastic QFP5-128pin



Unit : mm

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