HD81806R

4-ch DTMF/DT Receiver LSI

Description

The HD81806 is a CMOS single-chip signal processor. It can receive pushbutton signals sent from a terminal to a central office exchange or private automatic branch exchange (PABX), or sent end-to-end (EE) from one terminal to another. It can also function as a tone signal receiver.

The HD81806 processes four channels of serial input from a μ-law or A-law companding PCM-CODEC chip, or four channels of parallel input from an MPU (microprocessor) interface. The four channels can be switched independently between pushbutton (DTMF) and tone (DT) receiver modes. Future systems employing the HD81806 can therefore be reduced in terms of size and cost.

Functional Summary

- All-digital processing ensures excellent performance and reliability.
- Processes either four-channel serial input from a μ-law or A-law companding PCM CODEC chip, or four-channel parallel input from an MPU interface.
- Commands can switch the four channels independently between DTMF and DT receiver functions.
- Commands can modify sensitivity levels and other receiver characteristics (See the table below).
- Supports early steering.

Note
DTMF : Dual Tone Multi Frequency
DT : Dial Tone

Ordering Information

Type No.	Package	Operating Temperature	Note
HD81806RP	DP-40	–20 to +75°C	
HD81806RCP	CP-44	–20 to +75°C	
HD81806RPW	DP-40	–40 to +85°C	Wide temperature assurance
HD81806RCPW	CP-44	–40 to +85°C	

Specifications

(1) DTMF Receiver

Item	Description	
	Exchange	Terminal EE (END TO END)*2
Input sensitivity level	–3 to –24 dBm0/monotone*1	–3 to –42 dBm0/monotone*1
Input insensitivity level	≤ –29 dBm0/monotone*1	≤ –50 dBm0/monotone*1
Dial tone suppression (340 to 450 Hz)	–34 dB (Typ)	–43 dB (Typ)
Sensitive band	DTMF center frequency ±1.8%	
Dead band	DTMF center frequency ±3.0%	
Twist characteristic	±10 dB (Typ)*1	
Guard time	38 ms*1	

Notes: 1. Modifiable by command
2. Echo canceling is operative in terminal EE mode

(2) DT Receiver

Item	Description
Input sensitivity level	0 to –45 dBm0*1
Input insensitivity level	≥ 3 dBm0, ≤ –55 dBm0*1
Sensitive band	300 to 480 Hz
Dead band	≤ 200 Hz, ≥ 540 Hz
Sensitive-band/dead-band signal ratio (S/N)	6 dB (Typ)*1
Input signal level output	Output encoded in 5-dB steps
Guard time	30 ms*1

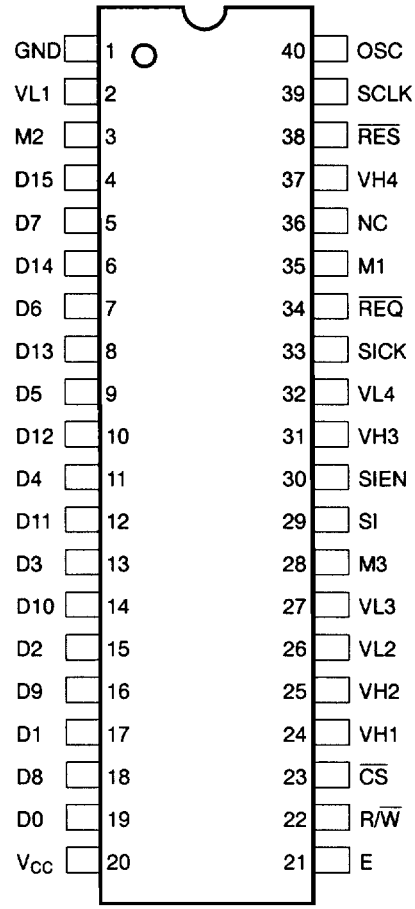
Note: 1. Modifiable by command

Features

Item		Description
Sampling frequency		8 kHz
Input data format		Four 8-bit channels for μ-law or A-law compressed PCM data
Serial interface (CODEC)		(1) μ-law PCM CODEC or (2) A-law PCM CODEC
Parallel interface (MPU)		8-bit MPU
CMOS Power dissipation		150 mW (Typ) (Unloaded output)
Supply voltage		Single +5 V power supply
Additional functions	DTMF receiver	(1) Selectable logic output format (2) Early steering flag output
	DT receiver	(1) Input signal level output (2) Early steering flag output

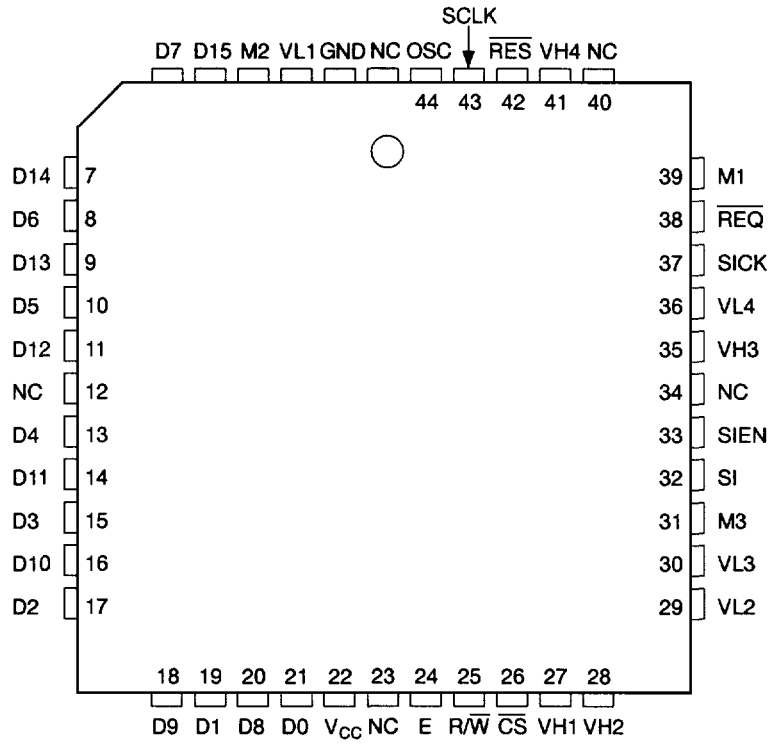
Pin Arrangement

DP-40



(Top view)

CP-44



(Top view)

Pin Description

Item	Symbol	Pin No. DP-40	Pin No. CP-44	I/O	Function
Power supply	V_{CC}	20	22		+5-V power supply pin
	GND	1	2		Ground pin
Clock	OSC	40	44	Input	System clock input pin for 40-MHz clock.
	SCLK	39	43	Output	Output pin for internal system clock. Output frequency is 1/4 of OSC. Not output during reset.
Serial input	SICK	33	37	Input	Serial input clock pin. Serial input data are latched on the falling edge of this clock. Clock input should continue at alltimes.
	SIEN	30	33	Input	After SIEN becomes High, the serial input data is fetched synchronous to the falling edge of the SICK clock.
	SI	29	32	Input	Serial data input pin. Send data MSB first in synchronization with SICK and SIEN. Data are clocked into a 16-bit internal register which holds input data for two channels. Send data for 4 channels: channels 1 and 2; then channels 3 and 4.
Mode control pins	M1	35	39	Input	These pins select the receiver mode at power-on. DTMF Logic output format selection (See table 4 on page 31)
	M2	3	4	Input	CODEC type selection (A-law or μ-law)
	M3	28	31	Input	Parallel/serial PCM data input selection

M1	DTMF Output Format
Low	Type 1 (MITEL format)
High	Type 2 (Other formats)

M2	CODEC Type
Low	A-law PCM
High	μ-law PCM

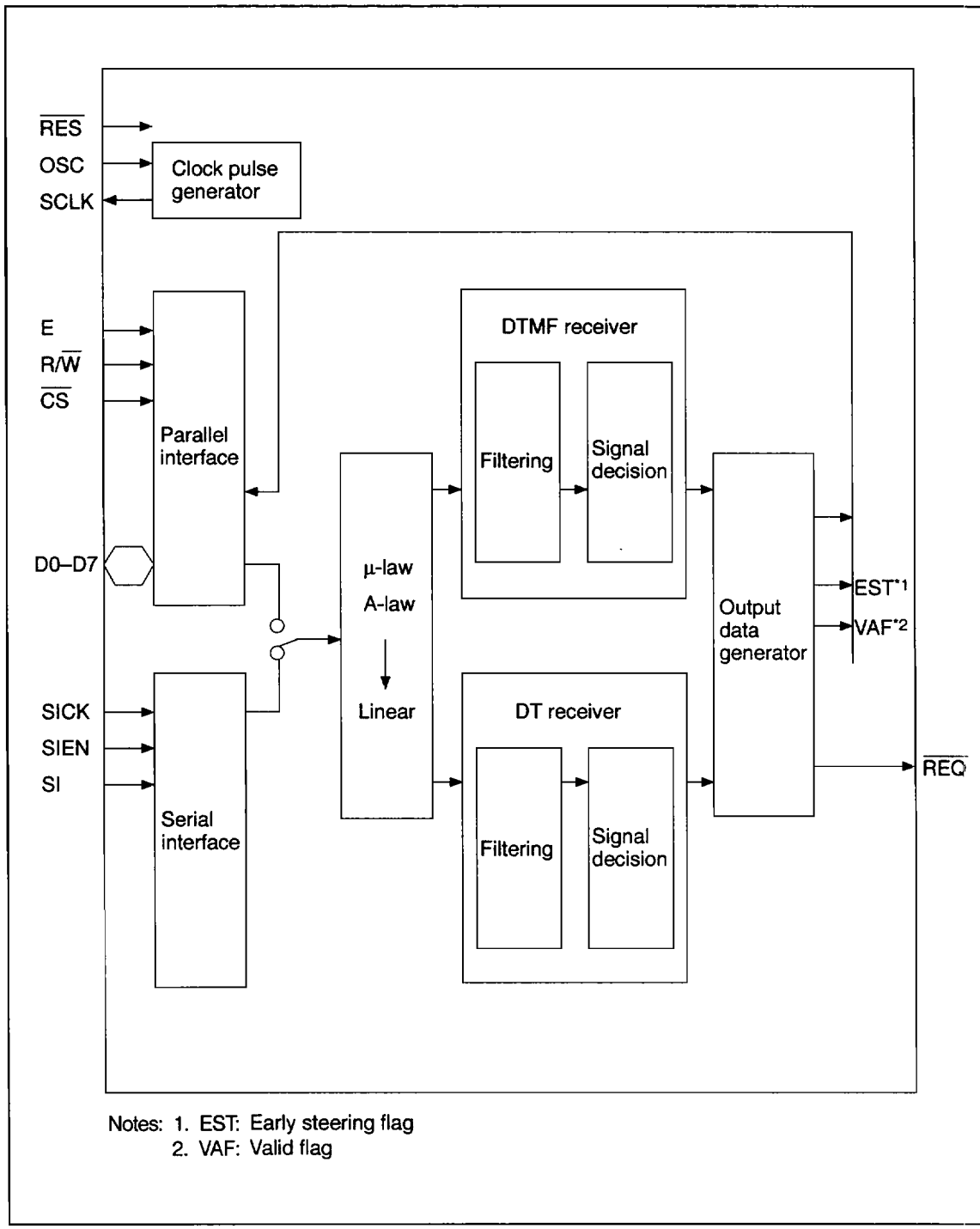
M3	PCM Data Input
Low	Serial input
High	Parallel input

These inputs should be pulled up or down.

Pin Description (cont)

Item	Symbol	Pin No. DP-40	Pin No. CP-44	I/O	Function
Parallel input/ output control	$\overline{CS}$	23	26	Input	Chip select input pin: enables parallel input and output. R/$\overline{W}$, E, and D0 to D15 are valid when $\overline{CS}$ is low.
	R/$\overline{W}$	22	25	Input	Input pin that selects the direction of the data bus. The HD81806 outputs data when R/$\overline{W}$ is high, and inputs data when R/$\overline{W}$ is low.
	E	21	24	Input	Enable signal for the parallel bidirectional data bus. Input and output are performed while E is high.
Data bus	D0	19	21	Input/Output	Bidirectional three-state bus for data input and output. The R/$\overline{W}$ control input selects the bus direction. The data bus is in the high-impedance state when $\overline{CS}$ is high. Data input and output are performed on the eight low-order data lines (D0 to D7). D8 to D15 should be tied to ground via pull-down resistors.
	D1	17	19	Input/Output	
	D2	15	17	Input/Output	
	D3	13	15	Input/Output	
	D4	11	13	Input/Output	
	D5	9	10	Input/Output	
	D6	7	8	Input/Output	
	D7	5	6	Input/Output	
	D8	18	20	Tied low	
	D9	16	18	Tied low	
	D10	14	16	Tied low	
	D11	12	14	Tied low	
	D12	10	11	Tied low	
	D13	8	9	Tied low	
	D14	6	7	Tied low	
	D15	4	5	Tied low	
Transfer request output	$\overline{REQ}$	34	38	Open-drain output	Output pin from which the HD81806 sends data transfer requests to the MPU. Goes low when the data are updated. However, when the CPU does not read the contents of the HD81806 register after asserting $\overline{REQ}$, the $\overline{REQ}$ signal is not negated. In addition, the data is updated every 500 µs regardless of whether or not the microcomputer reads data. Output at 500-µs intervals during receiver operation. The output data are held unchanged from output of $\overline{REQ}$ until read by the MPU.
Reset	$\overline{RES}$	38	42	Input	Low input resets the chip.
Other inputs	VL1–VL4	2, 26 27, 32	3, 29 30, 36	Input	Fixed voltage level pins. Tied low.
	VH1–VH4	24, 25 31, 37	27, 28 35, 41	Input	Fixed voltage level pins. Tied high.
NC	NC	36	1, 12, 23, 34, 40	—	Not used (connected internally). Leave open.

Block Diagram



Notes: 1. EST: Early steering flag
2. VAF: Valid flag

Figure 1 Block Diagram

Functional Flow

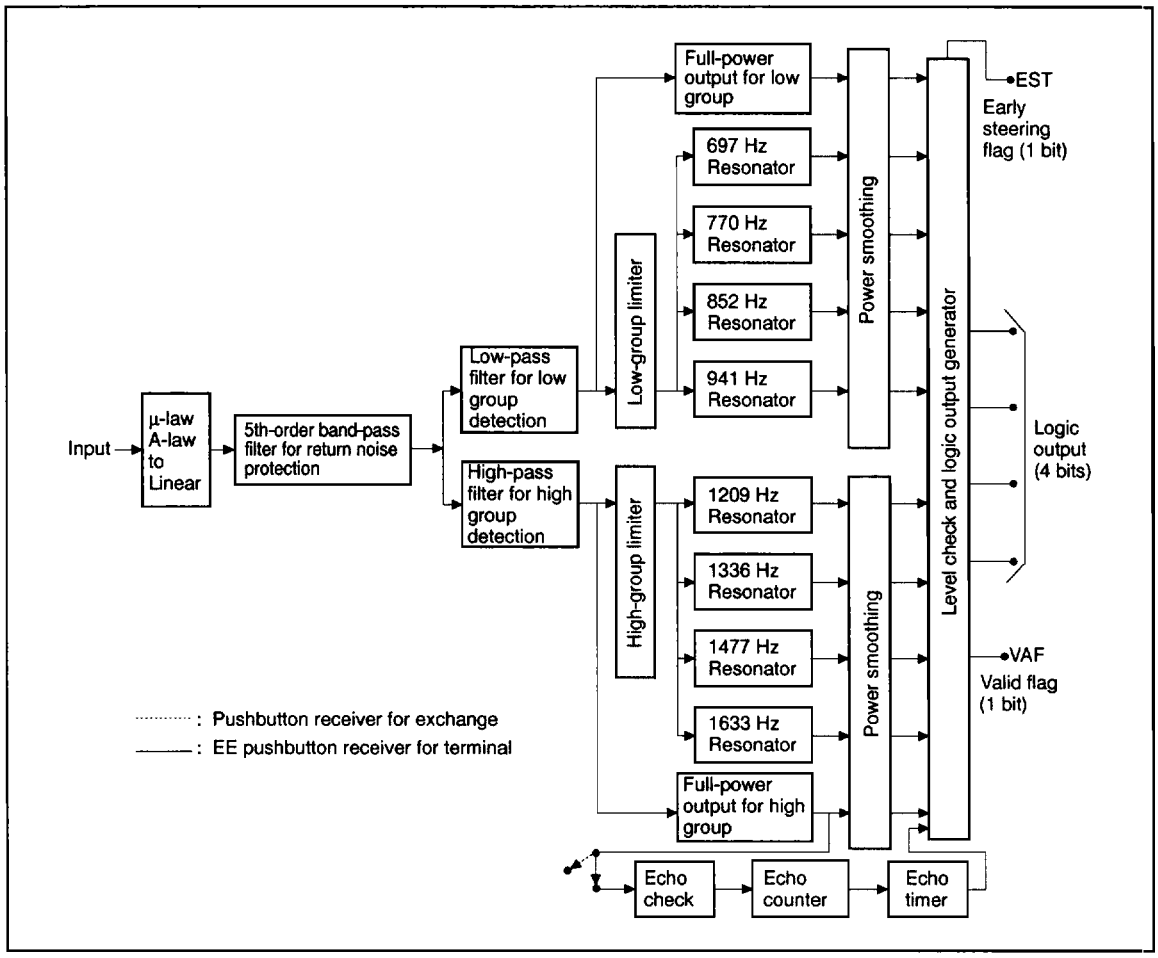


Figure 2 DTMF Receiver Functional Flow (One Channel)

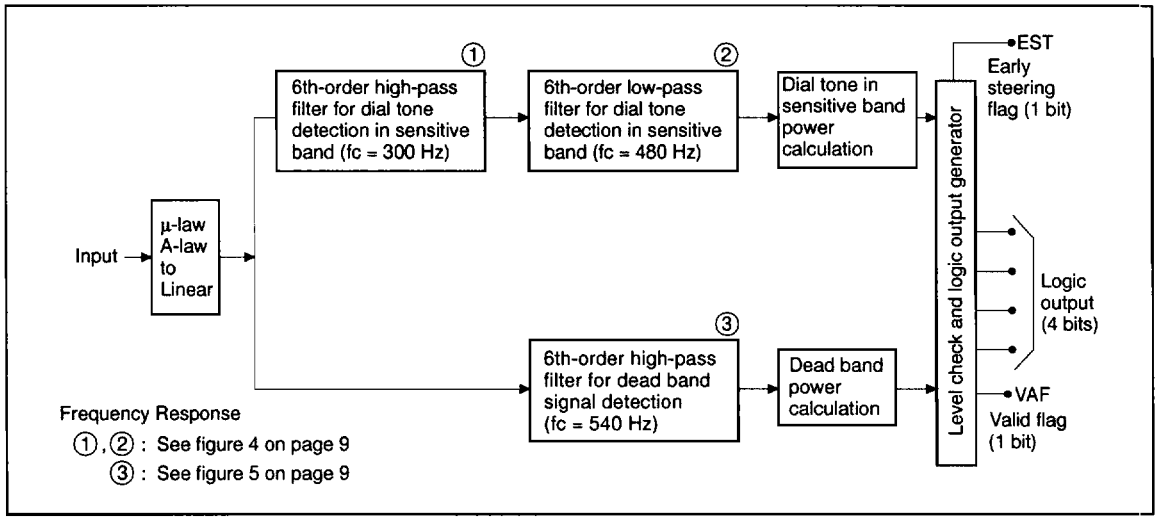


Figure 3 DT Receiver Functional Flow (One Channel)

Filter Frequency Characteristics

Figures 4 to 5 show the frequency characteristics of the filter sections (①, ②, ③) illustrated in the DTMF and DT functional flow diagrams. (See figure 2, 3.)

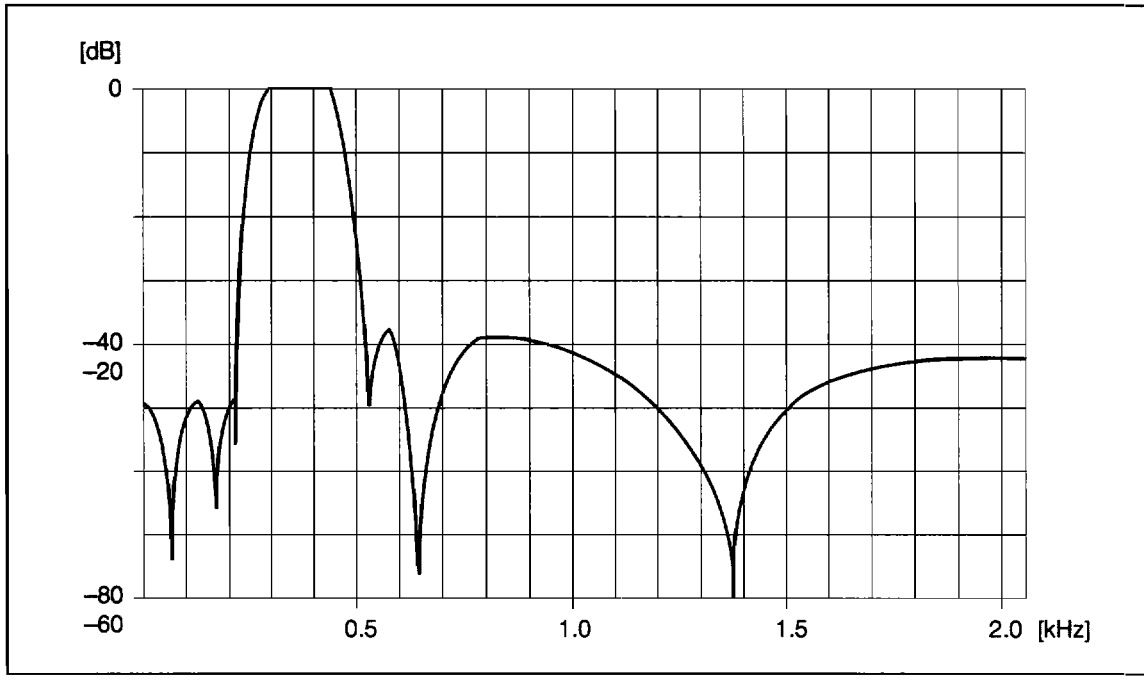


Figure 4 6th-Order High Pass Filter for Dial Tone Detection in Sensitive Band ① and Low Pass Filter ②

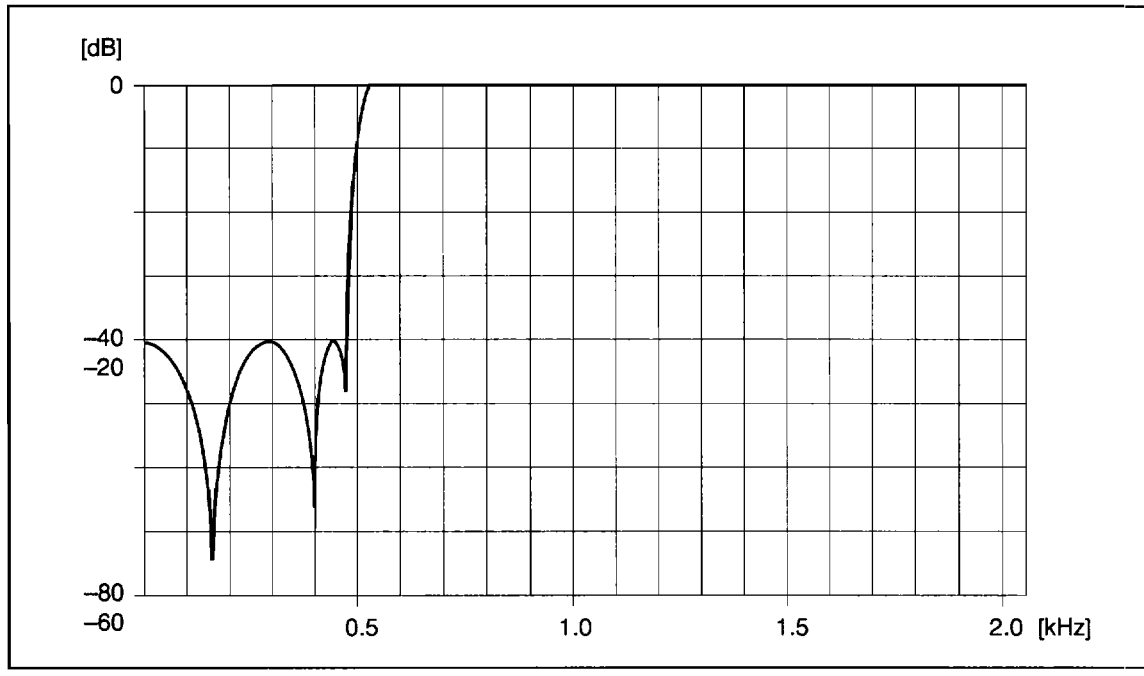


Figure 5 6th-Order High Pass Filter for Dead Band Signal Detection ③

Functional Description

The HD81806 converts serial or parallel PCM input data from μ-law or A-law encoded form to linear data, depending on to mode control pin M2. It then performs filtering and signal decision processes, and outputs the results as 8-bit data on the parallel bidirectional data bus (D0 to D7). (See figure 7, and figure 8 about system configuration.)

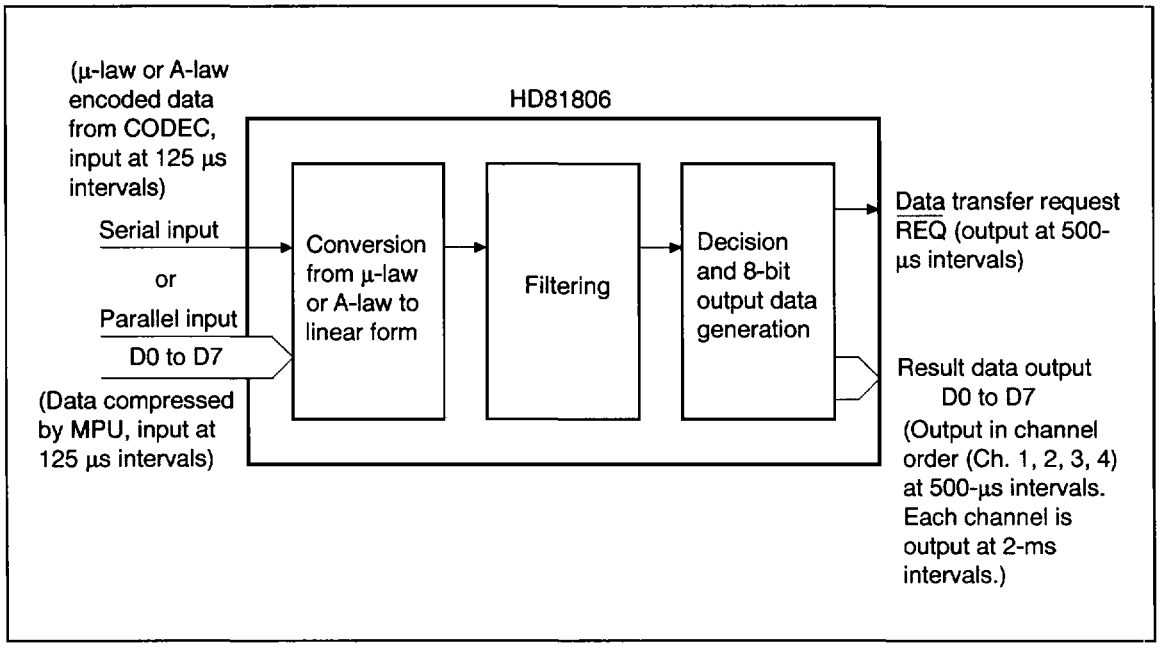


Figure 6 Data Flow in HD81806

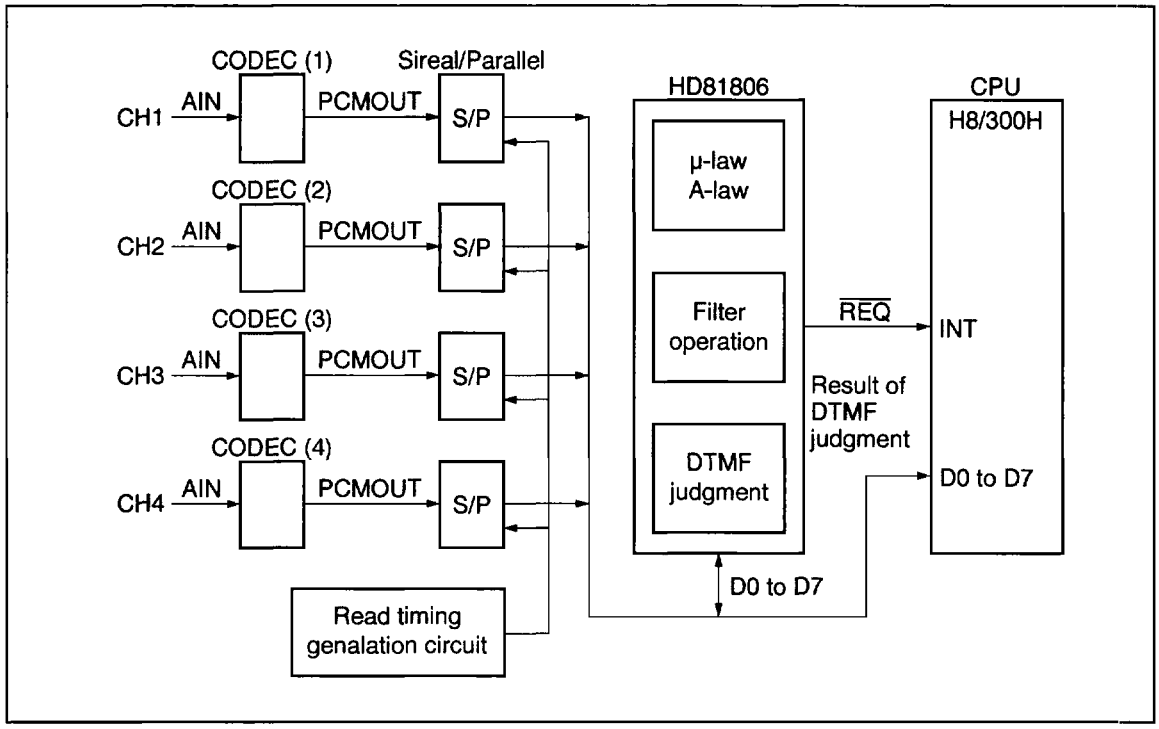


Figure 7 Construction of Parallel Interface

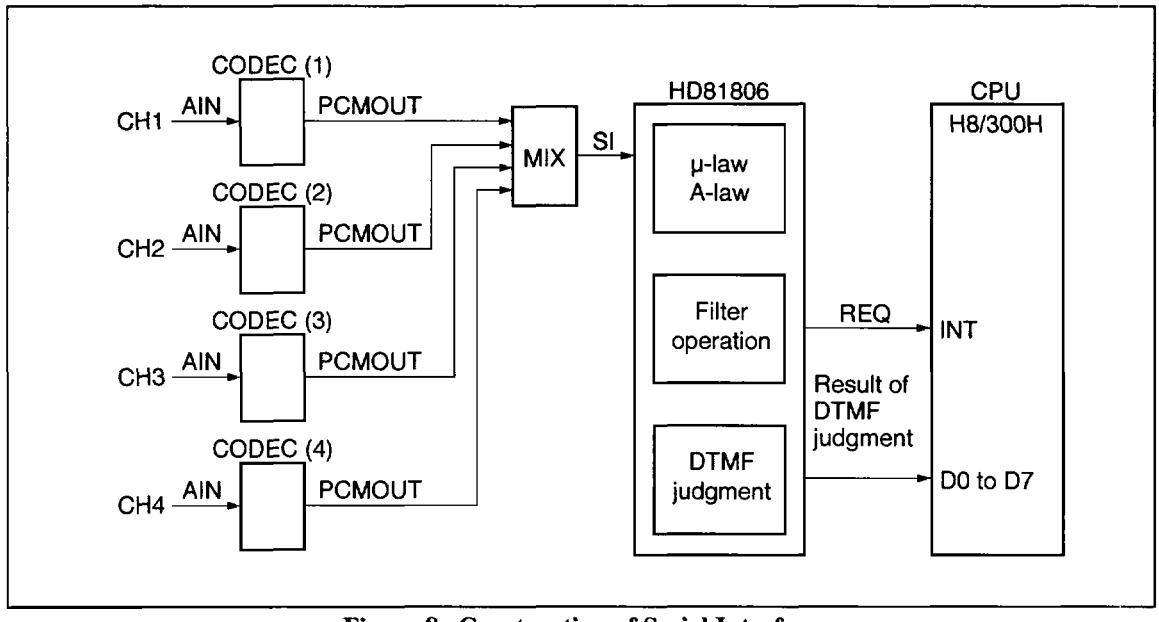


Figure 8 Construction of Serial Interface

Interface

The HD81806 has a serial line for CODEC interfacing and a parallel bus for MPU interfacing.

The serial interface is only for the input of PCM data. It can be connected to the PCM-out pin of the CODEC.

The parallel interface is an MPU data bus used for inputting PCM data, commands for controlling the operation of the HD81806, and the output of result data.

Mode control pin M3 selects whether the PCM data is input via the serial or parallel interface.

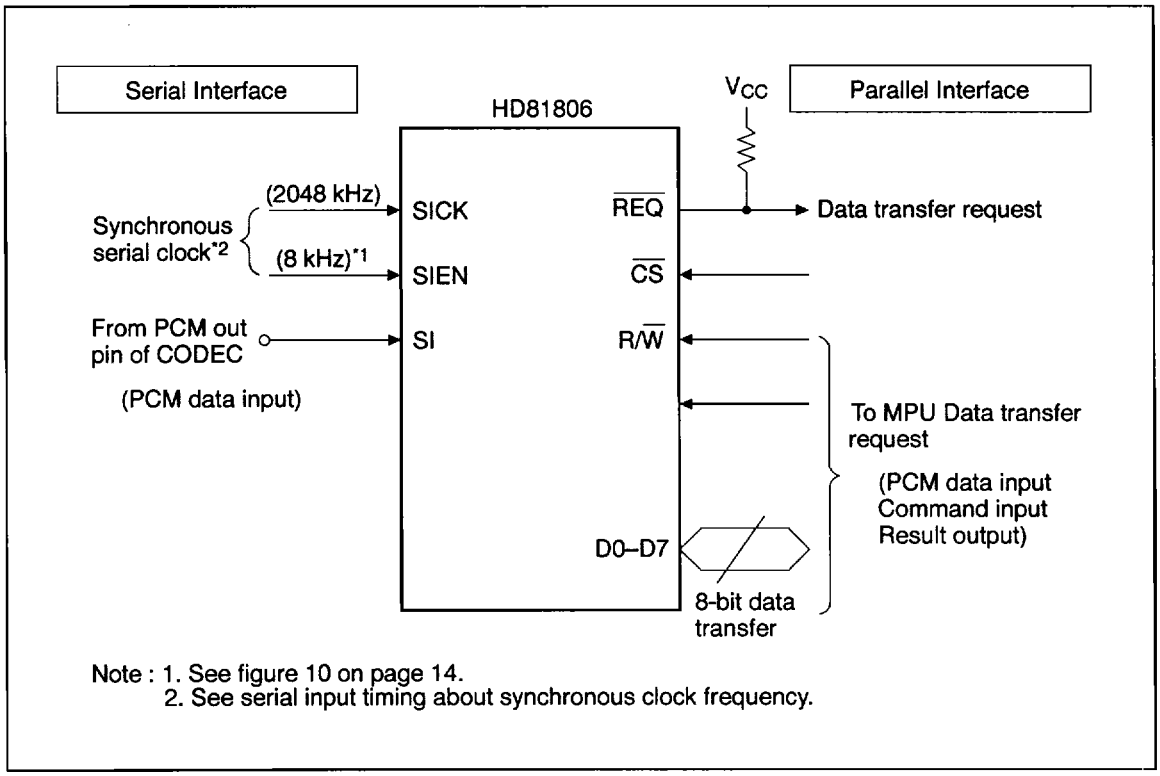


Figure 9 HD81806 Interface Signals

Serial Interface

(1) CODEC Selection

The serial interface is used exclusively for connecting a CODEC device, which may be either a μ-law or A-law PCM type, as specified in table 1. Type selection is facilitated by the signal level applied to mode control pin M2.

(2) Example of Interface with CODEC

Figure 10 shows the main circuit features for interfacing four CODEC channels to the HD81806. Figure 11 shows AC timing chart of figure 10.

In serial interfacing, the clock and enable signals for serial input must be supplied from an external source.

(3) Serial Input

For serial data input, the incomming data is clocked into the HD81806 in 16-bit data blocks by the synchronized serial input clock (SICK) and serial input enable (SIEN) signals.

Table 1 Connectable Serial Interfaces

No.	CODEC type	Input/Output Bit Count	Sampling Frequency	M2
1	A-law PCM CODEC	8 bits	8 kHz	L
2	μ-law PCM CODEC	8 bits	8 kHz	H

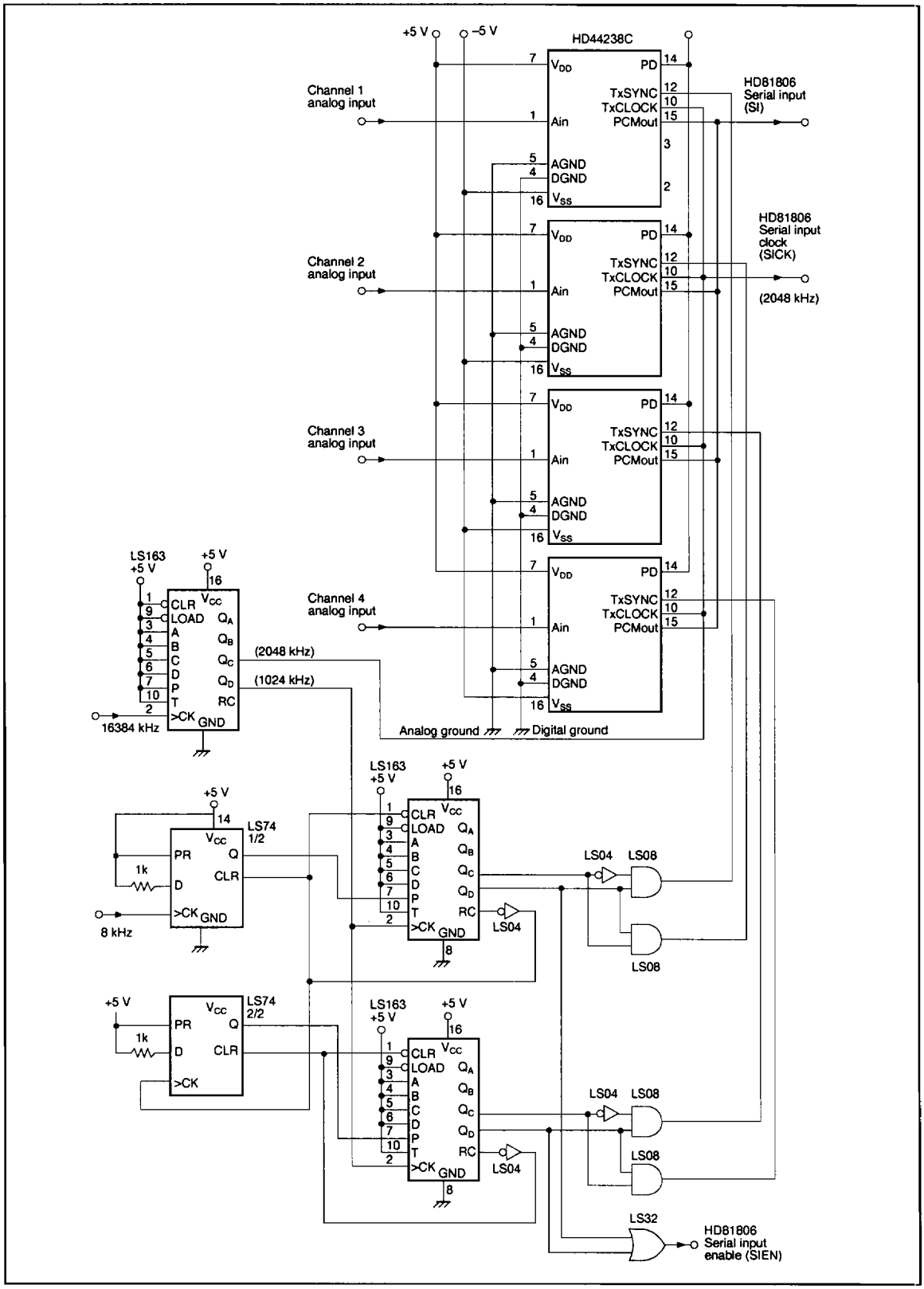


Figure 10 Example of CODEC Interfacing

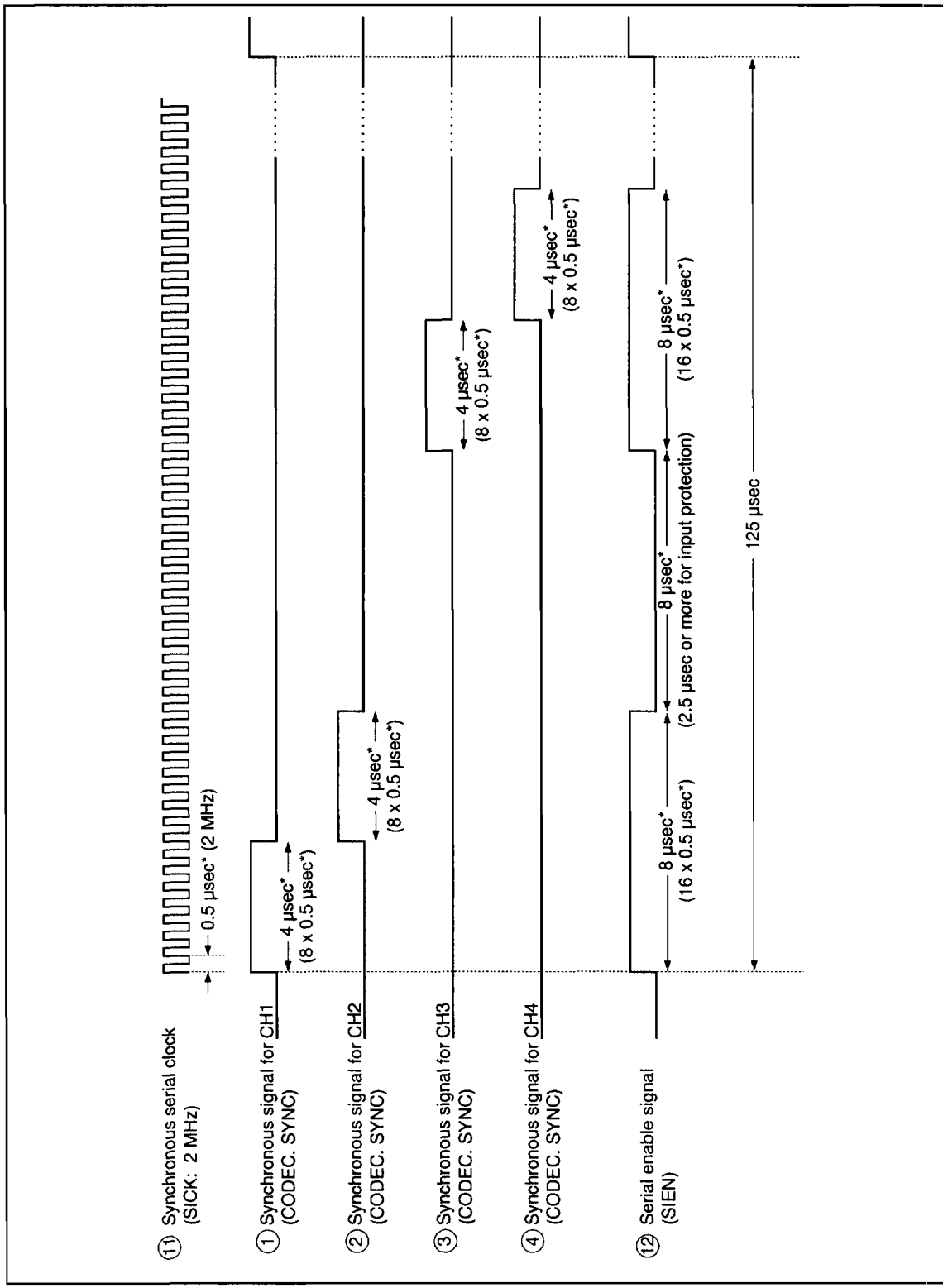


Figure 11 AC Timing Chart (figure 10) of CODEC Interface

Parallel Interface

The parallel interface connects to an 8-bit MPU.

Figure 11 shows the HD81806's data bus connections.

(1) Input (PCM data and commands)

The MPU writes PCM data or commands to the HD81806.

(2) Output (result output data describing received input signals)

The HD81806 outputs result data to the MPU at fixed intervals of 500 µs. The HD81806 simultaneously outputs the $\overline{REQ}$ signal. The MPU reads the data after detecting the $\overline{REQ}$ signal. A data read operation drives the $\overline{REQ}$ signal high.

Notes: 1. When the CPU does not access the HD81806 within 500 µs, after receiving $\overline{REQ}$, the $\overline{REQ}$ signal is left unnegated. When the HD81806 enters the register read status by the combination of the $\overline{CS}$, R/$\overline{W}$, and E signals, the $\overline{REQ}$ signal is negated.

2. If the CPU cannot read the HD81806 register within 500 µs after receiving the $\overline{REQ}$ signal, the HD81806 will overwrite the received result. Therefore, the CPU must read the internal register within 500 µs.

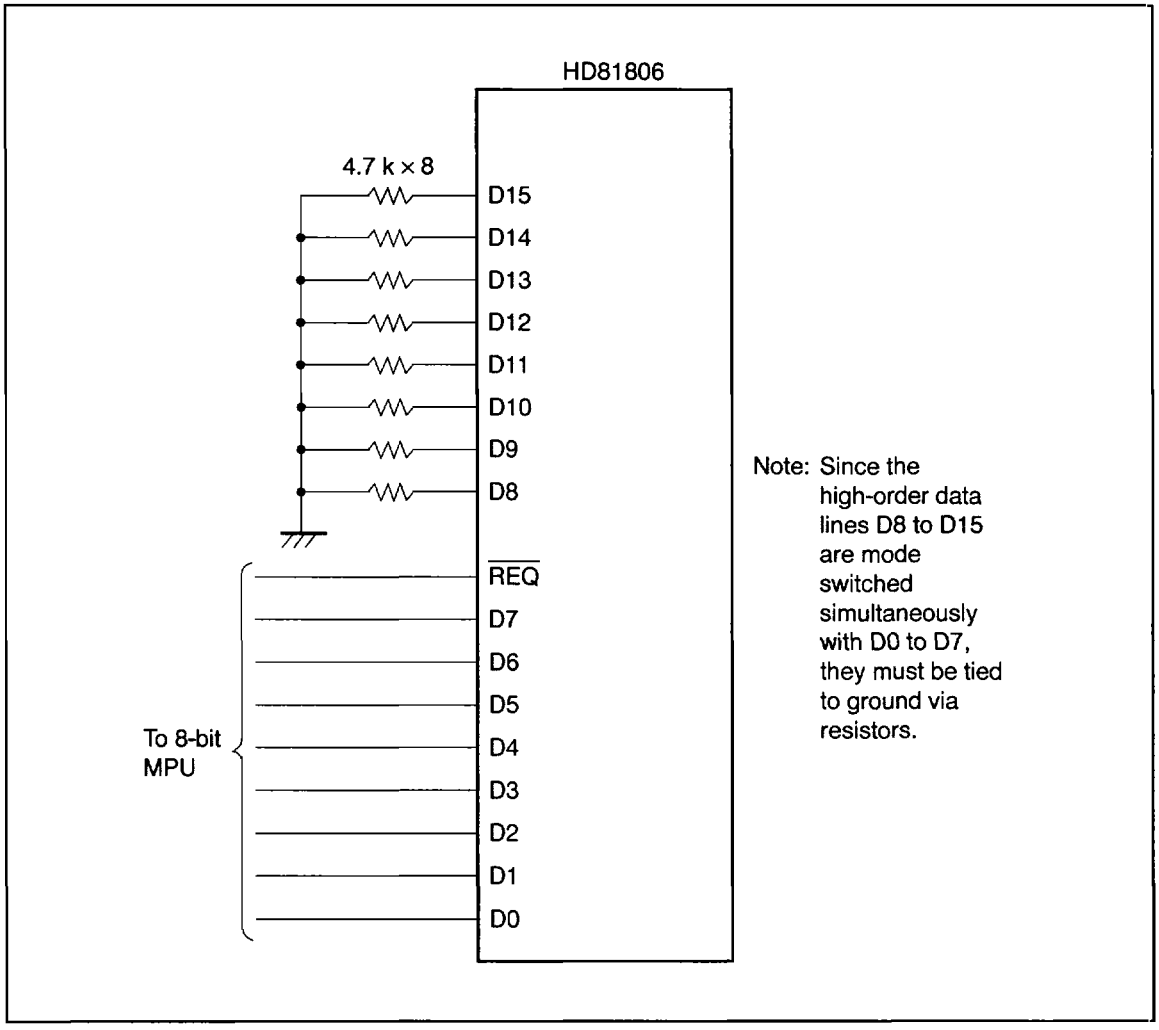


Figure 12 Data Bus Connections When 8-Bit MPU Is Used

(3) Interface with 6800-Family MPU

The parallel data transfer timing enables a Motorola 6800 interface to be used without any additional circuitry. Figure 13 shows an example of the interface with a Hitachi HD6303 8-bit MPU.

(4) Interface with 80-Family MPU

Since the HD81806 does not require a continuous E-clock input, it can be interfaced to the Intel 80xx family of MPUs with only a small amount of additional circuitry.

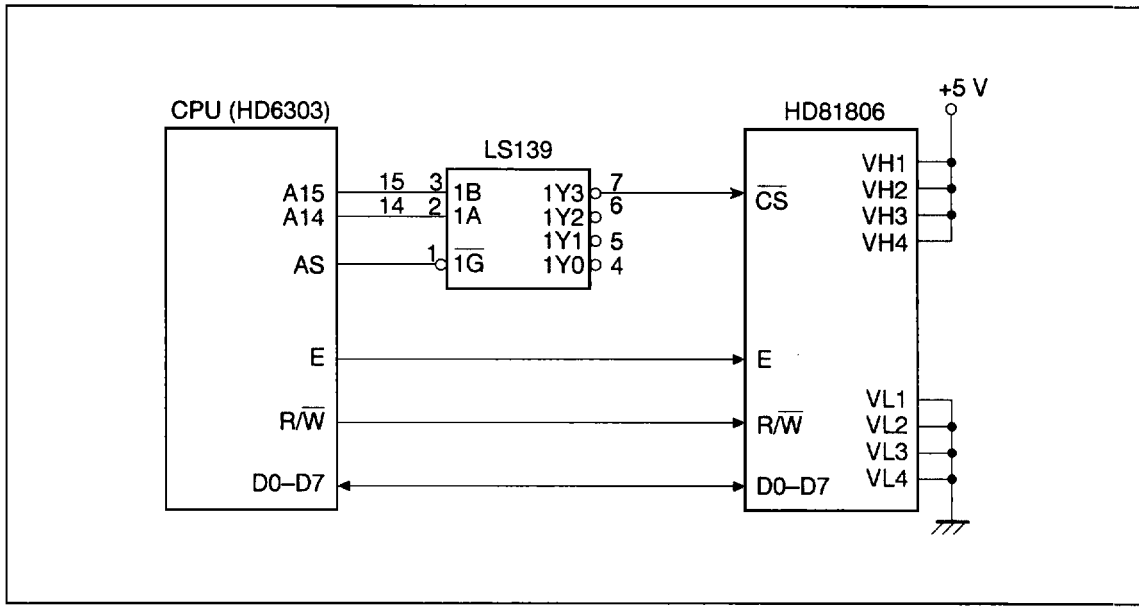


Figure 13 Interface Signals for the HD6303

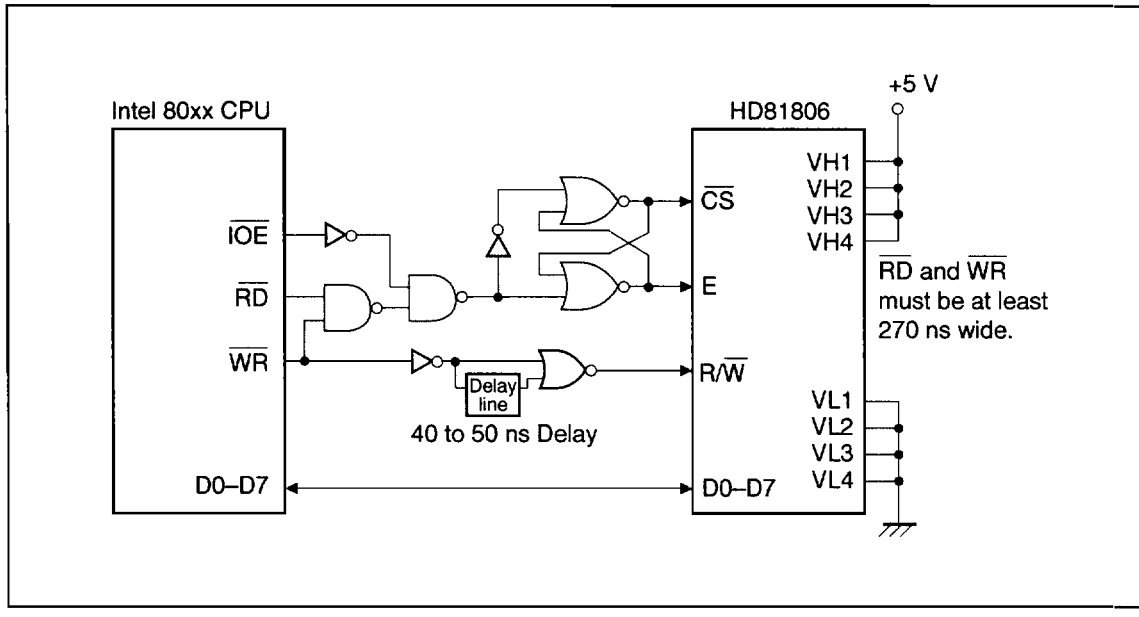


Figure 14 Example of an Intel 80xx CPU Interface

PCM Data Input

The HD81806 can receive PCM data via either its serial or parallel interface. The interface is selected by mode control pin M3.

(1) Initialization

① Once the hardware has been released reset, the HD81806 is ready to receive the DTMF signals for channels 1 to 4, and accept input commands from the CPU. The input command is used to set each parameter to its default value provided the parameter has not been previously modified. The input commands may be in either a serial or parallel data format. A parameter modification resulting from the input of a command is reflected in the characteristic within a maximum of 4 ms, following data input to each of the four channels. The first input command assigns the DTMF/DT signal to each channel, and subsequent input commands modify corresponding parameters.

② The HD81806 will accept only one command until SIEN is input after a reset cancellation. When two or more commands are to be input, the first is sent at least 125 µs after SIEN, and all subsequent commands must also be sent at least 125 µs apart.
SIEN and commands need not be synchronized.

③ The HD81806 regards the first SIEN input after a reset cancellation as channels 1 and 2 and fetches the following PCM data in this timing. However, the HD81806 cannot detect incorrect channel numbers during operation. Accordingly, when the first SIEN is input, input the PCM data of the channels 1 and 2. Configure the system so that the system operates with this timing.

(2) Serial PCM Data Input

In the serial interface, two-channel PCM data (16-bit data is input twice from the CODEC out pin to the HD81806. This procedure is described below. Figure 15 shows the data input timing. The detailed timing is shown in Figure 16.

① The PCM data input timing is determined by the speed of SICK/SIEN. The SICK timing is a maximum of 2048 kHz and a minimum of 500 kHz. Use within this range. In addition, synchronize SIEN with SICK.

② Keep a minimum interal of 2.5 µs from the SIEN falling edge of channels 1 and 2 to the SIEN rising edge of channels 3 and 4.

③ A command can be input concurrently with PCM data input. However, a command can be input asynchronously with PCM data with an input timing of once per 125 µs. If one-or-more commands are input within 125 µs, the operation becomes undefined.

(3) Parallel PCM Data Input

When PCM data are input via the parallel interface, the MPU must send the HD81806 8-bit data four times in succession, described below. Figure 17 shows the data input timing.

- Input PCM data of channels 1 to 4 within 40 µs. However, the intervals between each channel data input must be at least 3 µs.
- When PCM data is input, the data of all four channels must be input.
- Input a command within 15 µs after four-channel PCM data input.
- A command can be input once per one cycle (125 µs).
- The parallel access count within one cycle (125 µs) must be 5 times or less.

Notes: 1. In parallel PCM data input mode, one command and one set of 4-channel data are input every 125 µs. This order has been determined. The HD81806 cannot distinguish a command from data. Accordingly, a command must be input (only once) within 80 µs after input four channels, and PCM data for four channels must be written within 25 µs.

2. If one command and one set of 4-channel data cannot be input within 125 µs, parallel input data may be delayed endlessly.

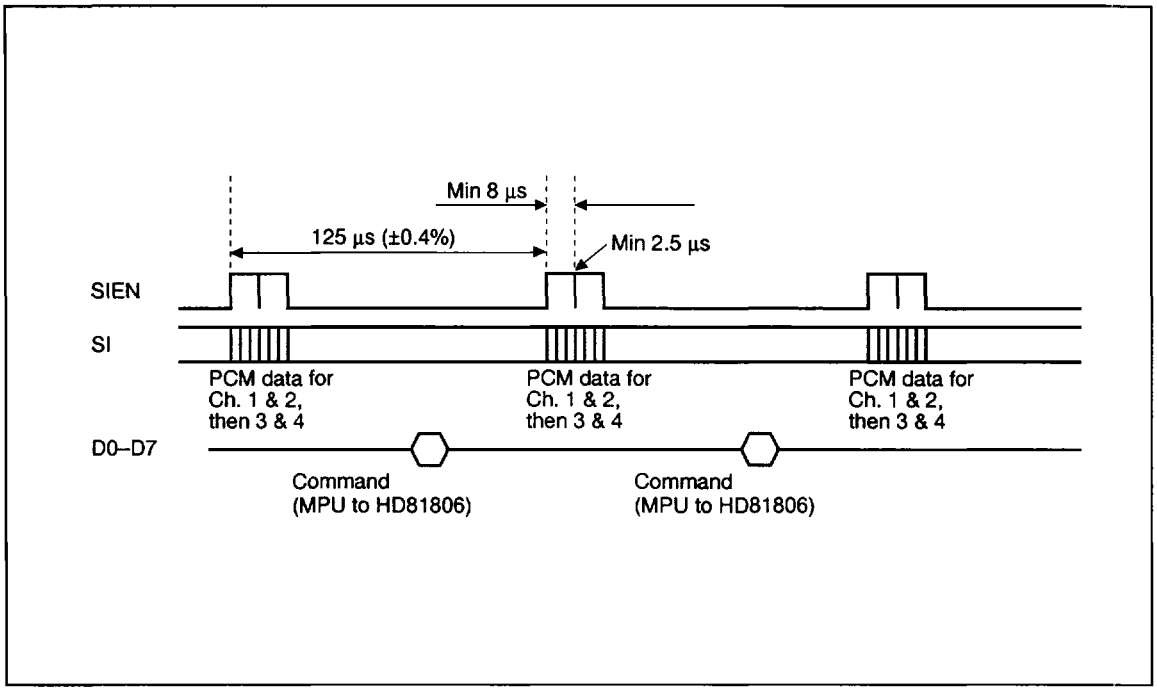
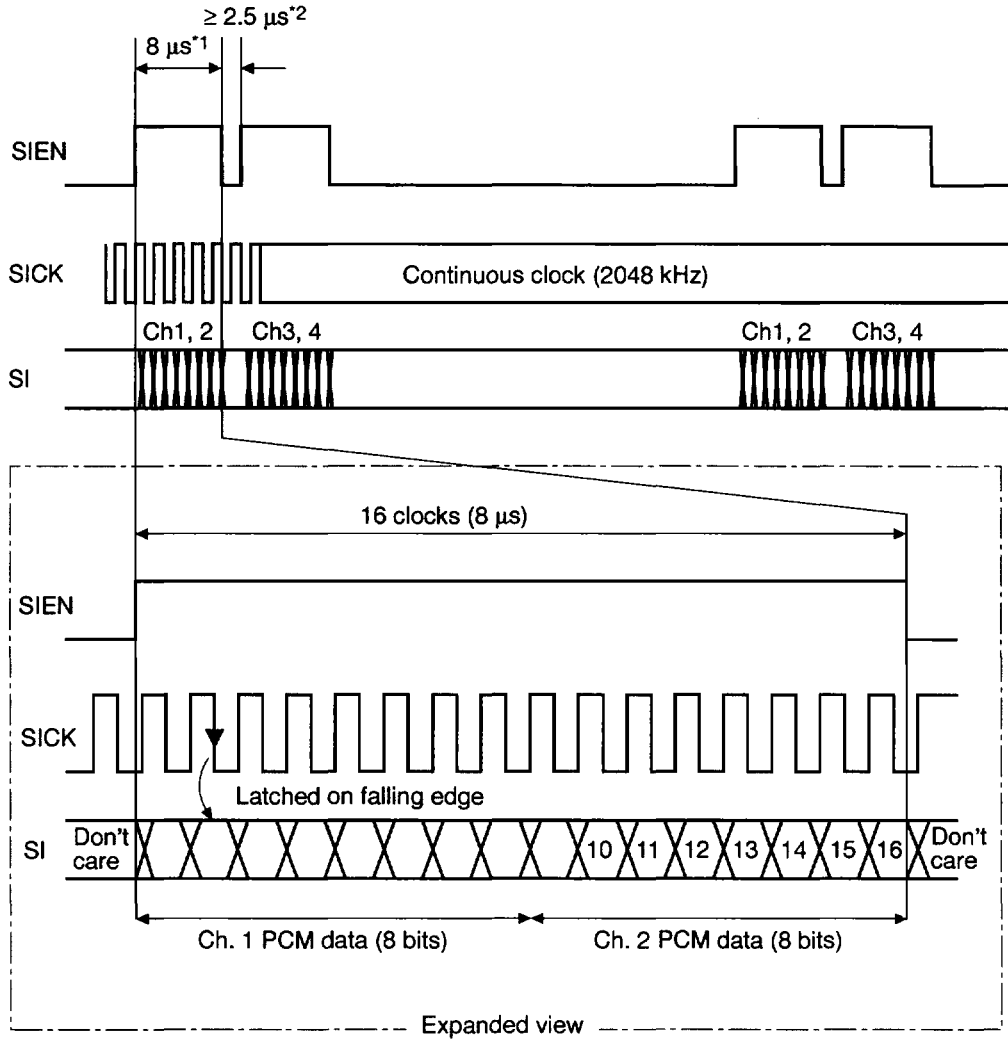


Figure 15 Timing of PCM Data Input via Serial Interface



Notes: 1. 8 µs = 1 clock (0.5 µs = 1/2048 kHz) • 16
2. 2.5 µs = 1 clock (0.5 µs = 1/2048 kHz) • 5

Figure 16 CODEC Interface Timing

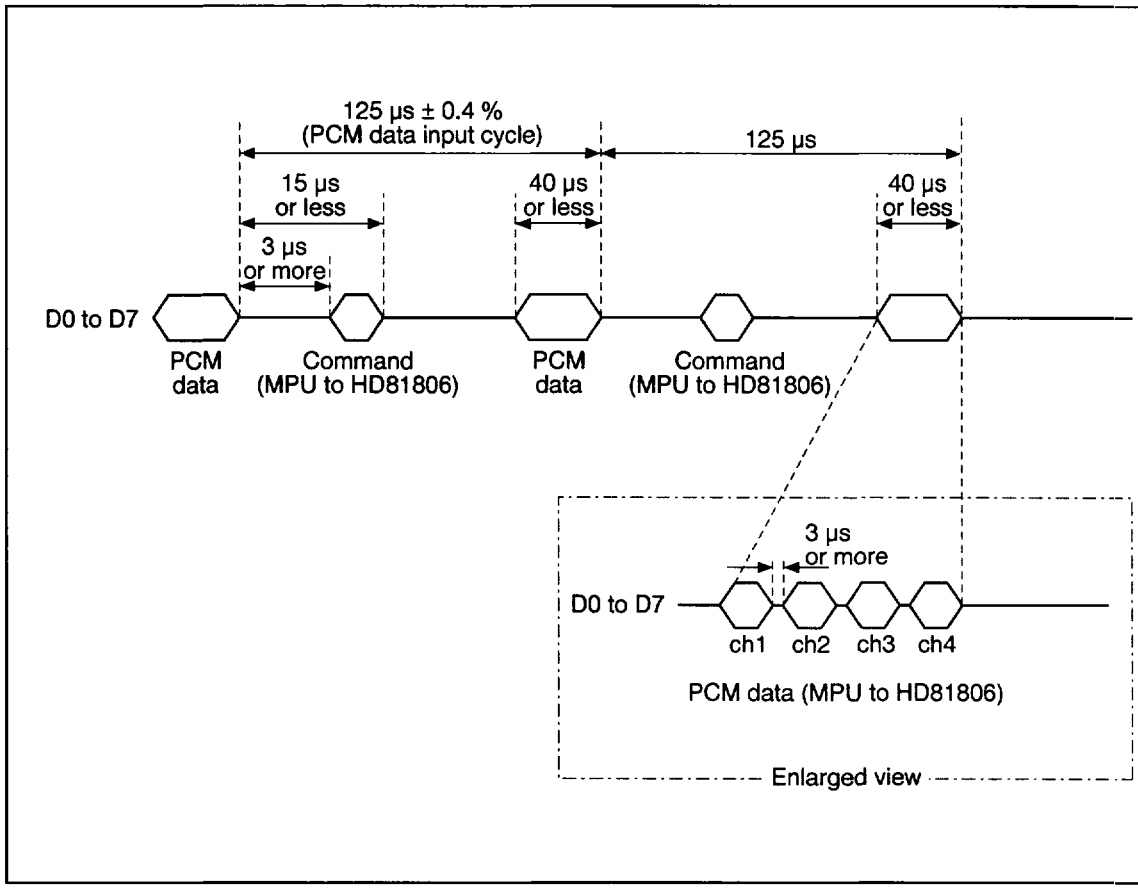


Figure 17 Timing of PCM Data Input via Parallel Interface

(4) 8-Channel Receiver Configuration

Figure 18 shows the block diagram and timing waveforms for eight individual CODEC channels. Each CODEC is connected to the common PCM data highway. The timing for the eight input data channels is controlled by the SIEN enable signal which controls the serial data input to the HD81806 DTMF/DT receiver LSIs. The upper HD81806 ① facilitates recognition of channels 1 and 2, and channels 5 and 6, and the lower HD81806 ② recognizes channels 3 and 4, and channels 7 and 8.

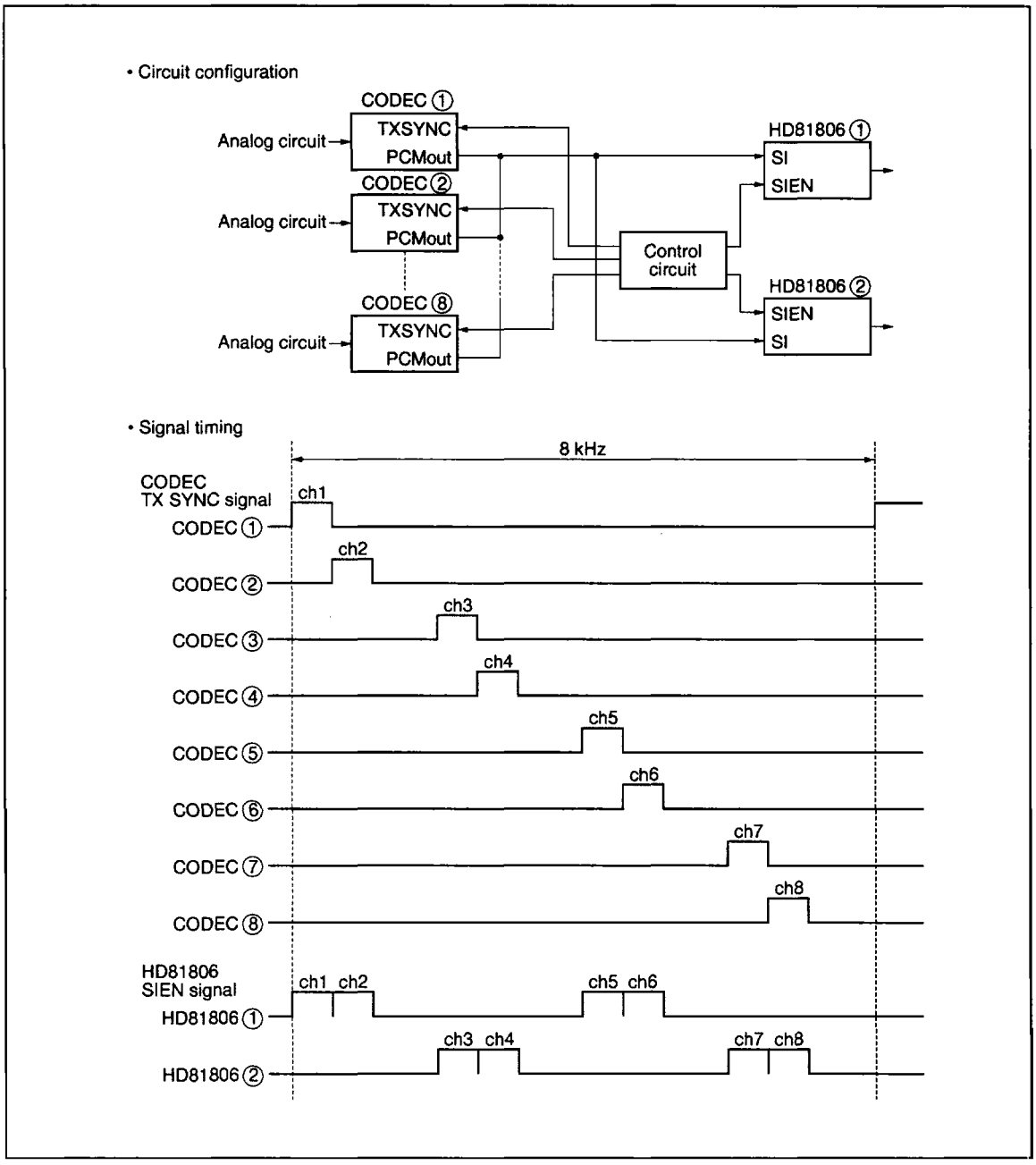


Figure 18 8-Channel Receiver Block Diagram

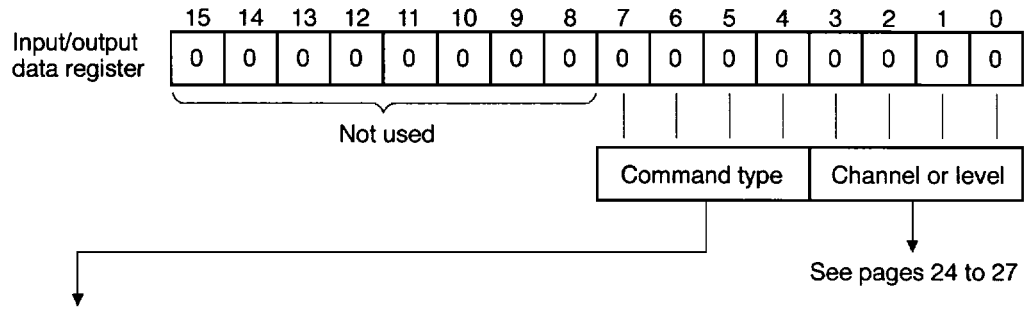
Operating Modes

The operating mode for each channel is selected by commands input via the parallel bidirectional data bus (D0 to D7). DTMF or DT operation can be selected separately for channels 1 to 4. The sensitivity level and other parameters can also be selected. Figure 19 shows the command format.

Bits 7 to 4 designate the command type. Bits 3 to 0 specify the channel or level.

If the input bit pattern corresponds to an undefined command or unassigned level, the HD81806 ignores the command input. The operating mode does not change.

Set the DTMF guard time after setting the line mode (for exchange/terminal).



Bit					
7	6	5	4	**Command Type**	**Specification**
0	0	0	0	Receiver mode (DTMF: 0, DT: 1)	Specified for each channel
0	0	0	1	Line mode (exchange: 0, terminal: 1)	
0	0	1	0	Upper limit of DTMF sensitivity level	
0	0	1	1	Lower limit of DTMF sensitivity level and upper limit of DTMF insensitivity level	
0	1	0	0	DTMF twist characteristic	
0	1	0	1	DTMF guard time	
0	1	1	0	Upper limit of DT sensitivity level and lower limit of DT insensitivity level	Specified for all channels
0	1	1	1	Lower limit of DT sensitivity level and upper limit of DT insensitivity level	
1	0	0	0	DT sensitive-band/dead-band signal ratio (S/N)	
1	0	0	1	DT dead-band signal rejection ratio	
1	0	1	0	DT guard time	
1	0	1	1	Undefined	—
1	1	0	0	Undefined	—
1	1	0	1	Undefined	—
1	1	1	0	Undefined	—
1	1	1	1	Undefined	—

Figure 19 Command Format

(1) Receiver Mode

	Specification for Each Channel			
Receiver Mode	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DTMF: 0, DT: 1	CH4 (0)	CH3 (0)	CH2 (0)	CH1 (0)

Default values are given in parentheses. Channels 1 to 4 default to DTMF.

(2) Line Mode

	Specification for All Channels			
Line Mode	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Exchange: 0, terminal: 1	—	—	—	CH1–4 (0)

Default values are given in parentheses. Channels 1 to 4 default to exchange mode.

(3) Upper Limit of DTMF Sensitivity Level

		Level Specification			
Level	**Upper Limit of Sensitivity Level**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Level 0	0 dBm0	0	0	0	0
Level 1	–1 dBm0	0	0	0	1
Level 2	–2 dBm0	0	0	1	0
Level 3*1	–3 dBm0	0	0	1	1
Level 4	–4 dBm0	0	1	0	0
Level 5	–5 dBm0	0	1	0	1

Note: 1. Default value

(4) Lower Limit of DTMF Sensitivity Level and Upper Limit of DTMF Insensitivity Level

	Lower Limit of Sensitivity Level		Upper Limit of Insensitivity Level		Level Specification			
Level	**Exchange**	**Terminal**	**Exchange**	**Terminal**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Level 0*1	–24 dBm0	–42 dBm0	–29 dBm0	–50 dBm0	0	0	0	0
Level 1	–25 dBm0	–43 dBm0	–30 dBm0	–51 dBm0	0	0	0	1
Level 2	–26 dBm0	–44 dBm0	–32 dBm0	–52 dBm0	0	0	1	0
Level 3	–27 dBm0	–45 dBm0	–33 dBm0	–53 dBm0	0	0	1	1
Level 4	–28 dBm0	–46 dBm0	–34 dBm0	–54 dBm0	0	1	0	0
Level 5	–29 dBm0	–47 dBm0	–35 dBm0	–55 dBm0	0	1	0	1

Note: 1. Default value

(5) DTMF Twist Characteristic

Level	Twist Characteristic	Level Specification			
		Bit 3	Bit 2	Bit 1	Bit 0
Level 0	±5 dB	0	0	0	0
Level 1	±6 dB	0	0	0	1
Level 2	±7 dB	0	0	1	0
Level 3	±8 dB	0	0	1	1
Level 4	±9 dB	0	1	0	0
Level 5*1	±10 dB	0	1	0	1

Note: 1. Default value

(6) DTMF Guard Time

Level	Guard Time	Level Specification			
		Bit 3	Bit 2	Bit 1	Bit 0
Level 0	10 ms	0	0	0	0
Level 1	14 ms	0	0	0	1
Level 2	18 ms	0	0	1	0
Level 3	22 ms	0	0	1	1
Level 4	26 ms	0	1	0	0
Level 5	30 ms	0	1	0	1
Level 6	34 ms	0	1	1	0
Level 7*1	38 ms	0	1	1	1

Note: 1. Default value

(7) Upper Limit of DT Sensitivity Level and Lower Limit of DT Insensitivity Level

Level	Upper Limit of Sensitivity Level	Lower Limit of Insensitivity Level	Level Specification			
			Bit 3	Bit 2	Bit 1	Bit 0
Level 0*1	0 dBm0	3 dBm0	0	0	0	0
Level 1	–1 dBm0	2 dBm0	0	0	0	1
Level 2	–2 dBm0	1 dBm0	0	0	1	0
Level 3	–3 dBm0	0 dBm0	0	0	1	1

Note: 1. Default value

(8) Lower Limit of DT Sensitivity Level and Upper Limit of DT Insensitivity Level

Level	Lower Limit of Sensitivity Level	Upper Limit of Insensitivity Level	Level Specification Bit 3	Bit 2	Bit 1	Bit 0
Level 0*1	–45 dBm0	–55 dBm0	0	0	0	0
Level 1	–46 dBm0	–56 dBm0	0	0	0	1
Level 2	–47 dBm0	–57 dBm0	0	0	1	0
Level 3	–48 dBm0	–58 dBm0	0	0	1	1

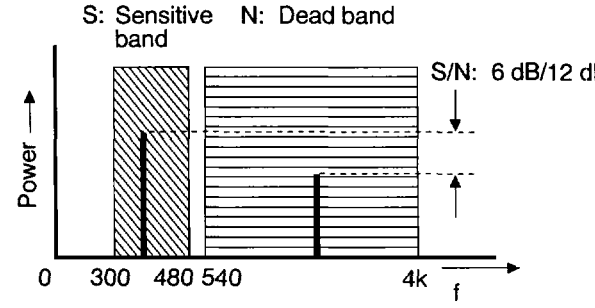
Note: 1. Default value

(9) DT Sensitive-Band/Dead-Band Signal Ratio (S/N)

Level	Sensitive-Band/Dead-Band Signal Ratio (S/N)	Level Specification Bit 3	Bit 2	Bit 1	Bit 0
Level 0*1	DT is not detected if S/N ≤ 6 dB	0	0	0	0
Level 1	DT is not detected if S/N ≤ 12 dB	0	0	1	0

Note: 1. Default value

The HD81806 detects DT by testing the power ratio of the bandpass filter output (300 to 480 Hz) in the sensitive band and the high-pass filter output (≥ 540 Hz) in the dead band (S/N ratio). DT is not detected when the S/N ratio is equal to or less than a selected value (6 dB or 12 dB). See diagram on right.

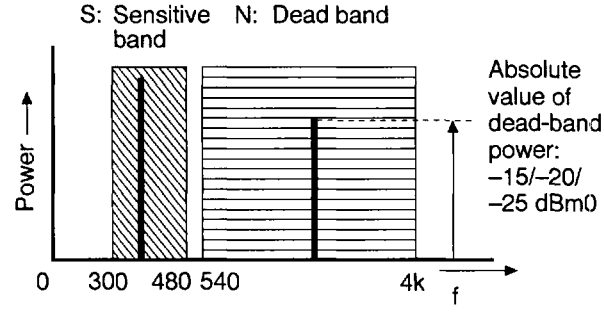


(10) DT Dead-Band Rejection Level

Level	Dead-Band Rejection Level	Level Specification Bit 3	Bit 2	Bit 1	Bit 0
Level 0	DT is not detected if dead-band power ≥ –15 dBm0	0	0	0	0
Level 1*1	DT is not detected if dead-band power ≥ –20 dBm0	0	0	0	1
Level 2	DT is not detected if dead-band power ≥ –25 dBm0	0	0	1	0

Note: 1. Default value

The HD81806 detects DT by testing the dead-band power of the high-pass filter output (≥ 540 Hz). DT is not detected when the absolute value of the dead-band power is equal to or greater than a selected value (–15, –20, or –25 dBm0). See diagram on right.



(11) DT Guard Time

		Level Specification			
Level	**Guard Time**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Level 0*1	30 ms	0	0	0	0
Level 1	40 ms	0	0	0	1
Level 2	50 ms	0	0	1	0
Level 3	80 ms	0	0	1	1
Level 4	120 ms	0	1	0	0
Level 5	330 ms	0	1	0	1
Level 6	380 ms	0	1	1	0
Level 7	400 ms	0	1	1	1

Note: 1. Default value

Early Steering Flag and Valid Flag

The HD81806 registers detection of a DTMF or DT signal by the early steering flag and valid flag in its output data. Figure 20 shows the detection timing in DTMF and DT modes. Tables 2 and 3 list the values of the timing parameters for DTMF and DT modes.

(1) Early steering flag (EST)

The early steering flag is set (EST = 1) during detection of the DTMF or DT signal.

(2) Valid Flag (VAF)

The valid flag is set (VAF = 1) when the DTMF or DT signal is detected for a period of time exceeding the guard time.

(3) The relationship between guard time and VAF

The relationship between guard time and VAF is shown in the following.
(For DTMF mode)
t_{VAFr} = guard time value + (10 to 26 ms)
t_{VAFf} = guard time value + (–8 to –6 ms)
(For DT mode)
t_{VAFrDT} = guard time value + (11 to 21 ms)
t_{VAFfDT} = guard time value + (–2 to –29 ms)

Table 2 DTMF Signal Detection Timing (Exchange/Terminal mode)

Item	Symbol	Min	Typ	Max	Unit
EST rise time	T_{ESTr}	8	—	10	ms
VAF rise time	T_{VAFr}	44	—	47	ms
EST fall time	T_{ESTf}	37	—	42	ms
VAF fall time	T_{VAFf}	30	—	32	ms

Table 3 DT Signal Detection Timing

Item	Symbol	Min	Typ	Max	Unit
EST rise time	T_{ESTrDT}	6	—	10	ms
VAF rise time	T_{VAFrDT}	38	—	88	ms
EST fall time	T_{ESTfDT}	4	—	6	ms
VAF fall time	T_{VAFfDT}	6	—	10	ms

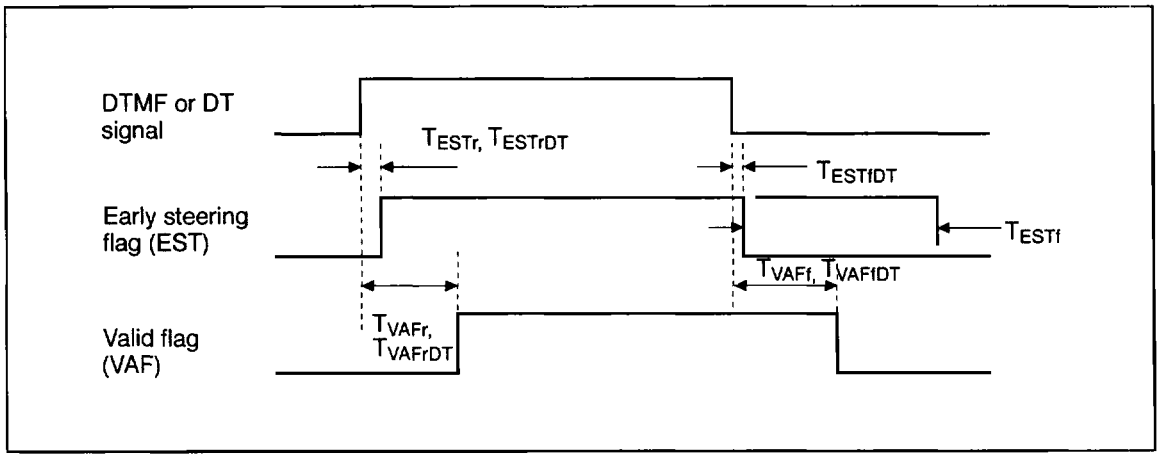


Figure 20 DTMF and DT Signal Detection Timing

Data Output

Data are output via the parallel interface by the procedure given next. Figure 21 shows the timing.

(1) Data for one channel are output at 500-µs intervals. The data for all four channels are accordingly updated every 2 ms.

(2) When the HD81806 outputs data (every 500 µs), it drives the $\overline{REQ}$ line low. The data are held on the data bus (D0 to D7) for 500 µs. Even if the $\overline{REQ}$ signal is negated, the contents of the data bus are preserved for 500 µs. Unless SIEN is input, the $\overline{REQ}$ pin will not be activated.

(3) The MPU reads the data after detecting the low $\overline{REQ}$ signal. The $\overline{REQ}$ signal returns high level once the MPU has read the data. When the CPU cannot read the HD81806 register within 500 µs, the $\overline{REQ}$ signal is not negated and the output data of the next channel is overwritten.

(4) When the operating mode is changed due to the input of a new command, the results appear within a maximum of 4 ms following the changeover. This is because all current processing must be completed prior to mode changeover.

(5) Since the input data is sampled at 8 kHz (or 125 µs) for a data output cycle of 2 ms, the output data for each channel is calculated based on the 16 time slots (2 ms/125µs) of the previous input data.

(6) The output cycle of the $\overline{REQ}$ signal may include a deviation of 7 µs depending on whether or not a command is input. However, since this deviation is within a 125 µs cycle, the operation is not affected.

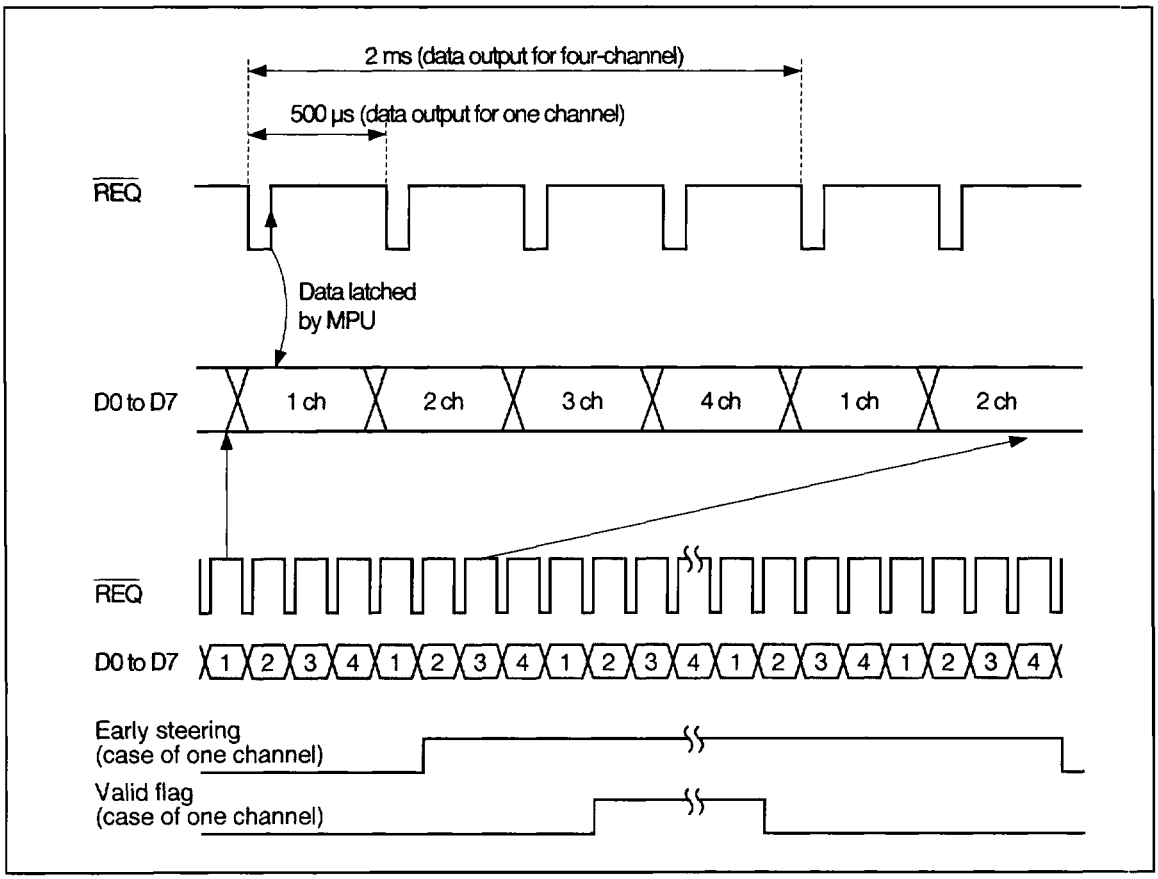


Figure 21 Output Timing

(1) Data Output Format in DTMF Mode

DTMF-mode output data

15 ... 8	7	6	5 4	3 2 1 0
Undetermined	VAF	EST	Ch No.	Logic output

bit 0 to bit 3: Logic output
Table 4 shows the output results.
Two types of logic output can be selected, as indicated in table 4.
The type selection is made at mode control pin M1.

bit 4 and bit 5: Channel number
Indicates the output data channel.

	Bit	
Ch No.	**5**	**4**
1	0	0
2	0	1
3	1	0
4	1	1

bit 6: EST (early steering flag)
0: No DTMF signal
1: DTMF signal present

bit 7: VAF (valid flag)
0: Output result data invalid
1: Output result data valid

Figure 22 Data Output Format in DTMF Mode

Table 4 Logic Output Table

Tone No.			Logic Output Type 1				Logic Output Type 2			
F_{LOW}	F_{HIGH}	No.	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0
697 Hz	1209 Hz	1	0	0	0	1	0	0	0	1
697	1336	2	0	0	1	0	0	0	1	0
697	1477	3	0	0	1	1	0	0	1	1
770	1209	4	0	1	0	0	0	1	0	0
770	1336	5	0	1	0	1	0	1	0	1
770	1477	6	0	1	1	0	0	1	1	0
852	1209	7	0	1	1	1	0	1	1	1
852	1336	8	1	0	0	0	1	0	0	0
852	1477	9	1	0	0	1	1	0	0	1
941	1336	0	1	0	1	0	0	0	0	0
941	1209	*	1	0	1	1	1	1	1	0
941	1477	#	1	1	0	0	1	1	1	1
697	1633	A	1	1	0	1	1	0	1	0
770	1633	B	1	1	1	0	1	0	1	1
852	1633	C	1	1	1	1	1	1	0	0
941	1633	D	0	0	0	0	1	1	0	1

(2) Data Output Format in DT Mode

DT-mode output data

15 ... 8	7	6	5 4	3 2 1 0
Undetermined	VAF	EST	Ch No.	Level detected

bit 0 to bit 3: Level detected
The received input level is output in 5-dB steps.

	Bit			
Level Detected	**3**	**2**	**1**	**0**
≥ –5 dBm0	0	0	0	1
≥ –10 dBm0	0	0	1	0
≥ –15 dBm0	0	0	1	1
≥ –20 dBm0	0	1	0	0
≥ –25 dBm0	0	1	0	1
≥ –30 dBm0	0	1	1	0
≥ –35 dBm0	0	1	1	1
≥ –40 dBm0	1	0	0	0
≥ –45 dBm0	1	0	0	1
Insensitive level	1	1	1	1

bit 4 and bit 5: Channel number
Indicates the output data channel. Same as bit 4 to bit 5 in figure 21.

bit 6: EST (early steering flag)
0: No DT signal
1: DT signal present

bit 7: VAF (valid flag)
0: Output result data invalid
1: Output result data valid

Figure 23 Data Output Format in DT Mode

Absolute Maximum Ratings (V_{SS} = 0 V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Pin voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature*1	t_{opr}	–20 to +75	°C
Storage temperature	t_{stg}	–55 to +125	°C

Note: The operating range of a wide-temperature-range product is from –40 to +75°C.

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ±5%, V_{SS} = 0 V, T_a = –20 to +75°C unless otherwise specified, wide-temperature-range product: Ta = –40 to +85°C)

Item	Pin(s)	Symbol	Min	Typ	Max	Unit	Test Conditions
Input high voltage	E, OSC, SICK	V_{IH}	2.4	—	V_{CC} + 0.3	V	
	$\overline{RES}$		V_{CC} × 0.7	—	V_{CC} + 0.3		
	Other input pins		2.2	—	V_{CC} + 0.3		
Input low voltage	E, OSC, SICK	V_{IL}	–0.3	—	0.4	V	
	$\overline{RES}$		–0.3	—	0.4		
	Other input pins		–0.3	—	0.4		
Input leakage current	E, R/$\overline{W}$, $\overline{CS}$, OSC SI, VL1–VL4 VH1–VH4, SICK $\overline{RES}$, SIEN	$\lvert I_{IL} \rvert$	—	—	10	µA	V_{in} = 0.4 to 2.4 V
Three-state current (off state)	D0–D15	$\lvert I_{TS} \rvert$	—	—	10	µA	V_{in} = 0.4 to 2.4 V
Open-drain current (off state)	$\overline{REQ}$, M1–M3	$\lvert I_{LOH} \rvert$	—	—	10	µA	V_{in} = 0.4 to 2.4 V
Output high voltage	D0–D15	V_{OH}	2.4	—	—	V	$-I_{OH}$ = 400 µA
Output low voltage	D0–D15	V_{OL}	—	—	0.8	V	I_{OL} = 1.6 mA
Input capacitance	All input pins	C_{in}	—	—	12.5	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
Current dissipation		I_{CC}	—	—	100	mA	Unloaded output

AC Characteristics (V_{CC} = 5.0 V ±5%, V_{SS} = 0 V, T_a = –20 to +75°C unless otherwise specified, wide-temperature-range product : T_a = –40 to +85°C)

• System Clock

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Clock (OSC) cycle time	ϕ_{cyc}	—	25	—	ns	Figure 24
Clock (OSC) pulse width	ϕ_{WH}	7.5	—	—	ns	
	ϕ_{WL}	7.5	—	—	ns	
Clock (OSC) rise time	ϕ_r	—	—	5	ns	
Clock (OSC) fall time	ϕ_f	—	—	5	ns	

• Reset Timing

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset time	t_{RC}	20	—	—	ms	Figure 25
Reset pulse width	t_{RST}	1.0	—	—	µs	

• Serial Input Timing

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Clock (SICK) cycle time	S_{cyc}	0.4	—	2	µs	Figure 26
Clock (SICK) pulse width	S_{WH}	100	200	—	ns	
	S_{WL}	100	200	—	ns	
Clock (SICK) rise time	S_r	—	—	40	ns	
Clock (SICK) fall time	S_f	—	—	40	ns	
Serial input data setup time	t_{SDS}	100	—	—	ns	
Serial input data hold time	t_{SDH}	100	—	—	ns	
Enable (SIEN) delay time	t_{ED}	100	—	—	ns	
Enable (SIEN) setup time	t_{ES}	100	—	—	ns	

• Parallel Input/Output Timing

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Enable (E) cycle time	t_{cyc}	0.5	—	—	µs	Figure 27
Enable (E) pulse width	t_{WH}	210	—	5000	ns	
	t_{WL}	210	—	—	ns	
Enable (E) rise time	t_r	—	—	20	ns	
Enable (E) fall time	t_f	—	—	20	ns	
$\overline{CS}$ setup time	t_{CS}	60	—	—	ns	
$\overline{CS}$ hold time	t_{CH}	10	—	—	ns	
Parallel input data setup time	t_{DSW}	60	—	—	ns	
Parallel input data hold time	t_{DHW}	10	—	—	ns	
Output data delay time	t_{DDR}	—	—	150	ns	
Output data hold time	t_{DHR}	20	—	—	ns	

Timing Diagrams

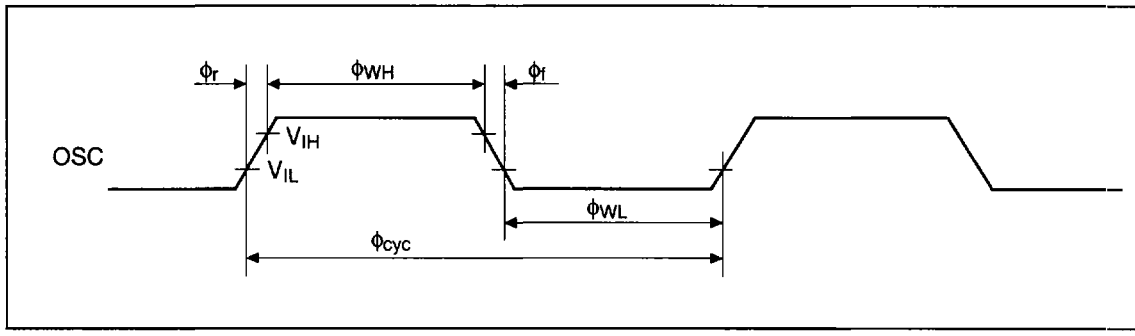


Figure 24 System Clock Waveform

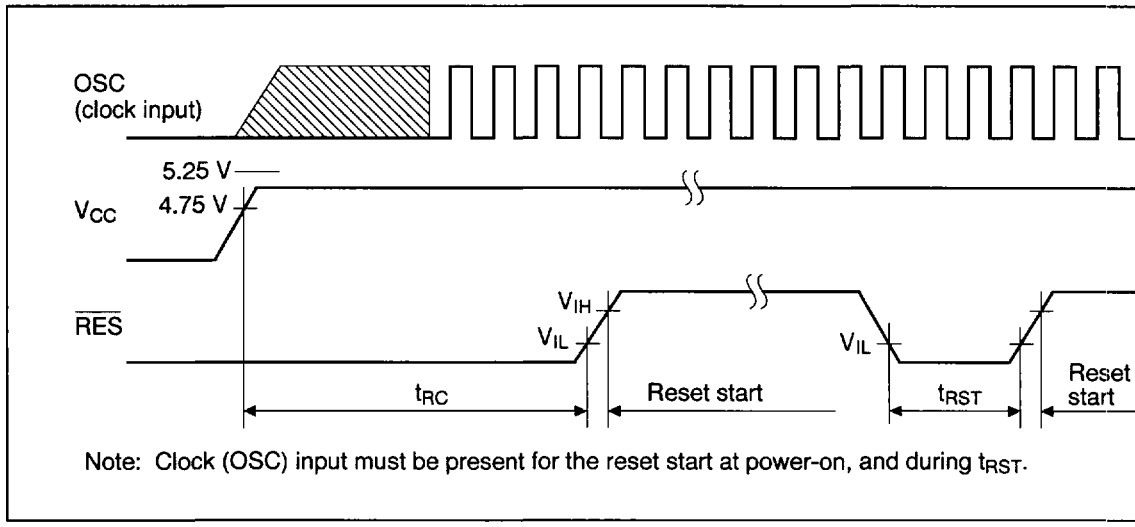


Figure 25 Reset Timing

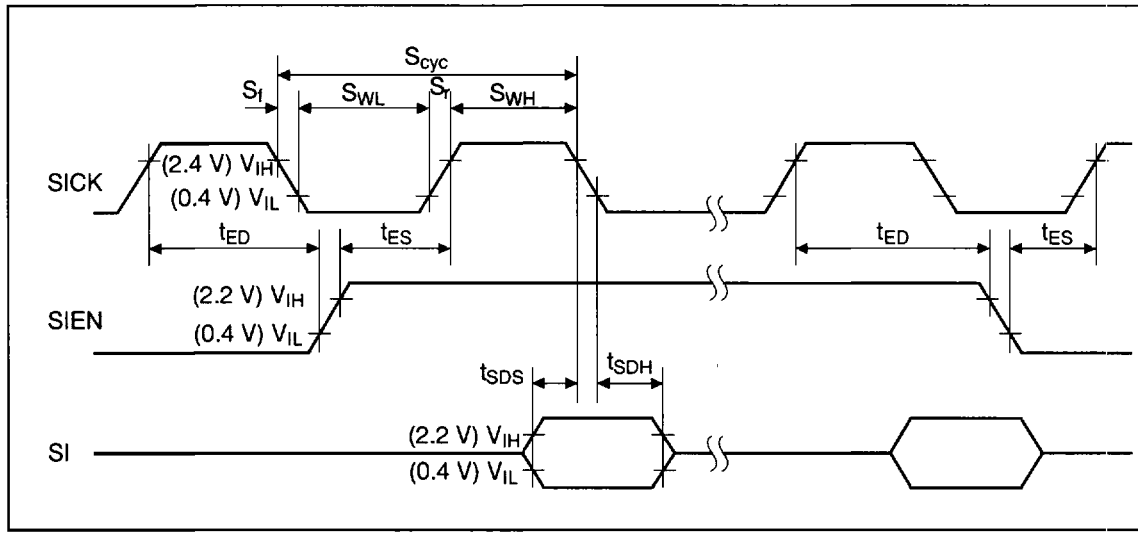


Figure 26 Serial Input Timing

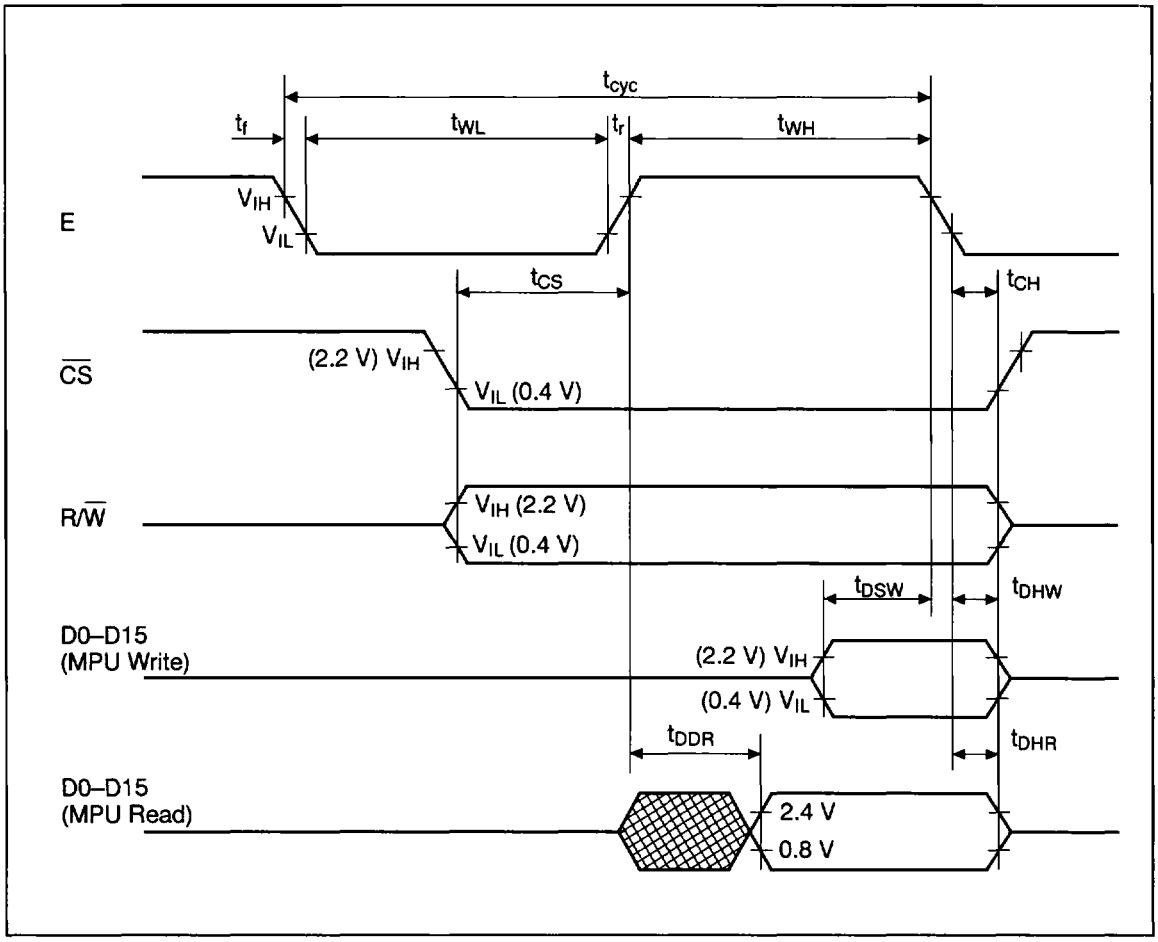


Figure 27 Parallel Input/Output Timing

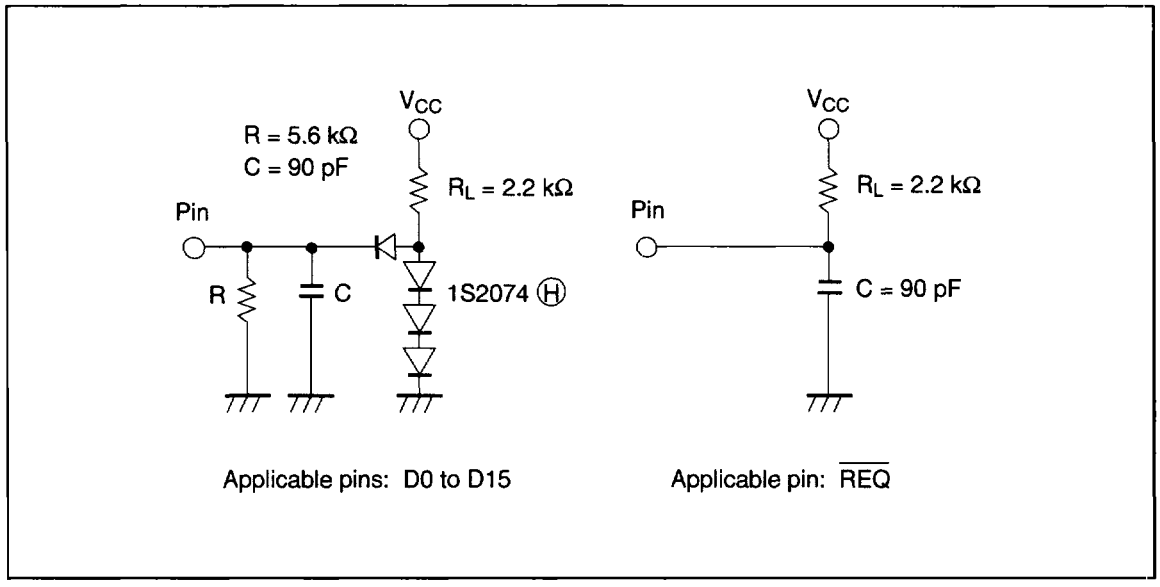


Figure 28 Load Circuit for Timing Tests