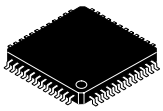


SLAS364A – APRIL 2002 – REVISED JUNE 2002

# 18-BIT, 500-kHz, UNIPOLAR INPUT, MICRO POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

## FEATURES

- High-Speed Parallel Interface
- 500-kHz Sample Rate
- Low Power: 100 mW at 500 kHz
- Unipolar Input Range
- Wide Digital Supply
- 8-/16-/18-Bit Bus Transfer
- 48-Pin TQFP Package

## APPLICATIONS

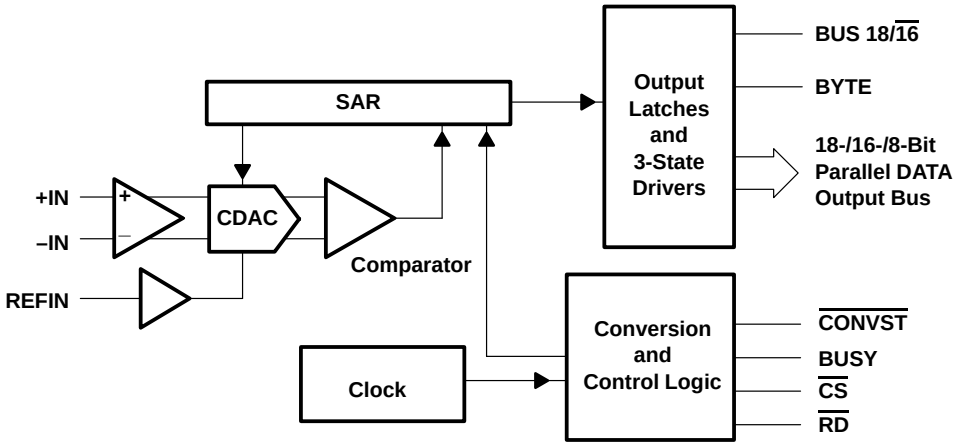
- Medical Instruments
- Optical Networking
- Transducer Interface
- High Accuracy Data Acquisition Systems
- Magnetometers

## DESCRIPTION

The ADS8381 is an 18-bit, 500 kHz A/D converter. The device includes a 18-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8381 offers a full 18-bit interface, a 16-bit option where data is read using two read cycles or even an 8-bit bus using three read cycles if necessary.

The ADS8381 is available in a 48-lead TQFP package and is characterized over the industrial –40°C to 85°C temperature range.

PRODUCT PREVIEW



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| MODEL | RELATIVE ACCURACY ($T_{min}$/$T_{max}$) | NO MISSING CODES RESOLUTION ($T_{min}$/$T_{max}$) | PACKAGE TYPE | TEMPERATURE RANGE |
|---|---|---|---|---|
| ADS8381Y | 18 | –40°C/85°C | 48 Pin TQFP | –40°C to 85°C |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†

Voltage, +IN to AGND . . . . . +VA + 0.1 V
Voltage, –IN to AGND . . . . . 0.5 V
Voltage range, +VA to AGND . . . . . –0.3 V to 7 V
Voltage range, +VBD to BDGND . . . . . –0.3 V to 7 V
Voltage range, +VA to +VBD . . . . . –0.3 V to 2.5 V
Digital input voltage to BDGND . . . . . –0.3 V to +VBD + 0.3 V
Digital output voltage to BDGND . . . . . –0.3 V to +VBD + 0.3 V
Operating free-air temperature range, $T_A$ . . . . . –40°C to 85°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Junction temperature ($T_J$ max) . . . . . 150°C
TQFP package: Power dissipation . . . . . $(T_J Max – T_A)/\theta_{JA}$
$\theta_{JA}$ thermal impedance . . . . . 86°C/W
Lead temperature, soldering: Vapor phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

## SPECIFICATIONS

+VA = 5 V, $T_A$ = –40°C to 85°C, +VBD = 2.7 V or 5 V, $f_{SAMPLE}$ = 500 kHz (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Analog Input** | | | | | |
| Full-scale input voltage (see Note 1) | +IN – –IN | 0 | | $V_{ref}$ | V |
| Absolute input voltage | +IN | –0.2 | | $V_{ref}$ + 0.2 | V |
| | –IN | –0.2 | | 0.2 | |
| Input capacitance | | | 45 | | pF |
| Input leakage current | | | | | pA |
| **System Performance** | | | | | |
| Resolution | | | 18 | | Bits |
| No missing codes | (+IN – –IN) < 0.45 FS | 18 | | | Bits |
| | (+IN – –IN) ≥ 0.45 FS | 17 | | | |
| Integral linearity | (+IN – –IN) < 0.125 FS | | ±2.5 | ±3 | LSB (18 bit) (see Note 2) |
| | (+IN – –IN) < 0.45 FS | | ±4 | ±5 | |
| | (+IN – –IN) ≥ 0.45 FS | | ±6 | ±7.5 | |
| Differential linearity | (+IN – –IN) < 0.125 FS | –1 | –0.9~1.5 | 2 | LSB (18 bit) |
| | (+IN – –IN) < 0.45 FS | –1 | –0.9~3 | 3 | |
| | (+IN – –IN) ≥ 0.45 FS | –2 | –0.9~4 | 4 | |
| Offset error (see Note 3) | | | 48 | | LSB (18 bit) |
| Gain error | | | 48 | | LSB (18 bit) |
| Common-mode rejection ratio | At dc | | | | dB |
| | +IN – – IN = 1 $V_{pp}$ at 1 MHz | | | | |
| Noise | | | 60 | | µV RMS |
| Power supply rejection ratio | At 3FFFF output code | | | | dB |
| **Sampling Dynamics** | | | | | |
| Conversion time | | | | 1.6 | µs |
| Acquisition time | | 0.4 | | | µs |
| Throughput rate | | | | 500 | kHz |
| Aperture delay | | | | | ns |
| Aperture jitter | | | | | ps |
| Step response | | | | | ns |
| Over voltage recovery | | | | | ns |
| **Dynamic Characteristics** | | | | | |
| Total harmonic distortion (see Note 4) | $V_{IN}$ = 4 $V_{pp}$ at 10 kHz | | 95 | | dB |
| | $V_{IN}$ = 4 $V_{pp}$ at 100 kHz | | 87 | | |
| Signal-to-noise (SNR) | $V_{IN}$ = 4 $V_{pp}$ at 10 kHz | | 88 | | dB |
| | $V_{IN}$ = 4 $V_{pp}$ at 100 kHz | | 85 | | |
| Signal-to-noise + distortion (SINAD) | $V_{IN}$ = 4 $V_{pp}$ at 10 kHz | | 88 | | dB |
| | $V_{IN}$ = 4 $V_{pp}$ at 100 kHz | | 87 | | |
| Spurious free dynamic range | $V_{IN}$ = 4 $V_{pp}$ at 10 kHz | | 87 | | dB |
| | $V_{IN}$ = 4 $V_{pp}$ at 100 kHz | | 87 | | |
| –3dB Small signal bandwidth | | | | | MHz |

NOTES: 1. Ideal input span, does not include gain or offset error.
2. LSB means least significant bit
3. Measured relative to an ideal full-scale input (+IN – –IN) of 4.096 V
4. Calculated on the first nine harmonics of the input frequency

PRODUCT PREVIEW

## SPECIFICATIONS

+VA = +5 V, At –40°C to 85°C, +VBD = 5 V or 2.7 V, $f_{SAMPLE}$ = 500 kHz (unless otherwise noted)(continued)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Voltage Reference Input** | | | | | | |
| $V_{REF}$ Reference voltage | | | 2.5 | 4.096 | 4.2 | V |
| $V_{REF}$ Reference resistance (see Note 1) | | | | 100 | | kΩ |
| **Digital Input/Output** | | | | | | |
| Logic family | | | | CMOS | | |
| Logic level | $V_{IH}$ | $I_{IH}$ = 5 μA | 2.0 | | $+V_{BD}$ + 0.3 | V |
| | $V_{IL}$ | $I_{IL}$ = 5 μA | –0.3 | | 0.8 | |
| | $V_{OH}$ | $I_{OH}$ = 2 TTL loads | $+V_{BD}$ – 0.6 | | | |
| | $V_{OL}$ | $I_{OL}$ = 2 TTL loads | | | 0.4 | |
| Data format | | | | Straight Binary | | |
| **Power Supply Requirements** | | | | | | |
| Power supply voltage | +VBD | | 2.7 | 3.3 | 5.25 | V |
| | +VA | | 4.75 | 5 | 5.25 | V |
| Supply current, 500-kHz sample rate | | | | 20 | 26 | mA |
| Power dissipation, 500-kHz sample rate | | | | 100 | 130 | mW |
| **Temperature Range** | | | | | | |
| Operating free-air | | | –40 | | 85 | °C |

NOTE 1: Can vary ±30%

PRODUCT PREVIEW

## TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA = +VBD = 5 V (see Notes 1 and 2)

| | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CONV}$ | Conversion time | | | 1.6 | µs |
| $t_{ACQ}$ | Acquisition time | 0.4 | | | µs |
| $t_4$ | $\overline{CONVST}$ low to conversion started (BUSY high) | 10 | | 20 | ns |
| $t_5$ | End of conversion to BUSY low | 10 | | 20 | ns |
| $t_6$ | Pulse duration, $\overline{CONVST}$ low | 20 | | | ns |
| $t_8$ | $\overline{CS}$ low to $\overline{CONVST}$ low | 0 | | | ns |
| $t_9$ | Pulse duration, $\overline{CONVST}$ high | 20 | | | ns |
| | $\overline{CONVST}$ falling edge jitter | | | 10 | ps |
| $t_{10}$ | BUSY signal low | Min($t_{ACQ}$) | | 1 | µs |
| $t_{11}$ | BUSY signal high | | | 1.65 | µs |
| $t_{12}$ | First data bus data transition ($\overline{RD}$ low, $\overline{CS}$ low for read cycle, BYTE or BUS18/$\overline{16}$ input changes) after $\overline{CONVST}$ low | 40 | | | ns |
| $t_{13}$ | $\overline{CS}$ low to $\overline{RD}$ low | 0 | | | ns |
| $t_{14}$ | $\overline{RD}$ high to $\overline{CS}$ high | 0 | | | ns |
| $t_{15}$ | $\overline{RD}$ low time | 50 | | | ns |
| $t_{16}$ | $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid | | | 20 | ns |
| $t_{17}$ | Data hold from $\overline{RD}$ high | 5 | | | ns |
| $t_{18}$ | BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid | 10 | | 20 | ns |
| $t_{19}$ | $\overline{RD}$ high time | 20 | | | ns |
| $t_{20}$ | Last $\overline{RD}$ (or $\overline{CS}$ for read cycle ) rising edge to $\overline{CONVST}$ falling edge | 125 | | | ns |
| $t_{21}$ | BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge | Max($t_{26}$) | | | ns |
| $t_{22}$ | BYTE edge to BUS18/$\overline{16}$ edge skew | 0 | | | ns |
| $t_{23}$ | BYTE or BUS18/$\overline{16}$ rising edge to $\overline{RD}$ falling edge setup time | 10 | | | ns |
| $t_{24}$ | BYTE or BUS18/$\overline{16}$ falling edge to $\overline{RD}$ falling edge hold time | 10 | | | ns |
| $t_{25}$ | $\overline{RD}$ High ($\overline{CS}$ high for read cycle) to 3-stated data bus | | | 20 | ns |
| $t_{26}$ | BUSY low to MSB data valid delay time | | | 30 | ns |

NOTES: 1. All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
2. See timing diagrams.

PRODUCT PREVIEW

## TIMING CHARACTERISTICS

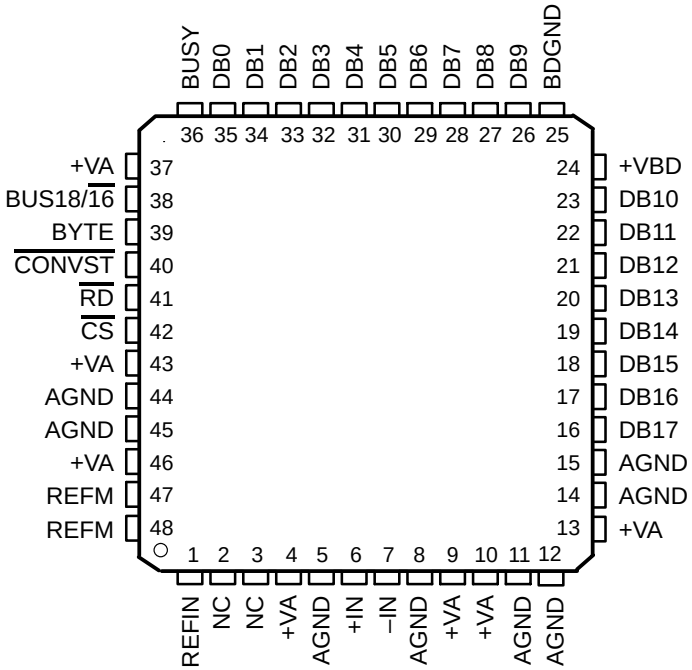
All specifications typical at –40°C to 85°C, +VA = 5 V, +VBD = 2.7 V (see Notes 1 and 2)

| | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CONV}$ | Conversion time | | | 1.6 | µs |
| $t_{ACQ}$ | Acquisition time | 0.4 | | | µs |
| $t_4$ | $\overline{CONVST}$ low to conversion started (BUSY high) | 10 | | 20 | ns |
| $t_5$ | End of conversion to BUSY low | 10 | | 20 | ns |
| $t_6$ | Pulse duration, $\overline{CONVST}$ low | 20 | | | ns |
| $t_8$ | $\overline{CS}$ low to $\overline{CONVST}$ low | 0 | | | ns |
| $t_9$ | Pulse duration, $\overline{CONVST}$ high | 20 | | | ns |
| | $\overline{CONVST}$ falling edge jitter | | | 10 | ps |
| $t_{10}$ | BUSY signal low | Min($t_{ACQ}$) | | 1 | µs |
| $t_{11}$ | BUSY signal high | | | 1.65 | µs |
| $t_{12}$ | First data bus transition ($\overline{RD}$ low, $\overline{CS}$ low for read cycle, BYTE or BUS 18/$\overline{16}$ input changes) after $\overline{CONVST}$ low | | | 40 | ns |
| $t_{13}$ | $\overline{CS}$ low to $\overline{RD}$ low | 0 | | | ns |
| $t_{14}$ | $\overline{RD}$ high to $\overline{CS}$ high | 0 | | | ns |
| $t_{15}$ | $\overline{RD}$ low time | 50 | | | ns |
| $t_{16}$ | $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid | | | 30 | ns |
| $t_{17}$ | Data hold from $\overline{RD}$ high | 10 | | | ns |
| $t_{18}$ | BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid | 10 | | 30 | ns |
| $t_{19}$ | $\overline{RD}$ high time | 20 | | | ns |
| $t_{20}$ | Last $\overline{RD}$ (or $\overline{CS}$ for read cycle ) rising edge to $\overline{CONVST}$ falling edge | 125 | | | ns |
| $t_{21}$ | BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge | Max($t_{26}$) | | | ns |
| $t_{22}$ | BYTE edge to BUS18/$\overline{16}$ edge skew | 0 | | | ns |
| $t_{23}$ | BYTE or BUS18/$\overline{16}$ rising edge to $\overline{RD}$ falling edge setup time | 10 | | | ns |
| $t_{24}$ | BYTE or BUS18/$\overline{16}$ falling edge to $\overline{RD}$ falling edge hold time | 10 | | | ns |
| $t_{25}$ | $\overline{RD}$ High ($\overline{CS}$ high for read cycle) to 3-stated data bus | | | 30 | ns |
| $t_{26}$ | BUSY low to MSB data valid delay time | | | 40 | ns |

NOTES: 1. All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
2. See timing diagrams.

## PIN ASSIGNMENTS

**PFB PACKAGE**
**(TOP VIEW)**




NC – No internal connection, not used in normal operation, do not connect.

PRODUCT PREVIEW

## TERMINAL FUNCTIONS

| NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 5, 8, 11, 12, 14, 15, 44, 45 | – | Analog ground |
| BDGND | 25 | – | Digital ground for bus interface digital supply |
| BUSY | 36 | O | Status output. High when a conversion is in progress. |
| BUS18/$\overline{16}$ | 38 | I | Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer.<br>0: Data bits output on the 18-bit data bus pins DB[17:0].<br>1: Last two data bits D[1:0] from 18-bit wide bus output on:<br>a) the low byte pins DB[9:2] if BYTE = 0<br>b) the high byte pins DB[17:10] if BYTE = 1 |
| BYTE | 39 | I | Byte select input. Used for 8-bit bus reading.<br>0: No fold back<br>1: Low byte D[9:2] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[17:10]. |
| $\overline{\text{CONVST}}$ | 40 | I | Convert start |
| $\overline{\text{CS}}$ | 42 | I | Chip select |

| Data Bus | | | 8-Bit Bus | | | 16-Bit Bus | | 18-Bit Bus |
|---|---|---|---|---|---|---|---|---|
| | | | BYTE = 0 | BYTE = 1 | BYTE = 1 | BYTE = 0 | BYTE = 0 | BYTE = 0 |
| | | | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 1 | BUS18/$\overline{16}$ = 0 | BUS18/$\overline{16}$ = 1 | BUS18/$\overline{16}$ = 0 |
| DB17 | 16 | O | D17 (MSB) | D9 | All ones | D17 (MSB) | All ones | D17 (MSB) |
| DB16 | 17 | O | D16 | D8 | All ones | D16 | All ones | D16 |
| DB15 | 18 | O | D15 | D7 | All ones | D15 | All ones | D15 |
| DB14 | 19 | O | D14 | D6 | All ones | D14 | All ones | D14 |
| DB13 | 20 | O | D13 | D5 | All ones | D13 | All ones | D13 |
| DB12 | 21 | O | D12 | D4 | All ones | D12 | All ones | D12 |
| DB11 | 22 | O | D11 | D3 | D1 | D11 | All ones | D11 |
| DB10 | 23 | O | D10 | D2 | D0(LSB) | D10 | All ones | D10 |
| DB9 | 26 | O | D9 | All ones | All ones | D9 | All ones | D9 |
| DB8 | 27 | O | D8 | All ones | All ones | D8 | All ones | D8 |
| DB7 | 28 | O | D7 | All ones | All ones | D7 | All ones | D7 |
| DB6 | 29 | O | D6 | All ones | All ones | D6 | All ones | D6 |
| DB5 | 30 | O | D5 | All ones | All ones | D5 | All ones | D5 |
| DB4 | 31 | O | D4 | All ones | All ones | D4 | All ones | D4 |
| DB3 | 32 | O | D3 | All ones | All ones | D3 | D1 | D3 |
| DB2 | 33 | O | D2 | All ones | All ones | D2 | D0 (LSB) | D2 |
| DB1 | 34 | O | D1 | All ones | All ones | D1 | All ones | D1 |
| DB0 | 35 | O | D0 (LSB) | All ones | All ones | D0 (LSB) | All ones | D0 (LSB) |

| | | | |
|---|---|---|---|
| –IN | 7 | I | Inverting input channel |
| +IN | 6 | I | Non inverting input channel |
| NC | 2, 3 | – | No connection |
| REFIN | 1 | I | Reference input. |
| REFM | 47, 48 | I | Reference ground. |
| $\overline{\text{RD}}$ | 41 | I | Synchronization pulse for the parallel output. |
| +VA | 4, 9, 10, 13, 37, 43, 46 | – | Analog power supplies, 5-V dc |
| +VBD | 24 | – | Digital power supply for bus |

## TIMING DIAGRAMS

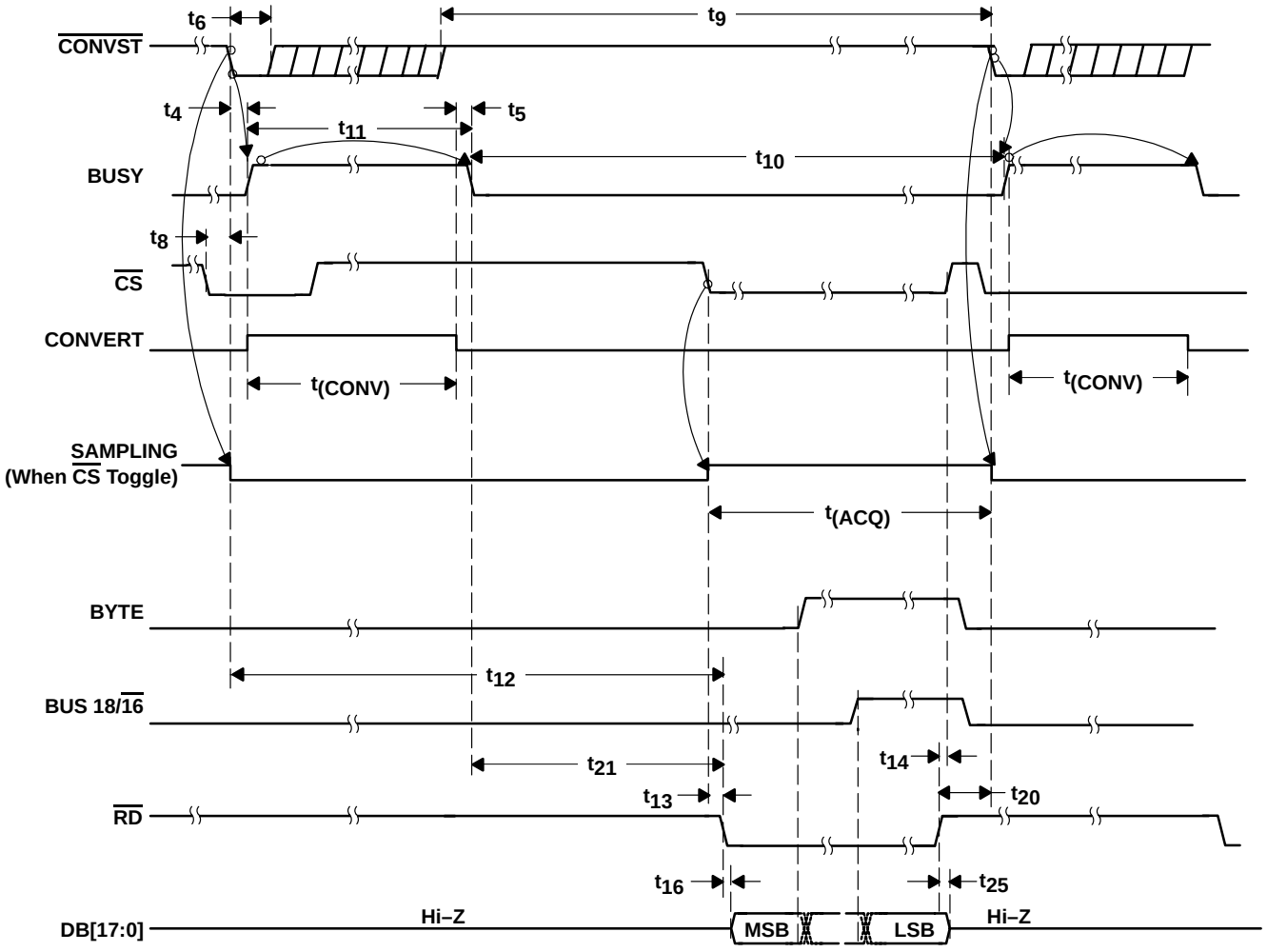
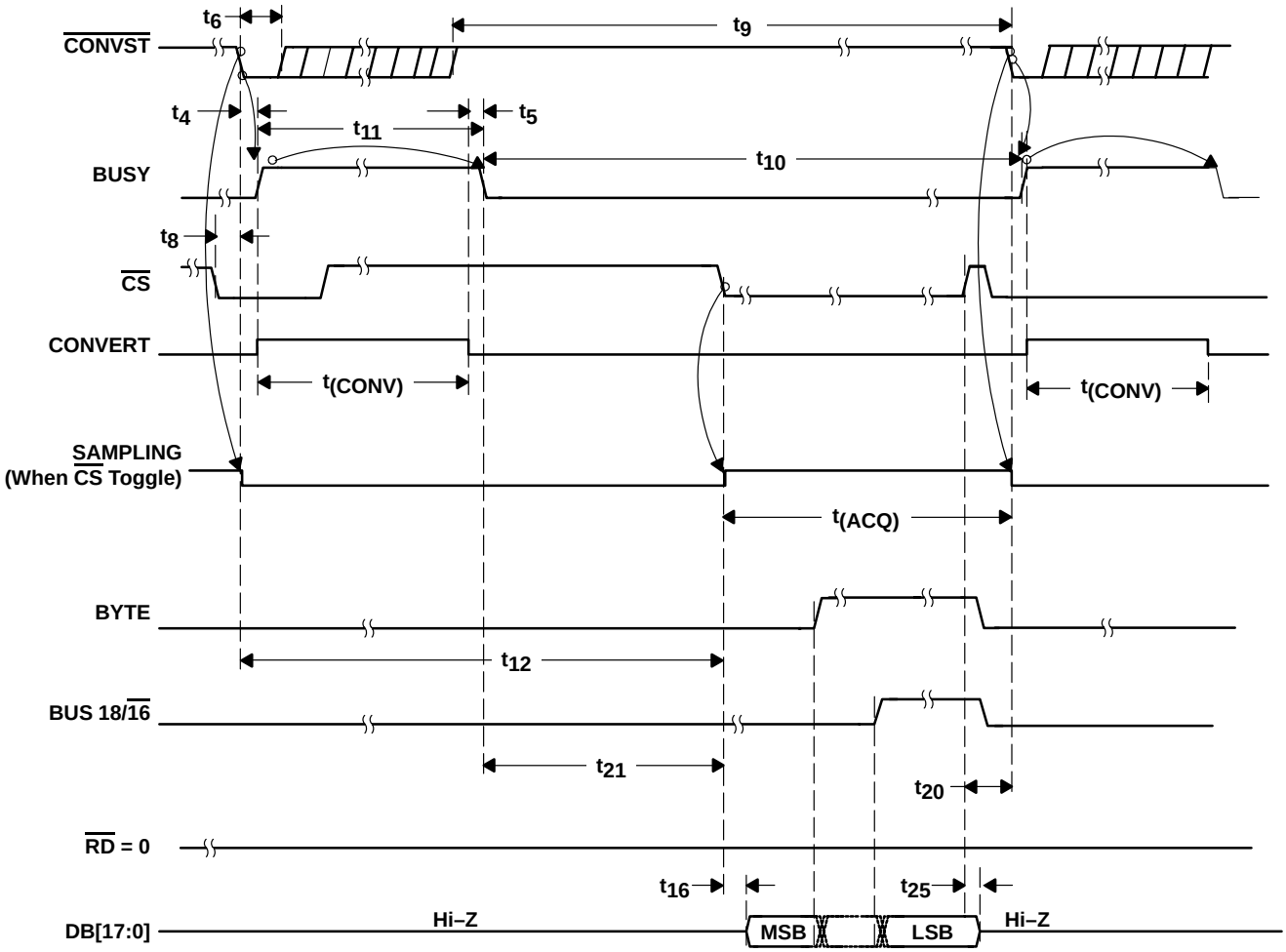



**Figure 1. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Toggling**

PRODUCT PREVIEW

## TIMING DIAGRAMS (CONTINUED)




NOTE: $\overline{RD}$ cannot be tied to BDGND. Three read cycles are required at power on.

**Figure 2. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Toggling, $\overline{RD}$ Hold Low**

## TIMING DIAGRAMS (CONTINUED)

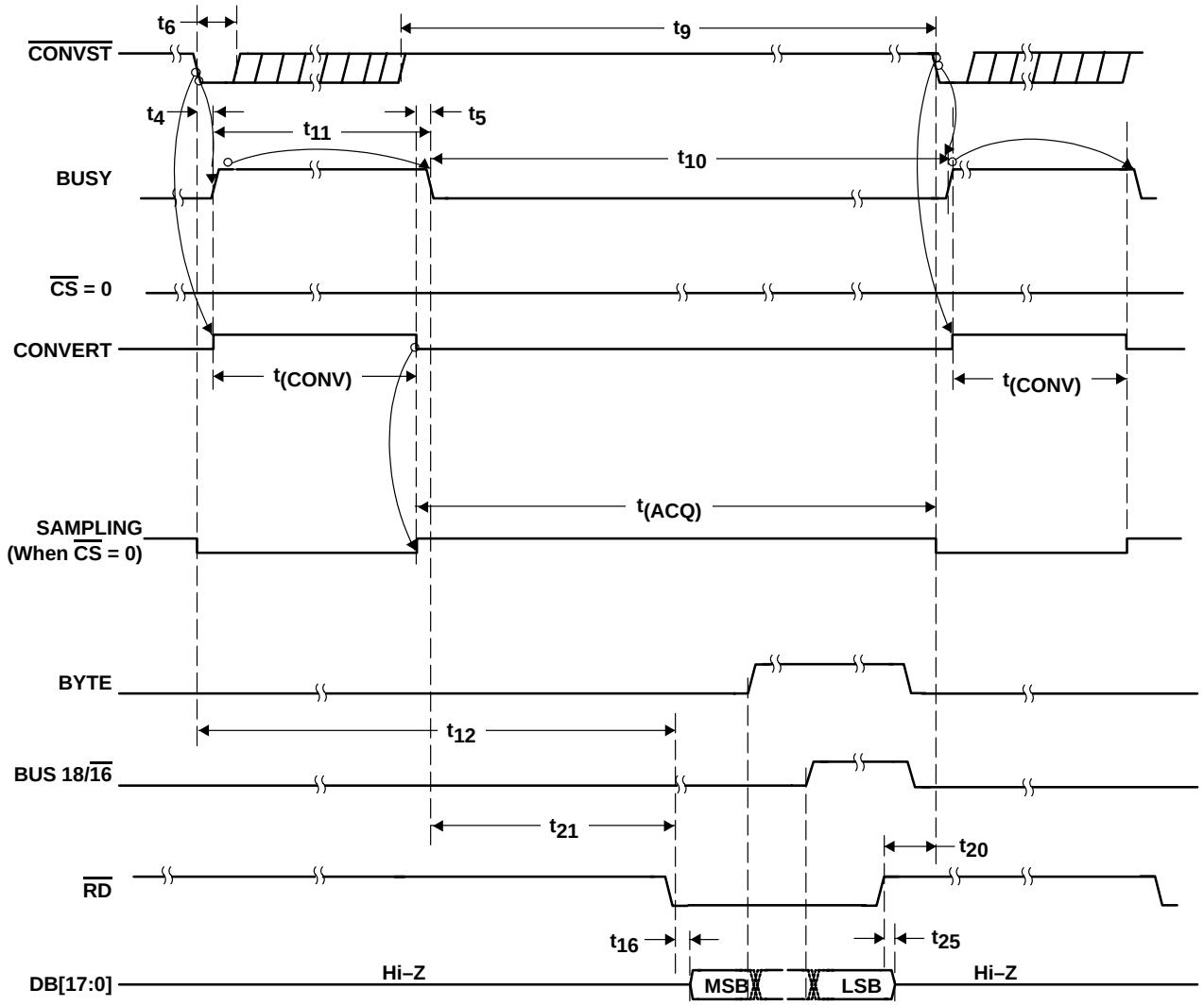
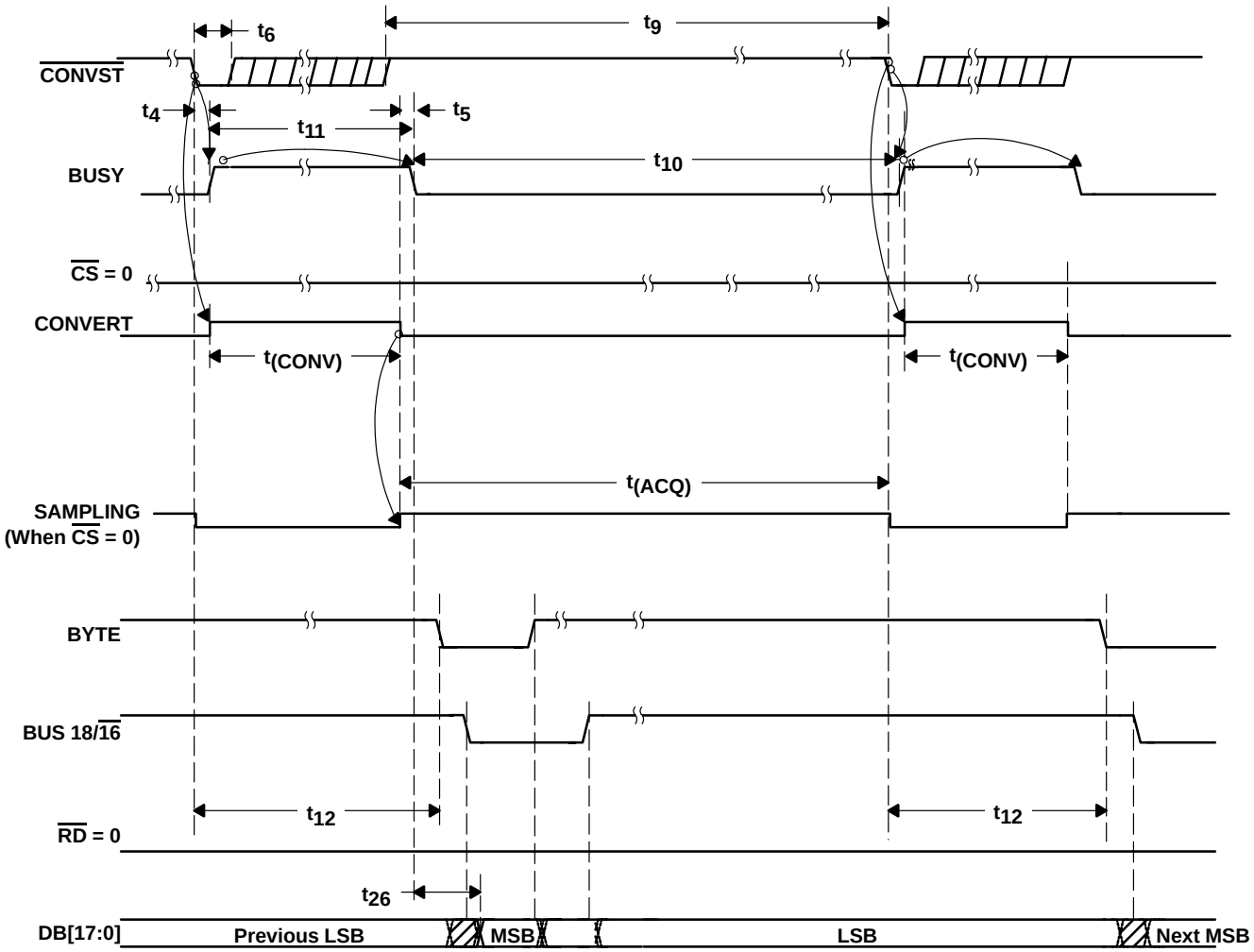



**Figure 3. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ Tied to BDGND, $\overline{RD}$ Toggling**

PRODUCT PREVIEW

## TIMING DIAGRAMS (CONTINUED)




NOTE: $\overline{RD}$ cannot be tied to BDGND. Three read cycles are required at power on.

**Figure 4. Timing for Conversion and Acquisition Cycles With $\overline{CS}$ and $\overline{RD}$ Hold Low - Auto Read**

## TIMING DIAGRAMS (CONTINUED)

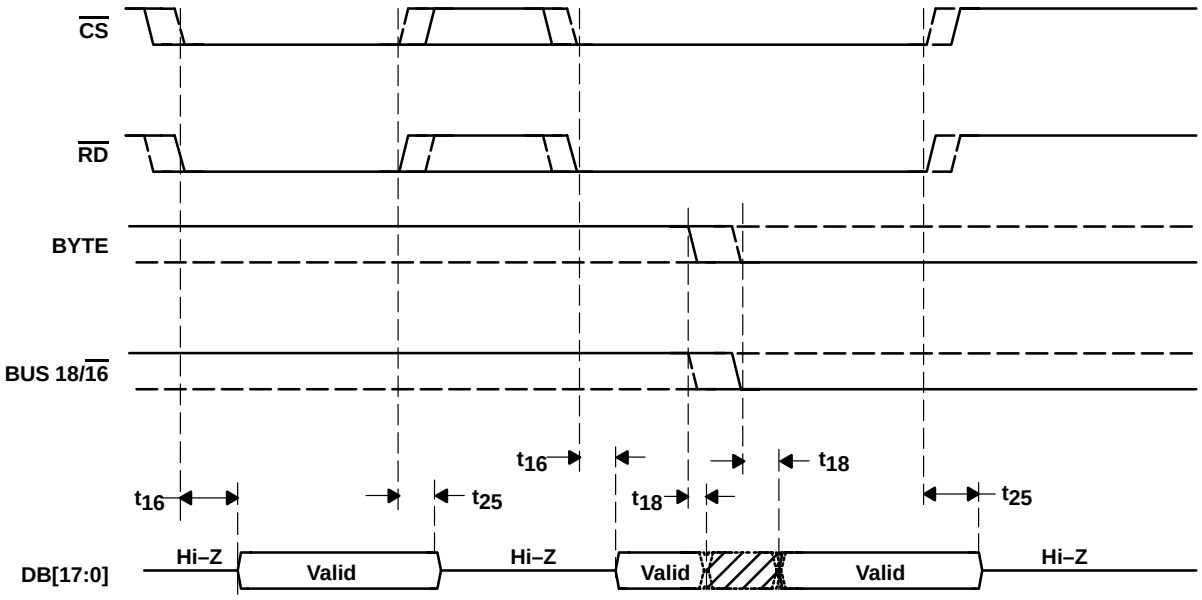



**Figure 5. Detailed Timing for Read Cycles**

## APPLICATION INFORMATION

### MICROPROCESSOR INTERFACING

#### ADS8381 to 8-Bit Microprocessor Interface

Figure 6 shows a parallel interface between the ADS8381 and a typical micro controller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microprocessor.

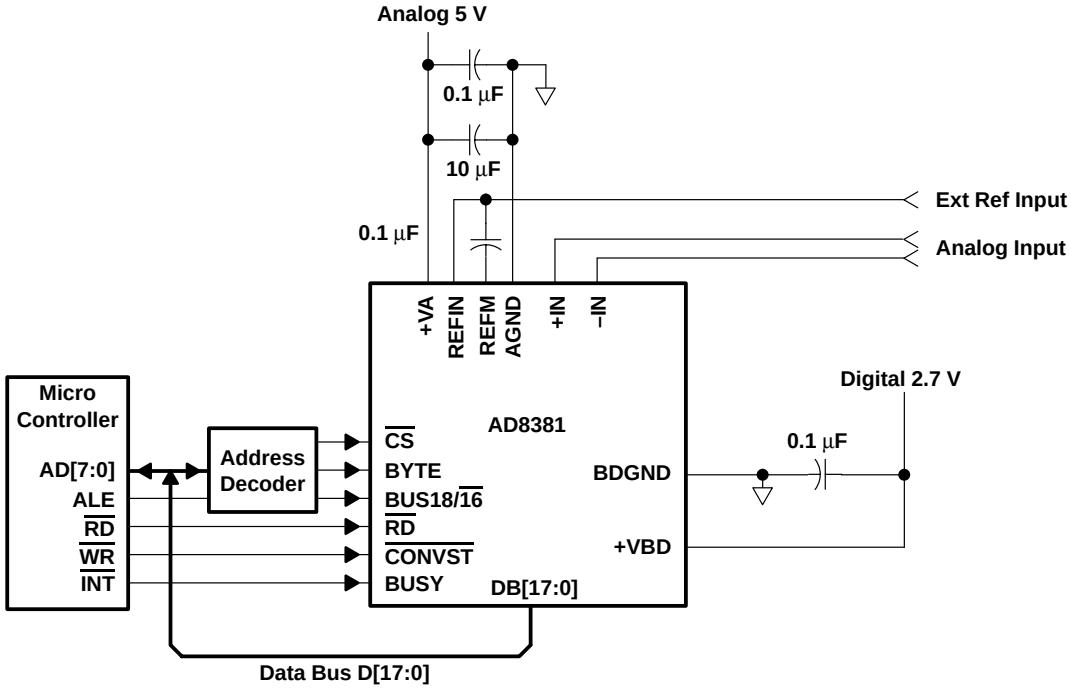



**Figure 6. ADS8381 Application Circuitry**

## PRINCIPLES OF OPERATION

The ADS8381 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 6 for the application circuit for the ADS8381.

The conversion clock is generated internally. The conversion time of 1.6 μs is capable of sustaining a 500-kHz throughput.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

### REFERENCE

The ADS8381 can operate with an external 4.096-V reference for a corresponding full-scale range of 4.096 V.

### ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2 V and 0.2 V, allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of –0.2 V to $+V_{ref}$ + 0.2 V. The input span (+IN – (–IN)) is limited to 0 V to $V_{ref}$.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8381 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to an 18-bit settling level within the acquisition time (400 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and –IN inputs and the span (+IN – (–IN)) should always remain within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

## PRINCIPLES OF OPERATION

### DIGITAL INTERFACE

#### Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8381 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high), while $\overline{\text{CS}}$ is low. The ADS8381 switches from the sample to the hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY output is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high through the conversion process and returns low when the conversion has ended.

Sampling starts with the falling edge of the BUSY signal when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought low in order to enable the parallel output bus with the conversion.

#### Reading Data

The ADS8381 outputs full parallel data in straight binary format as shown in Table 1. The parallel output is active when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{\text{CONVST}}$. This is 125 ns prior to the falling edge of $\overline{\text{CONVST}}$ and 40 ns after the falling edge. No data read should attempted within this zone. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ sets the parallel output to 3-state. BYTE and BUS18/$\overline{16}$ are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/$\overline{16}$ is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 1 for ideal output codes.

**Table 1. Ideal Input Voltages and Output Codes**

| DESCRIPTION | ANALOG VALUE | DIGITAL OUTPUT STRAIGHT BINARY | |
|---|---|---|---|
| FULL SCALE RANGE | $V_{REF}$ | | |
| Least significant bit (LSB) | $V_{REF}$/262144 | BINARY CODE | HEX CODE |
| Full scale | $V_{REF}$ – 1 LSB | 11 1111 1111 1111 1111 | 3FFFF |
| Midscale | $V_{REF}$/2 | 10 0000 0000 0000 0000 | 20000 |
| Midscale – 1 LSB | $V_{REF}$/2 – 1 LSB | 01 1111 1111 1111 1111 | 1FFFF |
| Zero | 0 V | 00 0000 0000 0000 0000 | 00000 |

The output data is a full 18-bit word (D17–D0) on DB17–DB0 (MSB–LSB) if both BUS18/$\overline{16}$ and BYTE are low.

The result may also be read on an 16-bit bus by using only pins DB17–DB2. In this case two reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 16 most significant bits (D17–D2) on pins DB17–DB2, then bringing BUS18/$\overline{16}$ high while holding BYTE low. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB3–DB2.

## PRINCIPLES OF OPERATION

### DIGITAL INTERFACE (CONTINUED)

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17–DB10. In this case three reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 8 most significant bits on pins DB17–DB10, then bringing BYTE high while holding BUS18/$\overline{16}$ low. When BYTE is high, the medium bits (D9–D2) appear on pins DB17–DB10. The last read is done by bringing BUS18/$\overline{16}$ high while holding BYTE high. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB11–DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active $\overline{RD}$ (toggling) or with $\overline{RD}$ held low for simplicity. This is referred to as the AUTO READ operation. Note that $\overline{RD}$ may not be tied to BDGND permanently due to the requirement of power-on initialization.

**Table 2. Conversion Data Read Out**

| BYTE | BUS18/$\overline{16}$ | DATA READ OUT | | | | |
|---|---|---|---|---|---|---|
| | | DB17–DB12 | DB11–DB10 | DB9–DB4 | DB3–DB2 | DB1–DB0 |
| High | High | All One's | D1–D0 | All One's | All One's | All One's |
| Low | High | All One's | All One's | All One's | DB1–DB0 | All One's |
| High | Low | D9–D4 | D3–D2 | All One's | All One's | All One's |
| Low | Low | D17–D12 | D11–D10 | D9–D4 | D3–D2 | D1–D0 |

### POWER ON

At first power on there are three read cycles (which do not produce valid conversion results) required. This is used to load factory trimming data for a specific device to assure high accuracy of the converter. Because of this requirement, the $\overline{RD}$ pin cannot be tied permanently to BDGND. System designers can still achieve the AUTO READ function if the power-on requirement is satisfied.

### LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8381 circuitry.

As the ADS8381 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8381 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-μF bypass capacitor is recommended from pin 1 directly to pin 48 (REFM).

## PRINCIPLES OF OPERATION

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

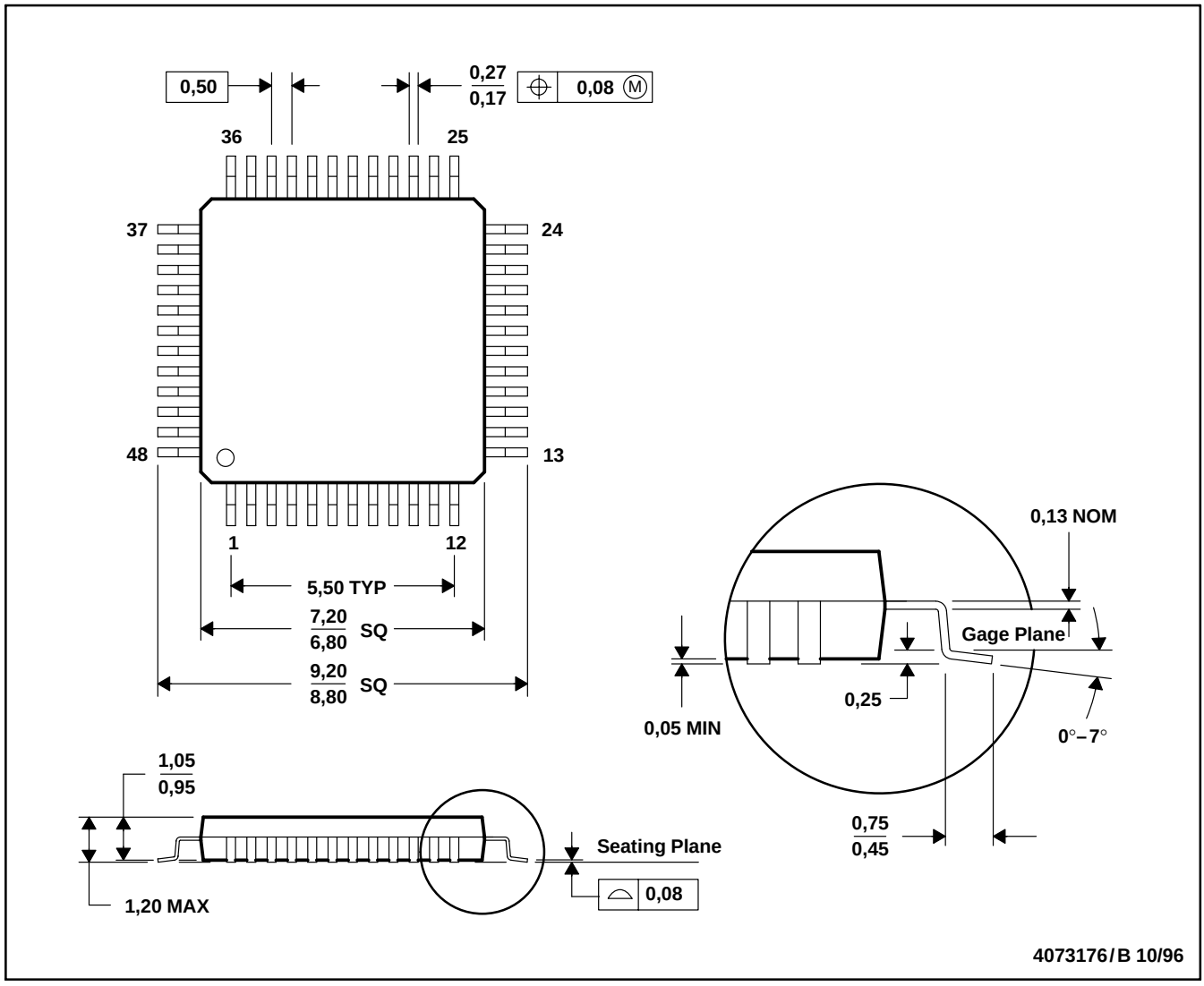
As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8381 should be clean and well bypassed. A 0.1-μF ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of the capacitor. In addition, a 1-μF to 10-μF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-μF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

**Table 3. Power Supply Decoupling Capacitor Placement**

| POWER SUPPLY PLANE<br>SUPPLY PINS | CONVERTER ANALOG SIDE | CONVERTER DIGITAL SIDE |
|---|---|---|
| Pin pairs that require shortest path to decoupling capacitors | (4,5), (8,9), (10,11), (13,15), (43,44), (45,46) | (24,25) |
| Pins that require no decoupling | 12, 14, 37 | |

## MECHANICAL DATA

**PFB (S-PQFP-G48)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PRODUCT PREVIEW

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265