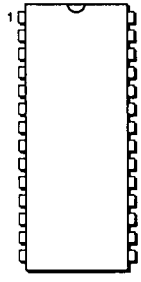
FEATURES

- ☐ Meets requirements of CCITT V.26, V.27, V.27bis/ter, V.29 and V.33
- ☐ Integrated call progress monitor and hybrid
- ☐ On-chip "Eye Dac"
- ☐ All transmit and receive filters on-chip including anti-aliasing and smoothing filters
- ☐ Serial I/O to DSP
- ☐ 16-step 1 dB/step transmit level adjust
- ☐ 128-step, 0.375 dB/step receiver programmable gain control
- ☐ Two code-controlled timing generators
- ☐ Analog and Digital loopback test diagnostics
- ☐ Available in DIP or PLCC package

GENERAL DESCRIPTION

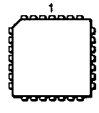
This Analog Front End (AFE) circuit can be used with a digital signal processing element to implement high speed modems operating in 4-wire full duplex or 2-wire half duplex modes. It meets the requirements of the CCITT V.26, V.27, V.27bis/ter, V.29 and V.33 recommendations.

28-PIN DIP PACKAGE



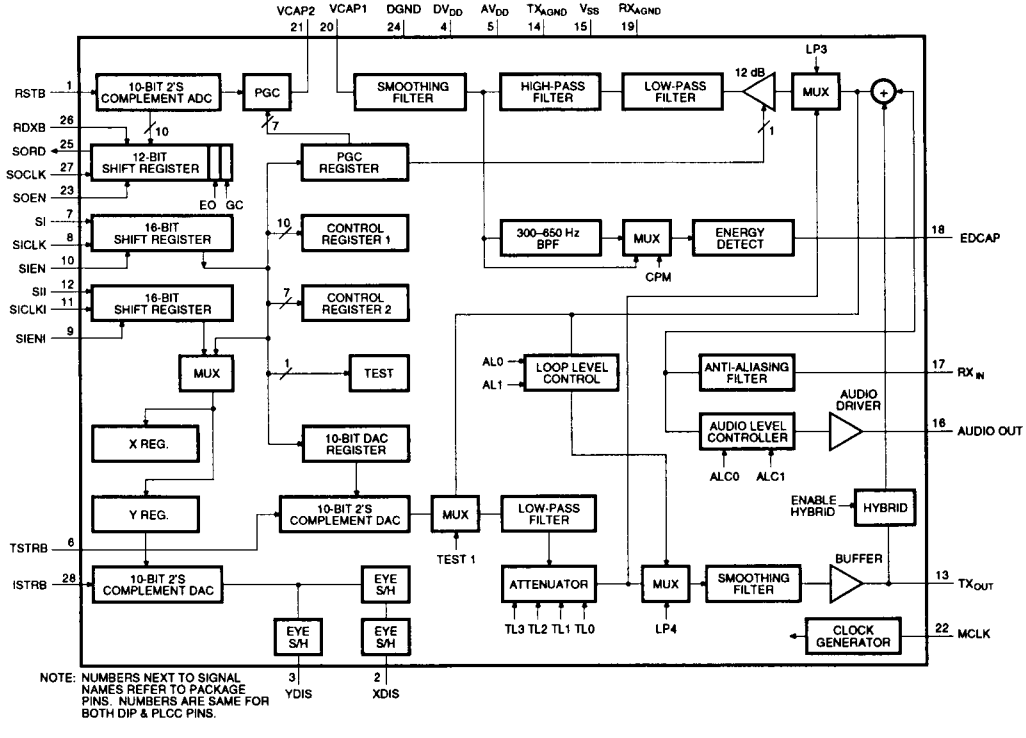
SC11033CN

28-PIN PLCC PACKAGE



SC11033CV

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE SAME FOR BOTH DIP & PLCC PINS.

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	RSTRB	Receive strove whose rising edge triggers the A/D conversion. The outputs of A/D are latched into the serial output shift register on following rising edge. RSTRB is 9.6 kHz.
2	XDIS	10 bits D/A output from Eye-X register.
3	YDIS	10 bits D/A output from Eye-Y register. Both X and Y data words are transferred in one ISTRB cycle (see Figure 7 for timing details) and they are ready to display simultaneously at XDIS and YDIS two cycles later.
4	DV_{DD}	Digital positive power supply pin. DV_{DD}= +5 V ±5 %
5	AV_{DD}	Analog positive power supply pin. AV_{DD}= +5 V ±5 %
6	TSTRB	Transmit strobe whose rising edge triggers the 10 bits D/A conversion. Transmit data word (or 2 transmit data words if they are used to load Eye-X and Eye-Y registers) is transferred in one TSTRB cycle (see Figure 5 for timing details) and D/A output is available two cycles later. TSTRB is 9.6 kHz.
7	SI	Serial digital input. It is shifted serially into a 16-bit register. The three most significant bits (D15–D13) destinate the contents of 10 least significant bits (D9–D0) into data/control register . (See Figure 5 for timing details.)
8	SICLK	Serial input clock (2.0 MHz max.). It is used to shift data into a 16-bit register. (See Figure 5 for timing details.)
9	SIENI	Eye-port serial input enable. It enables the writing of data into a 16-bit Eye-register. (See Figure 5 for timing details.)
10	SIEN	Serial input enable. It enables the writing of data into a 16-bit register.. (See Figure 5 for timing details.)
11	SICLKI	Eye-Port serial input clock. It is used to shift data into a 16-bit Eye-register. (See Figure 5 for timing details.)
12	SII	Eye-Port serial digital input. It is shifted serially into a 16-bit register. Bit 12 (E11) and bit 11 (E10) destinate the contents of 10 least significant bits (E9–E0) into either Eye-X register or Eye-Y register.
13	TX_{OUT}	Analog transmit signal.
14	TX_{AGND}	Analog ground for transmit section TX_{AGND} = 0 V
15	V_{SS}	Negative power supply pin V_{SS} = –5 V ±5 %
16	$AUDIO_{OUT}$	Audio monitor. The analog receive signal is passed through a level controller and a buffer to drive a speaker for line audio monitoring.
17	RX_{IN}	Analog receive signal.
18	EDCAP	Energy detect capacitor. The output is a DC level which indicates the amount of energy received within the pass band (300 Hz–3.4 kHz or 300 Hz– 650 Hz in CPM mode). The output needs one external capacitor which together with the internal 25 kΩ resistor forms a low-pass filter with $f_{-3dB} = \frac{1}{2\pi(25{,}000)\ C_{ex}}$
19	RX_{AGND}	Analog ground for receive section RX_{AGND}= 0 V
20, 21	VCAP1, VCAP2	An external capacitor is required between these two pins. These capacitor together with the internal 25 kΩ resistor provides AC coupled between the output of receive filter (VCAP1) and input of PGC (VCAP2). The –3 dB frequency for the high pass filter is given by $f_{-3dB} = \frac{1}{2\pi(25{,}000)\ C_{ext}}$

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
22	MCLK	Master clock. Must be 2.4576 MHz. This is the main clock which is used to derive various clocks for filters, A/D and D/A.
23	SOEN	Serial output enable. It enables the data stored at output shift register to be shifted out. (See Figure 6 for timing details.)
24	DGND	Digital ground DGND = 0 V
25	SO_{RD}	Serial output data. The first 10 bits corresponds to the ADC receive data. Bit 11 (ED) is energy detect output and bit 12 (GC) is gain change acknowledge flag. (See Figure 6 for timing details.)
26	RD_{XB}	Open drain output which goes low during serial out. (See Figure 6 for timing details.)
27	SOCLK	Serial output clock. It is used to shift data out of output shift register. (See Figure 6 for timing details.)
28	ISTRB	Eye strobe whose rising edge triggers the 10 bits D/A conversion. Both X and Y data words are transferred in one ISTRB cycle and they are ready to display simultaneously at XDIS and YDIS pins two cycles later. (See Figure 7 for timing details.)

FUNCTIONAL DESCRIPTION (Refer to Block Diagram)

Transmit Section

The transmit signal is generated in 10-bit two's compliment format by an external processor and is shifted serially into a 16-bit control/data register. The contents of this shift register is converted to analog and passed through a switched-capacitor low-pass filter, an attenuator, a smoothing filter and a buffer to drive a 600 Ω load. The transmit filter has a 6th order transfer function. Figure 2a shows the overall amplitude response, Figure 2b shows the details of the transition region and Figure 2c shows the passband detail and the group delay response. As seen in Figure 2c the passband response of the transmit filter has an x/sin(x) shape and it compensates for the loss distortion due to 9.6 kHz sample-and-hold effect. The 16-step, 1 dB/step attenuator can be programmed to adjust the output signal level.

TRANSMIT LOW-PASS FILTER CHARACTERISTICS

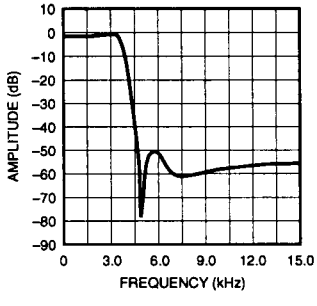


Figure 2a. Overall Response

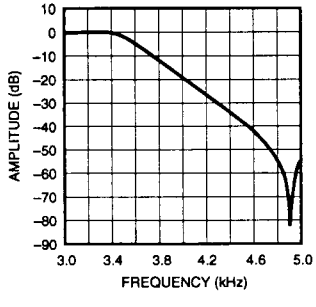


Figure 2b. Passband Detail

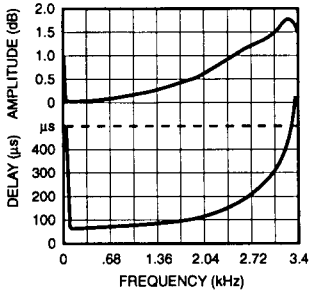


Figure 2c. Passband Amplitude and Group Delay Detail

Receive Section

On the receive side, the signal received from the line is passed through an antialiasing filter and a receive filter section. The receive filter section has 6th order low-pass, and 3rd order high-pass characteristics. The amplitude response of the filter is shown in Figure 3a. Figures 3b and 3c show the details of the upper and lower transition regions and Figure 3d shows the details of the passband amplitude and group-delay response.

The output of the smoothing filter is fed to a Programmable Gain Control stage (PGC) through an external capacitor for dc removal. The PGC can be programmed externally in 128 steps, 0.375 dB/step through a 7-bit control signal. To improve the signal to noise ratio under weak signal conditions a 12 dB front-end gain is enabled.

The output of the PGC is converted to digital 2's complement digital code by a 10-bit A/D converter (ADC). The ADC output can be read together with two other status bits by the external processor.

Test

An Eye DAC is provided to display the real and imaginary parts of any complex signal (i.e. eye patterns, signal constellations, etc.) at a sampling rate up to 14.4 kHz.

The 10-bit I and Q data are sent to the AFE through the 16-bit serial Tx-port under program control or through an independent 16-bit serial Eye-port with its separate enable and clock signals. Typically both data words are transferred in a bit cycle and they are ready to display simultaneously at XDIS and YDIS pins two cycles later. There are multiple sources of strobe for this DAC allowing it to be synchronized to Tx, Rx or be independently synchronized. The control word selects the DAC strobe from TxSTRB, RxSTRB and EyeSTRB.

If only one data word is sent per cycle the output will be available at XDIS pin and YDIS and will remain unchanged.

Call Progress Tone Monitor

The receive analog signal is passed through a bandpass filter with band edges at 300 and 650 Hz. The amplitude response of the call progress filter is shown in Figure 4. An energy detect circuit follows this filter. The energy detect needs one external capacitor. The detect level is selectable between two distinct levels. In the mode of operation where call progress is not selected (CPM = 0), the band-pass filter is removed from the signal path, and the energy detect monitors the signals that fall within the frequency band of the receive filter.

RECEIVE LOW-PASS AND HIGH-PASS FILTER CHARACTERISTICS

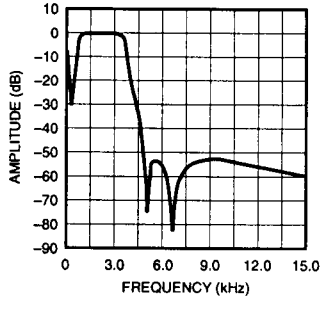


Figure 3a.

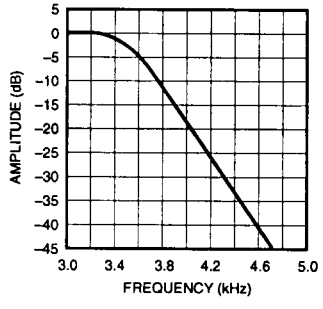


Figure 3b.

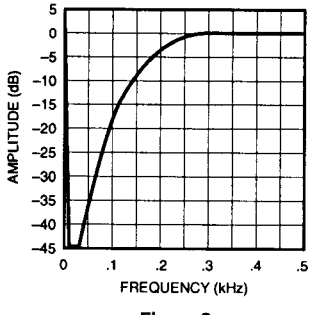


Figure 3c.

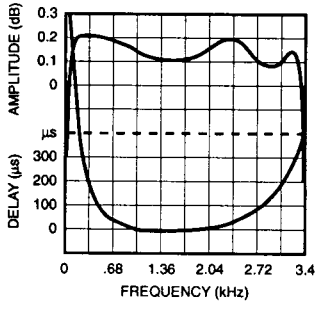


Figure 3d.

Audio Monitor

The analog receive signal is passed through a level controller and a buffer to drive a speaker for line audio monitoring.

This circuit is used during call progress detection to monitor call progress tones. The audio signal level can be controlled by ALC1 and ALC0 bits.

Serial I/O

The serial I/O is designed to be compatible with DSP chips such as TMS 320-series and matches standard codec interfaces.

Serial Input

Sixteen bits of control/data are shifted into the AFE using 16 periods of SICLK. The data on SI pin must be valid on the falling edge of the SICLK. The timing is shown in Figure 5a. A typical serial input example that illustrates the required relationship between SIEN and TSTRR is shown in Figure 5b.

After SIEN goes from Low to High, the data on SI pin is shifted into a 16-bit register on the falling edge of the SICLK.

MSB should be sent first. After the 16th bit (LSB) is received, no further bits are shifted in until SIEN has another Low to High transition.

The most significant 3 bits (D15–D13) are used for addressing as follows:

D15–D13	SOURCE AND DESTINATION
0	10 LSB's (D9–D0) Loaded into TX register
1	10 LSB's (D9–D0) Loaded into EYE-X register
2	10 LSB's (D9–D0) Loaded into EYE-Y register
3	10 LSB's (D9–D0) Loaded into CTRL-1 register
4	6 LSB's (D5–D0) Loaded into CTRL-2 register
5	8 LSB's (D7–D0) Loaded into PGC register
6	1 LSB (D0) Loaded into TEST register

CALL PROGRESS FILTER CHARACTERISTICS

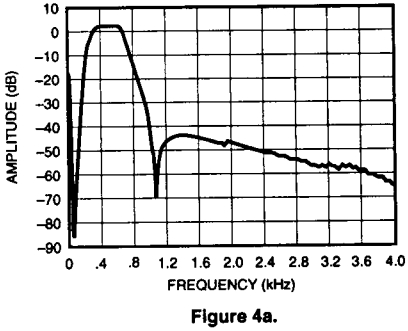


Figure 4a.

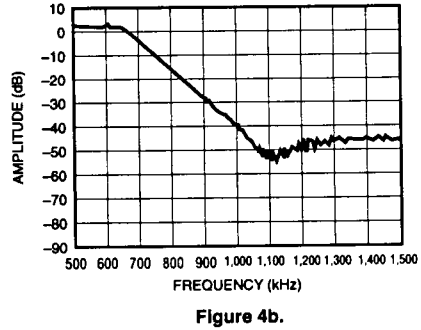


Figure 4b.

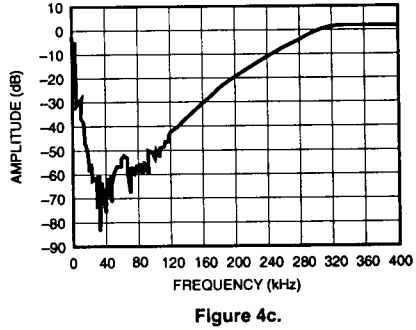


Figure 4c.

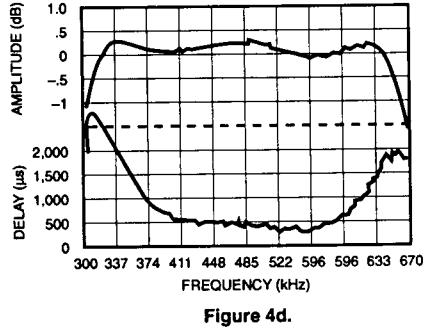


Figure 4d.

Serial Output

Twelve bits of data are shifted out of the AFE serial output (SO) pin using 12 periods of SOCLK. Transmission begins with an SOEN pulse as shown in Figure 6a. The data bits are valid on the falling edge of the SOCLK. The first output bit will be the MSB.

The first 10 bits of the data correspond to the ADC receive data. Bit 11 (ED) is energy detect output and bit 12 (GC) is gain change acknowledge flag. The gain change latch is reset whenever a new value of gain is loaded into the PGC register, and it becomes set when the gain change is taken into effect. A typical example of a serial output and the relationship between RSTRB and SOEN is shown in Figure 6b.

Eye Serial Port

A separate serial port is connected to the Eye pattern generator for sending 10-bit samples to the EYE DAC. The interface is identical to the transmit serial port. Sixteen bits are shifted in for each SIENI transition from low to high. The 10 MSB's of this shift register are transferred to the X and Y registers as selected by the bits E11 and E10 according to the table below.

The X and Y registers can also be loaded by the SI interface. In this case the contents of the Eye serial port will be ignored. The Eye-port serial timing and the relationship between ISTRB and SIENI is shown in Figure 7.

E11	E10	SOURCE AND DESTINATION
0	1	10 LSB's (D9–D0) Load into X register
1	0	10 LSB's (D9–D0) Load into Y register

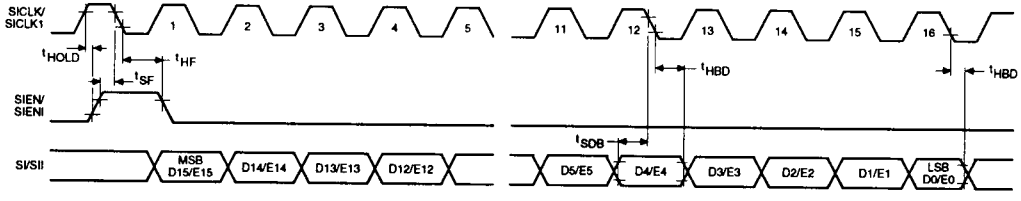


Figure 5a. Serial Input Timing

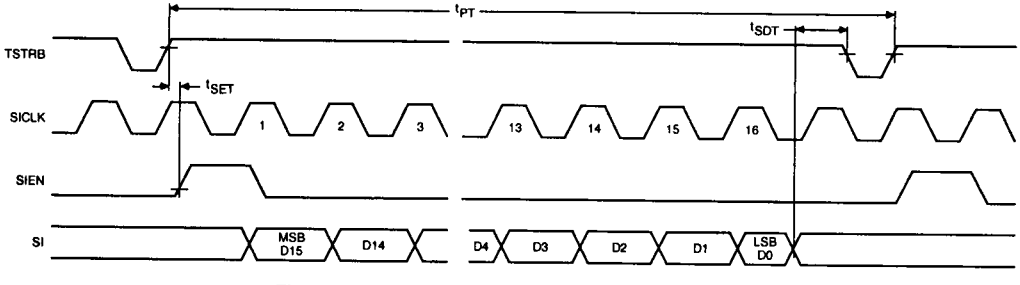


Figure 5b. Serial Input Timing with Respect to TSTRB

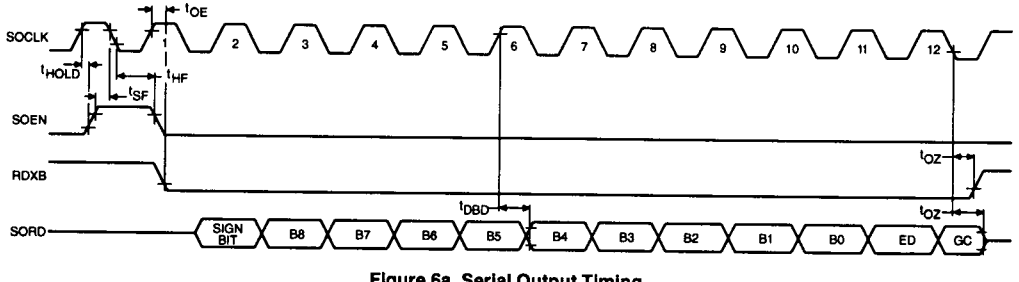


Figure 6a. Serial Output Timing

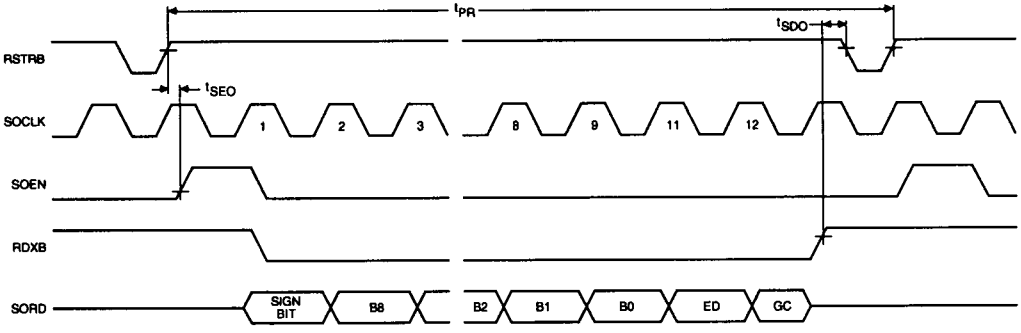


Figure 6b. Serial Output Timing with Respect to RSTRB

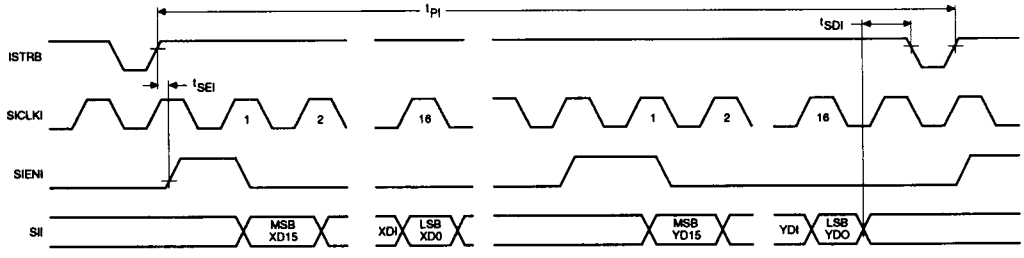


Figure 7. Eye-Port Serial Input Timing with Respect to ISTRB

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HOLD}	Holding time from Serial Clock high to Enable High	0			ns
t_{SF}	Set up time from Enable high to Serial Clock low	50			ns
t_{HF}	Hold time from Serial Clock low to Enable low	100			ns
t_{DBD}	Delay time from SOCLK high to data valid	0		180	ns
t_{OE}	Delay time to RDXB low			140	ns
t_{OZ}	Delay time from SOCLK low to data output disabled	50		165	ns
t_{SDB}	Set up time from SI/SII valid to SICLK/SICLKI low	50			ns
t_{HBD}	Hold time from SICLK/SICLKI low to SI/SII invalid	50			ns
t_{SEO}	Set up time from RSTRB high to SOEN high	0			ns
t_{SDO}	Hold time from RDXB high to RSTRB low	0			ns
t_{SET}	Set up time from TSTRB high to SIEN high	0			ns
t_{SDT}	Hold time from last input data to TSTRB low	0			ns
t_{SEI}	Set up time from ISTRB high to SIENI high	0			ns
t_{SDI}	Hold time from last input to ISTRB low	0			ns
$1/t_{PR}$ $1/t_{PT}$ $1/t_{PI}$	Frequency of receive strobe Frequency of transmit strobe Frequency of eye strobe		9–6 9–6 9–6		kHz kHz kHz

CONTROL REGISTERS

Control Register 1

Bit #	Function	
0 (LSB)	ALC0	Audio level control
1	ALC1	
2	AL0	Loop 4 gain control
3	AL1	
4	LP4	When set Loop 4 active
5	LP3	When set Loop 3 active
6	TL0	Transmit level control
7	TL1	
8	TL2	
9	TL3	

Code Definition

ALC1	ALC0	Audio Out
0	0	Off
0	1	12 dB loss
1	0	6 dB loss
1	1	0 dB

AL1	AL0	Loop Gain
1	1	–6 dB
0	0	0
0	1	+6 dB
1	0	+15 dB

LP3	LP4	Loop
0	0	Normal
1	0	Loop 3
0	1	Loop 4
1	1	Normal

TL3	TL2	TL1	TL0	Loss (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Control Register 2

Bit #	Function	
0 (LSB)	HBRD	Hybrid enable
1	EDLVL	Energy detect level control
2	CPM	Call progress mode selected
3	EYEC1	EYE DAC strobe select
4	EYEC2	
5	EYE DIS	Enables/disables EYE/DAC
6	SI/SIEB	Selects source for the X and Y registers of EYE DAC as SI or SIE

Code Definition

HBRD	Hybrid
1	Activated
0	Deactivated

EDLVL	Energy Detect
0	–43 dBm
1	–50 dBm

EYEC1	EYEC2	EYE DAC Strobe
0	0	EYESTRB
0	1	TXSTRB
1	0	RXSTRB
1	1	EYESTRB

EYE DIS	EYE DAC
1	Enabled
0	Disabled

SI/SIEB	EYE DAC Source
1	From SI interface
0	From SIE interface

PGC REGISTER

G6	G5	G4	G3	G2	G1	G0	Gain
0	0	0	0	0	0	0	0 dB
1	0	0	0	0	0	0	24 dB
0	1	0	0	0	0	0	12 dB
0	0	1	0	0	0	0	6 dB
0	0	0	1	0	0	0	3 dB
0	0	0	0	1	0	0	1.5 dB
0	0	0	0	0	1	0	0.75 dB
0	0	0	0	0	0	1	0.375 dB

G7	
1	RX low-pass has 12 dB gain
0	RX low-pass has 0 dB gain (default)

TEST REGISTER

There is one bit used for factory test and should be cleared in normal operation.

SPECIFICATIONS

Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{DD}+0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{DD}+0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 s)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	° C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
MCLK	Clock Frequency	CLKSEL = 0	2.4573	2.4576	2.4579	MHz
T_R, T_F	Input Rise or Fall Time	All Digital Inputs Except CLKIN			50	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			50	ns

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current			18	35	mA
I_{SS}	Quiescent Current			18	35	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V V_{SS}	±3			V

AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	PSRR (V_{DD}) @ 1 kHz PSRR (V_{SS}) @ 1 kHz	Transmit Path		–30 –35		dB dB
	PSRR (V_{DD}) @ 1 kHz PSRR (V_{SS}) @ 1 kHz	Receive Path		–40 –30		dB dB
	Idle Channel Noise	Both Transmit and Receive Filters		10		dBrnCo
	Total Harmonic Distortion for Receive Filter	Rx_{IN} = 3 V_{PP} @ f = 1000 Hz		–70		dB
	Total Harmonic Distortion for Transmit Filter	Tx_{OUT} = 3 V_{PP} @ f = 1000 Hz		–65		dB
	Channel-to Channel Separation (Crosstalk)			–70		dB

Notes: 4. Does not apply to CKOUT.
5. Min and max values are valid over the full temperature and operating voltage range. Typical values are from 25° C and ±5 V operation.