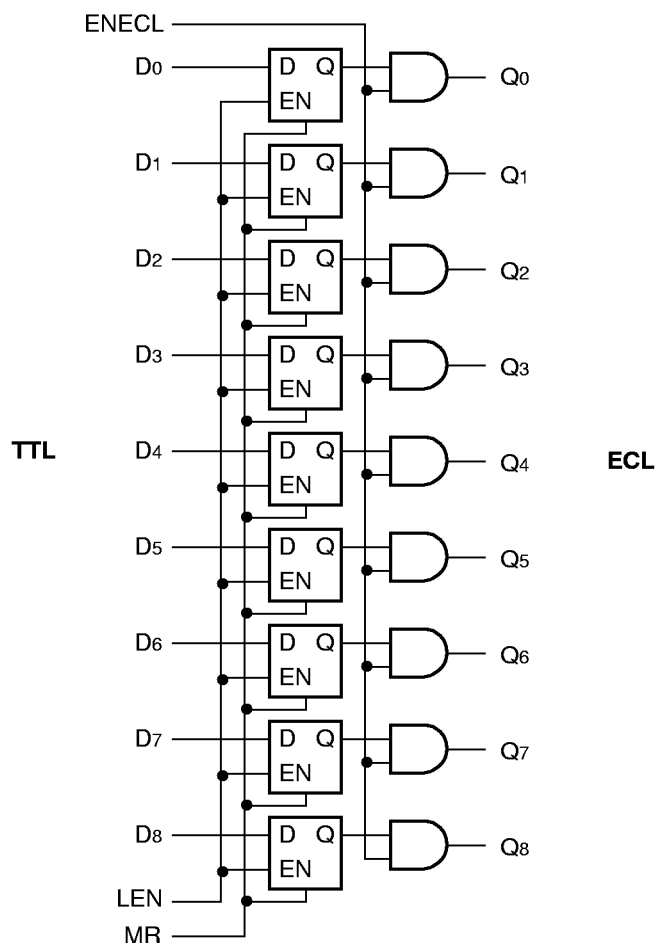


FEATURES

- 9-bit ideal for byte-parity applications
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- Dual supply
- 3.5ns max. D to Q
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- ESD protection of 2000V
- Fully compatible with Motorola MC10H/100H602
- Available in 28-pin PLCC package

BLOCK DIAGRAM



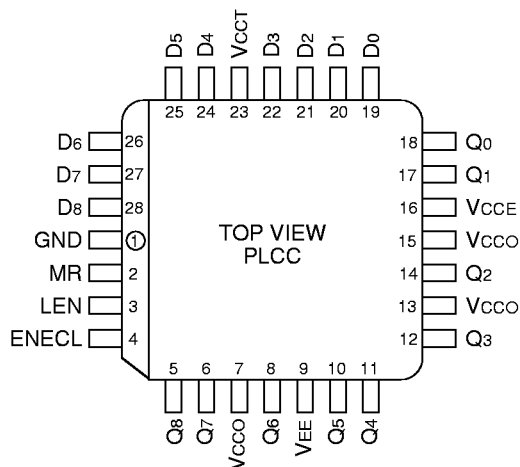
DESCRIPTION

The SY10/100H602 are 9-bit, dual supply TTL-to-ECL translators with latches. Devices in the Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
VcCe	ECL Vcc (0V)
VcCo	ECL Vcc (0V) — Outputs
Vcct	TTL Supply (+5.0V)
VEE	ECL Supply (-5.2/-4.5V)
D0-D8	Data Inputs (TTL)
Q0-Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q ₀
X	X	H	H	L
X	X	X	L	L

DC ELECTRICAL CHARACTERISTICS
 $V_{CC} = 5.0V \pm 10\%$; $V_{EE} = -4.75V$ to $-5.5V$ (10H Version); $V_{EE} = -4.2V$ to $-5.5V$ (100H Version)

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{EE}	Power Supply Current, ECL 10H 100H	—	125	—	125	—	125	mA	—
		—	122	—	123	—	132		
I _{CCH} I _{CCL}	Power Supply Current, TTL	—	48	—	48	—	48	mA	—
		—	50	—	50	—	50		

AC ELECTRICAL CHARACTERISTICS
 $V_{CC} = 5.0V \pm 10\%$; $V_{EE} = -4.75V$ to $-5.5V$ (10H Version); $V_{EE} = -4.2V$ to $-5.5V$ (100H Version)

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition		
		Min.	Max.	Min.	Max.	Min.	Max.				
t _{PLH} t _{PHL}	Propagation Delay to Output D LEN MR ENECL	1.4 2.0 2.0 1.6	3.0 3.4 3.4 3.2	1.5 2.1 2.1 1.7	3.2 3.5 3.5 3.3	1.7 2.4 2.5 1.8	3.5 3.7 3.9 3.7	ns	—		
t _s	Set-up Time, D to LEN	2.0	—	2.0	—	2.0	—			ns	—
t _H	Hold Time, D to LEN	1.0	—	1.0	—	1.0	—			ns	—
t _{w(L)}	LEN Pulse Width, LOW	2.0	—	2.0	—	2.0	—			ns	—
t _r t _f	Output Rise/Fall Time 20% to 80%, 80% to 20%	0.5	1.5	0.5	1.5	0.5	1.5	ns	—		

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H602JC	J28-1	Commercial
SY10H602JCTR	J28-1	Commercial
SY100H602JC	J28-1	Commercial
SY100H602JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

FILE/REV #: PD0008A03

PD/0008/ASCORP

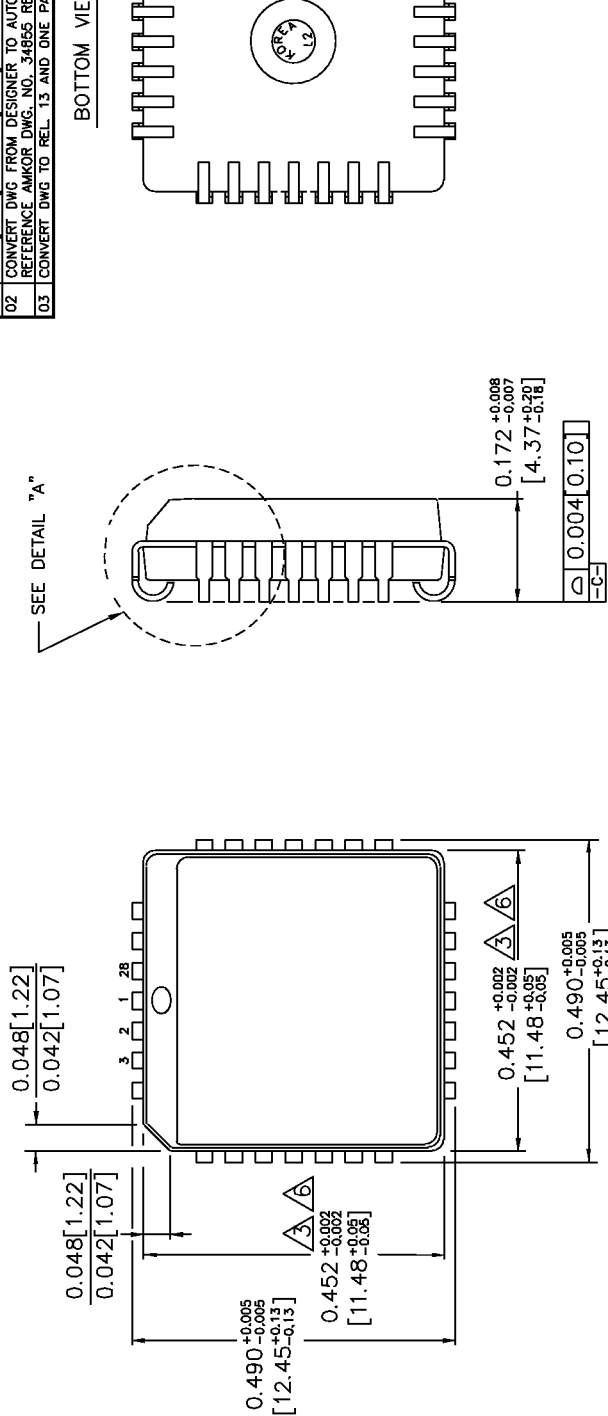
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450 [1.43] TO 0.443 [1.25]. TYPOGRAPHICAL ERROR.	06/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

TOP VIEW

SIDE VIEW

BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

SYNERGY
SEMICONDUCTOR

APPROVALS	DATE	APPROVALS	DATE	SIZE
ORIGINATOR: TERRIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO		
RELEASE DATE:				

28 LEAD PLCC
PACKAGE OUTLINE

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SCALE: N/A
REVISION: 03

