Integrated Device Technology, Inc.

256KB AND 512KB SECONDARY CACHE MODULES FOR THE INTEL PENTIUM™ CPU AND OPTi™ VIPER CORE LOGIC CHIPSET

PRELIMINARY
IDT7MPV6214
IDT7MPV6215
IDT7MPV6216
IDT7MPV6217

FEATURES

- For Intel 3.3V Pentium-based systems using the OPTi Viper core logic chipset
- Asynchronous and pipelined burst SRAM options in the same module pinout
- Low-cost, low-profile card edge module with 160 leads
- Uses Burndy Computerbus™ connector, part number CELP2X80SC3Z48
- Operates with Pentium CPU external bus speeds up to 66MHz
- Separate 5V (±5%) and 3.3V (±10%) power supplies
- Multiple GND pins and decoupling capacitors for maximum noise immunity

DESCRIPTION

The IDT7MPV6214/15/16/17 modules belong to a family of secondary caches intended for use with systems based on the Intel 3.3V Pentium CPU and the OPTi Viper core logic chipset. The IDT7MPV6214/15 use IDT's 71V256 32K x 8 static RAMs and FCT logic, and the IDT7MPV6216/17 use IDT's 71V432 32K x 32 pipelined synchronous burst static RAMs in plastic surface-mount packages mounted on a multilayer epoxy laminate (FR-4) board. In addition, each of the modules uses 5V SRAMs for the tag field and dirty bit. Extremely high speeds are achieved using IDT's high-reliability, low-cost CMOS technology. The specification for the IDT7MPV6216/17 is advance information only.

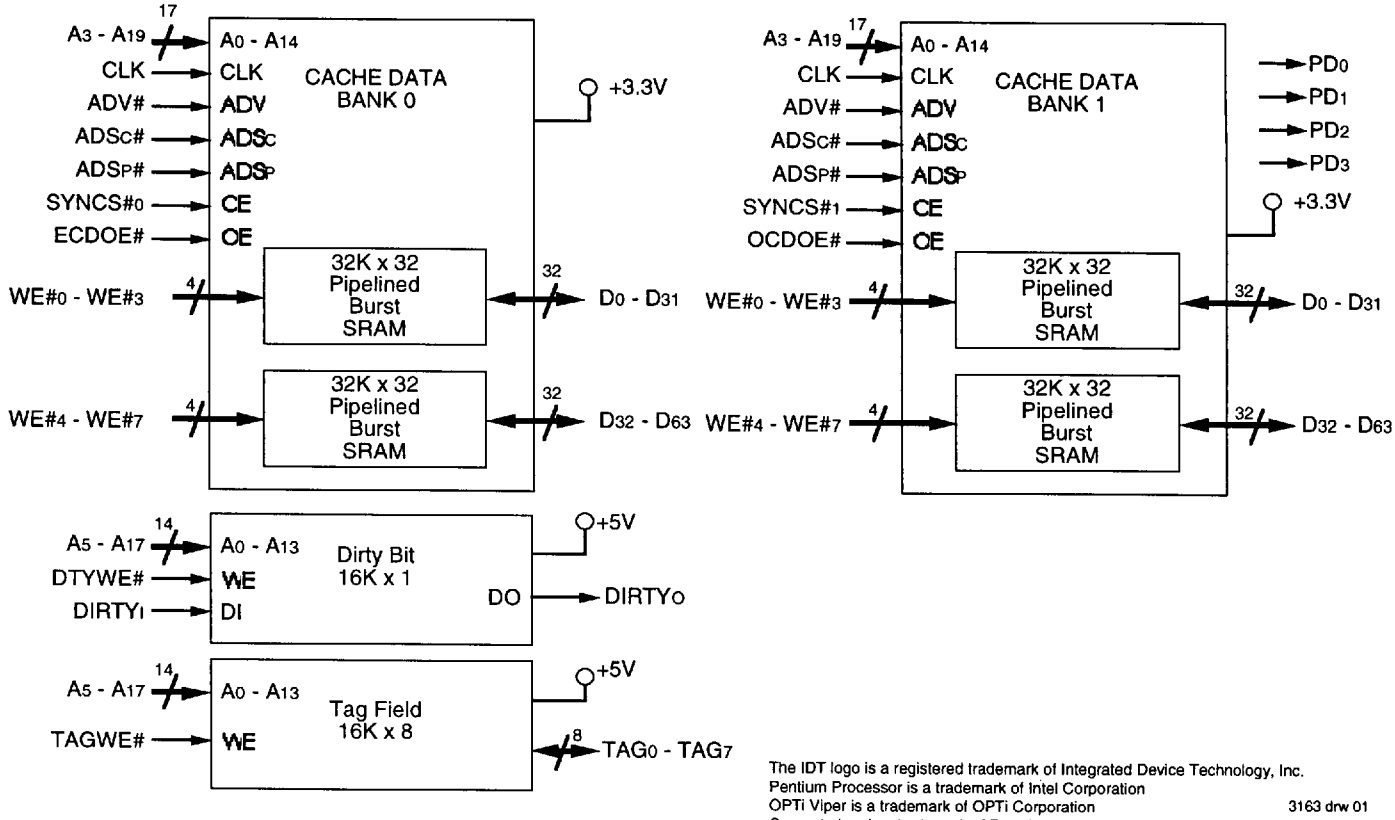
On-board logic, 3.3V data RAM, plus 5V tag and dirty RAM provide an exact interface between the module and the OPTi Viper chipset. Four PD (presence detect) input pins allow the system to determine if cache is present, the cache size and if the data SRAM is burst or asynchronous.

The low-profile card edge package allows 160 signal leads to be placed on a package 4.35" long, 0.365" thick and a maximum of 1.16" tall. The module space savings versus discrete components allows the OEM to design additional functions onto the system or to shrink the size of the motherboard for reduced cost.

All inputs and outputs are TTL-compatible, and operate from separate 5V (±5%) and 3.3V (±10%) power supplies. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6217 – 512KB PIPELINED BURST VERSION



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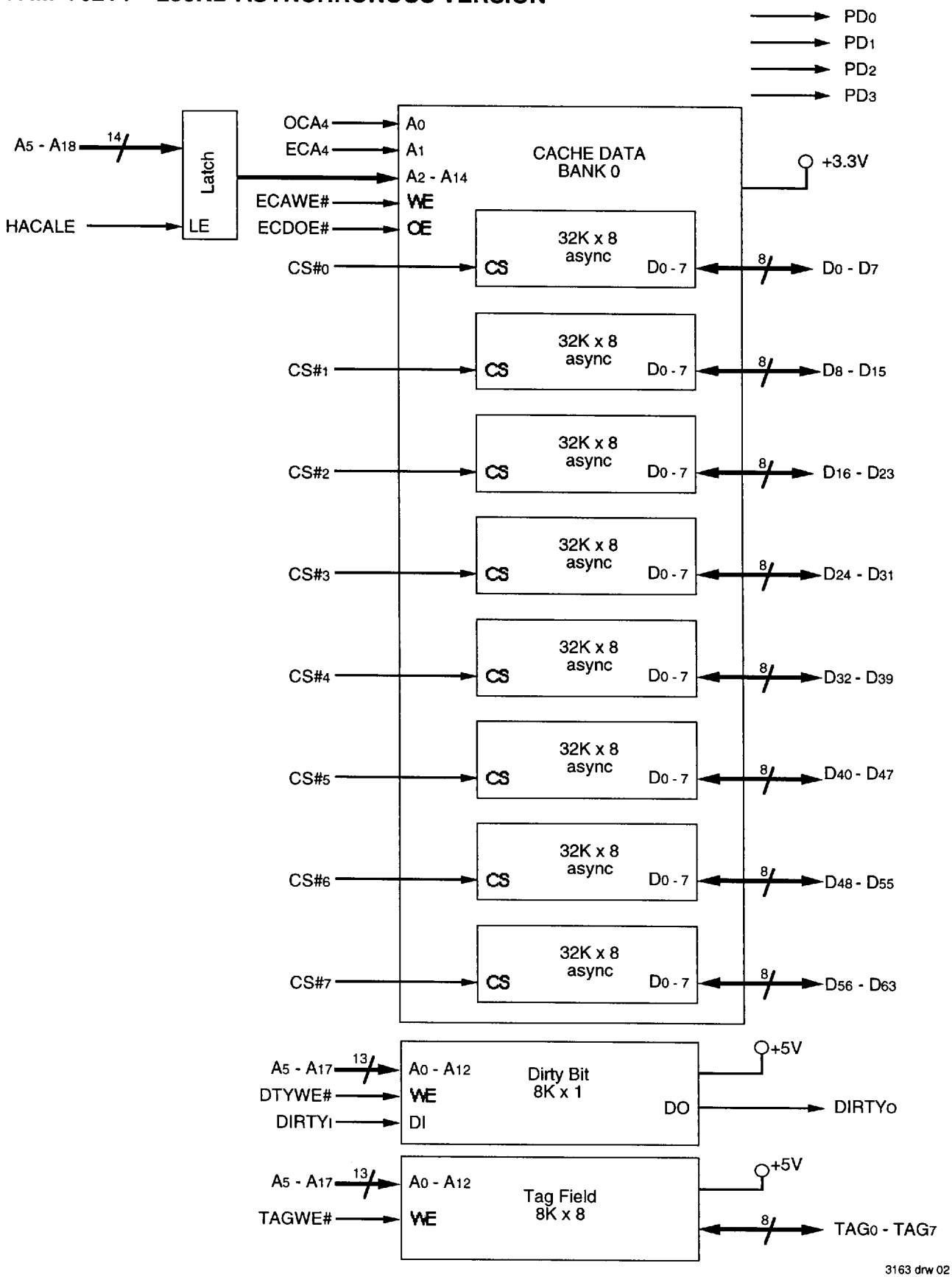
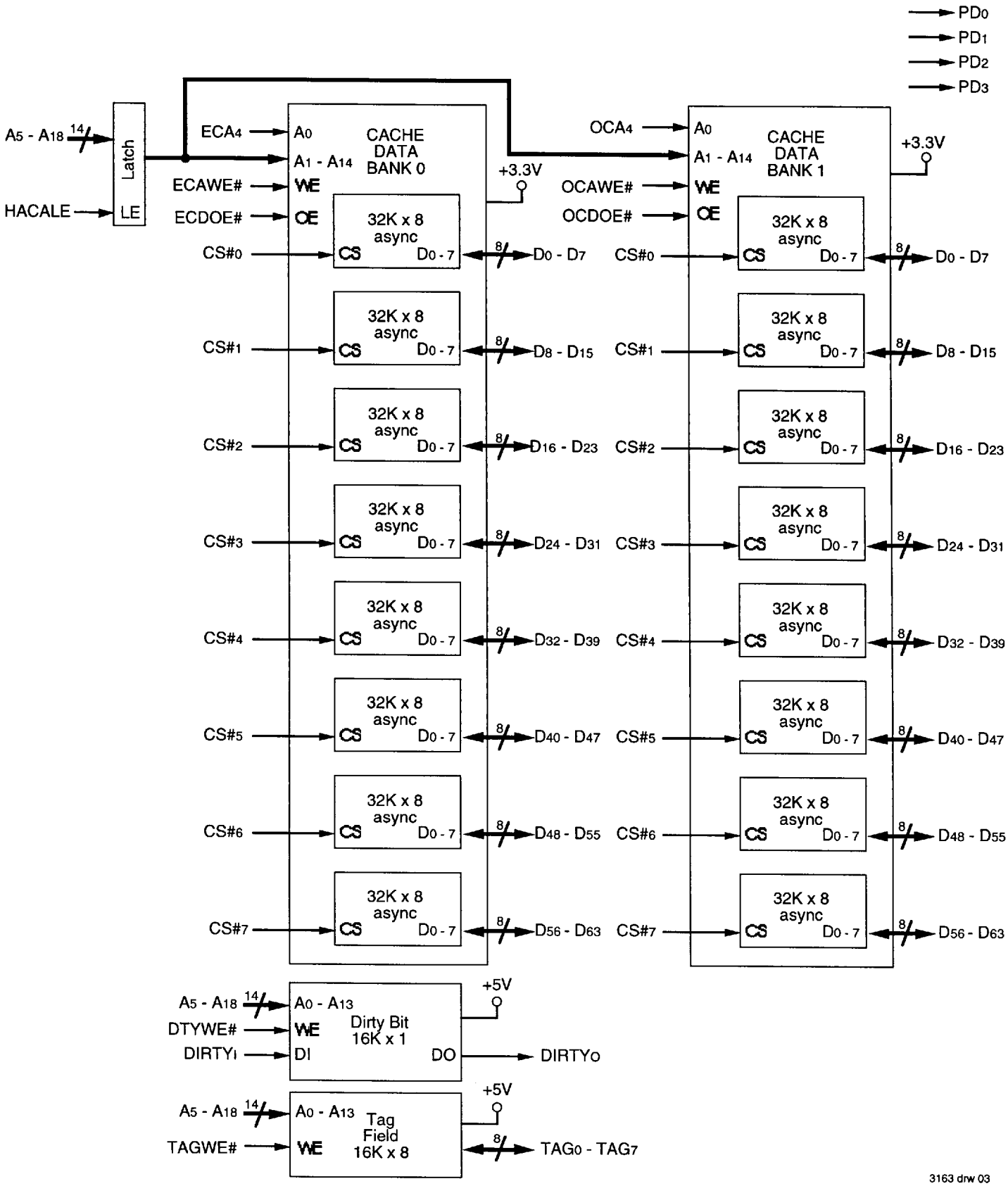
FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6214 – 256KB ASYNCHRONOUS VERSION



FUNCTIONAL BLOCK DIAGRAM

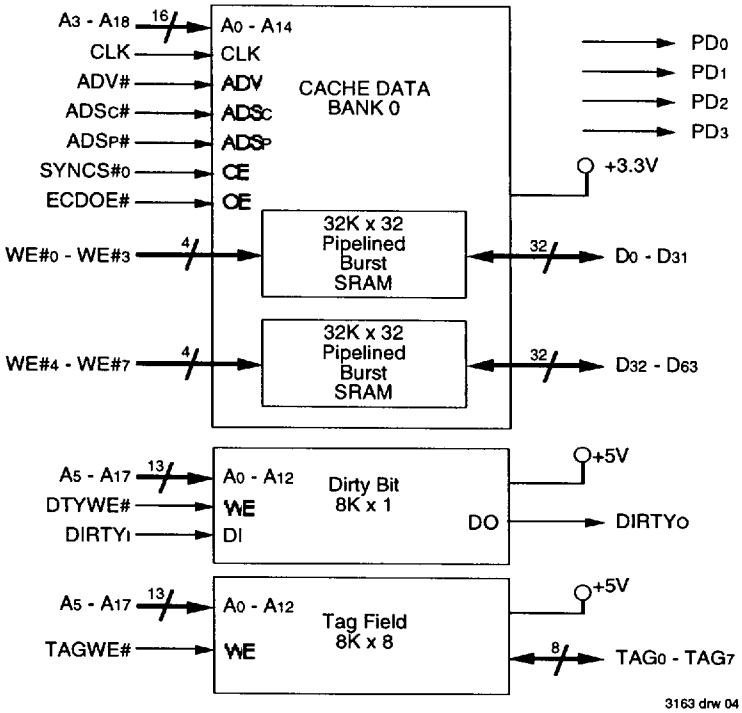
IDT7MPV6215 – 512KB ASYNCHRONOUS VERSION



3163 drw 03

FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6216 – 256KB BURST VERSION



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PIN NAMES

A5 – A18	Address Inputs
OCA4, ECA4	Address Inputs
D0 – D63	Inputs/Outputs
TAG0 – TAG7	Tag Inputs/Outputs
TAGWE#	Tag Write Enable Input
DTYWE#	Dirty Bit Write Enable Input
DIRTYI	Dirty Bit Data Input
DIRTYO	Dirty Bit Data Output
CAWE#	Cache Write Enable Inputs
CDOE#	Cache Output Enable Inputs
SYNCS#0-1	Chip Enable Input (Burst only)
CE#0 – CE#7	Chip Enable Inputs (Async only)
WE#0 – WE#7	Chip Enable Inputs (Burst only)
HACALE	Cache Latch Enable Input (Async only)
ADSC#	Cache Address Status Input (Burst only)
ADSP#	Processor Address Status Input (Burst only)
ADV#	Burst Address Advance Input (Burst only)
CLK	Clock Input (Burst only)
PD0 – PD3	Presence Detect Pins
N.C.	No Connect
GND	Ground
VCC5	5 Volt Power Supply
VCC3	3.3 Volt Power Supply

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PIN CONFIGURATION(1)

GND	81	1	GND
D63	82	2	D62
D61	83	3	D60
VCC5	84	4	VCC3
D59	85	5	D58
D57	86	6	D56
D55	87	7	D54
GND	88	8	GND
D53	89	9	D52
D51	90	10	D50
D49	91	11	D48
VCC5	92	12	VCC3
D47	93	13	D46
D45	94	14	D44
GND	95	15	GND
D43	96	16	D42
D41	97	17	D40
D39	98	18	D38
D37	99	19	D36
GND	100	20	GND
D35	101	21	D34
D33	102	22	D32
D31	103	23	D30
D29	104	24	D28
GND	105	25	GND
D27	106	26	D26
D25	107	27	D24
VCC5	108	28	VCC3
D23	109	29	D22
D21	110	30	D20
D19	111	31	D18
GND	112	32	GND
D17	113	33	D16
D15	114	34	D14
D13	115	35	D12
GND	116	36	GND
D11	117	37	D10
VCC5	118	38	VCC3
D9	119	39	D8
D7	120	40	D6
GND	121	41	GND
D5	122	42	D4
VCC5	123	43	VCC3
D3	124	44	D2
D1	125	45	D0
VCC5	126	46	VCC3
ADS#C/ECA4	127	47	ADV#/OCA4
SYNCS#0/ECAWE#	128	48	SYNCS#1/OCAWE#
ECDOE#	129	49	OCDOE#
WE#0/CE#0	130	50	WE#1/CE#1
GND	131	51	GND
WE#2/CE#2	132	52	WE#3/CE#3
WE#4/CE#4	133	53	WE#5/CE#5
VCC5	134	54	VCC3
WE#6/CE#6	135	55	WE#7/CE#7
CLK/N.C.	136	56	ADS#P/HACALE
GND	137	57	GND
DTYWE#	138	58	TAGWE#
A3/N.C.	139	59	A4/N.C.
A5	140	60	A6
A7	141	61	A8
GND	142	62	GND
A9	143	63	A10
A11	144	64	A12
A13	145	65	A14
VCC5	146	66	VCC3
A15	147	67	A16
A17	148	68	A18
A19	149	69	A20
GND	150	70	GND
DIRTY I	151	71	DIRTY O
TAG0	152	72	TAG1
VCC5	153	73	VCC3
TAG2	154	74	TAG3
TAG4	155	75	TAG5
GND	156	76	GND
TAG6	167	77	TAG7
PD0	158	78	PD1
PD2	159	79	PD3
VCC5	160	80	VCC3

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LOW PROFILE CARD EDGE MODULE
TOP VIEW

NOTE:
1. Pins with two names are for the burst and asynchronous functions respectively.

PRESENCE DETECT TABLE

PD3	PD2	PD1	PD0	Module
N.C.	N.C.	N.C.	N.C.	No cache present
N.C.	N.C.	GND	GND	IDT7MPV6214
N.C.	GND	GND	GND	IDT7MPV6215
N.C.	N.C.	GND	N.C.	IDT7MPV6216
N.C.	GND	GND	N.C.	IDT7MPV6217

3163 tbl 02

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
V_{TERM} for V_{CC3}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 3163 tbl 03

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC3}	Supply Voltage	3.0	3.3	3.6	V
V_{CC5}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3163 tbl 04

1. V_{IL} = –1.0V for pulse width less than 5ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Power Plane	Ambient Temperature	GND	Vcc
V_{CC3}	0°C to +70°C	0V	3.3V ± 10%
V_{CC5}	0°C to +70°C	0V	5.0V ± 5%

3163 tbl 05

DC ELECTRICAL CHARACTERISTICS (IDT7MPV6214/15 ONLY)

(V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address)	V_{CC} = Max, V_{IN} = GND to V_{CC}	–	20	µA
$\|I_{LI}\|$	Input Leakage Current (Data and Control)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output HighVoltage	I_{OH}= –4mA, V_{CC} = Min.	2.4	—	V
I_{CC3}	Operating 3.3V Power Supply Current	V_{CC3} = Max., $\overline{CE} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	1900	mA
I_{CC5}	Operating 5V Power Supply Current	V_{CC5} = Max., $\overline{CE} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	300	mA
I_{SB3}	Standby 3.3V Power Supply Current	V_{CC3} = Max., $\overline{CE} \ge V_{IH}$, f = f_{MAX}, Outputs Open	—	480	mA
I_{SB5}	Standby 5V Power Supply Current	V_{CC5} = Max., $\overline{CE} \ge V_{IH}$, f = f_{MAX}, Outputs Open	—	100	mA
I_{SB31}	Full Standby 3.3V Power Supply Current	V_{CC3} = Max., $\overline{CE} \ge V_{CC}$ - 0.2V, f = 0, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}$ - 0.2V, Outputs Open	—	50	mA
I_{SB51}	Full Standby 5V Power Supply Current	V_{CC5} = Max., $\overline{CE} \ge V_{CC}$ - 0.2V, f = 0, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}$ - 0.2V, Outputs Open	—	30	mA

3163 tbl 06

SRAM ACCESS TIMES

Bus Speed	Asynch	Burst[1]	Tag	Dirty
66MHz	15ns	8.5ns	12ns	15ns
60MHz	15ns	—	15ns	15ns
50MHz	25ns	—	20ns	20ns

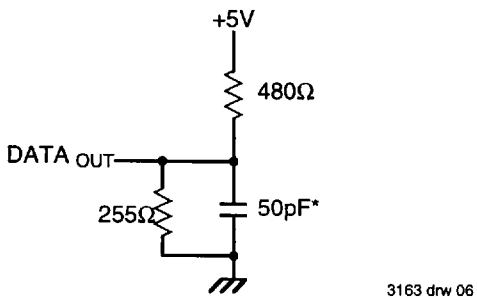
3163 tbl 07

NOTE:
1. Burst SRAMs are measured by Clock to Data Out (t_{CD}).

AC TEST CONDITIONS – 5V POWER SUPPLY

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

3163 tbl 09



*including scope and jig capacitances

Figure 1. Output Load

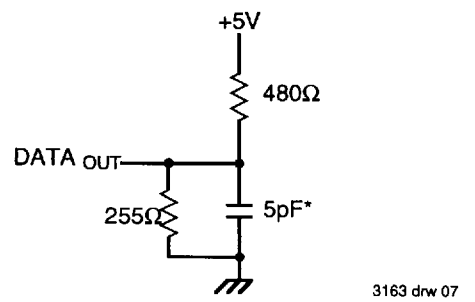
CAPACITANCE[1, 2] (IDT7MPV6214/15 ONLY)

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	'6214	'6215	Unit
C_{IN1}	Input Capacitance (Address)	V_{IN} = 0V	20	20	pF
C_{IN2}	Input Capacitance (CE#)	V_{IN} = 0V	8	15	pF
C_{IN3}	Input Capacitance (Cache WE#,OE#, OCA_4, ECA_4)	V_{IN} = 0V	45	45	pF
C_{IN4}	Input Capacitance (HACALE,DIRTYI, Dirty, Tag WE#)	V_{IN} = 0V	8	8	pF
$C_{I/O1}$	I/O Capacitance (Data)	V_{OUT} = 0V	10	17	pF
$C_{I/O2}$	I/O Capacitance (Tag, DIRTYO)	V_{OUT} = 0V	10	10	pF

3163 tbl 08

NOTES:
1. These parameters are guaranteed by design but not tested.
2. These parameters are maximum values.



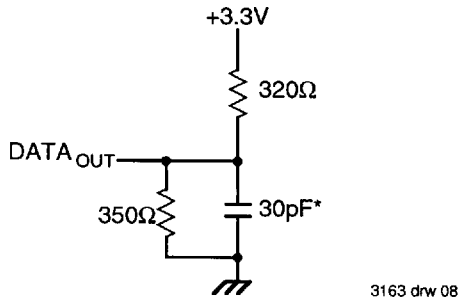
*including scope and jig capacitances

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

AC TEST CONDITIONS – 3.3V POWER SUPPLY

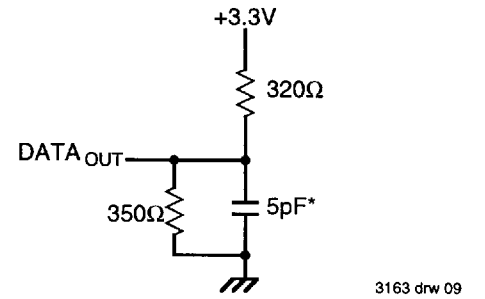
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 3 and 4

3163 tbl 10



*including scope and jig capacitances

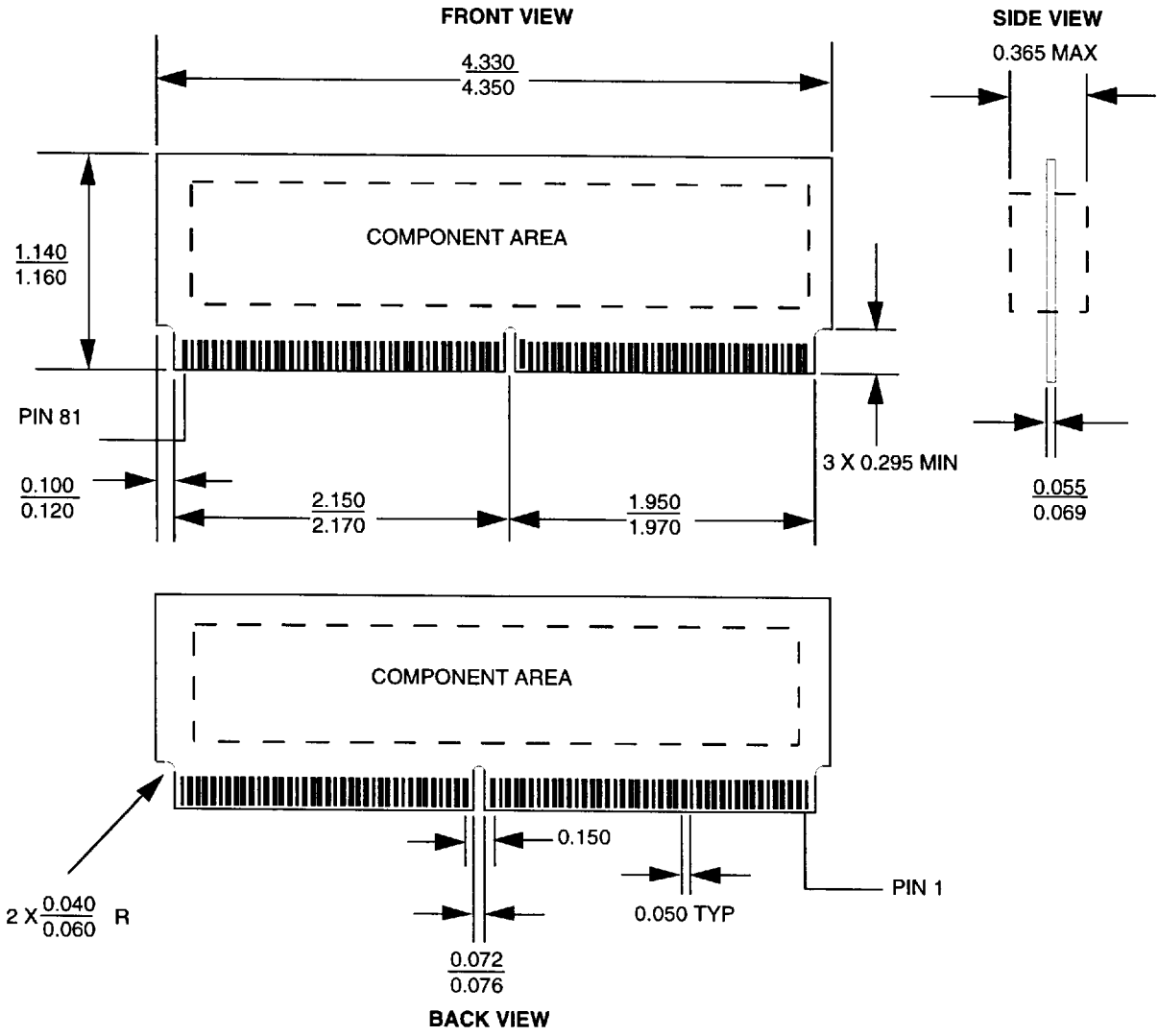
Figure 3. Output Load



*including scope and jig capacitances

Figure 4. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

PACKAGE DIMENSIONS - IDT7MPV6214/15



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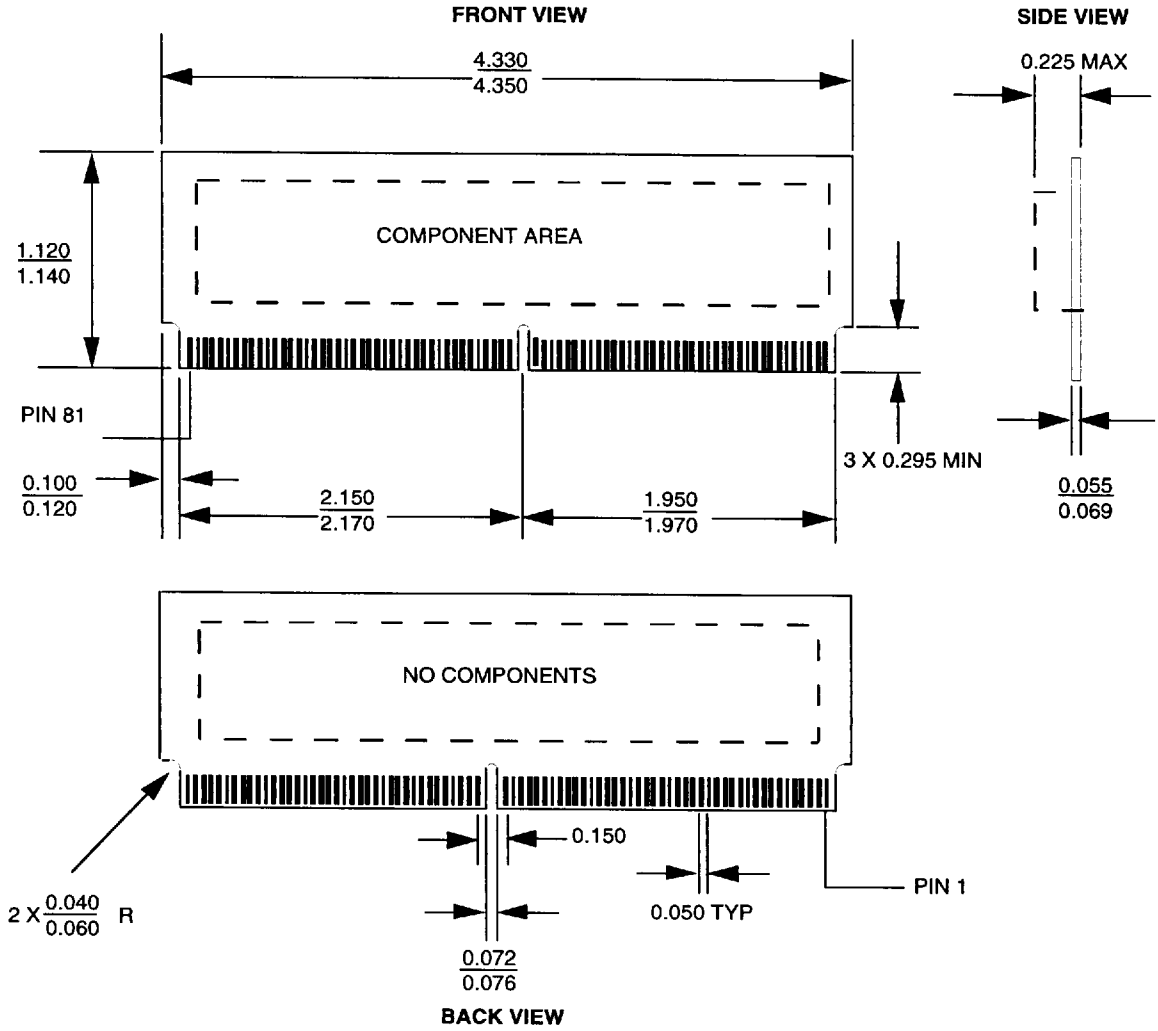
PACKAGE DIMENSIONS - IDT7MPV6216



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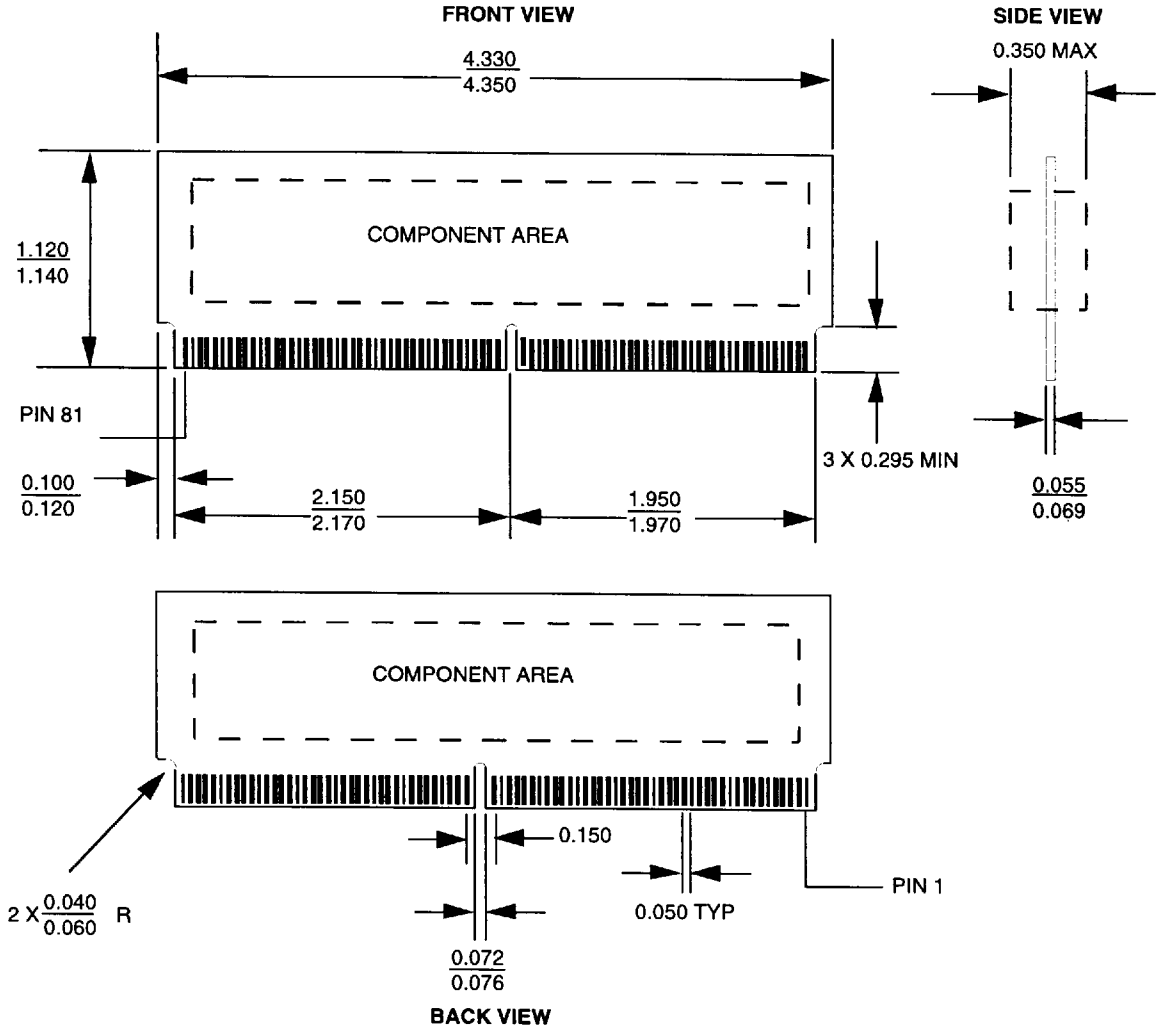
PACKAGE DIMENSIONS - IDT7MPV6217



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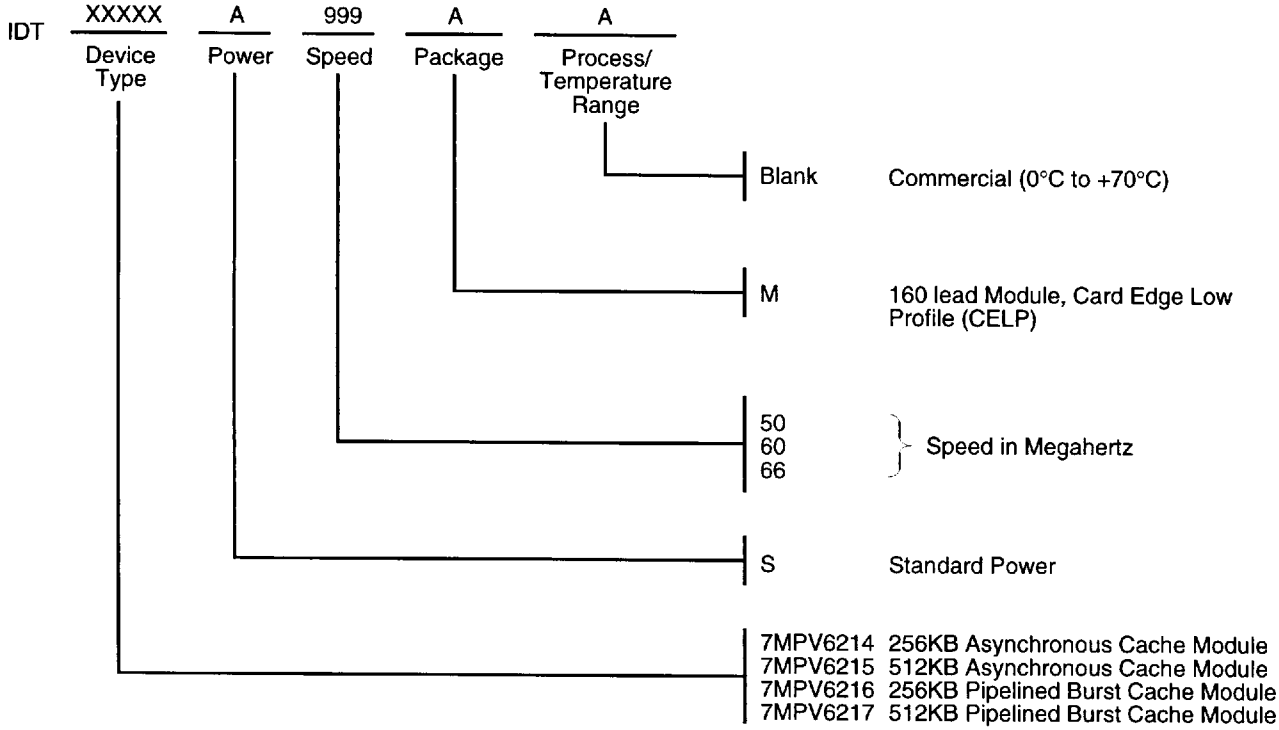
ORDERING INFORMATION



3163 drw 13