SN54HC85A, SN74HC85A
4-BIT MAGNITUDE COMPARATORS

T-45-17

D2684, DECEMBER 1982—REVISED JUNE 1989

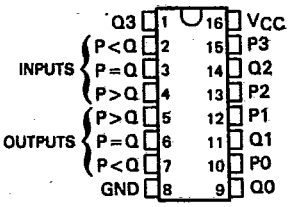
- **Package Options Include Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

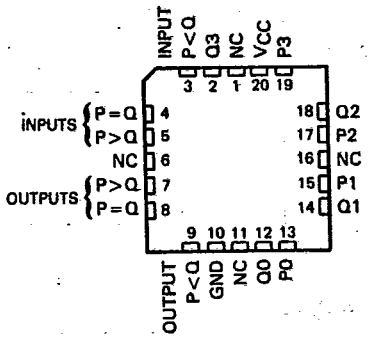
These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (P, Q) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The P>Q, P<Q, and P=Q outputs of a stage handling less significant bits are connected to the corresponding P>Q, P<Q, and P= inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a high-level voltage applied to the P=Q input. The cascading path of the 'HC85A is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

The SN54HC85A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC85A is characterized for operation from −40°C to 85°C.

SN54HC85A . . . J PACKAGE
SN74HC85A . . . N PACKAGE
(TOP VIEW)

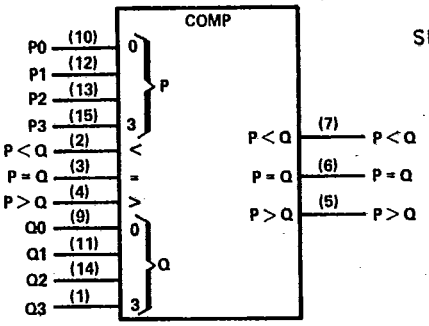


SN54HC85A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

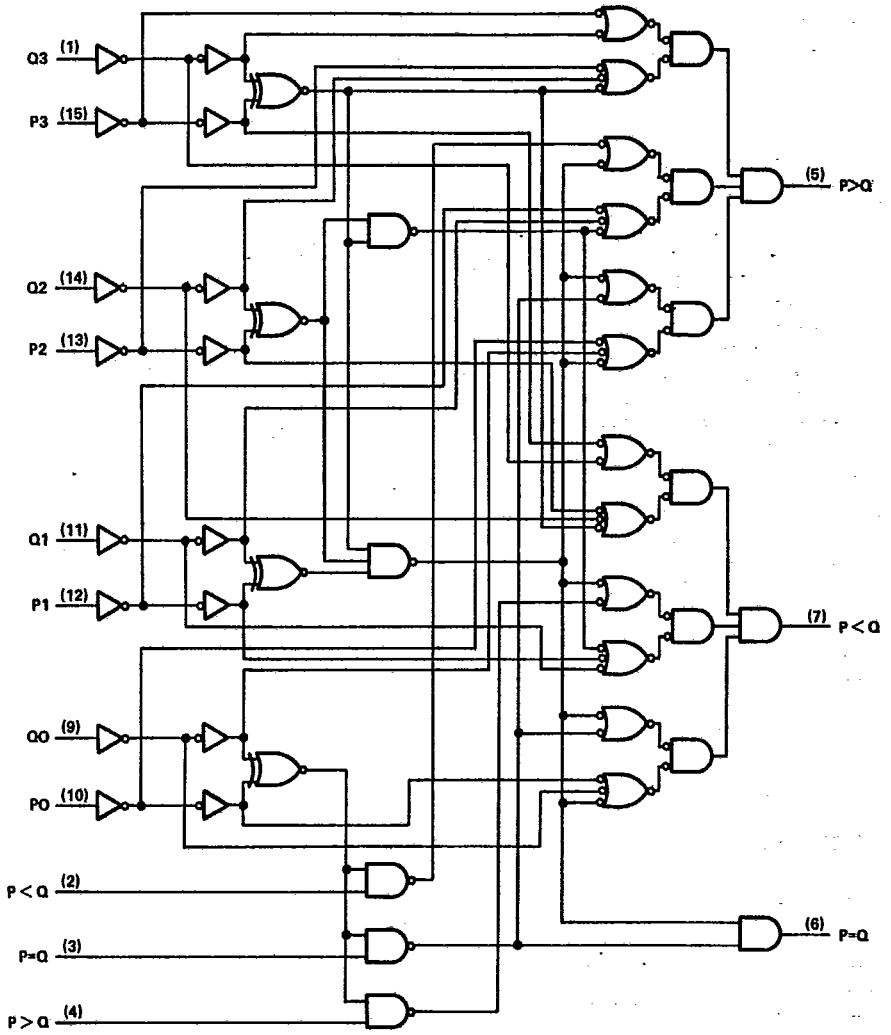
logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

NOTICE
SEE ORDER OF DATA FOR ERRATA INFORMATION

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

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FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
P3, Q3	P2, Q2	P1, Q1	P0, Q0	P>Q	P<Q	P=Q	P>Q	P<Q	P=Q
P3>Q3	X	X	X	X	X	X	H	L	L
P3<Q3	X	X	X	X	X	X	L	H	L
P3=Q3	P2>Q2	X	X	X	X	X	H	L	L
P3=Q3	P2<Q2	X	X	X	X	X	L	H	L
P3=Q3	P2=Q2	P1>Q1	X	X	X	X	H	L	L
P3=Q3	P2=Q2	P1<Q1	X	X	X	X	L	H	L
P3=Q3	P2=Q2	P1=Q1	P0>Q0	X	X	X	H	L	L
P3=Q3	P2=Q2	P1=Q1	P0<Q0	X	X	X	L	H	L
P3=Q3	P2=Q2	P1=Q1	P0=Q0	H	L	L	H	L	L
P3=Q3	P2=Q2	P1=Q1	P0=Q0	L	H	L	L	H	L
P3=Q3	P2=Q2	P1=Q1	P0=Q0	X	X	H	L	L	H
P3=Q3	P2=Q2	P1=Q1	P0=Q0	H	H	L	L	L	L
P3=Q3	P2=Q2	P1=Q1	P0=Q0	L	L	L	H	H	L

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC85A			SN74HC85A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC85A		SN74HC85A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_I		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC85A		SN74HC85A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P or Q	P>Q or P<Q	2 V		80	230		345		290	MHz
			4.5 V		26	46		69		58	
			6 V		22	39		59		49	
t_{pd}	Any P or Q	P=Q	2 V		66	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
t_{pd}	P<Q or P=Q	P>Q	2 V		63	175		260		220	ns
			4.5 V		21	41		58		50	
			6 V		18	33		46		39	
t_{pd}	P>Q or P=Q	P<Q	2 V		72	175		260		220	ns
			4.5 V		24	41		58		50	
			6 V		20	33		46		39	
t_{pd}	P=Q	P=Q	2 V		51	145		215		185	ns
			4.5 V		17	29		43		37	
			6 V		14	25		37		31	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	80 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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