MH12908TNA-85,-10,-12,-15/
MH12908TNA-85H,-10H,-12H,-15H

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The MH12908TNA is a 1048576-bits CMOS static RAM module organized as 131072-words by 8-bits. It consists of four industry standard 32K × 8 static RAMs and one decoder.

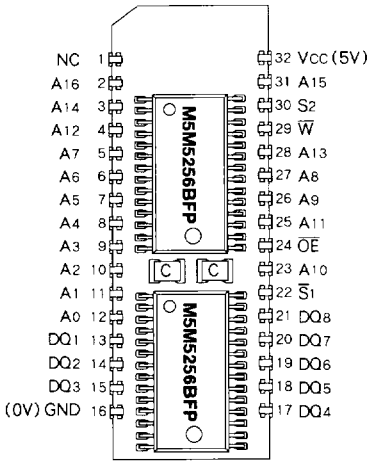
The stand-by currents is low enough for a barrery backup application. It is mounted a flat package on a 32-pin dual in line package and configured in an industrial standard 128K × 8-bits pin out.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH12908TNA-85	85ns	70mA	200 μA
MH12908TNA-10	100ns		
MH12908TNA-12	120ns		
MH12908TNA-15	150ns		
MH12908TNA-85H	85ns		40 μA
MH12908TNA-10H	100ns		
MH12908TNA-12H	120ns		
MH12908TNA-15H	150ns		

- JEDEC standard 32-pin 600 mil pin out
- Single +5V power supply
- Fully static operation : No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S1}$, S2
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O

PIN CONFIGURATION (TOP VIEW) [Both side]



Outline 32N1

NC : NO CONNECTION

APPLICATION

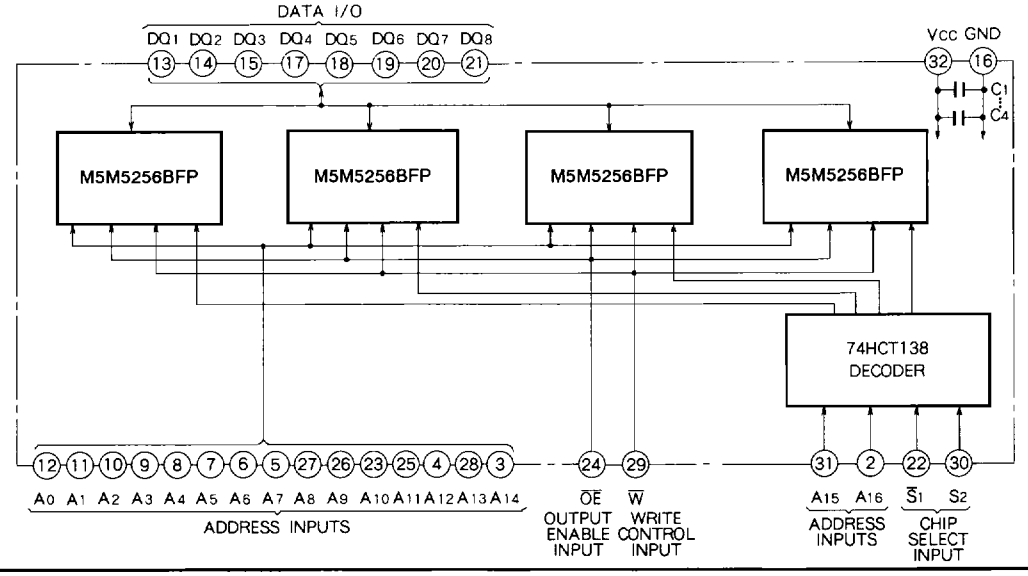
Small Capacity Memory Units

FUNCTION

The operation mode of the MH12908TNA is determined by a combination of the device control inputs $\overline{S1}$, S2, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is excuted whenever the low level $\overline{W}$ overlaps with the low level $\overline{S1}$ and the high level S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S1}$ or S2, whichever occurs first,requiring

BLOCK DIAGRAM



the set-up and hold time relative to these edge to be maintained. The Output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is excuted by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S1}$ and $S2$ are in an active state ($\overline{S1}$ = L, $S2$ = H)

When setting $\overline{S1}$ at a high level or $S2$ at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$ and $S2$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TALBE

$\overline{S1}$	$S2$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage		− 0.3~V_{CC} + 0.3	V
V_O	Output voltage		0~V_{CC}	V
P_d	Power dissipation	Ta = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 40~125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	− 0.3		0.8	V
V_{IH}	high input voltage	2.2		V_{CC}+0.3	V

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			− 0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = − 1mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_{OZH}	High level output current in off-state	$\overline{S1}$ = V_{IH} or $S2$ = V_{IL}, $\overline{OE}$ = V_{IH}				1	μA
I_{OZL}	Low level output current in off-state	$V_{I/O}$ = 0~V_{CC}				− 1	μA
I_{CC1}	Active supply current	$\overline{S1}$ ≦ 0.2, $S2$ ≧ V_{CC} − 0.2 Output open Other inputs ≦ 0.2 or ≧ V_{CC} − 0.2			30	65	mA
I_{CC2}	Active supply current	$\overline{S1}$ = V_{IL}, $S2$ = V_{IH} Output open Other inputs = V_{IH}			35	70	mA
I_{CC3}	Stand-by supply current	① $\overline{S1}$ and A_{15} and A_{16} ≦ 0.2 or ≧ V_{CC} − 0.2 $S2$ ≦ 0.2, Other inpts = 0~V_{CC} ② $\overline{S1}$ and $S2$ ≧ V_{CC} − 0.2 A_{15} and A_{16} ≦ 0.2 or ≧ V_{CC} − 0.2 Other inputs = 0~V_{CC}	TNA			200	μA
			TNA-H			40	
I_{CC4}	Stand-by supply current	$S2$=V_{IL}, $\overline{S1}$=V_{IH}, Other inputs=0~V_{CC}				15	mA
C_i	Input capacitance (Ta = 25℃)	V_i = GND, V_i = 25mVrms, f = 1MHz				30	pF
C_o	Output capacitance (Ta = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz				30	pF

Note 1 : Direction for current flowing into IC is indicated as positive (no mark)
2 : Typical value is V_{CC} = 5V, Ta = 25℃

MITSUBISHI ELECTRIC

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits												Unit
		MH12908TNA-85			MH12908TNA-10			MH12908TNA-12			MH12908TNA-15			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	85			100			120			150			ns
$t_{a(A)}$	Address access time			85			100			120			150	ns
$t_{a(\overline{S1})}$	Chip select 1 access time			85			100			120			150	ns
$t_{a(S2)}$	Chip select 2 access time			85			100			120			150	ns
$t_{a(OE)}$	Output enable access time			45			50			60			75	ns
$t_{dis(\overline{S1})}$	Output disable time after $\overline{S_1}$ high			30			35			40			45	ns
$t_{dis(S2)}$	Output disable time after S_2 low			30			35			40			45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			35			40			45	ns
$t_{en(\overline{S1})}$	Output enable time after $\overline{S_1}$ low	10			10			10			10			ns
$t_{en(S2)}$	Output enable time after S_2 high	10			10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			10			10			ns
$t_{v(A)}$	Data valid time after address change	20			20			20			20			ns

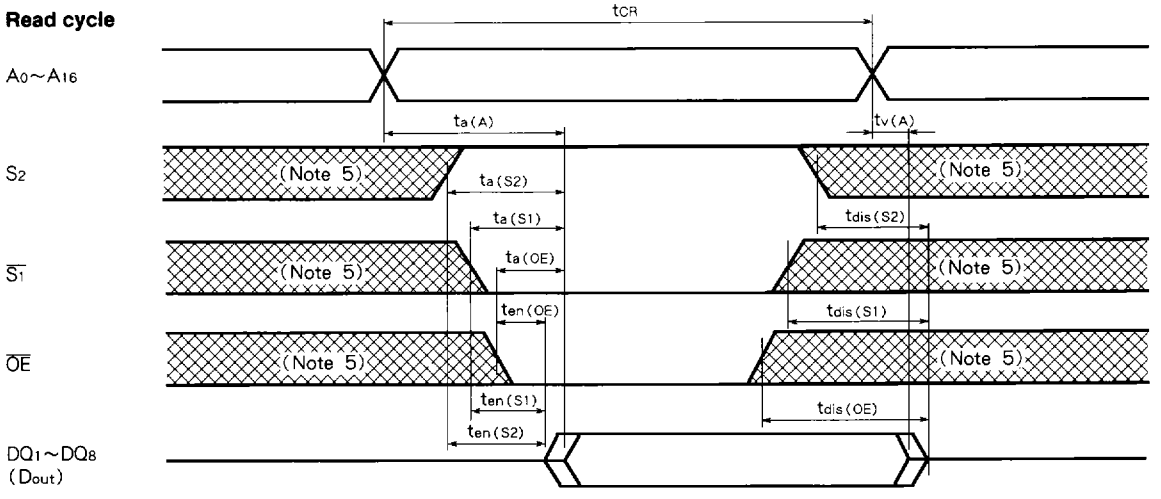
TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits												Unit
		MH12908TNA-85			MH128908TNA-10			MH12908TNA-12			MH12908TNA-15			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	85			100			120			150			ns
$t_{w(W)}$	Write pulse width	60			60			70			80			ns
$t_{su(A)}$	Address set up time	0			0			0			0			ns
$t_{su(S)}$	Chip select set up time	75			80			85			90			ns
$t_{su(D)}$	Data set up time	35			35			40			50			ns
$t_{h(D)}$	Data hold time	0			0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			30			35			40			45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high			30			35			40			45	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ low	10			10			10			10			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	10			10			10			10			ns

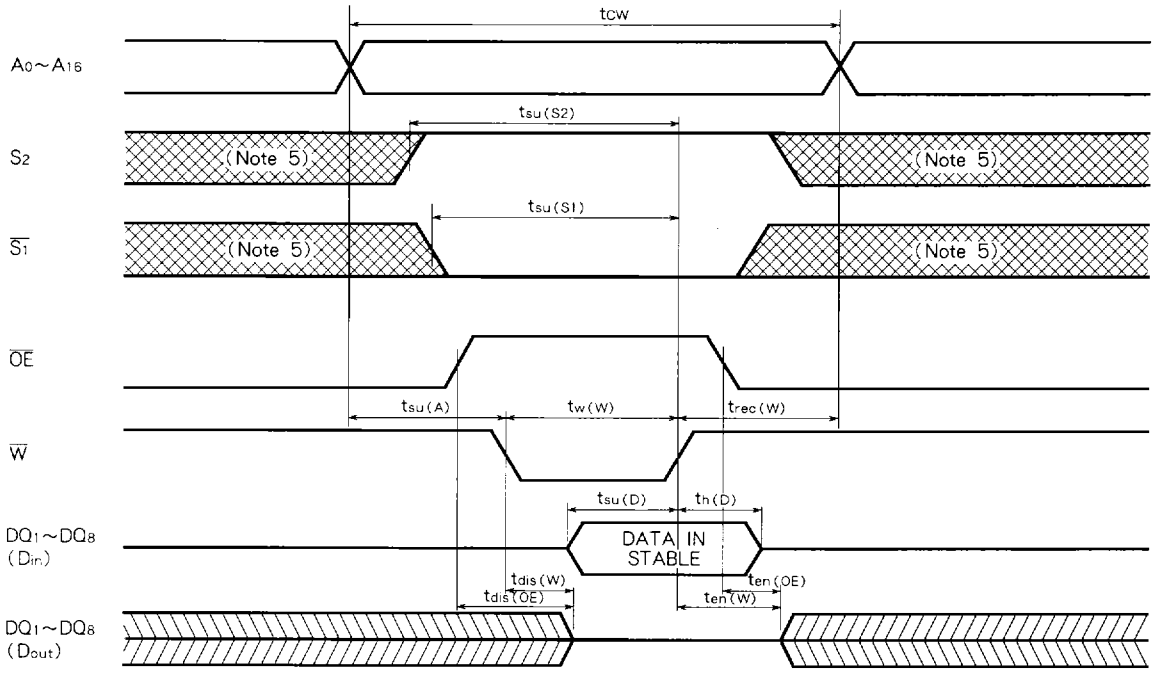
TIMING DIAGRAM

Read cycle

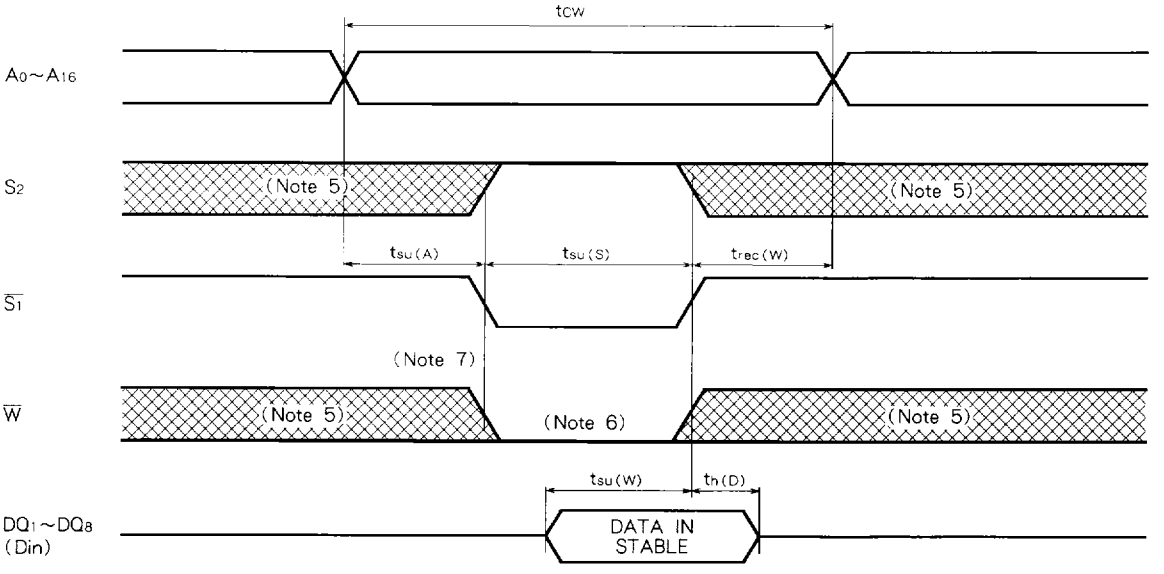


$\overline{W}$ = "H" level

Write cycle ($\overline{W}$ control)



Write cycle ($\overline{S_1}$, S_2 control)



Note 4 : Test condition
Input pulse level : 0.4~2.4V
Input pulse rise, fall time : 10ns
Load : 1TTL, CL = 100pF
Reference level : 1.5V

5 : Hatching indicates the state is don't care.
6 : Writing is executed while S_2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
7 : If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or S_2 high, the output remains in the high impedance state.
8 : Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{ST})}$	Chip selest input $\overline{S_1}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$V_{I(S2)}$	Ship select input S_2	4.5V ≦ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, A_{15} and A_{16} < 0.2V or > V_{CC} − 0.2V, Other inputs = 0~V_{CC}	TNA			100	μA
			TNA-H			40	

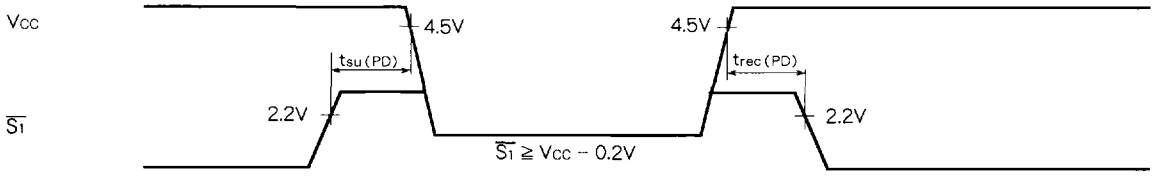
Note 9 : When $\overline{S_1}$ is operated at 2.2V (V_{IH} min) and the supply voltage is between 4.5V and 2.4V, supply current is defined as I_{CC4}.

TIMING REQUIREMENTS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control



S_2 control