LG Semicon Co.,Ltd.

GMM2642227CNTG

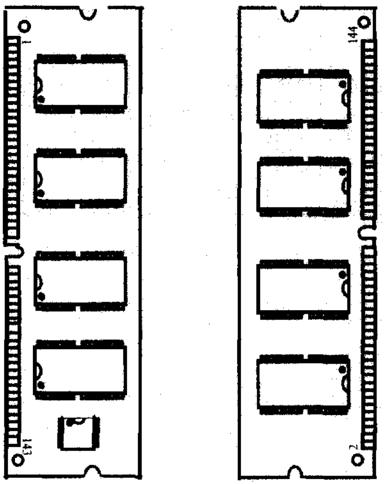
2,097,512 WORDS x 64 BIT
SYNCHRONOUS DYNAMIC RAM SO-DIMM

Description

The GMM2642227CNTG is a 2M x 64 bits Synchronous Dynamic RAM SO-DIMM which is assembled 8 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 144 pin printed circuit board with decoupling capacitors. The GMM2642227CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2642227CNTG provides common data inputs and outputs.

- **GMM2642227CNTG** (Both Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{\text{CAS}}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

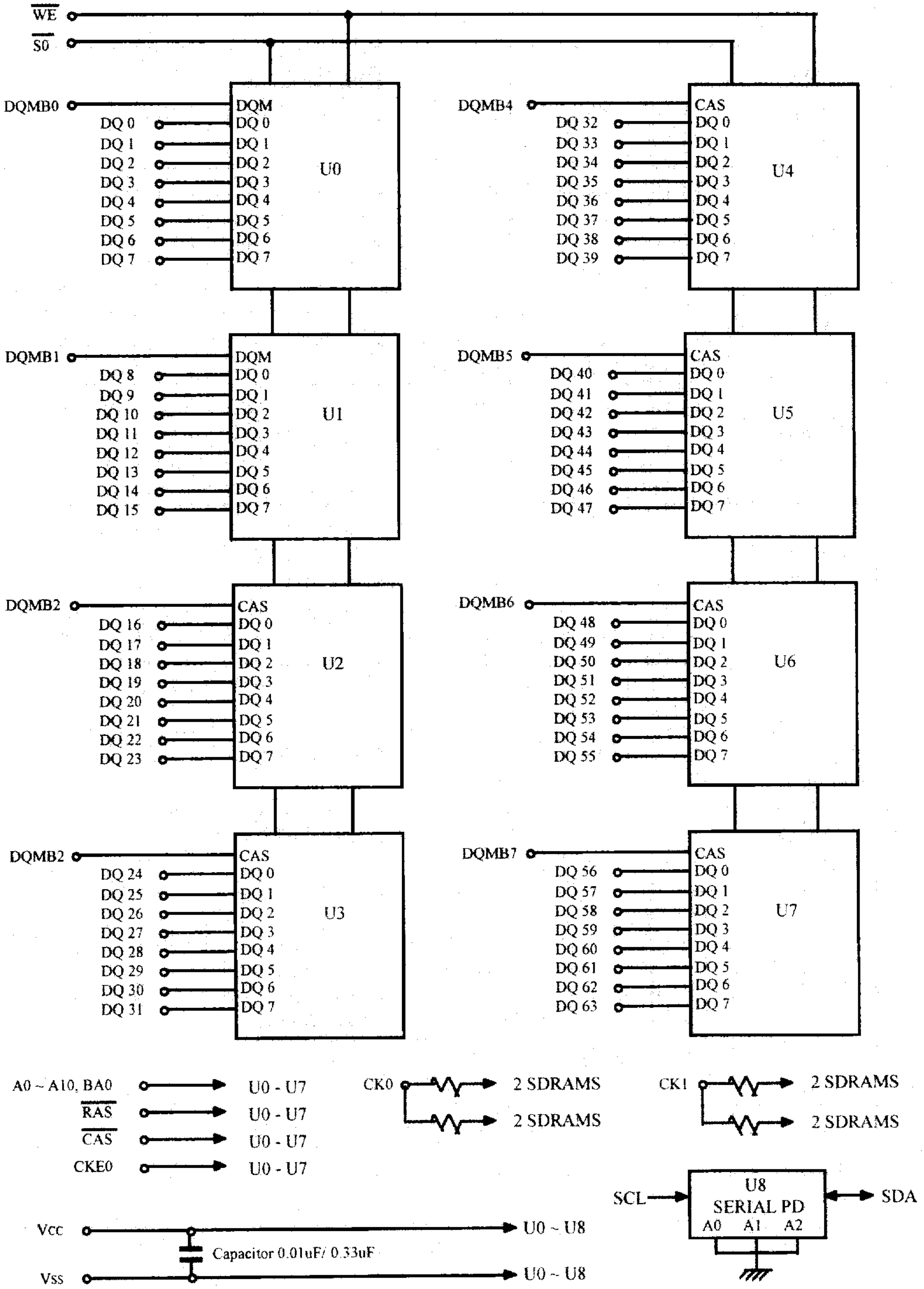
CK0,1	Clock inputs
CKE0	Clock Enable
$\overline{\text{S0}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
A0~A10	Address input
BA0	Bank Address input
DQ0~63	Data input / output
DQMB0~7	Data input / output Mask
Vcc	Power for internal circuit
Vss	Ground for internal circuit
NC	No Connect
VREF	Power Supply for Reference
SDA	Serial Data input / output
SCL	Serial Clock
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	25	DQMB1	49	DQ13	73	NU	97	DQ22	121	DQ24
2	Vss	26	DQMB5	50	DQ45	74	CK1	98	DQ54	122	DQ56
3	DQ0	27	Vcc	51	DQ14	75	Vss	99	DQ23	123	DQ25
4	DQ32	28	Vcc	52	DQ46	76	Vss	100	DQ55	124	DQ57
5	DQ1	29	A0	53	DQ15	77	NC	101	Vcc	125	DQ26
6	DQ33	30	A3	54	DQ47	78	NC	102	Vcc	126	DQ58
7	DQ2	31	A1	55	Vss	79	NC	103	A6	127	DQ27
8	DQ34	32	A4	56	Vss	80	NC	104	A7	128	DQ59
9	DQ3	33	A2	57	NC	81	Vcc	105	A8	129	Vcc
10	DQ35	34	A5	58	NC	82	Vcc	106	BA0	130	Vcc
11	VDD	35	Vss	59	NC	83	DQ16	107	Vss	131	DQ28
12	VDD	36	Vss	60	NC	84	DQ48	108	Vss	132	DQ60
13	DQ4	37	DQ8	61	CK0	85	DQ17	109	A9	133	DQ29
14	DQ36	38	DQ40	62	CKE0	86	DQ49	110	BA1*	134	DQ61
15	DQ5	39	DQ9	63	Vcc	87	DQ18	111	A10/AP	135	DQ30
16	DQ37	40	DQ41	64	Vcc	88	DQ50	112	A11*	136	DQ62
17	DQ5	41	DQ10	65	$\overline{\text{RAS}}$	89	DQ19	113	Vcc	137	DQ31
18	DQ38	42	DQ42	66	CAS	90	DQ51	114	Vcc	138	DQ63
19	DQ7	43	DQ11	67	$\overline{\text{WE}}$	91	Vss	115	DQMB2	139	Vss
20	DQ39	44	DQ43	68	CKE1*	92	Vss	116	DQMB6	140	Vss
21	Vss	45	Vcc	69	$\overline{\text{S0}}$	93	DQ20	117	DQMB3	141	SDA
22	Vss	46	Vcc	70	A12	94	DQ52	118	DQMB7	142	SCL
23	DQMB0	47	DQ12	71	S1	95	DQ21	119	Vss	143	Vcc
24	DQMB4	48	DQ44	72	A13	96	DQ53	120	Vss	144	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0,1 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pins)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{\text{S0}}$ (input pins)	When $\overline{\text{S}}$ is Low, the command input cycle becomes valid. When $\overline{\text{S}}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
Vcc (power supply pins)	3.3 V is applied. (Vcc is for the internal circuit)
Vss (power supply pins)	Ground is connected. (Vss is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver ≤ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes(2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	1
4	# of column addresses on this assembly	9	09h	2
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	64 bits	40h	
7	......Data width of this assembly(Continued)	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	10ns	A0h	3, 8
		12ns	C0h	3, 8
10	SDRAM access time from clock	7.5ns	75h	4, 8
		9ns	90h	4, 8
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	4096/64ms : Normal	00h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	none	00h	
15	Minimum clock delay, Back to Back Random Column Address	t_{CCD} = 1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	6
17	# of banks on each SDRAM device	2 banks	02h	
18	$\overline{CAS}$ Latency	$\overline{CAS}$ Latency = 1, 2 & 3	07h	7
19	$\overline{CS}$ Latency	$\overline{CS}$ latency = 0	01h	
20	Write Latency	Write latency = 0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	

Byte No.	Function description	Function support	Hex Value	Note
22	SDRAM device attributes : General		0Fh	5
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9.5ns	95h	
		t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	16MBytes	04h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		A3h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation Code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturer location	Korea	52h	
73	Manufacturer 's part number	G(GMM2642227CNTG-10K/J)	47h	
74	Allowed characters 0-9, a-z and space	M	4Dh	
75		M	4Dh	
76		2	32h	
77		6	36h	
78		4	34h	
79		2	32h	
80		2	32h	
81		2	32h	
82		7	37h	

Byte No.	Function description	Function support	Hex Value	Note
83		B	42h	
84		N	4Eh	
85		T	54h	
86		G	47h	
87		-	2Dh	
88		1	31h	
89		0	30h	
90		K	4Bh	
91~92	Revision Code	Initial release (Rev.0)	00h	
93	Date Code	WW	00h	
94		YY	00h	
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Specific Data	N/A	00h	
126	Intel specfication CAS# Latency Support	66MHz	66h	
127	Manufacturing Date		06h	
128~255	Reserved		00h	

- Above data are based on the SPD specification of JEDEC standard and can be changed.

- Note : 1. If the bank select address of RA11 is excluded, this byte must be programmed by 0Bh.
  2. If the bank select address of CA11 is excluded, this byte must be programmed by 0Ah
  3. In case of - 10 part, the minimum cycle time is 10ns, 15ns and 30ns @ $\overline{\text{CAS}}$ latency = 3, 2 and 1 respectively.
     So, the value of A0h is based on the minimum cycle time @ $\overline{\text{CAS}}$ latency = 3.
     In case of - 12 part, the minimum cycle time is 12ns, 18ns and 36ns @ $\overline{\text{CAS}}$ latency = 3, 2 and 1 respectively.
     So, the value of C0h is based on the minimum cycle time @ $\overline{\text{CAS}}$ latency = 3.

4. In case of - 10 part, the access time is 7.5ns, 9.5ns and 27ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
   So, the value of 75h is based on the access time @ $\overline{CAS}$ latency = 3.
   In case of - 12 part, the access time is 9ns, 12ns and 32ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
   So, the value of 90h is based on the access time @ $\overline{CAS}$ latency = 3.
5. LGS' SDRAM supports Burst Read Single-bit Write, Precharge all and Auto precharge functions.
   If Burst Read Single-bit Write function is not supports, this byte must be programmed by 06h.
6. LGS' SDRAM supports burst lengths of 1, 2, 4, 8 and full page. If burst lengths of 1 and 4 are only supports, this byte must be programmed by 05h.
7. LGS' SDRAM supports $\overline{CAS}$ latency of 1, 2 and 3. If $\overline{CAS}$ latency of 2 and 3 are only supported, this byte must be programmed by 06h.
8. This value is based on the component specification.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	8	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	- 10		- 12		Unit	Test conditions	Notes
			Min	Max	Min	Max			
Operating current		I_{CC1}	-	800	-	680	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	24	-	24	mA	CKE=V_{IL}, t_{CK}=min	5
			-	16	-	16	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	240	-	200	mA	CKE=V_{IH}, NOP command t_{CK}=15ns	3
Active standby current (Bank Active)		I_{CC3}	-	56	-	56	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
			-	280	-	240	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current	(CL=2)	I_{CC4}	-	800	-	680	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=3)	I_{CC4}	-	1200	-	1000	mA		
Auto Refresh current		I_{CC5}	-	680	-	560	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	16	-	16	mA	$V_{IH} \geq V_{CC} - 0.2$ $0V \leq V_{IL} \leq 0.2V$	7
Input leakage current		I_{LI}	-10	10	-10	10	μA	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current		I_{LO}	-10	10	-10	10	μA	$0 \leq V_{out} \leq V_{CC}$ I/O = disable	
Output high voltage		V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the *output open condition*.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	50	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	45	pF	1, 3
C_{I3}	Input capacitance (CK0 ~ CK1)	-	45	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$)	-	45	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	15	pF	1, 3
$C_{I/O}$	Input / output capacitance (DQ0 ~ DQ63)	-	15	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 10		- 12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9.5	-	12		
	(CL=3)	t_{AC}	-	8	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V) (Continued)

Parameter	Symbol	-10		-12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

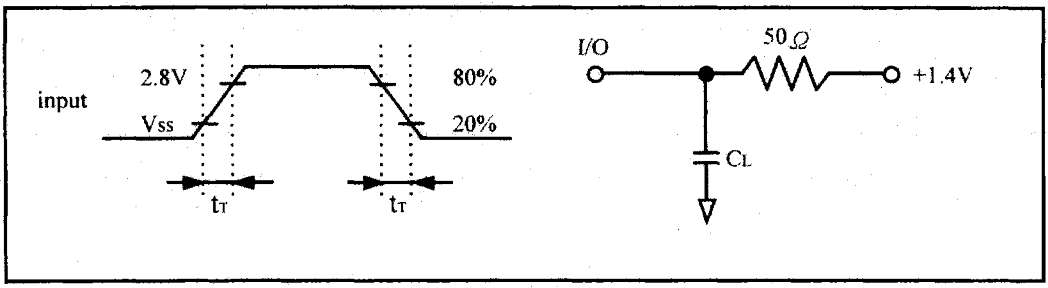
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

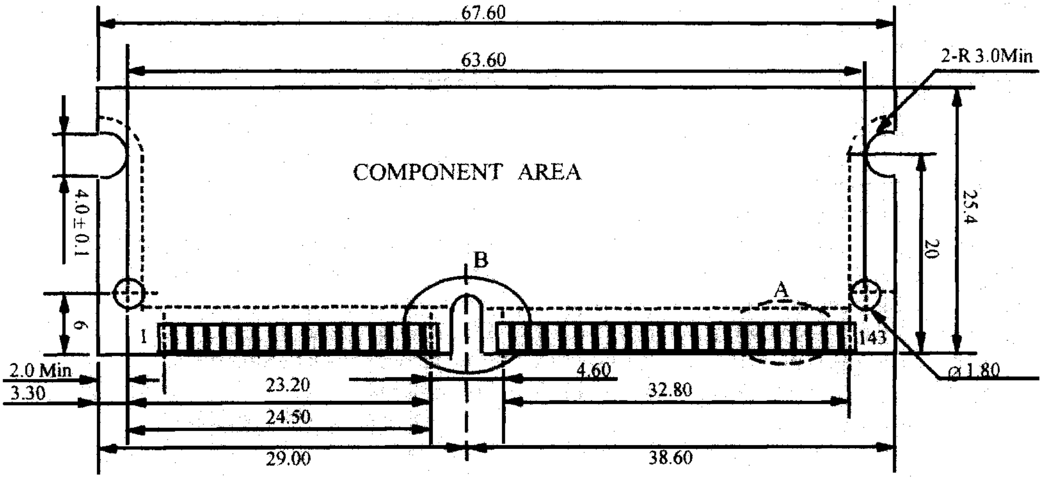
Relationship Between Frequency and Minimum Latency. (Continued)

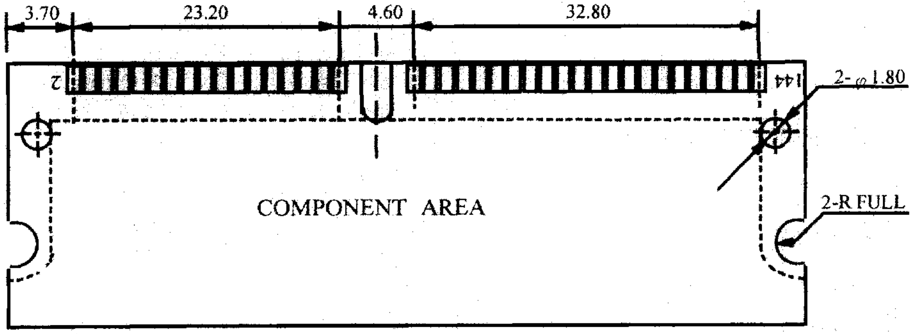
Parameter		**Symbol**	**- 10**			**- 12**			**Notes**
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	I_{BSH}	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	

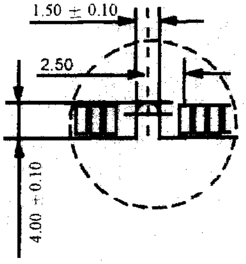
Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

Package Dimension

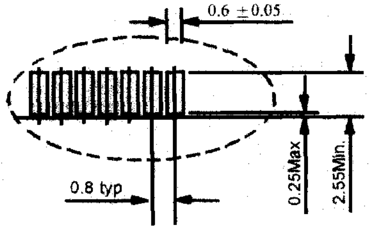
Unit: mm



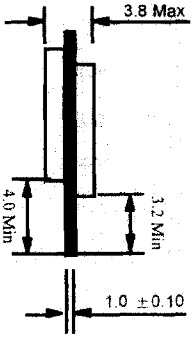




DETAIL "B"



DETAIL "A"



NOTE : 1. Tolerances on all dimensions ±0.15 unless otherwise specified.
2. Thickness(* Mark) includes Plating and / or Metallization.